AMD GEODE™ CLOCK SOURCE

MK1491-06

Description

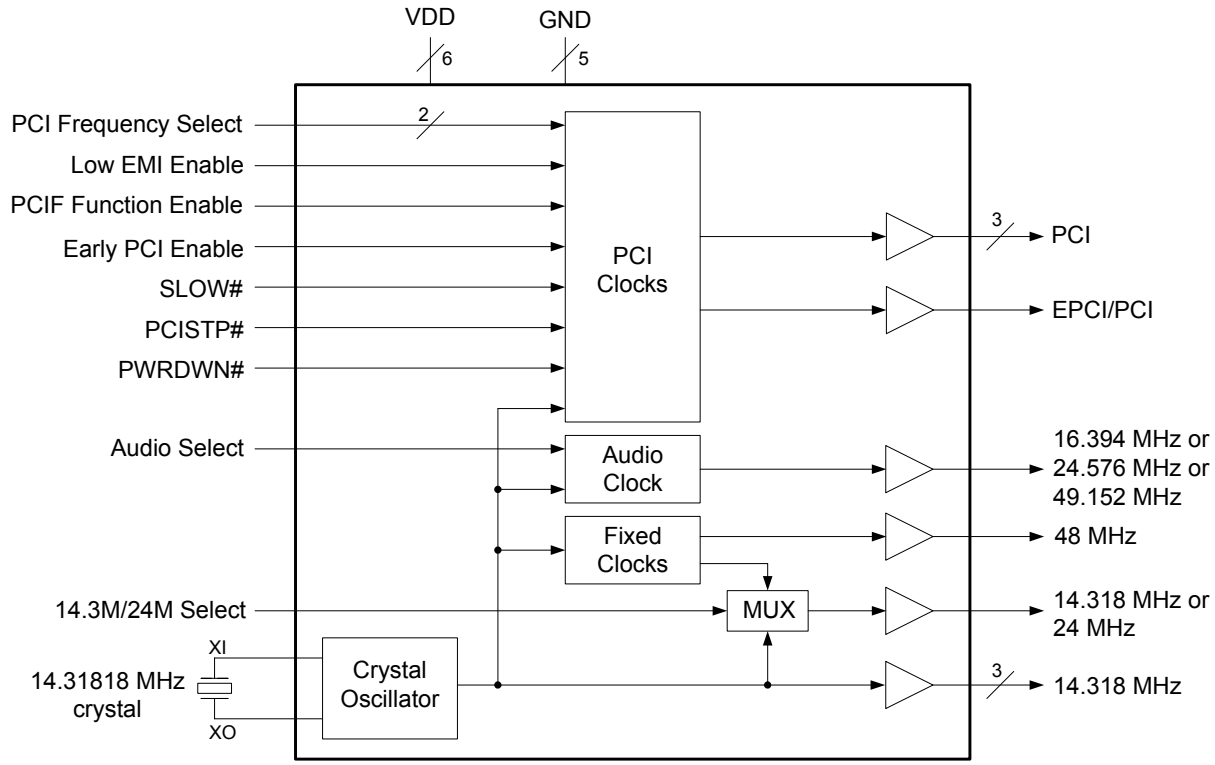
The MK1491-06 is a low-cost, low-jitter, high-performance clock synthesizer for AMD's Geode-based computer and portable appliance applications. Using patented analog Phased-Locked Loop (PLL) techniques, the device accepts a 14.318 MHz crystal input to produce multiple output clocks. It provides selectable PCI local bus and AC97 audio clocks, 24 MHz and 48 MHz clocks for Super I/O and USB, as well as multiple Reference outputs.

The device has multiple power-down modes to reduce power consumption.

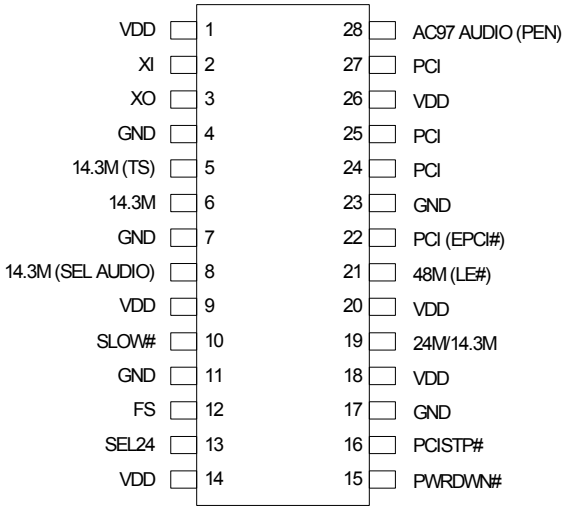
Features

- Packaged in 28-pin SOIC or in 28-pin SSOP
- Pb (lead) free, RoHS compliant
- Provides all critical timing for the AMD Geode companion chip
- Four PCI clocks
- Selectable PCIF on up to 2 outputs
- Early PCI clock selectability
- Up to 4 Reference clocks
- 48 MHz USB and 24MHz SIO support
- AC97 audio clock
- Multiple power down modes
- Low EMI Enable pin reduces EMI radiation on PCI clocks (patented)
- Operating voltage of 3.3 V ±5%

Block Diagram



Pin Assignment



Early PCI Control Table

EPCI#	PCI (Pin 22)
0	1 ns early
1	Normal

EMI Control

LE#	PCI Low EMI
0	ON
1	OFF

Spread direction is DOWN.

PCI Frequency Select Table

TS	FS	PCI
0	0	Tristate all clocks
0	1	Reserved
M	0	30 MHz
M	1	33.3 MHz
1	0	25 MHz
1	1	37.5 MHz

24M/14.3M Frequency Select Table

SEL24	24M/14.3M
0	14.31818 MHz
1	24.0 MHz

PCIF Enable Control

PEN	Pin 25	Pin 24
0	PCI	PCI
M	PCI	PCIF
1	PCIF	PCIF

PCIF continues to run in PCI STOP mode. See table on page 4.

AC97 Audio Frequency Select

SEL AUDIO	AC97 AUDIO
0	16.9344 MHz
M	24.576 MHz
1	49.152 MHz

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1, 9, 14	VDD	P	Connect to +3.3 V. Must be same voltage on all pins.
2	XI	I	Crystal connection. Connect to a 14.31818 MHz crystal or input clock.
3	XO	O	Crystal connection. Connect to a 14.31818 MHz crystal, or leave unconnected for clock.
4, 7, 11, 17, 23	GND	P	Connect to Ground.
5	14.3M (TS)	TI/O	14.318 MHz output. Input control for all clocks per table above.
6	14.3M	O	14.318 MHz buffered reference clock output.

Pin Number	Pin Name	Pin Type	Pin Description
8	14.3M (SEL AUDIO)	TI/O	14.318 MHz output and audio frequency select input per table above.
10	SLOW#	I	PCI normal or slow mode select input per table on page 4.
12	FS	I	Frequency Select for PCI clocks per table above.
13	SEL24	I	Fixed frequency select input per table above. Selects frequency on pin 19.
15	PWRDWN#	I	Power down control; defined in table on page 4.
16	PCISTP#	I	PCI Stop power down control; defined in table on page 4.
18, 20, 26	VDD	P	Connect to +3.3 V. Must be same voltage on all pins.
19	24M/14.3M	O	Fixed frequency clock output per table above.
21	48 (LE#)	I/O	Fixed frequency clock output and low EMI (spread spectrum) enable input per table above.
22	PCI (EPCI#)	I/O	PCI Output clock that can be early. Input control for Early PCI per table above.
24	PCI	O	PCI Output clock. PCI/PCIF control set by PEN per table above.
25	PCI	O	PCI Output clock. PCI/PCIF control set by PEN per table above.
27	PCI	O	PCI Output clock.
28	AC97 AUDIO (PEN)	TI/O	Audio clock output and PCIF Function Enable per table above.

KEY:

I = Input

TI = Tri-level

O = Output

P = Power supply connection

(T)I/O = Input on power up, becomes an Output after 10 ms

Weak internal pull-up resistors are present on SEL24, EPCI#, FS, LE#, PCISTP#, and SLOW#. These pins should be tied to VDD or GND, and not be left floating. Internal resistors on PEN, SEL AUDIO, and TS pull to mid-level (M).

Power Down Control Table

PCISTP#	PWRDWN#	SLOW#	MODE	PCI	PCIF	24/14.3	14.3	Description
X	0	X	Power down	LOW	LOW	LOW	LOW	All outputs low. PLL's and oscillators off.
0	1	X	PCI STOP	LOW	ON	ON	ON	PCI clocks synchronously enter and leave low state.
1	1	X	ON	ON	ON	ON	ON	All clocks on.

Key: 1 = connected to VDD, 0 = connected to ground, X = any valid logic level, combination inputs/outputs should be connected to VDD or ground through a 10 kΩ resistor as shown below.

Power-on Default Conditions

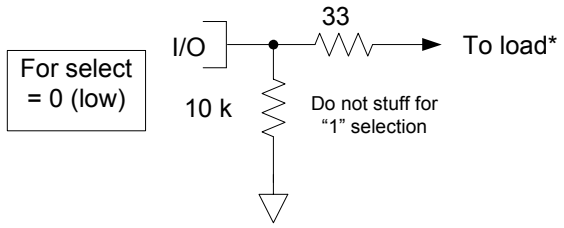
Pin #	Function	Default	Condition
5	TS	M	All outputs enabled.
8	SEL AUDIO	M	Audio clock (pin 28) set to 24.576 MHz
10	SLOW#	1	PCI clocks set to 33.3 MHz. Refer to Power Down Control Table above.
12	FS	1	PCI frequency = 33.3 MHz.
13	SEL 24	1	24M/14.3M (pin 19) set to 24 MHz.
15	PWRDWN#	1	All clocks running.
16	PCISTP#	1	PCI clocks running.
21	LE#	1	Low EMI function OFF
22	EPCI#	1	Pin 22 set to normal PCI signal (not early).
28	PEN	M	PCI (pin 25) set to PCI clock (33.33 MHz). PCI (pin 24) set to PCIF clock (33.33 MHz).

External Components

The MK1491-06 requires some inexpensive external components for proper operation. Decoupling capacitors of 0.1µF should be connected on each VDD pin to ground, as close to the MK1491-06 as possible. A series termination resistor of 33Ω may be used for each clock output. See the discussion below for other external resistors required for proper I/O operation. The 14.3 MHz oscillator has internal caps that provide the proper load for a parallel resonant crystal with CL=18 pF. For tuning with other values of C_L, the formula 2*(C_L-18) gives the value of each capacitor that should be connected between X1 and ground and X2 and ground.

I/O Structure

The MK1491-06 provides more functionality in a 28-pin package by using a unique I/O technique. The device checks the status of all I/O pins during power-up and at exit from the Power Down state. This status (pulled high, low, or mid-level) then determines the frequency selections and power down modes (see the tables on pages 2 and 4). Within 10ms after power up, the inputs change to outputs and the clocks start up. In the diagrams to the right, the 33Ω resistors are the normal output termination resistors. The 10kΩ resistor pulls low to generate a logic zero. Weak internal pull-up resistors are present on SEL24, EPCI#, FS, LE#, PCISTP#, and SLOW#. These pins should be connected directly to VDD or GND if not under active control. Internal resistors on PEN, SEL AUDIO, and TS pull to a mid-level (M).



*Note: Do not use a TTL load. This will overcome the 10 kΩ pull-down and force the input to a logic 1.

Absolute Maximum Ratings

Item	Rating
	°
	°
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

VDD = 3.3 V ±5% °

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Input High Voltage	V_{IH}		2			V
Input Mid-level Voltage	V_{IM}		1.2	1.4	1.6	V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Operating Supply Current	IDD	33 MHz, no load		30		mA
Power Down Mode Supply Current				15		µA
Short Circuit Current, SIngle Output Driver		VDD = 3.3 V		±60		mA
Input Capacitance	C_{IN}			7		pF

AC Electrical Characteristics

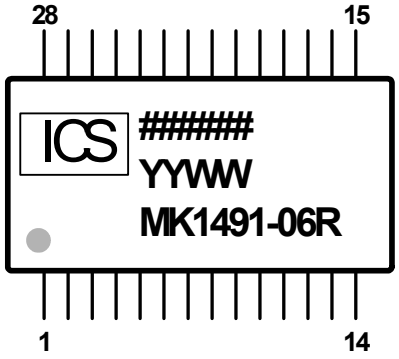
Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}			14.31818		MHz
Output Clock Rise Time	t_{OR}	20% to 80%			1.5	ns
Output Clock Fall Time	t_{OF}	80% to 20%			1.5	ns
Output Clock Duty Cycle, all MHz Clocks	t_{OD}	At 1.5 V	45	49 to 51	55	%
PCI Output to Output Skew		Rising edges at 1.5 V			500	ps
Skew of EPCI with respect to PCI				1		ns
Cycle-to-Cycle Jitter, PCI clocks				250		ps
EMI Reduction, peaks of 5th - 19th odd harmonics		33.3 MHz PCI Clock		6	11	dB
Power-up Time, PWRDWN# High to all Clocks Stable				8	20	ms
Power-on Time, applied VDD to all Clocks Stable				12	25	ms

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		100		°C/W
	θ_{JA}	1 m/s air flow		80		°C/W
	θ_{JA}	3 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

Marking Diagram

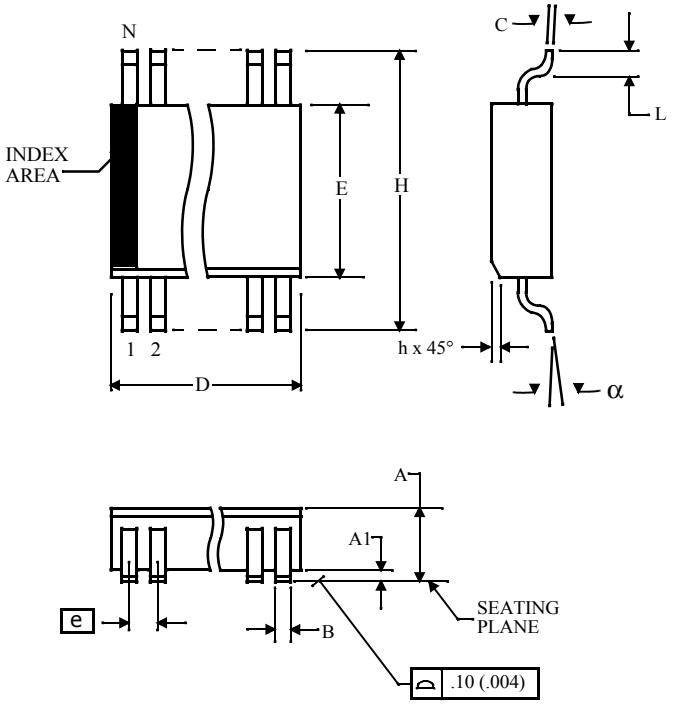


Notes:

1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. Bottom marking: country of origin.

Package Outline and Package Dimensions (28-pin SOIC, 150 mil Body)

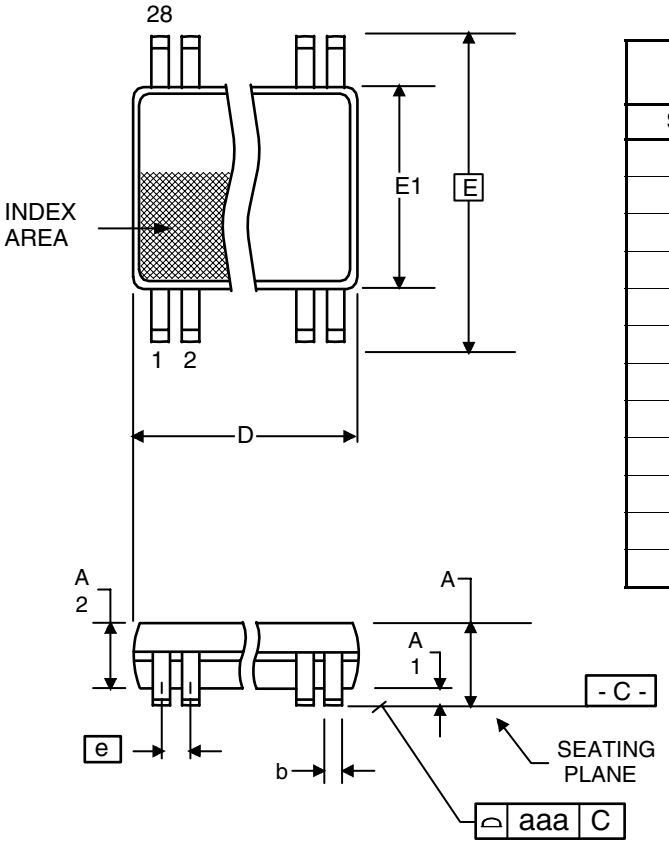
Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A		2.65		0.104
A1	0.10		.0040	
B	0.33	0.51	.013	.020
C	0.18	0.32	.007	.013
D	17.70	18.40	.697	.724
E	7.40	7.60	.291	.299
e	1.27 Basic		0.050 Basic	
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Package Outline and Package Dimensions (28-pin SSOP, 150 mil Body, 0.025 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	.008	.012
C	0.18	0.25	.007	.010
D	9.80	10.00	.386	.394
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1491-06RLF	MK1491-06RLF	Tubes	28-pin SSOP	0 to +70° C
MK1491-06RLFTR	MK1491-06RLF	Tape and Reel	28-pin SSOP	0 to +70° C
MK1491-06SLF	MK1491-06SLF	Tubes	28-pin SOIC	0 to +70° C
MK1491-06SLFTR	MK1491-06SLF	Tape and Reel	28-pin SOIC	0 to +70° C

"LF" denotes Pb (lead) free package.

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