

FEATURES

- <1 pC charge injection over full signal range
- 1 pF off capacitance
- 33 V supply range
- 120 Ω on resistance
- Fully specified at ± 15 V/+12 V
- 3 V logic compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- Available in 16-lead TSSOP, 4 mm $\times$ 4 mm LFCSP_VQ, and 16-lead SOIC
- Typical power consumption < 0.03 μ W

APPLICATIONS

- Audio and video routing
- Automatic test equipment
- Data-acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Communication systems

GENERAL DESCRIPTION

The ADG1208 and ADG1209 are monolithic, $\text{iCMOS}^{\circledast}$ analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG1208 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG1209 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

The iCMOS (industrial CMOS) modular manufacturing process combines high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, iCMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

Rev. B

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FUNCTIONAL BLOCK DIAGRAMS

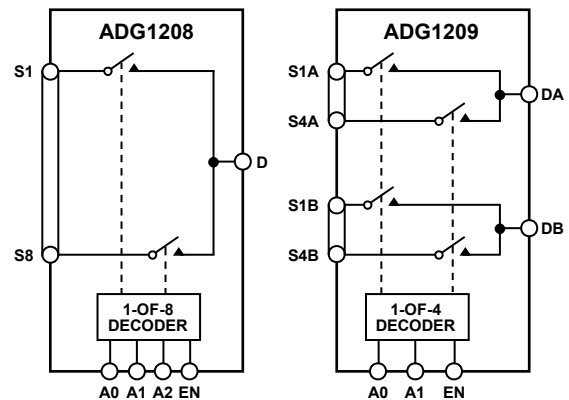


Figure 1.

The ultralow capacitance and exceptionally low charge injection of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Figure 2 shows that there is minimum charge injection over the entire signal range of the device. iCMOS construction also ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

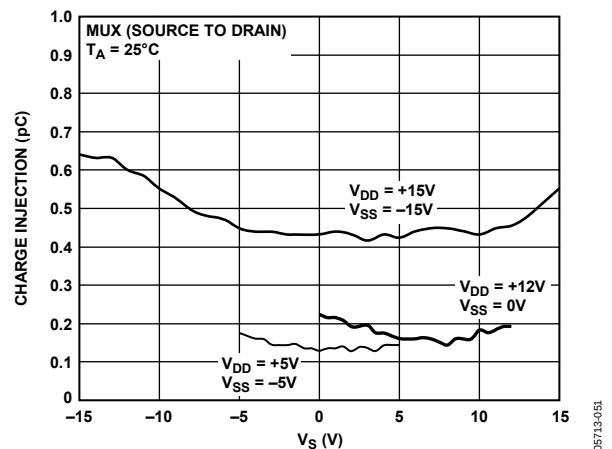


Figure 2. Source to Drain Charge Injection vs. Source Voltage

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REVISION HISTORY

1/09—Rev. A to Rev. B	
Change to I _{DD} Parameter, Table 1	4
Change to I _{DD} Parameter, Table 2	6
4/07—Rev. 0 to Rev. A	
Added 16-lead SOIC	Universal
Changes to Table 1.....	3
Changes to Table 2.....	5
Changes to Figure 10 and Figure 11.....	10
Updated Outline Dimensions	17
Changes to Ordering Guide	18
4/06—Revision 0: Initial Version	

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.¹

Table 1.

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance, R_{ON}	120			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$, see Figure 29
	200	240	270	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
	6	10	12	Ω max	
On Resistance Flatness, R_{FLAT} (On)	20			Ω typ	$V_S = -5\text{ V}/0\text{ V}/+5\text{ V}$, $I_S = -1\text{ mA}$
	64	76	83	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.003			nA typ	$V_D = \pm 10\text{ V}$, $V_S = -10\text{ V}$, see Figure 30
	± 0.1	± 0.6	± 1	nA max	
Drain Off Leakage, I_D (Off)	± 0.003			nA typ	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$, see Figure 30
ADG1208	± 0.1	± 0.6	± 1	nA max	
ADG1209	± 0.1	± 0.6	± 1	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.02			nA typ	$V_S = V_D = \pm 10\text{ V}$, see Figure 31
ADG1208	± 0.2	± 0.6	± 1	nA max	
ADG1209	± 0.2	± 0.6	± 1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	± 0.005			μA max	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS²					
Transition Time, $t_{TRANSITION}$	80			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	130	165	185	ns max	$V_S = 10\text{ V}$, see Figure 32
t_{ON} (EN)	75			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	95	105	115	ns max	$V_S = 10\text{ V}$, see Figure 34
t_{OFF} (EN)	83			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	100	125	140	ns max	$V_S = 10\text{ V}$, see Figure 34
Break-Before-Make Time Delay, t_{BBM}	25			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = 10\text{ V}$, see Figure 33
Charge Injection	0.4			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 35
Off Isolation	–85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 36
Channel-to-Channel Crosstalk	–85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 38
Total Harmonic Distortion + Noise	0.15			% typ	$R_L = 10\text{ k}\Omega$, 5 V rms, $f = 20\text{ Hz}$ to 20 kHz, see Figure 39
–3 dB Bandwidth	550			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 37
C_S (Off)	1			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
	1.5			pF max	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
C_D (Off) ADG1208	6			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
	7			pF max	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
C_D (Off) ADG1209	3.5			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
	4.5			pF max	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$

ADG1208/ADG1209

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
C_D, C_S (On) ADG1208	7			pF typ	$f = 1 \text{ MHz}, V_S = 0 \text{ V}$
	8			pF max	$f = 1 \text{ MHz}, V_S = 0 \text{ V}$
C_D, C_S (On) ADG1209	5			pF typ	$f = 1 \text{ MHz}, V_S = 0 \text{ V}$
	6			pF max	$f = 1 \text{ MHz}, V_S = 0 \text{ V}$
POWER REQUIREMENTS					
I_{DD}	0.002		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$ Digital inputs = 0 V or V_{DD}
I_{DD}	220		380	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 5 V
I_{SS}	0.002		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
I_{SS}	0.002		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 5 V
V_{DD}/V_{SS}			$\pm 5/\pm 16.5$	V min/max	$ V_{DD} = V_{SS} $

¹ Temperature range is as follows: Y version: –40°C to +125°C.

² Guaranteed by design, not subject to production test.

SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.¹

Table 2.

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	300			Ω typ	$V_S = 0\text{ V}$ to 10 V , $I_S = -1\text{ mA}$, see Figure 29
	475	567	625	Ω max	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels, ΔR_{ON}	5			Ω typ	$V_S = 0\text{ V}$ to 10 V , $I_S = -1\text{ mA}$
	16	26	27	Ω max	
On Resistance Flatness, R_{FLAT} (On)	60			Ω typ	$V_S = 3\text{ V}/6\text{ V}/9\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.003			nA typ	$V_{DD} = 13.2\text{ V}$
	± 0.1	± 0.6	± 1	nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$, see Figure 30
Drain Off Leakage, I_D (Off)	± 0.003			nA typ	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$, see Figure 30
ADG1208	± 0.1	± 0.6	± 1	nA max	
ADG1209	± 0.1	± 0.6	± 1	nA max	
Channel On Leakage I_D , I_S (On)	± 0.02			nA typ	$V_S = V_D = 1\text{ V}$ or 10 V , see Figure 31
ADG1208	± 0.2	± 0.6	± 1	nA max	
ADG1209	± 0.2	± 0.6	± 1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	± 0.001			μA max	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS²					
Transition Time, $t_{TRANSITION}$	100			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	170	210	235		$V_S = 8\text{ V}$, see Figure 32
t_{ON} (EN)	90			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	110	140	160		$V_S = 8\text{ V}$, see Figure 34
t_{OFF} (EN)	105			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	130	155	175		$V_S = 8\text{ V}$, see Figure 34
Break-Before-Make Time Delay, t_{BBM}	45			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			20	ns min	$V_{S1} = V_{S2} = 8\text{ V}$, see Figure 33
Charge Injection	–0.2			pC typ	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 35
Off Isolation	–85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 36
Channel-to-Channel Crosstalk	–85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 38
–3 dB Bandwidth	450			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 37
C_S (Off)	1.2			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
	1.8			pF max	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
C_D (Off) ADG1208	7.5			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
	9			pF max	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
C_D (Off) ADG1209	4.5			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
	5.5			pF max	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
C_D , C_S (On) ADG1208	9			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
	10.5			pF max	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
C_D , C_S (On) ADG1209	6			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
	7.5			pF max	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$

ADG1208/ADG1209

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = 13.2\text{ V}$
I_{DD}	0.002		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
I_{DD}	220		380	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 5 V
V_{DD}			5/16.5	V min/max	$V_{SS} = 0\text{ V}$, GND = 0 V

¹ Temperature range is as follows: Y version: –40°C to +125°C.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs ¹	$V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$ or 30 mA (whichever occurs first)
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	100 mA
Operating Temperature Range	
Industrial (Y Version)	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} , Thermal Impedance, TSSOP	112°C/W
θ_{JA} , Thermal Impedance, LFCSP_VQ	30.4°C/W
θ_{JA} , Thermal Impedance, SOIC_N	77°C/W
Reflow Soldering Peak Temperature (Pb-Free)	260(+0/−5)°C

¹ Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG1208/ADG1209

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

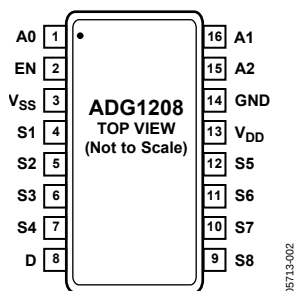


Figure 3. ADG1208 Pin Configuration (TSSOP/SOIC)

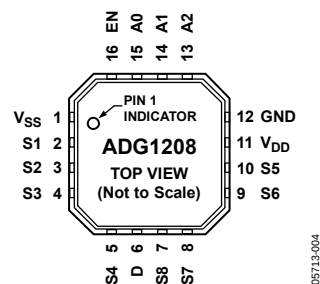


Figure 4. ADG1208 Pin Configuration (LFCSP_VQ), Exposed Pad Tied to Substrate, V_{SS}

Table 4. ADG1208 Pin Function Descriptions

Pin Number		Mnemonic	Description
TSSOP/SOIC	LFCSP_VQ		
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, A_x logic inputs determine on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, it can be connected to ground.
4	2	S1	Source Terminal 1. Can be an input or an output.
5	3	S2	Source Terminal 2. Can be an input or an output.
6	4	S3	Source Terminal 3. Can be an input or an output.
7	5	S4	Source Terminal 4. Can be an input or an output.
8	6	D	Drain Terminal. Can be an input or an output.
9	7	S8	Source Terminal 8. Can be an input or an output.
10	8	S7	Source Terminal 7. Can be an input or an output.
11	9	S6	Source Terminal 6. Can be an input or an output.
12	10	S5	Source Terminal 5. Can be an input or an output.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	GND	Ground (0 V) Reference.
15	13	A2	Logic Control Input.
16	14	A1	Logic Control Input.

Table 5. ADG1208 Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

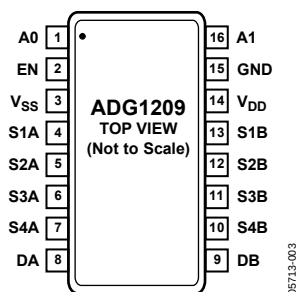


Figure 5. ADG1209 Pin Configuration (TSSOP/SOIC)

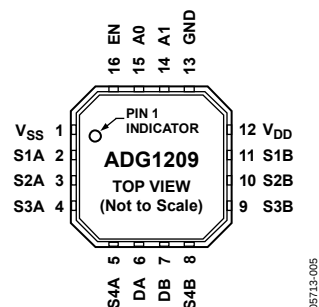


Figure 6. ADG1209 Pin Configurations (LFCSP_VQ), Exposed Pad Tied to Substrate, V_{SS}

Table 6. ADG1209 Pin Function Descriptions

Pin Number		Mnemonic	Description
TSSOP/SOIC	LFCSP_VQ		
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	1	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, it can be connected to ground.
4	2	S1A	Source Terminal 1A. Can be an input or an output.
5	3	S2A	Source Terminal 2A. Can be an input or an output.
6	4	S3A	Source Terminal 3A. Can be an input or an output.
7	5	S4A	Source Terminal 4A. Can be an input or an output.
8	6	DA	Drain Terminal A. Can be an input or an output.
9	7	DB	Drain Terminal B. Can be an input or an output.
10	8	S4B	Source Terminal 4B. Can be an input or an output.
11	9	S3B	Source Terminal 3B. Can be an input or an output.
12	10	S2B	Source Terminal 2B. Can be an input or an output.
13	11	S1B	Source Terminal 1B. Can be an input or an output.
14	12	V _{DD}	Most Positive Power Supply Potential.
15	13	GND	Ground (0 V) Reference.
16	14	A1	Logic Control Input.

Table 7. ADG1209 Truth Table

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TYPICAL PERFORMANCE CHARACTERISTICS

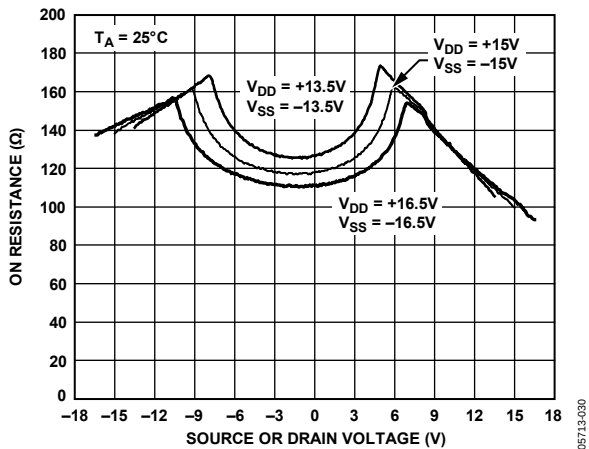


Figure 7. On Resistance as a Function of V_D (V_S) for Dual Supply

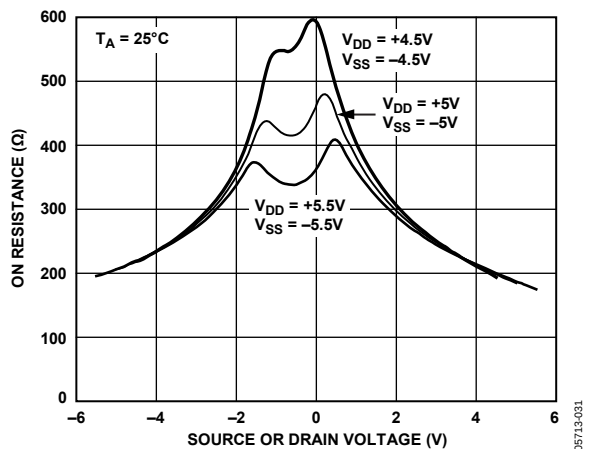


Figure 8. On Resistance as a Function of V_D (V_S) for Dual Supply

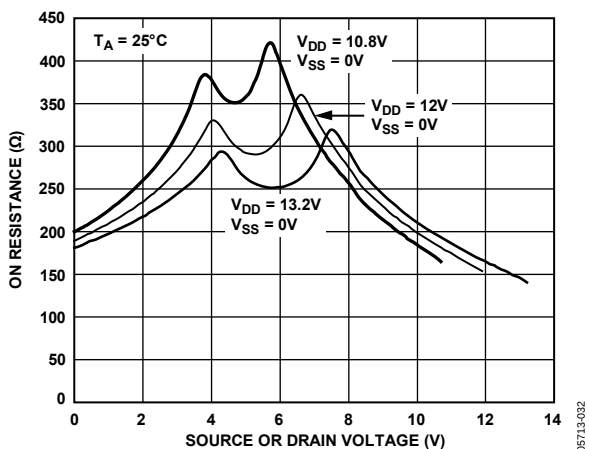


Figure 9. On Resistance as a Function of V_D (V_S) for Single Supply

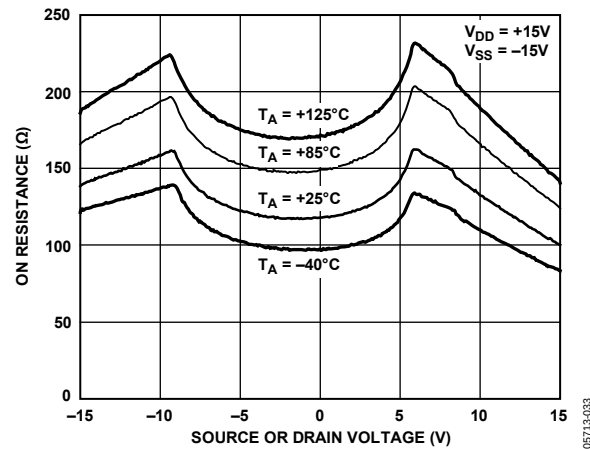


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

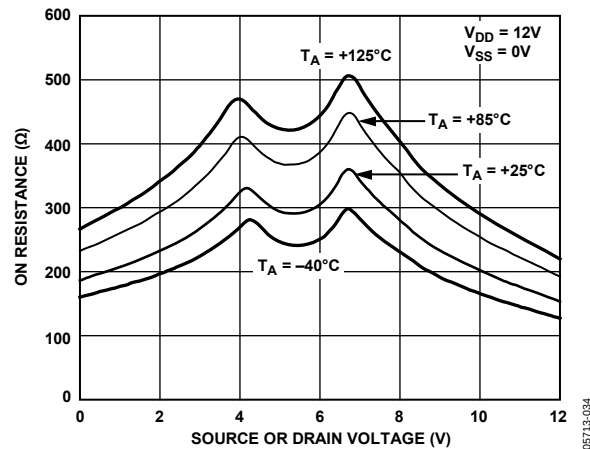


Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

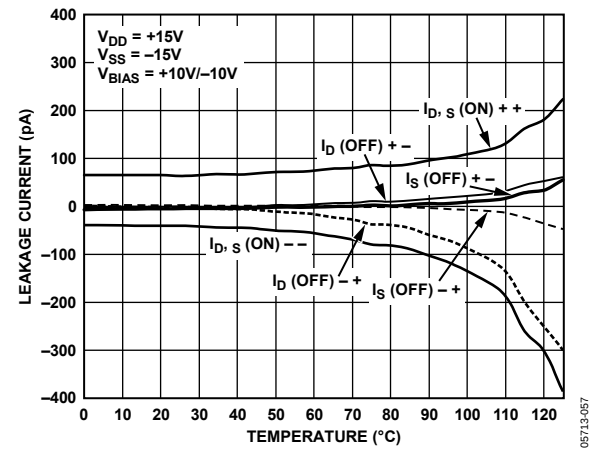


Figure 12. ADG1208 Leakage Currents as a Function of Temperature, Dual Supply

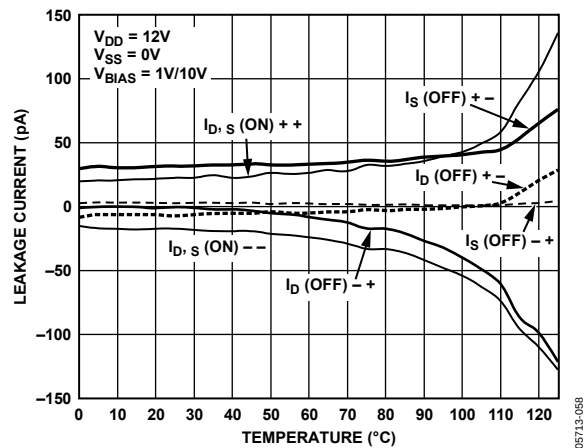


Figure 13. ADG1208 Leakage Currents as a Function of Temperature, Single Supply

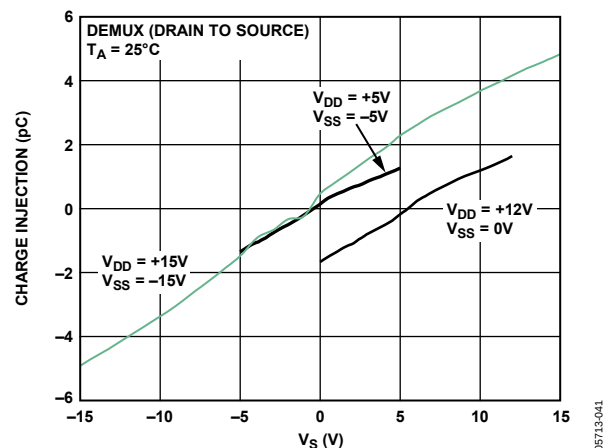


Figure 16. Drain-to-Source Charge Injection vs. Source Voltage

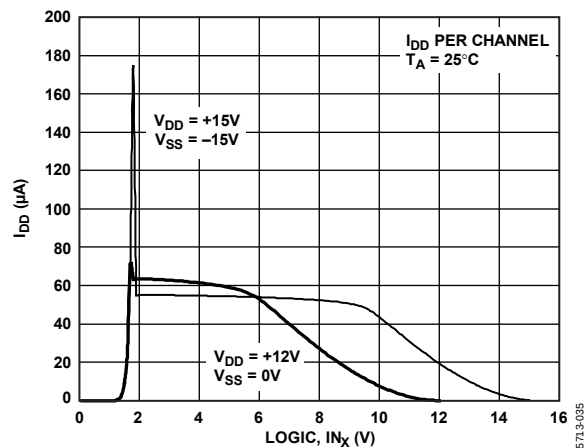


Figure 14. I_{DD} vs. Logic Level

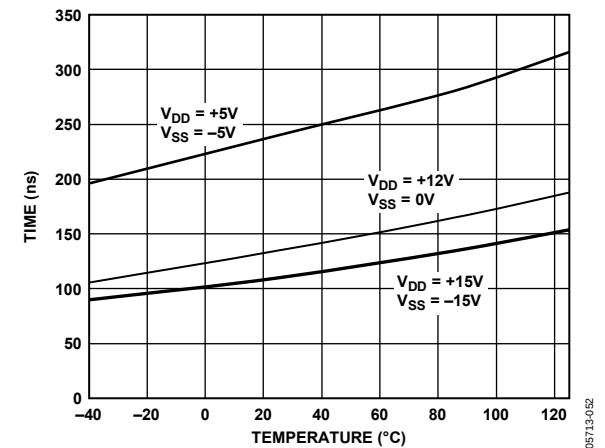


Figure 17. t_{ON}/t_{OFF} Times vs. Temperature

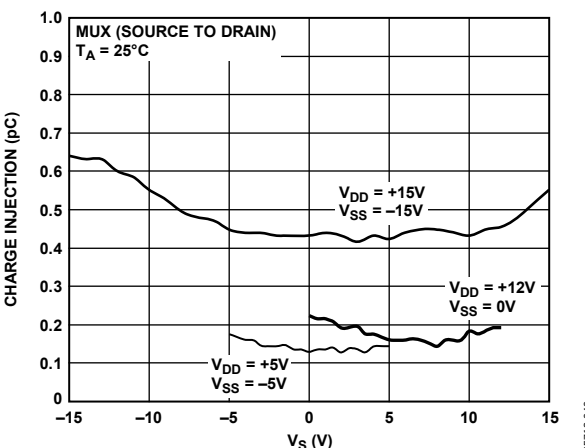


Figure 15. Source-to-Drain Charge Injection vs. Source Voltage

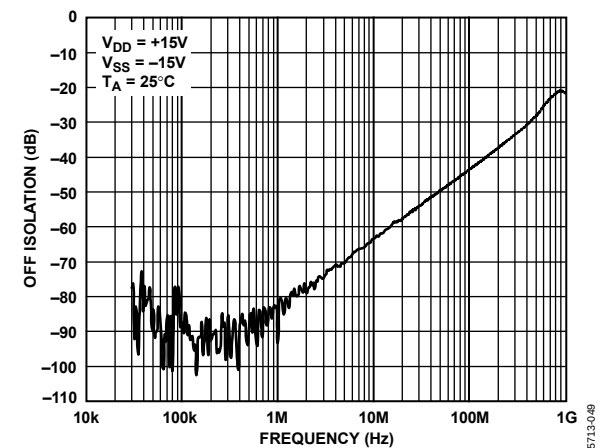


Figure 18. Off Isolation vs. Frequency

ADG1208/ADG1209

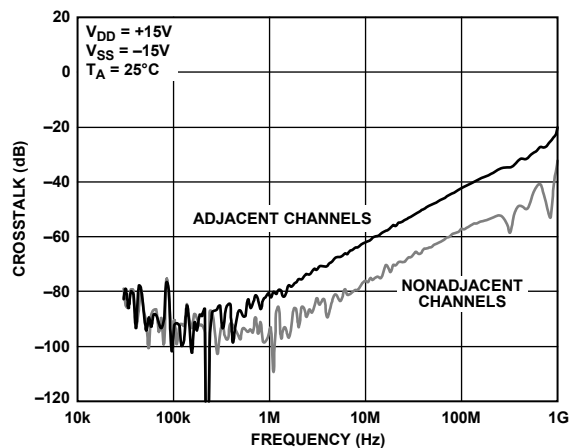


Figure 19. ADG1208 Crosstalk vs. Frequency

05713-042

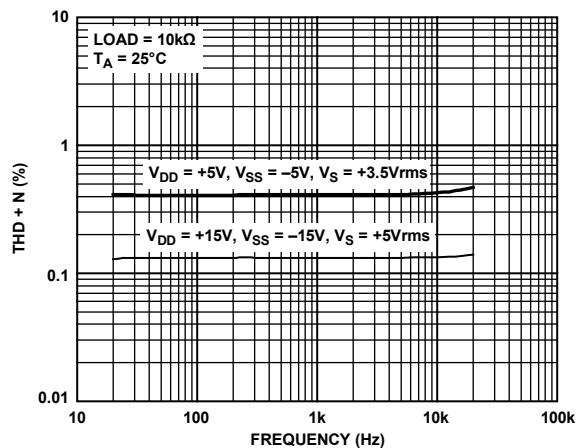


Figure 22. THD + N vs. Frequency

05713-036

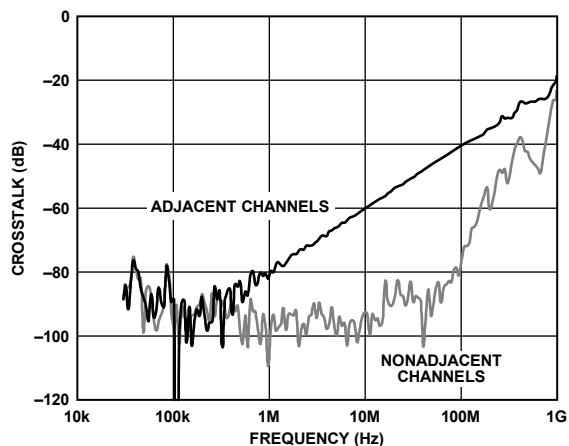


Figure 20. ADG1209 Crosstalk vs. Frequency

05713-053

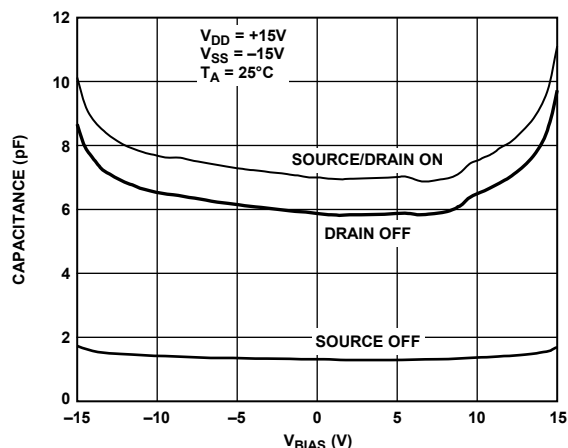


Figure 23. ADG1208 Capacitance vs. Source Voltage, ± 15 V Dual Supply

05713-043

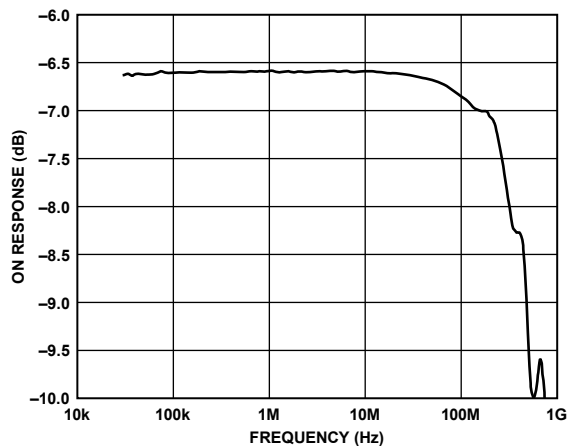


Figure 21. On Response vs. Frequency

05713-054

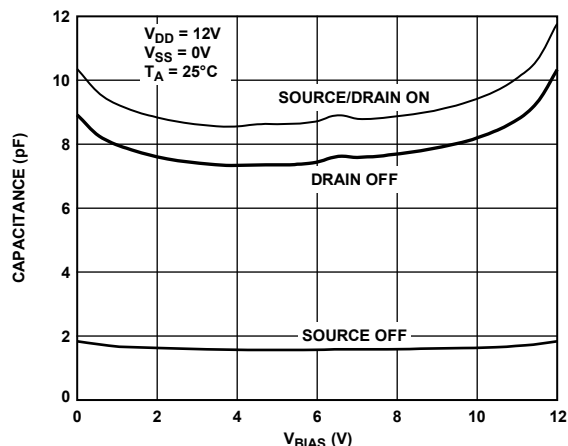


Figure 24. ADG1208 Capacitance vs. Source Voltage, 12 V Single Supply

05713-045

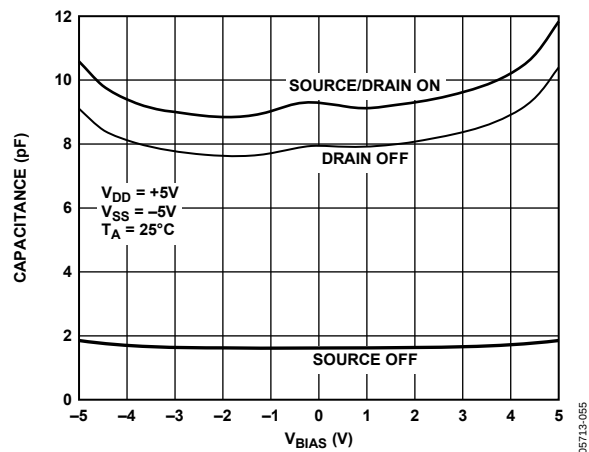


Figure 25. ADG1208 Capacitance vs. Source Voltage, ± 5 V Dual Supply

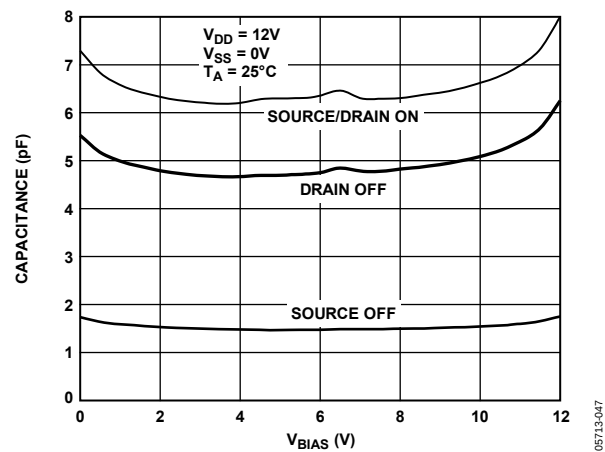


Figure 27. ADG1209 Capacitance vs. Source Voltage, 12 V Single Supply

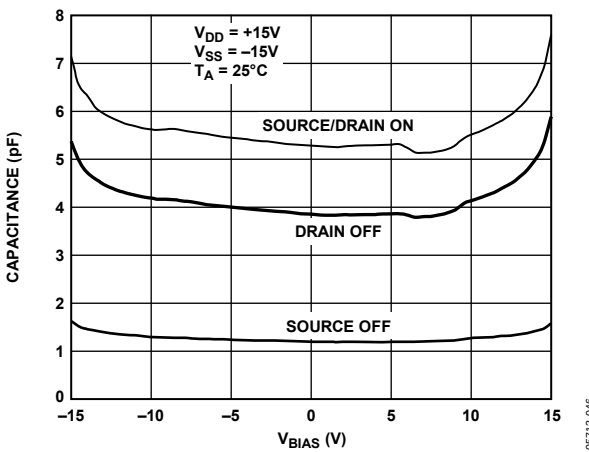


Figure 26. ADG1209 Capacitance vs. Source Voltage, ± 15 V Dual Supply

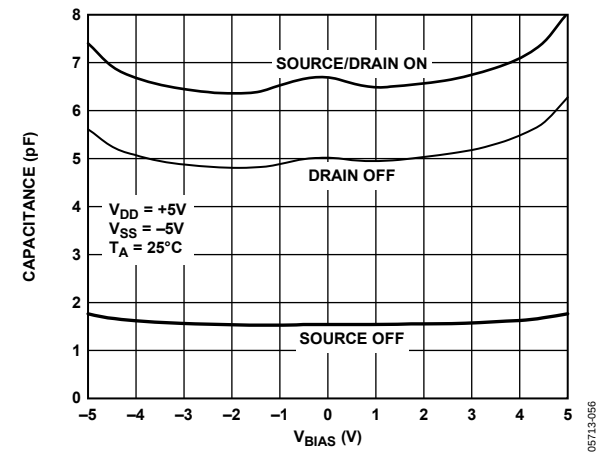


Figure 28. ADG1209 Capacitance vs. Source Voltage, ± 5 V Dual Supply

TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

ΔR_{ON}

Difference between the R_{ON} of any two channels.

I_S (Off)

Source leakage current when the switch is off.

I_D (Off)

Drain leakage current when the switch is off.

I_D, I_S (On)

Channel leakage current when the switch is on.

V_D (V_S)

Analog voltage on Terminal D, Terminal S.

C_S (Off)

Channel input capacitance for off condition.

C_D (Off)

Channel output capacitance for off condition.

C_D, C_S (On)

On switch capacitance.

C_{IN}

Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{TRANSITION}

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}

Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

Off Isolation

A measure of unwanted signal coupling through an off channel.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TEST CIRCUITS

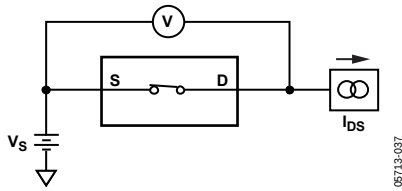


Figure 29. On Resistance

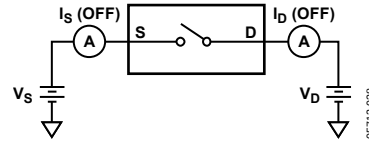


Figure 30. Off Leakage

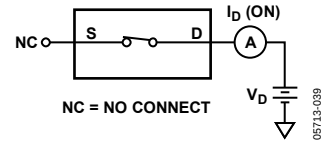


Figure 31. On Leakage

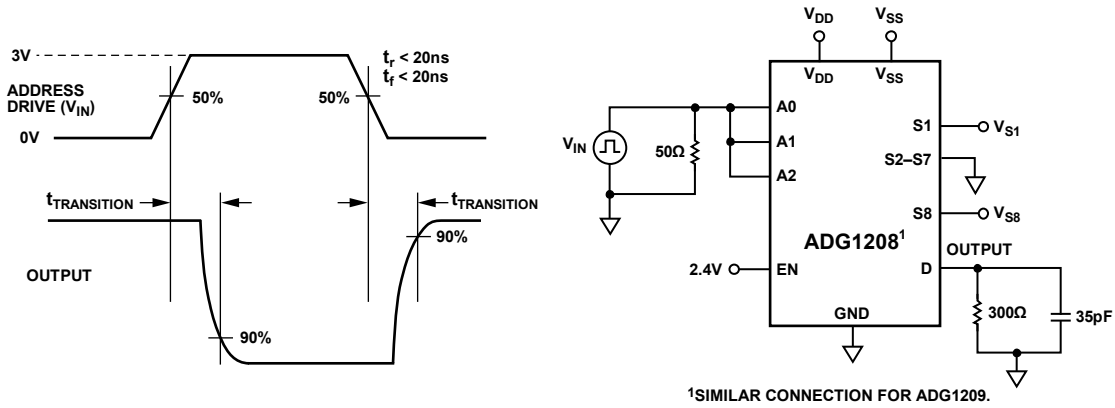


Figure 32. Address to Output Switching Times, $t_{\text{TRANSITION}}$

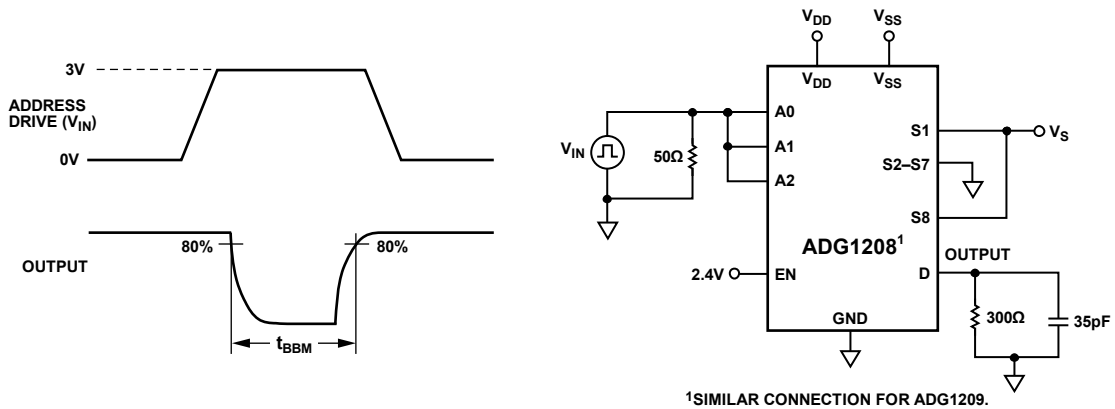


Figure 33. Break-Before-Make Delay, t_{BBM}

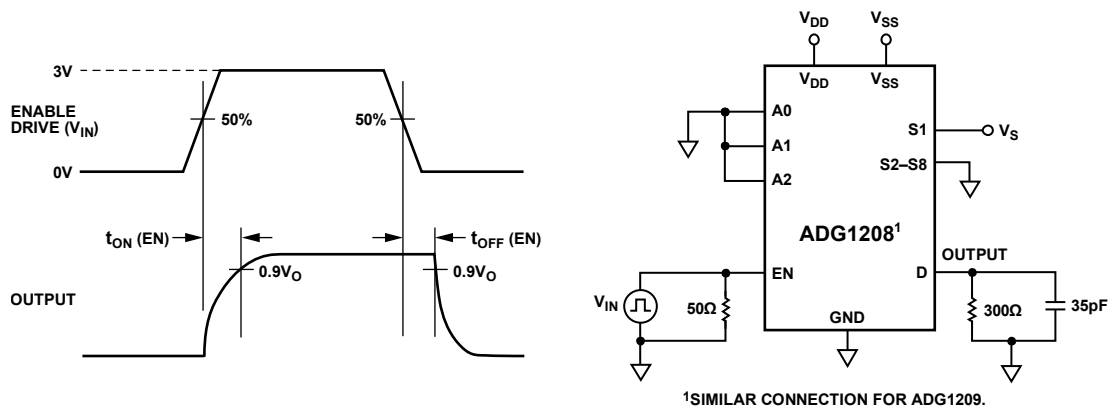
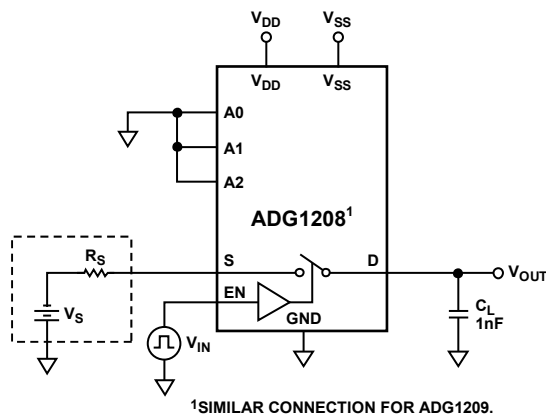
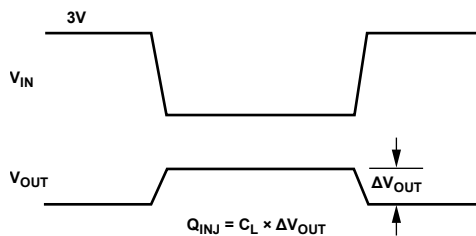


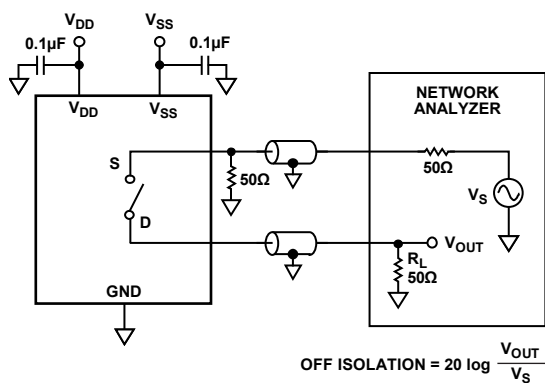
Figure 34. Enable Delay, $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$

ADG1208/ADG1209



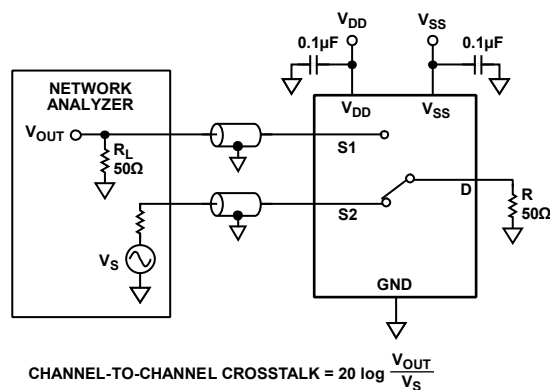
05713-025

Figure 35. Charge Injection



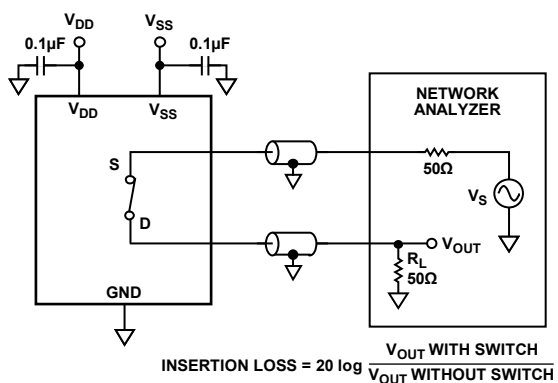
05713-026

Figure 36. Off Isolation



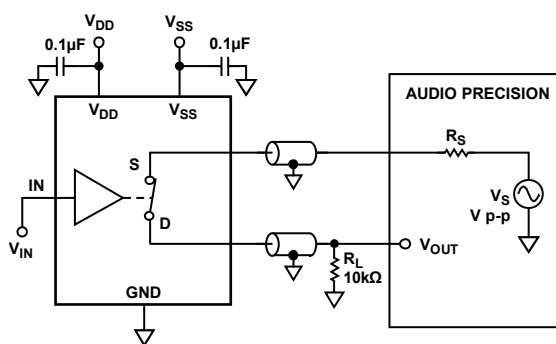
05713-028

Figure 38. Channel-to-Channel Crosstalk



05713-027

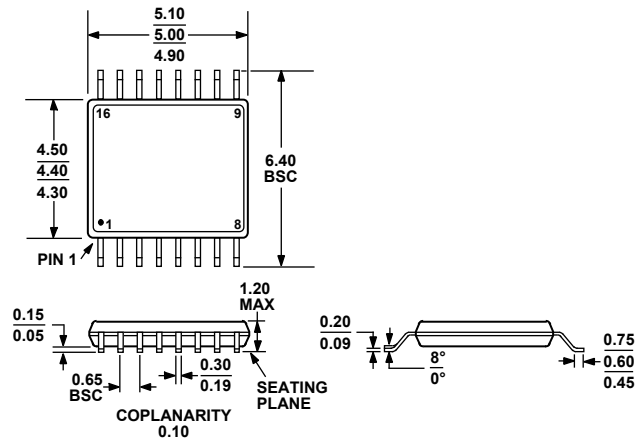
Figure 37. Bandwidth



05713-029

Figure 39. THD + Noise

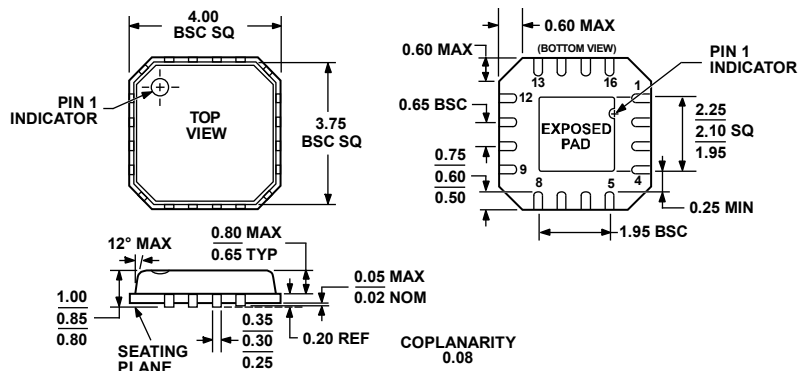
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 40. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

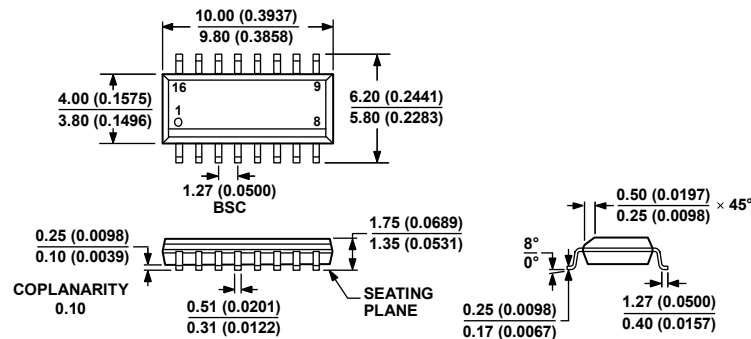
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 41. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad (CP-16-4)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 42. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-16)

Dimensions shown in millimeters and (inches)

ADG1208/ADG1209

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1208YRUZ ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1208YRUZ-REEL7 ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1208YCPZ-REEL ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADG1208YCPZ-REEL7 ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADG1208YRZ ¹	–40°C to +125°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1208YRZ-REEL7 ¹	–40°C to +125°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1209YRUZ ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1209YRUZ-REEL7 ¹	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1209YCPZ-REEL ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADG1209YCPZ-REEL7 ¹	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADG1209YRZ ¹	–40°C to +125°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1209YRZ-REEL7 ¹	–40°C to +125°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16

¹ Z = RoHS compliant part.

NOTES

NOTES