

Rail-to-rail input/output 8MHz operational amplifiers

Features

- Rail-to-rail input and output
- Wide bandwidth
- Low power consumption: 1.1mA max.
- Unity gain stability
- High output current: 35mA
- Operating from 2.5V to 5.5V
- Low input bias current, 1pA typ
- ESD Internal protection $\geq 5kV$
- Latch-up immunity

Applications

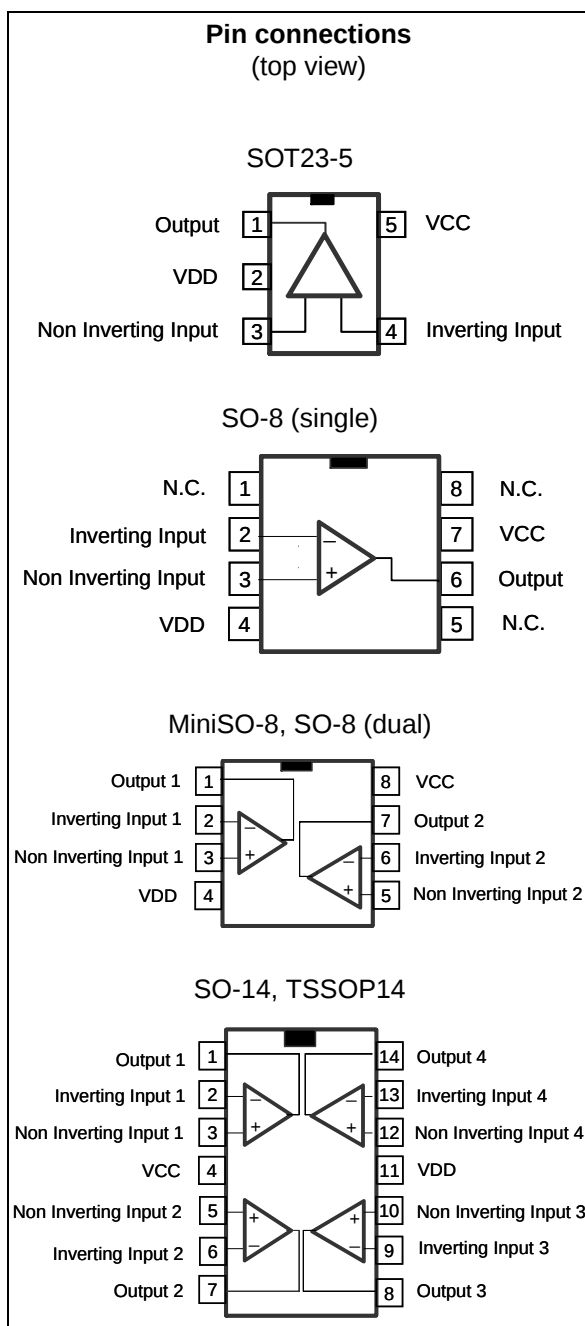
- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation
- Automotive

Description

The TSV911/2/4 family of single, dual and quad operational amplifiers offers low voltage operation and rail-to-rail input and output.

This family features an excellent speed/power consumption ratio, offering an 8MHz gain-bandwidth product while consuming only 1.1mA max at 5V supply voltage. These op-amps are unity gain stable for capacitive loads up to 200pF. They also feature an ultra-low input bias current.

These characteristics make the TSV911/2/4 family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.



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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_{id}	Differential input voltage ⁽²⁾	$\pm V_{CC}$	V
V_{in}	Input voltage ⁽³⁾	$V_{DD}-0.2$ to $V_{CC}+0.2$	V
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient ^{(4) (5)}		
	SOT23-5	250	°C/W
	SO-8	125	
	MiniSO-8	190	
	SO-14	103	
	TSSOP14	100	
R_{thjc}	Thermal resistance junction to case		
	SOT23-5	81	°C/W
	SO-8	40	
	MiniSO-8	39	
	SO-14	31	
	TSSOP14	32	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model ⁽⁶⁾	5	kV
	MM: machine model ⁽⁷⁾	300	V
	CDM: charged device model ⁽⁸⁾		V
	SOT23-5, SO-8, MiniSO-8	1500	
	TSSOP14	750	
	SO-14	500	
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. $V_{CC}-V_{in}$ must not exceed 6V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: 100pF discharged through a 1.5k Ω resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
7. Machine model: a 200pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). Done for all couples of pin combinations with other pins floating.
8. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{icm}	Common mode input voltage range	$V_{DD} - 0.1$ to $V_{CC} + 0.1$	V
T_{oper}	Operating free air temperature range	-40 to +125	°C

2 Electrical characteristics

Table 3. Electrical characteristics at $V_{CC} = +2.5V$ with $V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	0.1	4.5	mV
	TSV91xA	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	-	7.5	
DV_{io}/DT	Input offset voltage drift		-	2	-	$\mu V/^{\circ}C$
I_{io}	Input offset current	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	1	$10^{(2)}$	pA
I_{ib}	Input bias current	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	-	100	
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0V$ to $2.5V$, $V_{out} = 1.25V$	58	75	-	dB
A_{vd}	Large signal voltage gain	$R_L = 10k\Omega$, $V_{out} = 0.5V$ to $2V$, $T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	80	89	-	dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$	-	15	40	
V_{OL}	Low level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$	-	45	150	mV
I_{out}	I_{sink}	$V_o = 2.5V$, $T = 25^{\circ}C$ $T_{min} < T_{amb} < T_{max}$	18	32	-	mA
	I_{source}	$V_o = 0V$, $T = 25^{\circ}C$ $T_{min} < T_{amb} < T_{max}$	16	-	-	
I_{CC}	Supply current (per operator)	No load, $V_{out}=V_{CC}/2$	-	0.78	1.1	mA
AC performance						
GBP	Gain bandwidth product	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$, $T = 25^{\circ}C$	-	8	-	MHz
F_u	Unity gain frequency	$R_L = 2k\Omega$, $C_L = 100pF$, $T = 25^{\circ}C$	-	7.2	-	MHz
ϕ_m	Phase margin	$R_L = 2k\Omega$, $C_L = 100pF$, $T = 25^{\circ}C$	-	45	-	Degrees
G_m	Gain margin	$R_L = 2k\Omega$, $C_L = 100pF$, $T = 25^{\circ}C$	-	8	-	dB
SR	Slew rate	$R_L = 2k\Omega$, $C_L = 100pF$, $A_v = 1$, $T = 25^{\circ}C$	-	4.5	-	$V/\mu s$
e_n	Equivalent input noise voltage	$f = 10kHz$, $T = 25^{\circ}C$	-	21	-	$\frac{nV}{\sqrt{Hz}}$
THD+ e_n	Total harmonic distortion	$G=1$, $f=1kHz$, $R_L=2k\Omega$, $Bw= 22kHz$, $T=25^{\circ}C$, $V_{icm}=(V_{CC}+1)/2$, $V_{out}=1.1V_{pp}$	-	0.001	-	%

1. All parameter limits at temperatures other than $25^{\circ}C$ are guaranteed by correlation.
2. Guaranteed by design.

Table 4. Electrical characteristics at $V_{CC} = +3.3V$ with $V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	0.1	4.5	mV
	TSV91xA	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	-	7.5	
DV_{io}	Input offset voltage drift		-	2	-	$\mu V/^{\circ}C$
I_{io}	Input offset current	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	1	$10^{(2)}$ 100	pA
I_{ib}	Input bias current	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	1	$10^{(2)}$ 100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0V to 3.3V, $V_{out} = 1.65V$	60	78	-	dB
A_{vd}	Large signal voltage gain	$R_L = 10k\Omega$, $V_{out} = 0.5V$ to $2.8V$, $T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	80 75	90	-	dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$		15 45	40 150	mV
V_{OL}	Low level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$	-	15 45	40 150	mV
I_{out}	I_{sink}	$V_o = 3.3V$, $T = 25^{\circ}C$ $T_{min} < T_{amb} < T_{max}$	18 16	32 -	- -	mA
	I_{source}	$V_o = 0V$, $T = 25^{\circ}C$ $T_{min} < T_{amb} < T_{max}$	18 16	35 -	- -	
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$	-	0.8	1.1	mA
AC performance						
GBP	Gain bandwidth product	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$, $T = 25^{\circ}C$	-	8	-	MHz
F_u	Unity gain frequency	$R_L = 2k\Omega$, $C_L = 100pF$, $T = 25^{\circ}C$	-	7.2	-	MHz
ϕ_m	Phase margin	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$, $T = 25^{\circ}C$	-	45	-	Degrees
G_m	Gain margin	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$, $T = 25^{\circ}C$	-	8	-	dB
SR	Slew rate	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$, $A_v = 1$, $T = 25^{\circ}C$	-	4.5	-	V/ μs
e_n	Equivalent input noise voltage	$f = 10kHz$, $T = 25^{\circ}C$	-	21	-	$\frac{nV}{\sqrt{Hz}}$
THD+ e_n	Total harmonic distortion	$G = 1$, $f = 1kHz$, $R_L = 2k\Omega$, $BW = 22kHz$, $V_{icm} = (V_{CC} + 1)/2$, $V_{out} = 1.9V_{pp}$, $T = 25^{\circ}C$	-	0.0007	-	%

1. All parameter limits at temperatures other than $25^{\circ}C$ are guaranteed by correlation.

2. Guaranteed by design.

Table 5. Electrical characteristics at $V_{CC} = +5V$ with $V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	0.1	4.5	mV
	TSV91xA	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	-	7.5	
DV_{io}	Input offset voltage drift		-	2	-	$\mu V/^{\circ}C$
I_{io}	Input offset current	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	1	$10^{(2)}$ 100	pA
I_{ib}	Input bias current	$T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	-	1	$10^{(2)}$ 100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0V to 5V, $V_{out} = 2.5V$	62	82	-	dB
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$	$V_{CC} = 2.5$ to 5V	70	86	-	dB
A_{vd}	Large signal voltage gain	$R_L = 10k\Omega$, $V_{out} = 0.5V$ to 4.5V, $T = 25^{\circ}C$ $T_{min} < T_{op} < T_{max}$	80 75	91	-	dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$		15 45	40 150	mV
V_{OL}	Low level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$	-	15 45	40 150	mV
I_{out}	I_{sink}	$V_o = 5V$, $T = 25^{\circ}C$ $T_{min} < T_{amb} < T_{max}$	18 16	32 -	- -	mA
	I_{source}	$V_o = 0V$, $T = 25^{\circ}C$ $T_{min} < T_{amb} < T_{max}$	18 16	35 -	- -	
I_{CC}	Supply current (per operator)	No load, $V_{out} = 2.5V$	-	0.82	1.1	mA
AC performance						
GBP	Gain bandwidth product	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$, $T = 25^{\circ}C$	-	8	-	MHz
F_u	Unity gain frequency	$R_L = 2k\Omega$, $C_L = 100pF$, $T = 25^{\circ}C$	-	7.5	-	MHz
ϕ_m	Phase margin	$R_L = 2k\Omega$, $C_L = 100pF$, $T = 25^{\circ}C$	-	45	-	Degrees
G_m	Gain margin	$R_L = 2k\Omega$, $C_L = 100pF$, $T = 25^{\circ}C$	-	8	-	dB
SR	Slew rate	$R_L = 2k\Omega$, $C_L = 100pF$, $A_v = 1$, $T = 25^{\circ}C$	-	4.5	-	V/ μs
e_n	Equivalent input noise voltage	$f = 1kHz$, $T = 25^{\circ}C$	-	27	-	$\frac{nV}{\sqrt{Hz}}$
		$f = 10kHz$, $T = 25^{\circ}C$	-	21	-	
THD+ e_n	Total harmonic distortion	$G = 1$, $f = 1kHz$, $R_L = 2k\Omega$, $Bw = 22kHz$, $T = 25^{\circ}C$, $V_{icm} = (V_{CC} + 1)/2$, $V_{out} = 3.6V_{pp}$	-	0.0004	-	%

1. All parameter limits at temperatures other than $25^{\circ}C$ are guaranteed by correlation.
2. Guaranteed by design.

Figure 1. Input offset voltage distribution at $T = 25^{\circ}\text{C}$

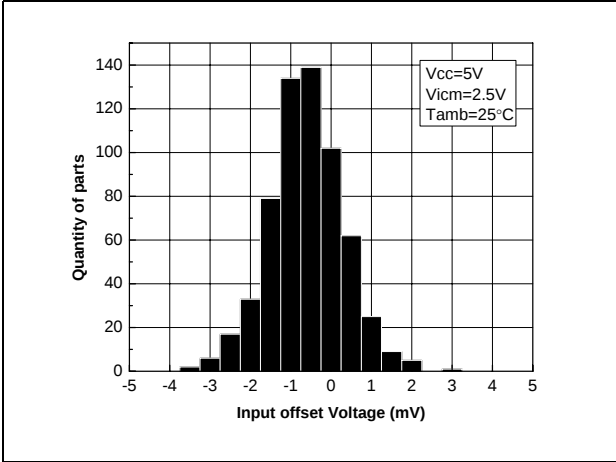


Figure 2. Input offset voltage distribution at $T = 125^{\circ}\text{C}$

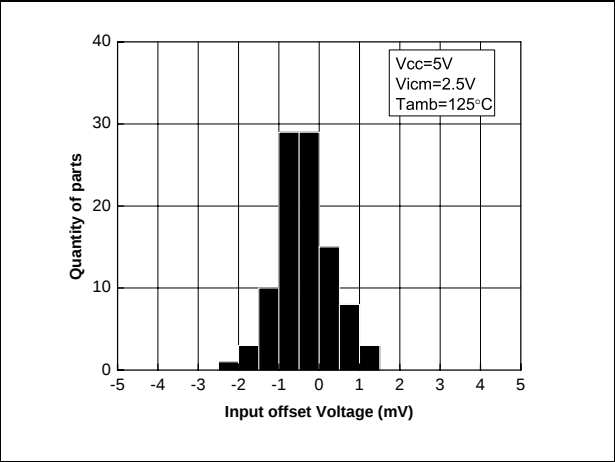


Figure 3. Supply current vs. input common mode voltage at $V_{CC} = 2.5\text{V}$

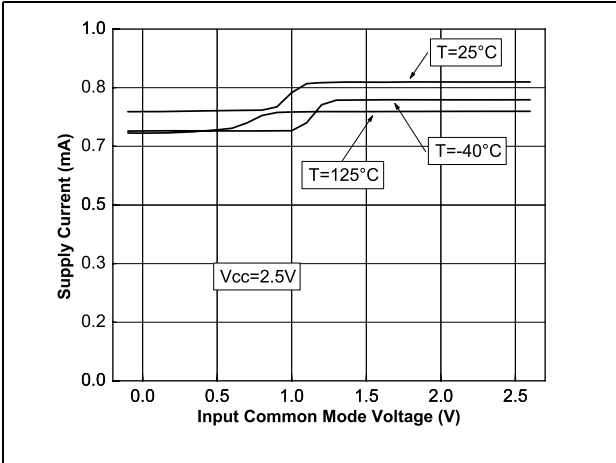


Figure 4. Supply current vs. input common mode voltage at $V_{CC} = 5\text{V}$

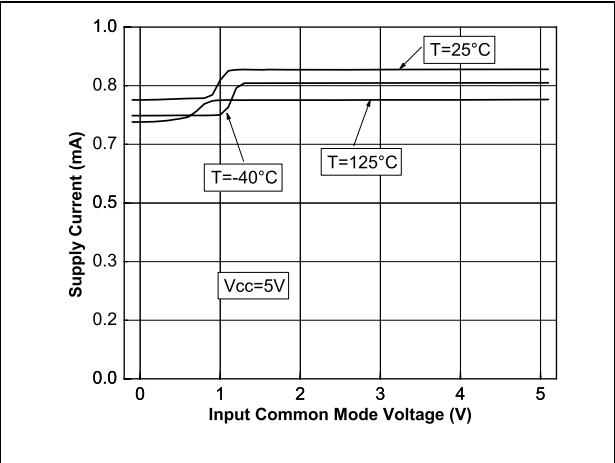


Figure 5. Output current vs. output voltage at $V_{CC} = 2.5\text{V}$

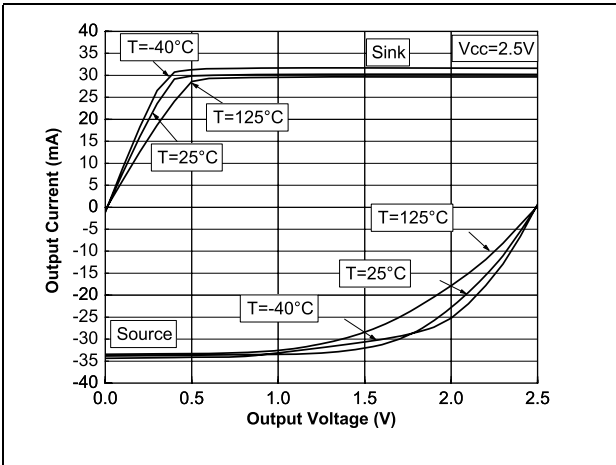


Figure 6. Output current vs. output voltage at $V_{CC} = 5\text{V}$

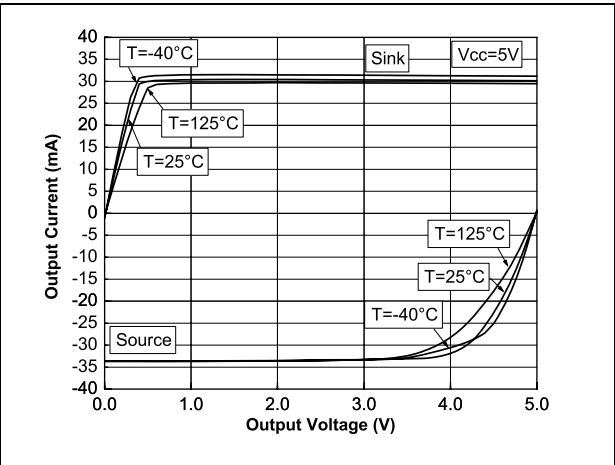


Figure 7. Voltage gain and phase vs frequency at $V_{CC}=2.5V$ and $V_{icm}=0.5V$

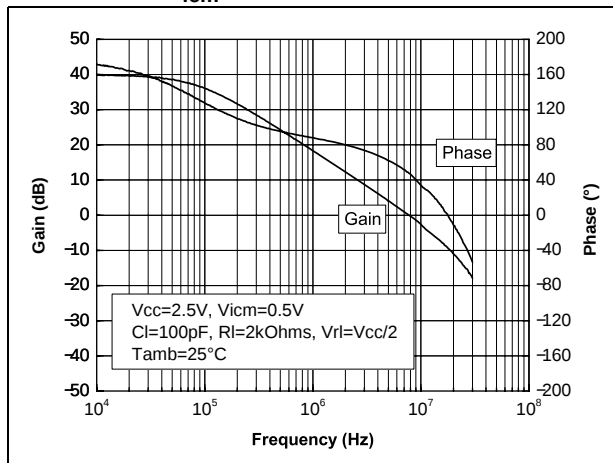


Figure 8. Voltage gain and phase vs frequency at $V_{CC}=5.5V$ and $V_{icm}=0.5V$

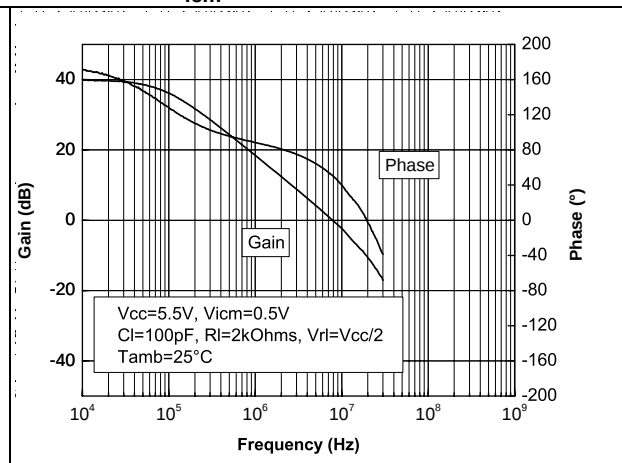


Figure 9. Phase margin vs. capacitive load

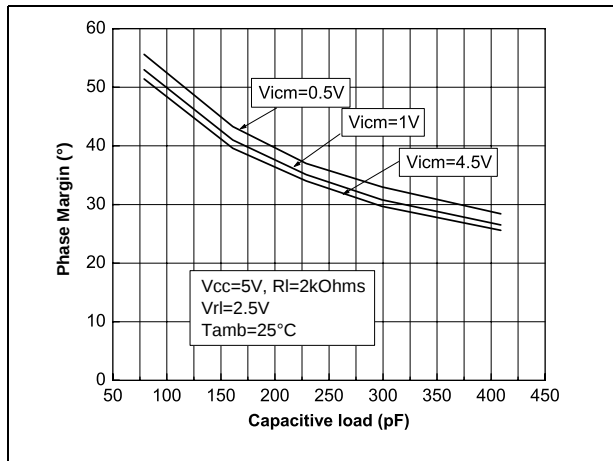


Figure 10. Phase margin vs. output current

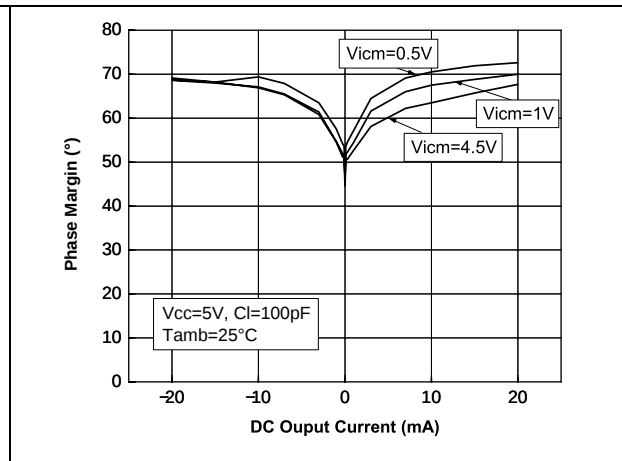


Figure 11. Positive slew rate

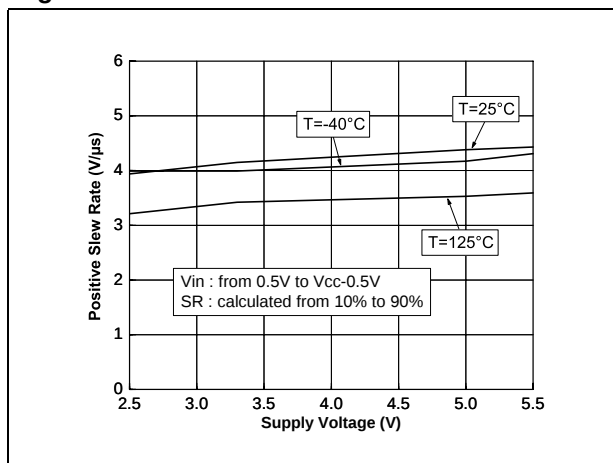


Figure 12. Negative slew rate

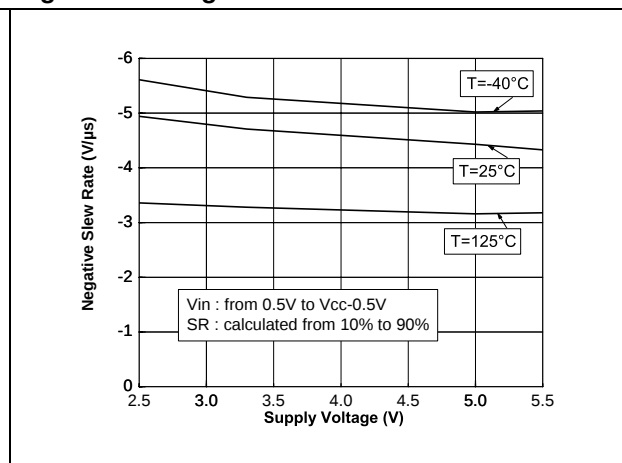


Figure 13. Distorsion + noise vs. frequency

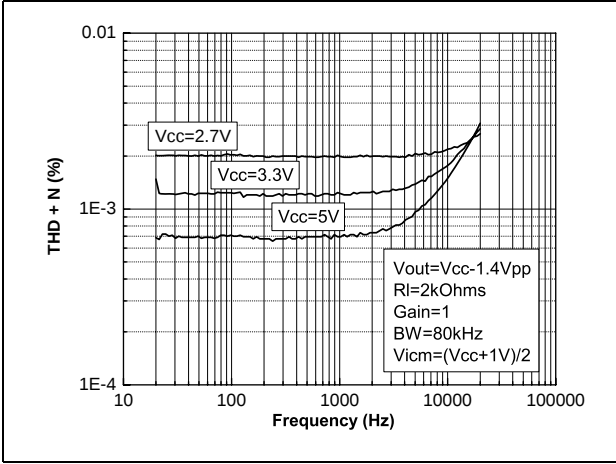


Figure 14. Distorsion + noise vs. output voltage

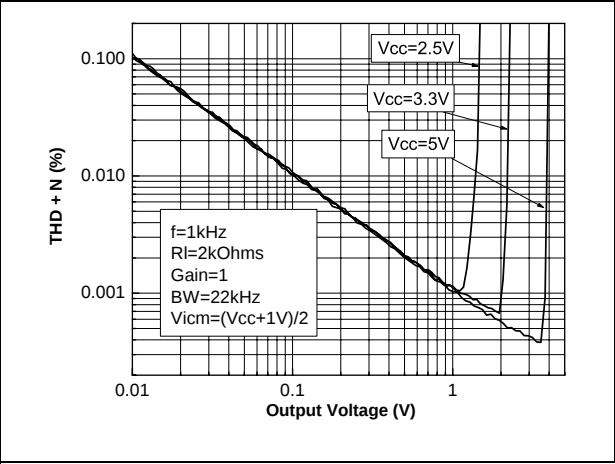


Figure 15. Noise vs. frequency

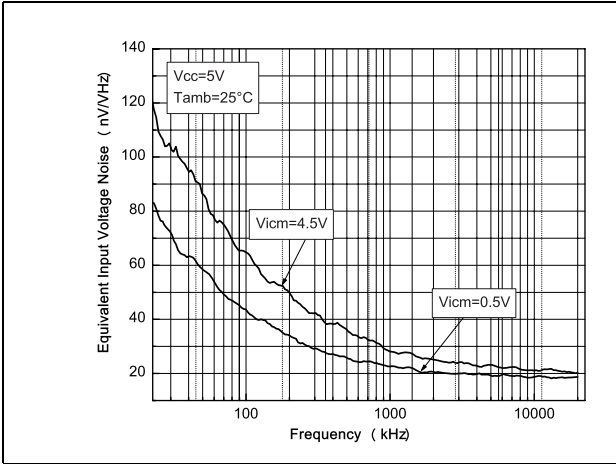
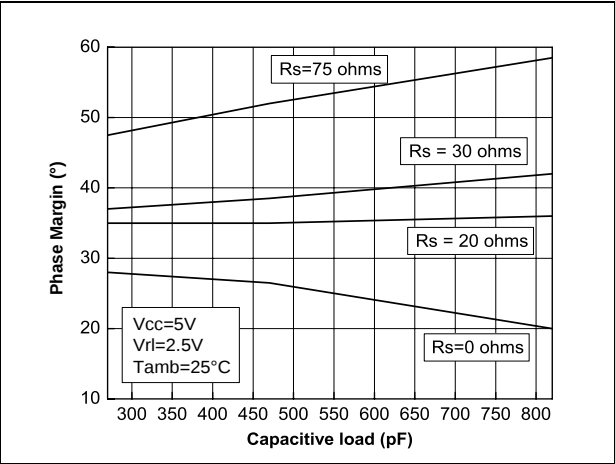


Figure 16. Phase margin vs. capacitive load and serial resistor



3 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Note: All packages are Moisture Sensitivity Level 1 as per Jedec J-STD-020-C, except SO-14 which is Jedec level 3.

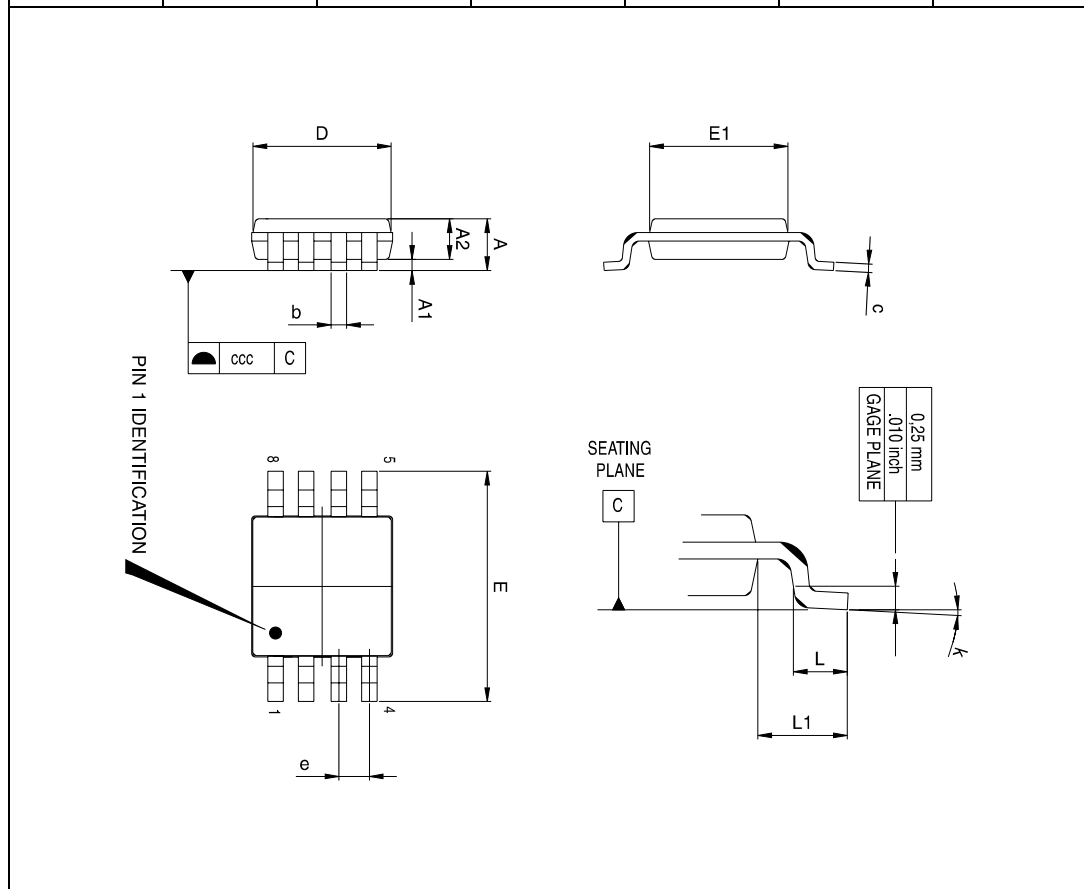
3.1 SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.00		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6

The diagram illustrates the mechanical dimensions of the SOT23-5 package. The left side shows a side profile with dimensions A (total width), A1 (lead thickness), A2 (lead width), C (lead thickness at base), and L (lead height). The right side shows a top-down view with dimensions D (package width), b (lead spacing), E (package height), E1 (package height to lead top), e (lead pitch), and e1 (lead pitch to package edge).

3.2 MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



3.3 SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
H	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

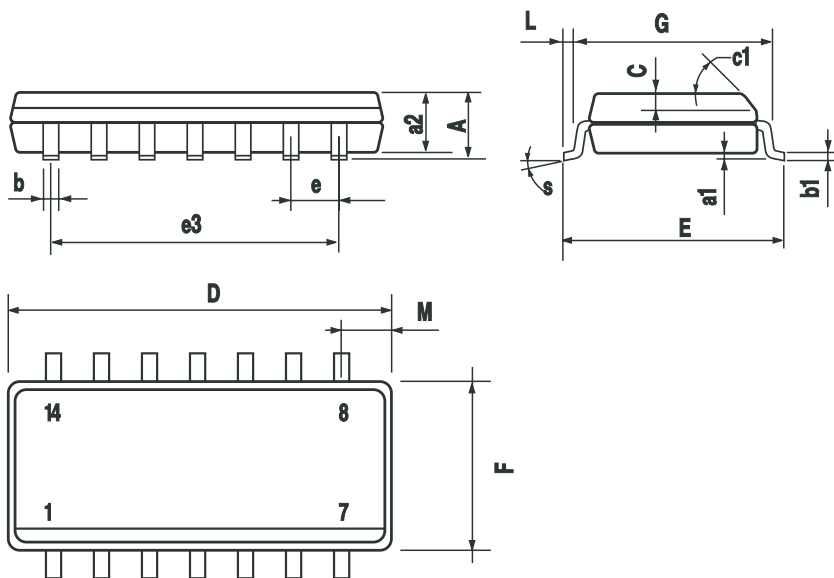
3.4 TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L1	0.45	0.60	0.75	0.018	0.024	0.030

PIN 1 IDENTIFICATION

1

3.5 SO-14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					
						

4 Ordering information

Table 6. Order codes⁽¹⁾

Part number	Temperature range	Package	Packing	Marking
TSV911ID TSV911IDT	-40°C to - 125°C	SO-8	Tube o Tape & reel	V911I
TSV911AID TSV911AIDT				V911AI
TSV911ILT		SOT23-5	Tape & reel	K127
TSV911AILT				
TSV912IST		MiniSO-8		K125
TSV912AIST				
TSV912ID TSV912IDT		SO-8	Tube or Tape & reel	V912I
TSV912AID TSV912AIDT				V912AI
TSV914IPT		TSSOP14	Tape & reel	V914I
TSV914AIPT				V914AI
TSV914ID TSV914IDT		SO-14 ⁽¹⁾	Tube or Tape & reel	V914I
TSV914AID TSV914AIDT				V914AI
TSV911IYD TSV911IYDT ⁽²⁾		SO-8 Automotive grade level		V911IY
TSV911AIYD TSV911AIYDT ⁽²⁾				V911IAY
TSV912IYD TSV912IYDT ⁽²⁾				V912IY
TSV912AIYD TSV912AIYDT ⁽²⁾				V912AY
TSV914IYD TSV914IYDT ⁽²⁾		SO-14 ⁽¹⁾ Automotive grade level		V914IY
TSV914AIYD TSV914AIYDT ⁽²⁾				V914AY

1. All packages are Moisture Sensitivity Level 1 as per Jedec J-STD-020-C, except SO-14 which is Jedec level 3.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

5 Revision history

Date	Revision	Changes
28-Aug-2006	1	First release.
7-Jun-2007	3	Modified ESD CDM parameter for SO-14 package in Table 1: Absolute maximum ratings (AMR) . Noise parameters updated in Section 2: Electrical characteristics . Added limits in temperature in Section 2: Electrical characteristics . Added automotive grade level description in Table 6: Order codes . Added footnote about SO-14 package in Table 6: Order codes . Added Figure 16: Phase margin vs. capacitive load and serial resistor .

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