Energy Metering IC with Integrated Oscillator

ADE7757*

FEATURES

On-Chip Oscillator as Clock Source
High Accuracy, Supposes 50 Hz/60 Hz IEC 521/IEC 61036
Less than 0.1% Error over a Dynamic Range of 500 to 1
The ADE7757 Supplies Average Real Power on the Frequency Outputs F1 and F2
The High Frequency Output CF Is Intended for Calibration and Supplies Instantaneous Real Power
The Logic Output REVP Can Be Used to Indicate a Potential Miswiring or Negative Power
Direct Drive for Electromechanical Counters and 2-Phase Stepper Motors (F1 and F2)
Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time
On-Chip Power Supply Monitoring
On-Chip Creep Protection (No Load Threshold)
On-Chip Reference 2.5 V (20 ppm/°C Typical) with External Overdrive Capability
Single 5 V Supply, Low Power (20 mW Typical)
Low Cost CMOS Process
AC Input Only

GENERAL DESCRIPTION

The ADE7757 is a high accuracy electrical energy measurement IC. It is a pin reduction version of the ADE7755 with an enhancement of a precise oscillator circuit that serves as a clock source to the chip. The ADE7757 eliminates the cost of an external crystal or resonator, thus reducing the overall cost of a meter built with this IC. The chip directly interfaces with the shunt resistor and operates only with ac input.

The ADE7757 specifications surpass the accuracy requirements as quoted in the IEC 61036 standard. The AN-679 Application Note can be used as a basis for a description of an IEC 61036 low cost watt-hour meter reference design.

The only analog circuitry used in the ADE7757 is in the Σ-Δ ADCs and reference circuit. All other signal processing (e.g., multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over time and extreme environmental conditions.

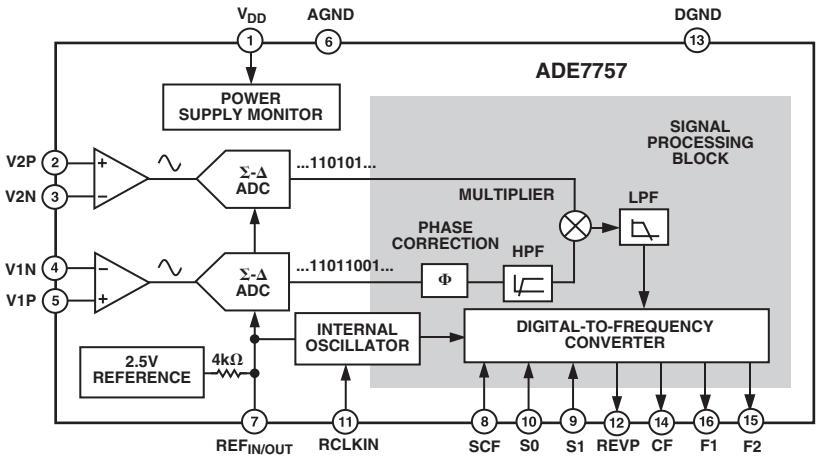
The ADE7757 supplies average real power information on the low frequency outputs F1 and F2. These outputs may be used to directly drive an electromechanical counter or interface with an MCU. The high frequency CF logic output, ideal for calibration purposes, provides instantaneous real power information.

The ADE7757 includes a power supply monitoring circuit on the V_{DD} supply pin. The ADE7757 will remain inactive until the supply voltage on V_{DD} reaches approximately 4 V. If the supply falls below 4 V, the ADE7757 will also remain inactive and the F1, F2, and CF outputs will be in their nonactive modes.

Internal phase matching circuitry ensures that the voltage and current channels are phase matched while the HPF in the current channel eliminates dc offsets. An internal no-load threshold ensures that the ADE7757 does not exhibit creep when no load is present.

The ADE7757 is available in a 16-lead SOIC narrow-body package.

FUNCTIONAL BLOCK DIAGRAM



*U.S. Patents 5,745,323; 5,760,617; 5,862,069; 5,872,469; others pending.

REV. A

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ADE7757—SPECIFICATIONS (V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, RCLKIN = 6.2 kΩ, 0.5% ± 50 ppm/°C, T_{MIN} to T_{MAX} = –40°C to +85°C, unless otherwise noted.)

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY[1, 2]			
Measurement Error[1] on Channel V1	0.1	% Reading typ	Channel V2 with Full-Scale Signal (±165 mV), 25°C Over a Dynamic Range 500 to 1
Phase Error[1] between Channels			Line Frequency = 45 Hz to 65 Hz
V1 Phase Lead 37° (PF = 0.8 Capacitive)	±0.1	Degrees (°) max	
V1 Phase Lag 60° (PF = 0.5 Inductive)	±0.1	Degrees (°) max	
AC Power Supply Rejection[1]			S0 = S1 = 1,
Output Frequency Variation (CF)	0.2	% Reading typ	V1 = 21.2 mV rms, V2 = 116.7 mV rms @ 50 Hz Ripple on V_{DD} of 200 mV rms @ 100 Hz
DC Power Supply Rejection[1]			S0 = S1 = 1,
Output Frequency Variation (CF)	±0.3	% Reading typ	V1 = 21.2 mV rms, V2 = 116.7 mV rms, V_{DD} = 5 V ± 250 mV
ANALOG INPUTS			See Analog Inputs section
Channel V1 Maximum Signal Level	±30	mV max	V1P and V1N to AGND
Channel V2 Maximum Signal Level	±165	mV max	V2P and V2N to AGND
Input Impedance (DC)	320	kΩ min	OSC = 450 kHz, RCLKIN = 6.2 kΩ, 0.5% ± 50 ppm/°C
Bandwidth (–3 dB)	7	kHz nominal	OSC = 450 kHz, RCLKIN = 6.2 kΩ, 0.5% ± 50 ppm/°C
ADC Offset Error[1, 2]	±18	mV max	See Terminology Section and Typical Performance Characteristics
Gain Error[1]	±4	% Ideal typ	External 2.5 V Reference V1 = 21.2 mV rms, V2 = 116.7 mV rms
OSCILLATOR FREQUENCY (OSC)	450	kHz nominal	RCLKIN = 6.2 kΩ, 0.5% ± 50 ppm/°C
Oscillator Frequency Tolerance[1]	±12	% Reading typ	
Oscillator Frequency Stability[1]	±30	ppm/°C typ	
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.7	V max	2.5 V + 8%
	2.3	V min	2.5 V – 8%
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.5 V
Reference Error	±200	mV max	
Temperature Coefficient	±20	ppm/°C typ	
LOGIC INPUTS[3]			
SCF, S0, S1,			
Input High Voltage, V_{INH}	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±1	μA max	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS[3]			
F1 and F2			
Output High Voltage, V_{OH}	4.5	V min	I_{SOURCE} = 10 mA V_{DD} = 5 V
Output Low Voltage, V_{OL}	0.5	V max	I_{SINK} = 10 mA V_{DD} = 5 V
CF			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA V_{DD} = 5 V
Output Low Voltage, VOL	0.5	V max	I_{SINK} = 5 mA V_{DD} = 5 V
Frequency Output Error[1, 2] (CF)	±10	% Ideal typ	External 2.5 V Reference, V1 = 21.2 mV rms, V2 = 116.7 mV rms
POWER SUPPLY			For Specified Performance
V_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
I_{DD}	5	mA max	Typically 4 mA

NOTES
[1]See Terminology section for explanation of specifications.
[2]See plots in Typical Performance Characteristics.
[3]Sample tested during initial release and after any redesign or process change that may affect this parameter.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, RCLKIN = 6.2 kΩ, 0.5% ± 50 ppm/°C, T_{MIN} to T_{MAX} = –40°C to +85°C, unless otherwise noted.)

Parameter	A, B Versions	Unit	Test Conditions/Comments
t_1[3]	244	ms	F1 and F2 Pulse Width (Logic Low).
t_2	See Table II	sec	Output Pulse Period. See Transfer Function section.
t_3	1/2 t_2	sec	Time between F1 Falling Edge and F2 Falling Edge.
t_4[3, 4]	173	ms	CF Pulse Width (Logic High).
t_5	See Table III	sec	CF Pulse Period. See Transfer Function section.
t_6	2	µs	Minimum Time between F1 and F2 Pulses.

NOTES
[1]Sample tested during initial release and after any redesign or process change that may affect this parameter.
[2]See Figure 1.
[3]The pulse widths of F1, F2, and CF are not fixed for higher output frequencies. See Frequency Outputs section.
[4]The CF pulse is always 35 µs in the high frequency mode. See Frequency Outputs section and Table III.

Specifications subject to change without notice.

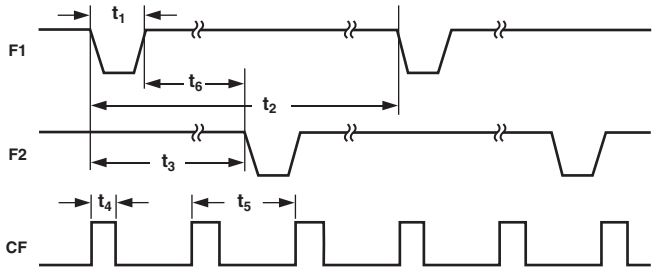


Figure 1. Timing Diagram for Frequency Outputs

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND
V1P, V1N, V2P, and V2N ..... –6 V to +6 V
Reference Input Voltage to AGND ... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND .... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A, B Versions) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
16-Lead Plastic SOIC, Power Dissipation ..... 350 mW
θ_{JA} Thermal Impedance[2] .....124.9°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] JEDEC 1S Standard (2-layer) Board Data.

ORDERING GUIDE

Model	Package Description	Package Options
ADE7757ARN	SOIC Narrow-Body	RN-16
ADE7757ARNRL	SOIC Narrow-Body in Reel	RN-16
EVAL-ADE7757EB	Evaluation Board	Evaluation Board
ADE7757ARN-REF	Reference Design	Reference Design

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7757 is defined by the following formula

$$\%Error = \frac{Energy\ Registered\ by\ ADE7757 – True\ Energy}{True\ Energy} \times 100\%$$

Phase Error between Channels

The HPF (high-pass filter) in the current channel (Channel V1) has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase correction network is also placed in Channel V1. The phase correction network matches the phase to within ±0.1° over a range of 45 Hz to 65 Hz, and ±0.2° over a range 40 Hz to 1 kHz (see Figures 11 and 12).

Power Supply Rejection

This quantifies the ADE7757 measurement error as a percentage of reading when the power supplies are varied.

For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A 200 mV rms/100 Hz signal is then introduced onto the supplies and a second reading is obtained under the same input signal levels. Any error introduced is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. The supplies are then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of reading.

ADC Offset Error

This refers to the small dc signal (offset) associated with the analog inputs to the ADCs. However, the HPF in Channel V1 eliminates the offset in the circuitry. Therefore, the power calculation is not affected by this offset.

Frequency Output Error (CF)

The frequency output error of the ADE7757 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7757 transfer function (see the Transfer Function section).

Gain Error

The gain error of the ADE7757 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7757 transfer function (see the Transfer Function section).

Oscillator Frequency Tolerance

The oscillator frequency tolerance of the ADE7757 is defined as part-to-part frequency variation in terms of percentage at room temperature (25°C). It is measured by taking the difference between the measured oscillator frequency and the nominal frequency defined in the Specifications section.

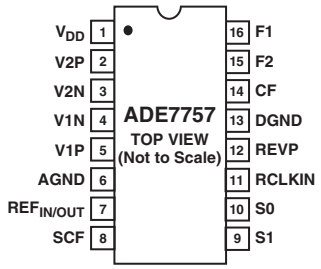
Oscillator Frequency Stability

Oscillator frequency stability is defined as frequency variation in terms of parts-per-million drift over the operating temperature range. In a metering application, the temperature range is –40°C to +85°C. Oscillator frequency stability is measured by taking the difference between the measured oscillator frequency at –40°C and +85°C and the measured oscillator frequency at +25°C.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADE7757 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply. This pin provides the supply voltage for the circuitry in the ADE7757. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
2, 3	V2P, V2N	Analog Inputs for Channel V2 (voltage channel). These inputs provide a fully differential input pair. The maximum differential input voltage is ±165 mV for specified operation. Both inputs have internal ESD protection circuitry; an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
4, 5	V1N, V1P	Analog Inputs for Channel V1 (current channel). These inputs are fully differential voltage inputs with a maximum signal level of ±30 mV with respect to the V1N pin for specified operation. Both inputs have internal ESD protection circuitry and, in addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
6	AGND	This provides the ground reference for the analog circuitry in the ADE7757, i.e., ADCs and reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry, e.g., antialiasing filters, current and voltage sensors, and so forth. For accurate noise suppression, the analog ground plane should be connected to the digital ground plane at only one point. A star ground configuration will help to keep noisy digital currents away from the analog circuits.
7	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5 V and a typical temperature coefficient of 20 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF tantalum capacitor and a 100 nF ceramic capacitor. The internal reference cannot be used to drive an external load.
8	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table III shows calibration frequencies selection.
9, 10	S1, S0	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. With this logic input, designers have greater flexibility when designing an energy meter. See the Selecting a Frequency for an Energy Meter Application section.
11	RCLKIN	To enable the internal oscillator as a clock source to the chip, a precise low temperature drift resistor at a nominal value of 6.2 kΩ must be connected from this pin to DGND.
12	REVP	This logic output will go high when negative power is detected, i.e., when the phase angle between the voltage and current signals is greater than 90°. This output is not latched and will be reset when positive power is once again detected. The output will go high or low at the same time that a pulse is issued on CF.
13	DGND	This provides the ground reference for the digital circuitry in the ADE7757, i.e., multiplier, filters, and digital-to-frequency converter. This pin should be tied to the digital ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry, e.g., counters (mechanical and digital), MCUs, and indicator LEDs. For accurate noise suppression, the analog ground plane should be connected to the digital ground plane at one point only, i.e., a star ground.
14	CF	Calibration Frequency Logic Output. The CF logic output provides instantaneous real power information. This output is intended for calibration purposes. Also see SCF pin description.
15, 16	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply *average real power* information. The logic outputs can be used to directly drive electromechanical counters and 2-phase stepper motors. See the Transfer Function section.

ADE7757–Typical Performance Characteristics

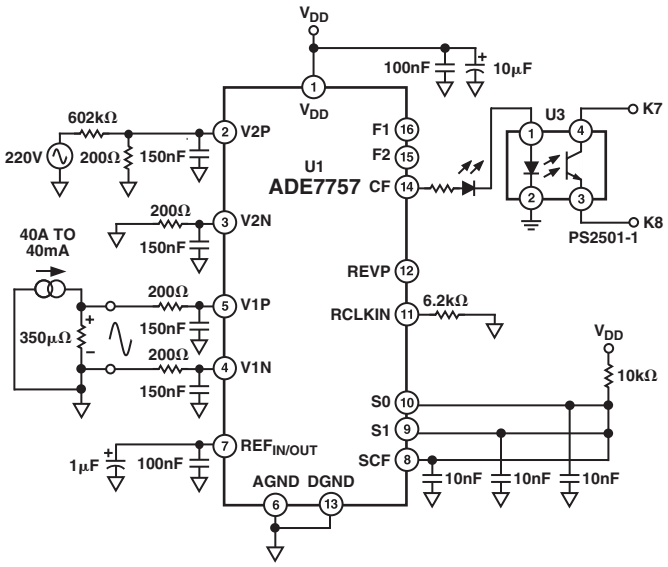
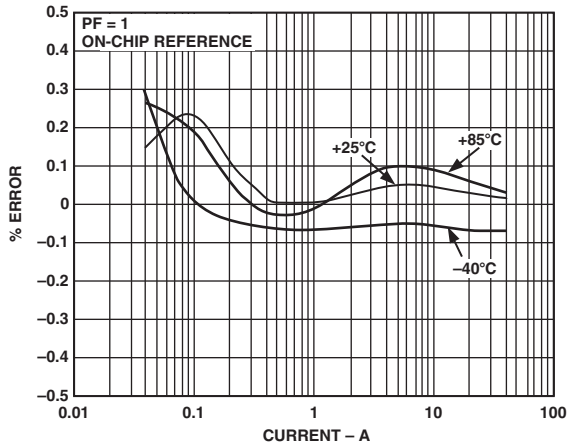
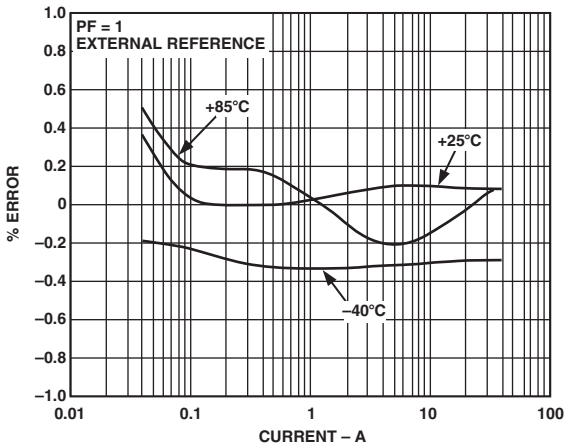


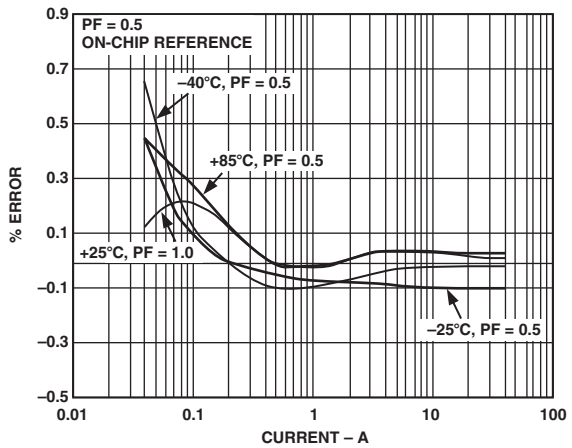
Figure 2. Test Circuit for Performance Curves



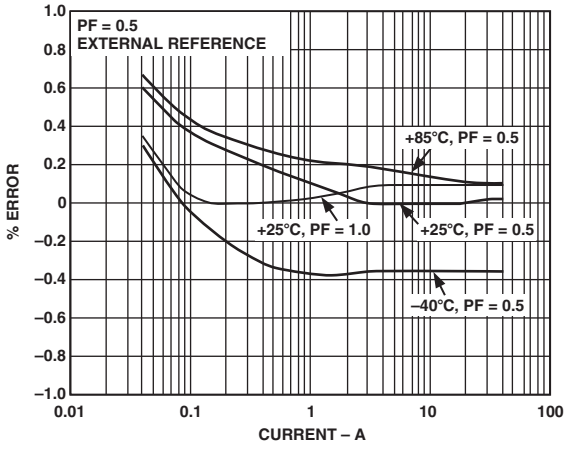
TPC 1. Error as a % of Reading over Temperature with On-Chip Reference (PF = 1)



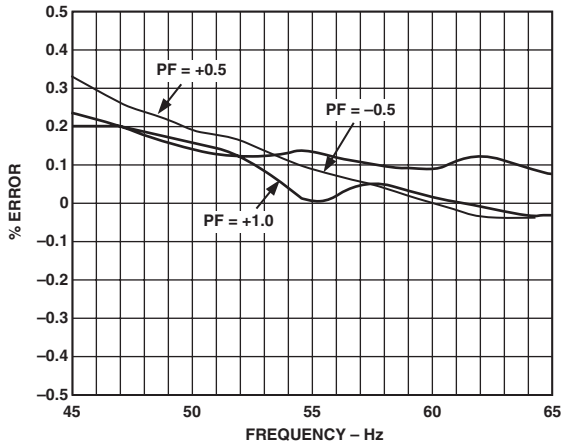
TPC 3. Error as a % of Reading over Temperature with External Reference (PF = 1)



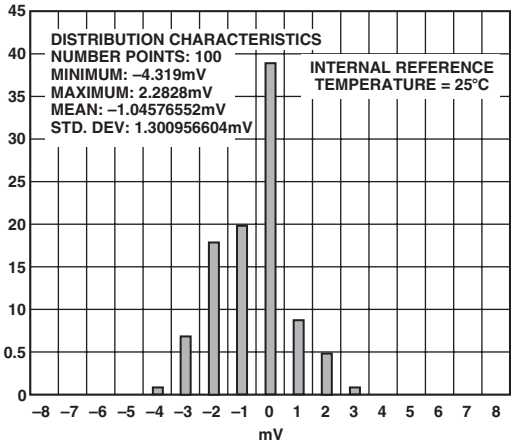
TPC 2. Error as a % of Reading over Temperature with On-Chip Reference (PF = 0.5)



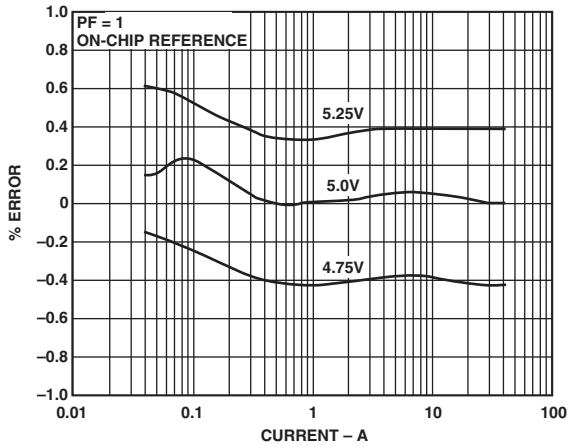
TPC 4. Error as a % of Reading over Temperature with External Reference (PF = 0.5)



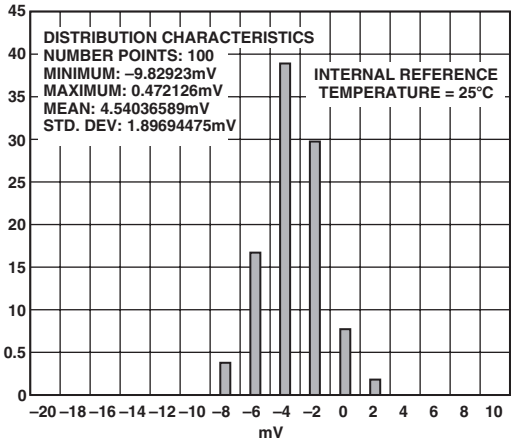
TPC 5. Error as a % of Reading over Input Frequency



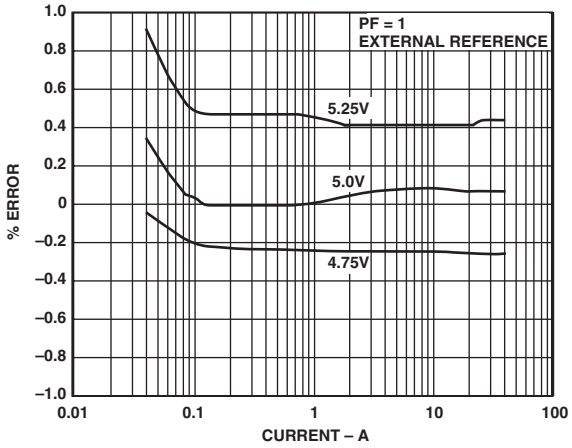
TPC 8. Channel V1 Offset Distribution



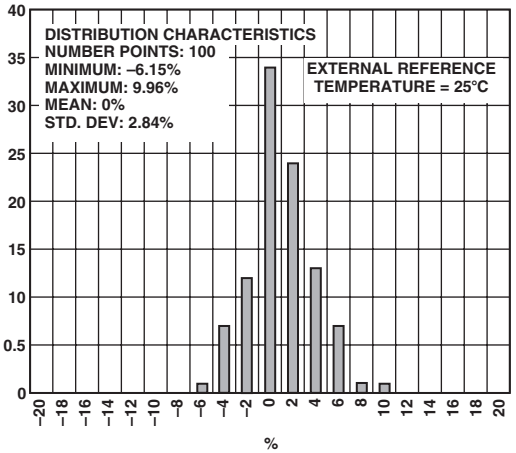
TPC 6. PSR with Internal Reference



TPC 9. Channel V2 Offset Distribution



TPC 7. PSR with External Reference



TPC 10. Part-to-Part CF Distribution from Mean

THEORY OF OPERATION

The two ADCs digitize the voltage signals from the current and voltage sensors. These ADCs are 16-bit Σ-Δ with an oversampling rate of 450 kHz. This analog input structure greatly simplifies sensor interfacing by providing a wide dynamic range for direct connection to the sensor and also simplifies the antialiasing filter design. A high-pass filter in the current channel removes any dc component from the current signal. This eliminates any inaccuracies in the real power calculation due to offsets in the voltage or current signals. Because the HPF is always enabled, the IC will operate only with ac input (see HPF and Offset Effects section).

The real power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. In order to extract the real power component (i.e., the dc component), the instantaneous power signal is low-pass filtered. Figure 3 illustrates the instantaneous real power signal and shows how the real power information can be extracted by low-pass filtering the instantaneous power signal. This scheme correctly calculates real power for sinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

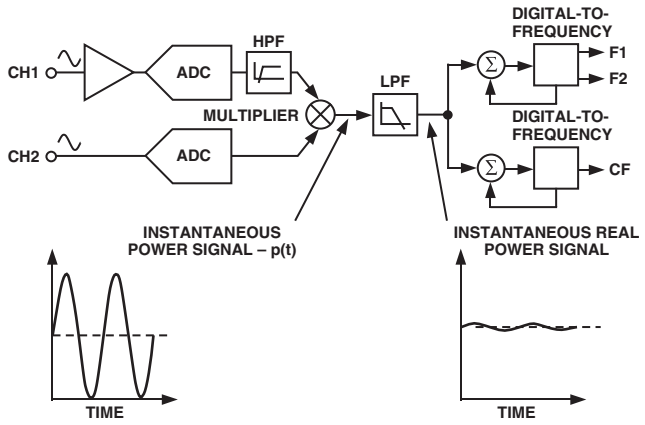


Figure 3. Signal Processing Block Diagram

The low frequency outputs (F1, F2) of the ADE7757 are generated by accumulating this real power information. This low frequency inherently means a long accumulation time between output pulses. Consequently, the resulting output frequency is proportional to the average real power. This average real power information is then accumulated (e.g., by a counter) to generate real energy information. Conversely, due to its high output frequency and hence shorter integration time, the CF output frequency is proportional to the instantaneous real power. This is useful for system calibration, which can be done faster under steady load conditions.

Power Factor Considerations

The method used to extract the real power information from the instantaneous power signal (i.e., by low-pass filtering) is still valid even when the voltage and current signals are not in phase. Figure 4 displays the unity power factor condition and a DPF (displacement power factor) = 0.5, i.e., current signal lagging the voltage by 60°. If we assume the voltage and current waveforms are sinusoidal, the real power component of the instantaneous power signal (i.e., the dc term) is given by

$$\left(\frac{V \times 1}{2}\right) \times \cos(60°)$$

This is the correct real power calculation.

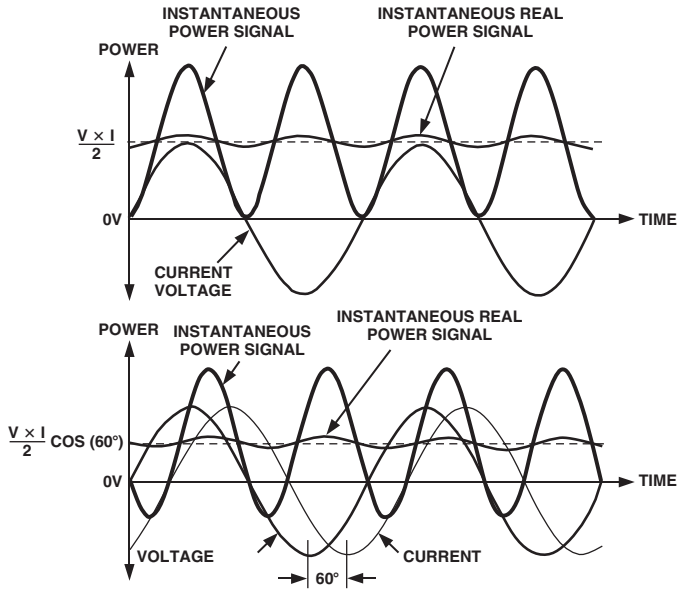


Figure 4. DC Component of Instantaneous Power Signal Conveys Real Power Information, PF < 1

Nonsinusoidal Voltage and Current

The real power calculation method also holds true for nonsinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications will have some harmonic content. Using the Fourier Transform, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content.

$$v(t) = V_0 + \sqrt{2} \times \sum_{h \neq o}^{\infty} V_h \times \sin\left(h\omega t + \alpha_h\right) \quad (1)$$

where:

$v(t)$ is the instantaneous voltage.
V_0 is the average value.
V_h is the rms value of voltage harmonic h.
α_h is the phase angle of the voltage harmonic.

$$i(t) = I_0 + \sqrt{2} \times \sum_{h \neq o}^{\infty} I_h \times sin\left(h\omega t + \beta_h\right) \quad (2)$$

where:

$i(t)$ is the instantaneous current.
I_0 is the dc component.
I_h is the rms value of current harmonic h.
β_h is the phase angle of the current harmonic.

Using Equations 1 and 2, the real power P can be expressed in terms of its fundamental real power (P_1) and harmonic real power (P_H).

$$P = P_1 + P_H$$

where

$$P_1 = V_1 \times I_1 \cos\phi_1$$
$$\phi_1 = \alpha_1 - \beta_1 \quad (3)$$

and

$$P_H = \sum_{h \neq 1}^{\infty} V_h \times I_h \cos\phi_h$$
$$\phi_h = \alpha_h - \beta_h \quad (4)$$

As can be seen from Equation 4, a harmonic real power component is generated for every harmonic, provided that harmonic is present in both the voltage and current waveforms. The power factor calculation has previously been shown to be accurate in the case of a pure sinusoid. Therefore, the harmonic real power must also correctly account for power factor since it is made up of a series of pure sinusoids.

Note that the input bandwidth of the analog inputs is 7 kHz at the nominal internal oscillator frequency of 450 kHz.

ANALOG INPUTS

Channel V1 (Current Channel)

The voltage output from the current sensor is connected to the ADE7757 here. Channel V1 is a fully differential voltage input. V1P is the positive input with respect to V1N.

The maximum peak differential signal on Channel V1 should be less than ±30 mV (21 mV rms for a pure sinusoidal signal) for specified operation.

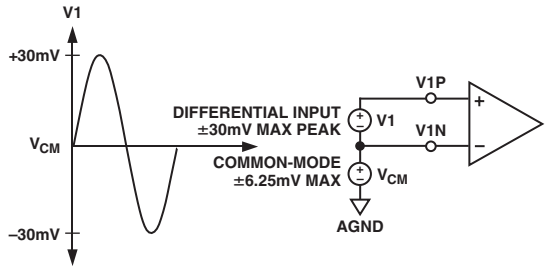


Figure 5. Maximum Signal Levels, Channel V1

The diagram in Figure 5 illustrates the maximum signal levels on V1P and V1N. The maximum differential voltage is ±30 mV. The differential voltage signal on the inputs must be referenced to a common mode, e.g., AGND. The maximum common-mode signal is ±6.25 mV, as shown in Figure 5.

Channel V2 (Voltage Channel)

The output of the line voltage sensor is connected to the ADE7757 at this analog input. Channel V2 is a fully differential voltage input with a maximum peak differential signal of ±165 mV. Figure 6 illustrates the maximum signal levels that can be connected to the ADE7757 Channel V2.

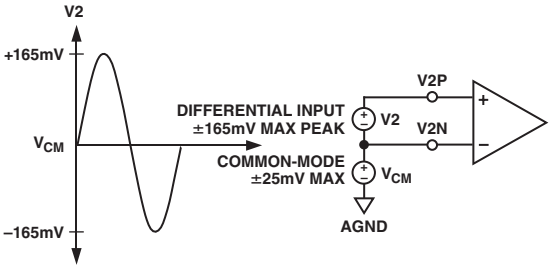


Figure 6. Maximum Signal Levels, Channel V2

Channel V2 is usually driven from a common-mode voltage, i.e., the differential voltage signal on the input is referenced to a common mode (usually AGND). The analog inputs of the ADE7757 can be driven with common-mode voltages of up to 25 mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

Typical Connection Diagrams

Figure 7 shows a typical connection diagram for Channel V1. A shunt is the current sensor selected for this example because of its low cost compared to other current sensors such as the CT (current transformer). This IC is ideal for low current meters.

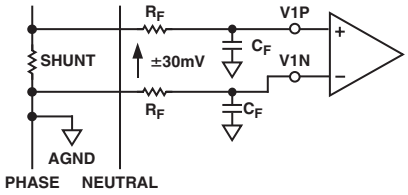


Figure 7. Typical Connection for Channel V1

Figure 8 shows a typical connection for Channel V2. Typically, the ADE7757 is biased around the phase wire, and a resistor divider is used to provide a voltage signal that is proportional to the line voltage. Adjusting the ratio of R_A, R_B, and R_F is also a convenient way of carrying out a gain calibration on a meter.

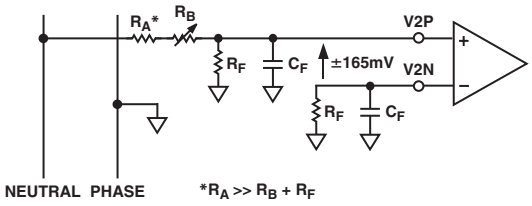


Figure 8. Typical Connections for Channel V2

POWER SUPPLY MONITOR

The ADE7757 contains an on-chip power supply monitor. The power supply (V_{DD}) is continuously monitored by the ADE7757. If the supply is less than 4 V, the ADE7757 becomes inactive. This is useful to ensure proper device operation at power-up and power-down. The power supply monitor has built in hysteresis and filtering that provide a high degree of immunity to false triggering from noisy supplies.

As can be seen from Figure 9, the trigger level is nominally set at 4 V. The tolerance on this trigger level is within ±5%. The power supply and decoupling for the part should be such that the ripple at V_{DD} does not exceed 5 V ± 5% as specified for normal operation.

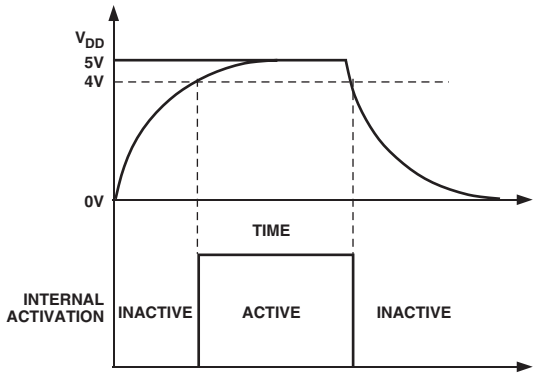


Figure 9. On-Chip Power Supply Monitor

HPF and Offset Effects

Figure 10 illustrates the effect of offsets on the real power calculation. As can be seen, offsets on Channel V1 and Channel V2 will contribute a dc component after multiplication. Since this dc component is extracted by the LPF and used to generate the real power information, the offsets will contribute a constant error to the real power calculation. This problem is easily avoided by the built-in HPF in Channel V1. By removing the offsets from at least one channel, no error component can be generated at dc by the multiplication. Error terms at the line frequency (ω) are removed by the LPF and the digital-to-frequency conversion (see Digital-to-Frequency Conversion section).

The equation below shows how the power calculation is affected by the dc offsets in the current and voltage channels.

$$\left\{V\cos(\omega t)+V_{OS}\right\}\times\left\{I\cos(\omega t)+I_{OS}\right\}$$
$$=\frac{V\times I}{2}+V_{OS}\times I_{OS}+V_{OS}\times I\cos(\omega t)+I_{OS}\times V\cos(\omega t)$$
$$+\frac{V\times I}{2}\times\cos(2\omega t)$$

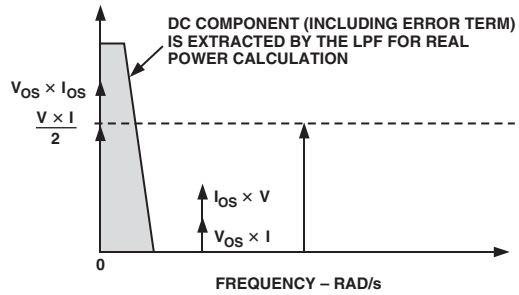


Figure 10. Effect of Channel Offset on the Real Power Calculation

The HPF in Channel V1 has an associated phase response that is compensated for on-chip. Figures 11 and 12 show the phase error between channels with the compensation network activated. The ADE7757 is phase compensated up to 1 kHz as shown. This will ensure correct active harmonic power calculation even at low power factors.

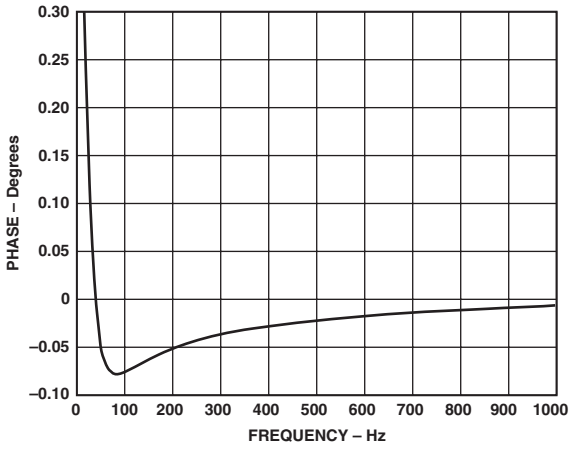


Figure 11. Phase Error between Channels (0 Hz to 1 kHz)

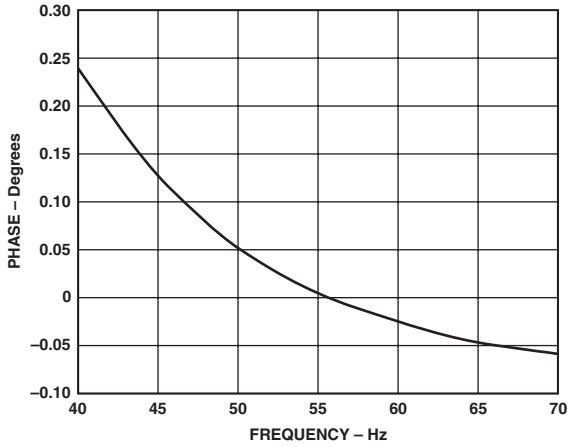


Figure 12. Phase Error between Channels (40 Hz to 70 Hz)

Digital-to-Frequency Conversion

As previously described, the digital output of the low-pass filter after multiplication contains the real power information. However, since this LPF is not an ideal "brick wall" filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics, i.e., cos(hωt) where h = 1, 2, 3, . . . and so on.

The magnitude response of the filter is given by

$$|H(f)| = \frac{1}{\sqrt{1+\frac{f^2}{4.45^2}}} \quad (5)$$

For a line frequency of 50 Hz, this would give an attenuation of the 2ω (100 Hz) component of approximately 22 dB. The dominating harmonic will be at twice the line frequency (2ω) due to the instantaneous power calculation.

Figure 13 shows the instantaneous real power signal at the output of the LPF that still contains a significant amount of instantaneous power information, i.e., cos(2ωt). This signal is then passed to the digital-to-frequency converter where it is integrated (accumulated) over time in order to produce an output frequency. The accumulation of the signal will suppress or average out any non-dc components in the instantaneous real power signal. The average value of a sinusoidal signal is zero. Thus, the frequency generated by the ADE7757 is proportional to the average real power. Figure 13 shows the digital-to-frequency conversion for steady load conditions, i.e., constant voltage and current.

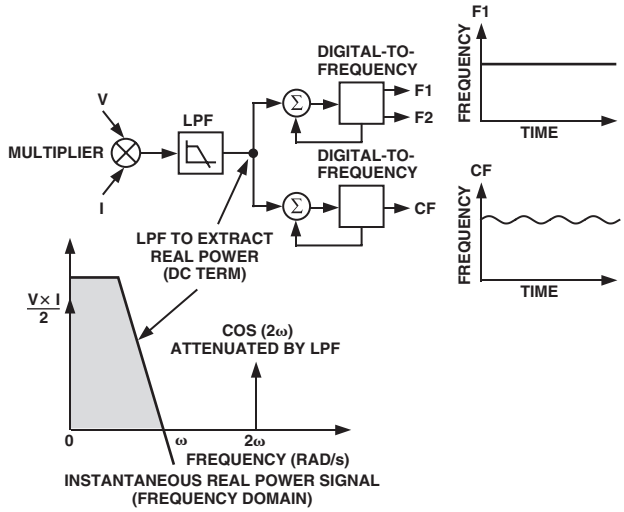


Figure 13. Real Power-to-Frequency Conversion

As can be seen in the diagram, the frequency output CF is seen to vary over time, even under steady load conditions. This frequency variation is primarily due to the cos(2ωt) component in the instantaneous real power signal. The output frequency on CF can be up to 2048 times higher than the frequency on F1 and F2. This higher output frequency is generated by accumulating the instantaneous real power signal over a much shorter time while converting it to a frequency. This shorter accumulation period means less averaging of the cos(2ωt) component. Consequently, some of this instantaneous power signal passes through the digital-to-frequency conversion. This will not be a problem in the application. Where CF is used for calibration purposes, the frequency should be averaged by the frequency counter, which will remove any ripple. If CF is being used to measure energy, for example in a microprocessor based application, the CF output should also be averaged to calculate power.

Because the outputs F1 and F2 operate at a much lower frequency, a lot more averaging of the instantaneous real power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output.

Interfacing the ADE7757 to a Microcontroller for Energy Measurement

The easiest way to interface the ADE7757 to a microcontroller is to use the CF high frequency output with the output frequency scaling set to 2048 × F1, F2. This is done by setting SCF = 0 and S0 = S1 = 1 (see Table III). With full-scale ac signals on the analog inputs, the output frequency on CF will be approximately 2.867 kHz. Figure 14 illustrates one scheme that could be used to digitize the output frequency and carry out the necessary averaging mentioned in the previous section.

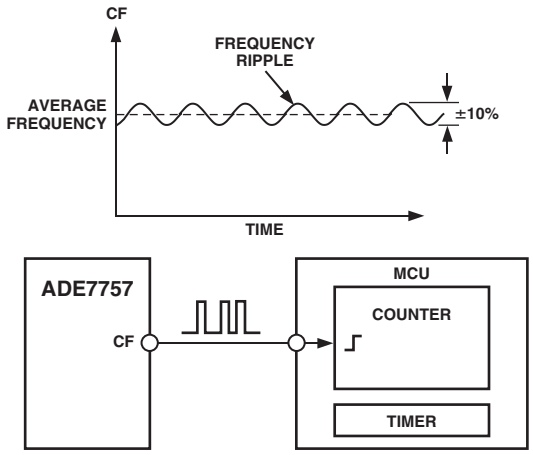


Figure 14. Interfacing the ADE7757 to an MCU

As shown, the frequency output CF is connected to an MCU counter or port. This will count the number of pulses in a given integration time, which is determined by an MCU internal timer. The average power proportional to the average frequency is given by

$$Average\ Frequency = Average\ Power = \frac{Counter}{Time}$$

The energy consumed during an integration period is given by

$$Energy = Average\ Power \times Time = \frac{Counter}{Time} \times Time = Counter$$

For the purpose of calibration, this integration time could be 10 seconds to 20 seconds in order to accumulate enough pulses to ensure correct averaging of the frequency. In normal operation, the integration time could be reduced to one or two seconds, depending, for example, on the required update rate of a display. With shorter integration times on the MCU, the amount of energy in each update may still have some small amount of ripple, even under steady load conditions. However, over a minute or more the measured energy will have no ripple.

Power Measurement Considerations

Calculating and displaying power information will always have some associated ripple that will depend on the integration period used in the MCU to determine average power and also on the load. For example, at light loads, the output frequency may be 10 Hz. With an integration period of two seconds, only about 20 pulses will be counted. The possibility of missing one pulse always exists as the ADE7757 output frequency is running asynchronously to the MCU timer. This would result in a one-in-twenty or 5% error in the power measurement.

INTERNAL OSCILLATOR (OSC)

The nominal internal oscillator frequency is 450 kHz when used with RCLKIN with a nominal value of 6.2 kΩ. The frequency outputs are directly proportional to the oscillator frequency, thus RCLKIN must have low tolerance and low temperature drift to ensure stability and linearity of the chip. The oscillator frequency is inversely proportional to the RCLKIN as shown in Figure 15. Although the internal oscillator operates when used with RCLKIN values between 5.5 kΩ and 20 kΩ, choosing a value within the range of the nominal value, as shown in Figure 15, is recommended.

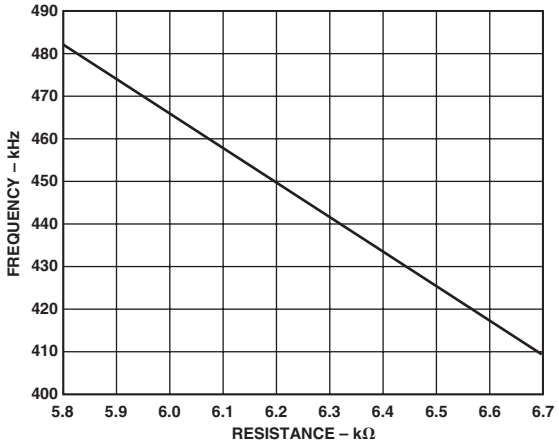


Figure 15. Effect of RCLKIN on Internal Oscillator Frequency (OSC)

TRANSFER FUNCTION

Frequency Outputs F1 and F2

The ADE7757 calculates the product of two voltage signals (on Channel V1 and Channel V2) and then low-pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low, e.g., 0.175 Hz maximum for ac signals with S0 = S1 = 0 (see Table II). This means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The averaging of the real power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation

$$Freq = \frac{515.84 \times V1_{rms} \times V2_{rms} \times F_{1-4}}{V_{REF}^{\ 2}}$$

where

$Freq$ = Output frequency on F1 and F2 (Hz).
$V1_{rms}$ = Differential rms voltage signal on Channel V1 (V).
$V2_{rms}$ = Differential rms voltage signal on Channel V2 (V).
V_{REF} = The reference voltage (2.5 V ± 8%) (V).
F_{1-4} = One of four possible frequencies selected by using the logic inputs S0 and S1—see Table I.

Table I. F_{1-4} Frequency Selection

S1	S0	OSC Relation[1]	F_{1-4} at Nominal OSC (Hz)[2]
0	0	$OSC/2_{19}$	0.86
0	1	$OSC/2_{18}$	1.72
1	0	$OSC/2_{17}$	3.44
1	1	$OSC/2_{16}$	6.86

NOTES
[1]F_{1-4} is a binary fraction of the internal oscillator frequency (OSC).
[2]Values are generated using the nominal frequency of 450 kHz.

Example

In this example, with ac voltages of ±30 mV peak applied to V1 and ±165 mV peak applied to V2, the expected output frequency is calculated as follows:

F_{1-4} = $OSC/2^{19}$ *Hz*, *S*0 = *S*1 = 0
$V1_{rms}$ = $0.03/\sqrt{2}$ *V*
$V2_{rms}$ = $0.165/\sqrt{2}$ *V*
V_{REF} = 2.5 *V (nominal reference value)*

NOTE: If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = \frac{515.85 \times 0.03 \times 0.165 \times F_1}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.204 \times F_1 = 0.175$$

Table II. Maximum Output Frequency on F1 and F2

S1	S0	OSC Relation	Max Frequency* for AC Inputs (Hz)
0	0	$0.204 \times F_1$	0.175
0	1	$0.204 \times F_2$	0.35
1	0	$0.204 \times F_3$	0.70
1	1	$0.204 \times F_4$	1.40

*Values are generated using the nominal frequency of 450 kHz

Frequency Output CF

The pulse output CF (calibration frequency) is intended for calibration purposes. The output pulse rate on CF can be up to 2048 times the pulse rate on F1 and F2. The lower the F_{1-4} frequency selected, the higher the CF scaling (except for the high frequency mode SCF = 0, S1 = S0 = 1). Table III shows how the two frequencies are related, depending on the states of the logic inputs S0, S1, and SCF. Due to its relatively high pulse rate, the frequency at CF logic output is proportional to the instantaneous real power. As with F1 and F2, CF is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this real power information is accumulated over a much shorter time. Therefore, less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the real power signal, the CF output is much more responsive to power fluctuations (see the Signal Processing Block in Figure 3).

Table III. Maximum Output Frequency on CF

SCF	S1	S0	CF Max for AC Signals (Hz)*
1	0	0	128 × F1, F2 = 22.4
0	0	0	64 × F1, F2 = 11.2
1	0	1	64 × F1, F2 = 22.4
0	0	1	32 × F1, F2 = 11.2
1	1	0	32 × F1, F2 = 22.4
0	1	0	16 × F1, F2 = 11.2
1	1	1	16 × F1, F2 = 22.4
0	1	1	2048 × F1, F2 = 2.867 kHz

*Values are generated using the nominal frequency of 450 kHz.

SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION

As shown in Table I, the user can select one of four frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended for driving an energy register (electromechanical or others). Since only four different output frequencies can be selected, the available frequency selection has been optimized for a meter constant of 100 imp/kWh with a maximum current of between 10 A and 120 A. Table IV shows the output frequency for several maximum currents (I_{MAX}) with a line voltage of 220 V. In all cases, the meter constant is 100 imp/kWh.

Table IV. F1 and F2 Frequency at 100 imp/kWh

I_{MAX} (A)	F1 and F2 (Hz)
12.5	0.076
25.0	0.153
40.0	0.244
60.0	0.367
80.0	0.489
120.0	0.733

The F_{1-4} frequencies allow complete coverage of this range of output frequencies (F1, F2). When designing an energy meter, the nominal design voltage on Channel V2 (voltage) should be set to half-scale to allow for calibration of the meter constant. The current channel should also be no more than half-scale when the meter sees maximum load. This will allow overcurrent signals and signals with high crest factors to be accommodated. Table V shows the output frequency on F1 and F2 when both analog inputs are half-scale. The frequencies listed in Table V align very well with those listed in Table IV for maximum load.

Table V. F1 and F2 Frequency with Half-Scale AC Inputs

S1	S0	F_{1-4} (Hz)*	Frequency on F1 and F2– CH1 and CH2 Half-Scale AC Input*
0	0	0.86	$0.051 \times F_1$ 0.044 Hz
0	1	1.72	$0.051 \times F_2$ 0.088 Hz
1	0	3.44	$0.051 \times F_3$ 0.176 Hz
1	1	6.86	$0.051 \times F_4$ 0.352 Hz

*Values are generated using the nominal frequency of 450 kHz.

When selecting a suitable F_{1-4} frequency for a meter design, the frequency output at I_{MAX} (maximum load) with a meter constant of 100 imp/kWh should be compared with column four of Table V. The closest frequency in Table V will determine the best choice of frequency (F_{1-4}). For example, if a meter with a maximum current of 25 A is being designed, the output frequency on F1 and F2 with a meter constant of 100 imp/kWh is 0.153 Hz at 25 A and 220 V (from Table IV). Looking at Table V, the closest frequency to 0.153 Hz in column four is 0.176 Hz. Therefore, F3 (3.44 Hz—see Table I) is selected for this design.

Frequency Outputs

Figure 1 shows a timing diagram for the various frequency outputs. The outputs F1 and F2 are the low frequency outputs that can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating low frequency pulses. The F1 and F2 pulse widths (t_1) are set such that if they fall below 1062 ms (0.942 Hz) they are set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table II.

The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 173 ms wide active high pulse (t_4) at a frequency proportional to active power. The CF output frequencies are given in Table III. As in the case of F1 and F2, if the period of CF (t_5) falls below 346 ms, the CF pulse width is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulse width is 25 ms.

NOTE: When the high frequency mode is selected (i.e., SCF = 0, S1 = S0 = 1), the CF pulse width is fixed at 35 µs. Therefore, t_4 will always be 35 µs, regardless of output frequency on CF.

NO LOAD THRESHOLD

The ADE7757 also includes a no-load threshold and start-up current feature that will eliminate any creep effects in the meter. The ADE7757 is designed to issue a minimum output frequency. Any load generating a frequency lower than this minimum frequency will not cause a pulse to be issued on F1, F2, or CF. The minimum output frequency is given as 0.0014% for each of the F_{1-4} frequency selections (see Table I). For example, for an energy meter with a meter constant of 100 imp/kWh on F1, F2 using F_3 (3.44 Hz), the minimum output frequency at F1 or F2 would be 0.0014% of 3.44 Hz or 4.81×10^{-5} Hz. This would be 3.08×10^{-3} Hz at CF ($64 \times$ F1 Hz) when SCF = S0 = 1, S1 = 0. In this example, the no-load threshold would be equivalent to 1.7 W of load or a start-up current of 8 mA at 220 V. Compare this value to the IEC 1036 specification which states that the meter must start up with a load equal to or less than 0.4% Ib. For a 5 A (Ib) meter, 0.4% of Ib is equivalent to 20 mA.

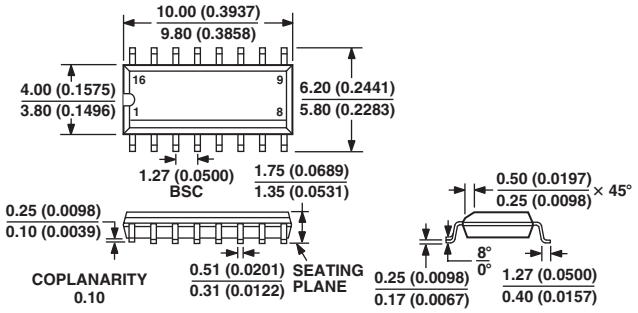
Negative Power Information

The ADE7757 detects when the current and voltage channels have a phase shift greater than 90°. This mechanism can detect wrong connection of the meter or generation of negative power. The REVP pin output will go active high when negative power is detected and active low if positive power is detected. The REVP pin output changes state as a pulse is issued on CF. The REVP pin is not functional in the current version and will only work in the A version (ADE7757A).

OUTLINE DIMENSIONS

16-Lead Standard Small Outline Package [SOIC]
Narrow Body
(RN-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
10/03—Data Sheet changed from REV. 0 to REV. A.	
Changes to FEATURES	1
Changes to GENERAL DESCRIPTION	1
Changes to ORDERING GUIDE	4
Change to Typical Connection Diagrams section	10
Updated OUTLINE DIMENSIONS	15

C02898–0–10/03(A)