

Small Signal Product

Features

- ◇ Meet IEC61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
- ◇ Meet IEC61000-4-4 (EFT) rating. 40A (5/50 μs)
- ◇ Protects one Bi-directional I/O line
- ◇ Working Voltage : 5V
- ◇ Pb free version, RoHS compliant, and Halogen free

Mechanical Data

- ◇ Case : SOD-523F flat lead small outline plastic package
- ◇ Terminal : Matte tin plated, lead free, solderable per MIL-STD-202, method 208 guaranteed
- ◇ High temperature soldering guaranteed : 260°C/10s
- ◇ Mounting Position : Any
- ◇ Weight : 2 mg (approximately)

Applications

- ◇ Cell Phone Handsets and Accessories
- ◇ Microprocessor Based Equipment
- ◇ Personal Digital Assistants (PDA's)
- ◇ Portable Instrumentation
- ◇ Peripherals

Ordering Information

Part No.	Package	Packing	Packing code	Packing code (Green)	Marking	Manufacture code
TESDD5V0HC	SOD-523F	3K / 7" Reel	RK	RKG	B5	

Note : Detail please see "Ordering Information(detail, example)" below.

Maximum Ratings and Electrical Characteristics

Rating at 25 °C ambient temperature unless otherwise specified.

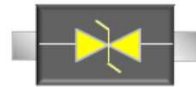
Maximum Ratings

Parameter	Symbol	Value	Units
Power Dissipation	P_D	150	W
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 30	KV
ESD per IEC 61000-4-2 (Contact)		± 30	
Thermal Resistance form Junction to Ambient	R_{thJA}	833	°C/W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics

Parameter	Symbol	Min	Max	Units
Reverse Stand-Off Voltage	V_{RWM}	-	5	V
Reverse Breakdown Voltage $I_R = 1\text{ mA}$	$V_{(BR)}$	5.8	-	V
Reverse Leakage Current $V_R = 5\text{ V}$	I_R	-	1	μA
Clamping Voltage $I_{PP} = 5\text{ A}$ $I_{PP} = 12\text{ A}$	V_C	-	9.5	V
		-	13	
Junction Capacitance $V_R = 0\text{ V}, f = 1.0\text{ MHz}$	C_J	27 (Typ.)		pF

SOD-523F



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RATINGS AND CHARACTERISTIC CURVES

Fig. 1 Non-Repetitive Peak Pulse Power VS. Pulse Time

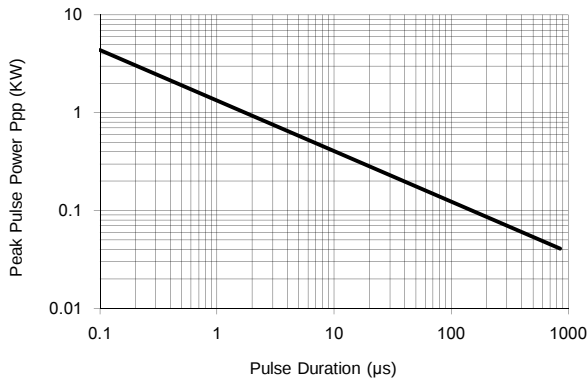


Fig. 2 Pulse Waveform

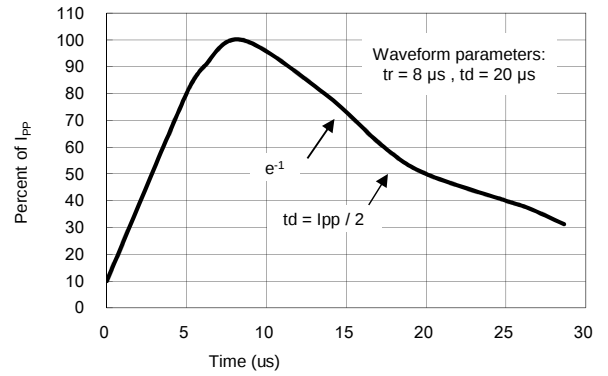


Fig. 3 Admissible Power Dissipation Curve

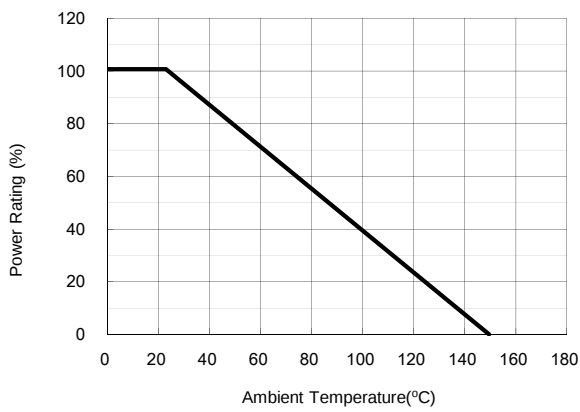


Fig. 4 Typical Junction Capacitance

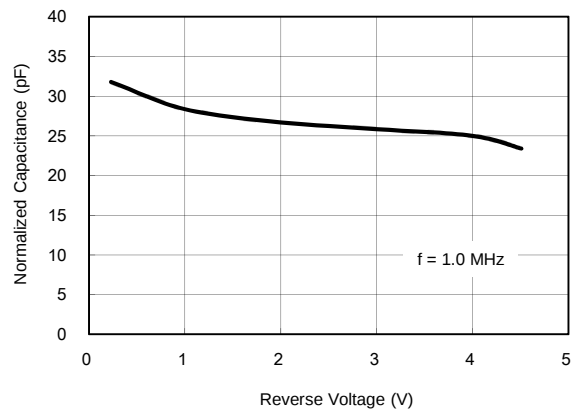
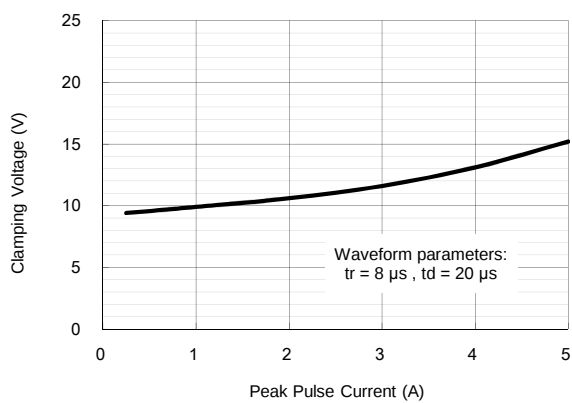


Fig. 5 Clamping Voltage VS. Peak Pulse Current



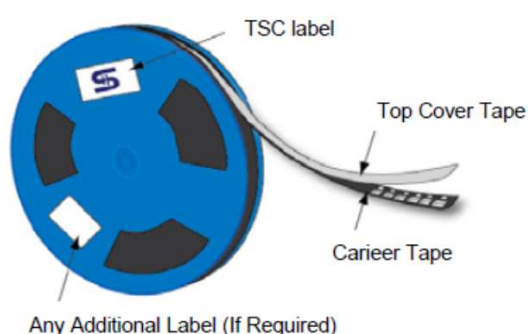
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Ordering information (Detail, example)

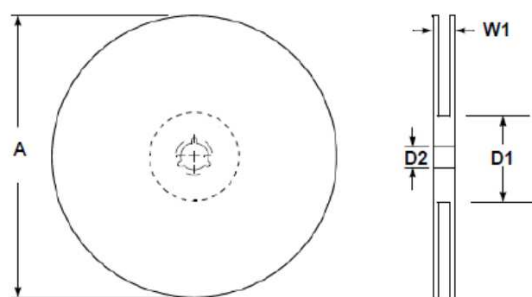
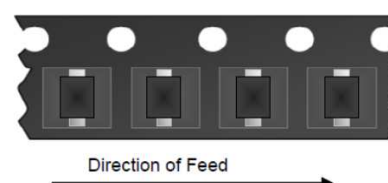
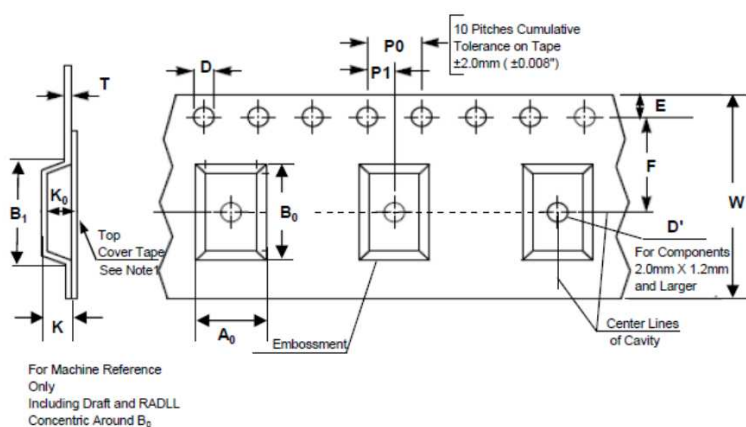
Part No.	Package	Packing	Packing code	Packing code (Green)	Marking	Manufacture code
TESDD5V0HC	SOD-523F	3K / 7" Reel	RK	RKG	B5	(Note)
TESDD5V0HC	SOD-523F	3K / 7" Reel	RK	RKG	B5	M0
TESDD5V0HC	SOD-523F	3K / 7" Reel	RK	RKG	B5	

Note : Manufacture special control, if empty means no special control requirement.

Tape & Reel specification



Item	Symbol	Dimension(mm)
Carrier depth	K	2.40 Max.
Sprocket hole	D	1.50 ± 0.10
Reel outside diameter	A	178 ± 1
Reel inner diameter	D1	50 Min.
Feed hole width	D2	13.0 ± 0.5
Sprocket hole position	E	1.75 ± 0.10
Punch hole position	F	3.50 ± 0.05
Sprocket hole pitch	P0	4.00 ± 0.10
Embossment center	P1	2.00 ± 0.10
Overall tape thickness	T	0.6 Max.
Tape width	W	8.30 Max.
Reel width	W1	14.4 Max.

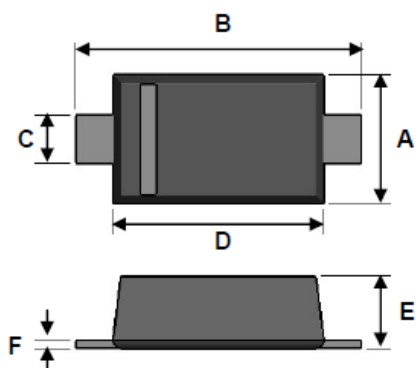


Note 1 : A_0 , B_0 , and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max. The component cannot rotate more than 10° within the determined cavity.

Note 2 : If B_1 exceeds 4.2mm(0.165") for 8 mm embossed tape, the tape may not feed through all tape feeders.

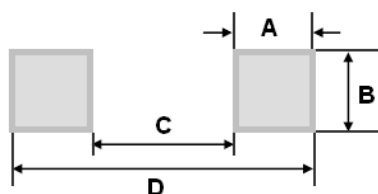
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Dimensions



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	0.70	0.90	0.028	0.035
B	1.50	1.70	0.059	0.067
C	0.25	0.40	0.010	0.016
D	1.10	1.30	0.043	0.051
E	0.50	0.77	0.020	0.030
F	0.07	0.20	0.003	0.008

Suggested PAD Layout



DIM.	Unit(mm)	Unit(inch)
	Typ.	Typ.
A	0.40	0.016
B	0.40	0.016
C	1.00	0.039
D	1.80	0.071

Notes : 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

Applications Information

- ◇ Designed to protect one data, I/O, or power supply line
- ◇ Designed to protect sensitive electronics from damage or latch-up due to ESD
- ◇ Designed to replace multilayer varistors (MLVs) in portable applications
- ◇ Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
- ◇ The combination of small size and high ESD surge capability makes them ideal for use in portable applications

Circuit Board Layout Recommendations

Good circuit board layout is critical for the suppression of ESD induced transients

- ◇ Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling
- ◇ Minimize the path length between the ESD Protection Diode and the protected line
- ◇ Minimize all conductive loops including power and ground loops
- ◇ The ESD transient return path to ground should be kept as short as possible