January 16, 2009
Datasheet No. - PD97376

IRS21856S

High(Dual Mode) and Low Side Driver

Features

- High side Programmable ramp gate drive
- High side generic gate driver integrated using the same high side output pin
- Low side generic gate driver
- Under voltage lockout for VCC & VBS
- 5V input logic compatible
- Tolerant to negative transient voltage on VS
- Shoot through prevention
- RoHS compliant

Product Summary

Topology	PDP
V_{OFFSET}	≤ 600 V
HO1 SR+	4.5V/us
I_{o+} & I_{o-} (typical)	0.5A & 0.5A
t_{ON} & t_{OFF} (typical)	160ns & 160ns

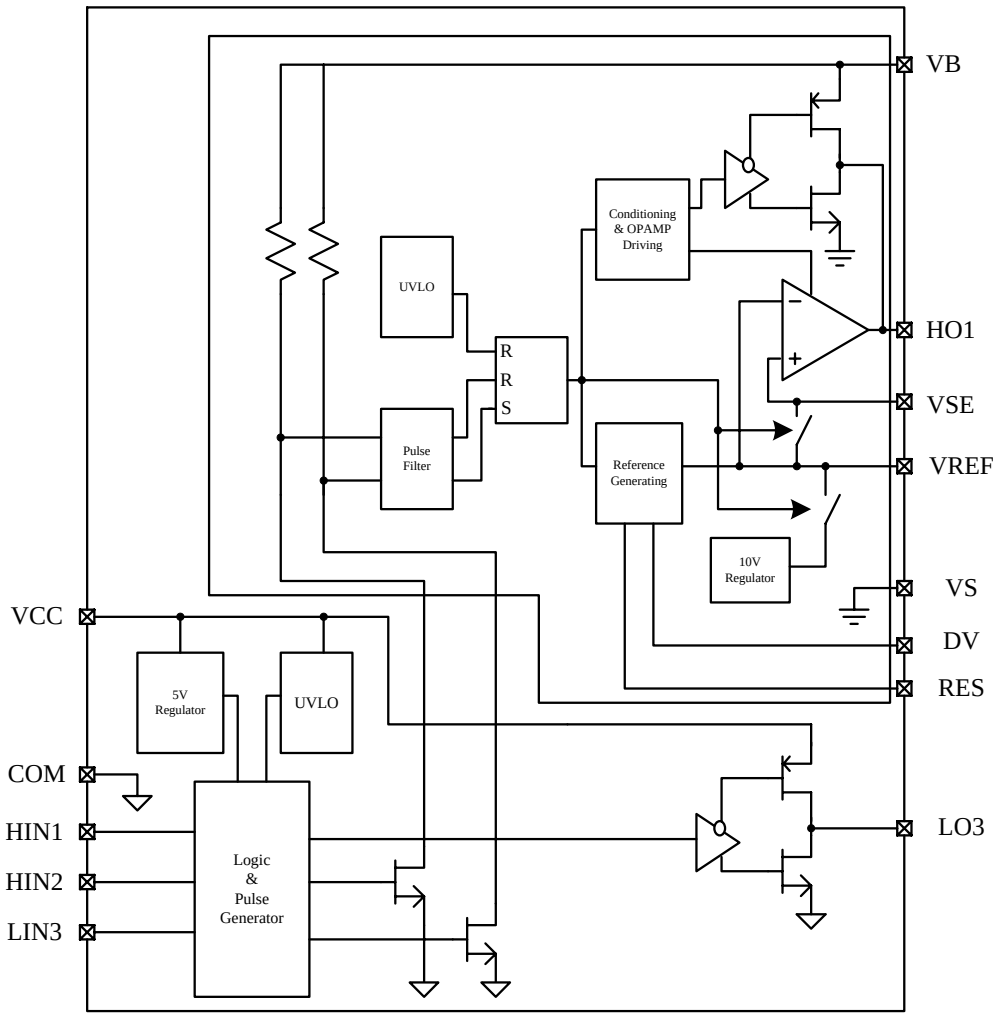
Package Options

14-Lead SOIC (narrow body)

Description

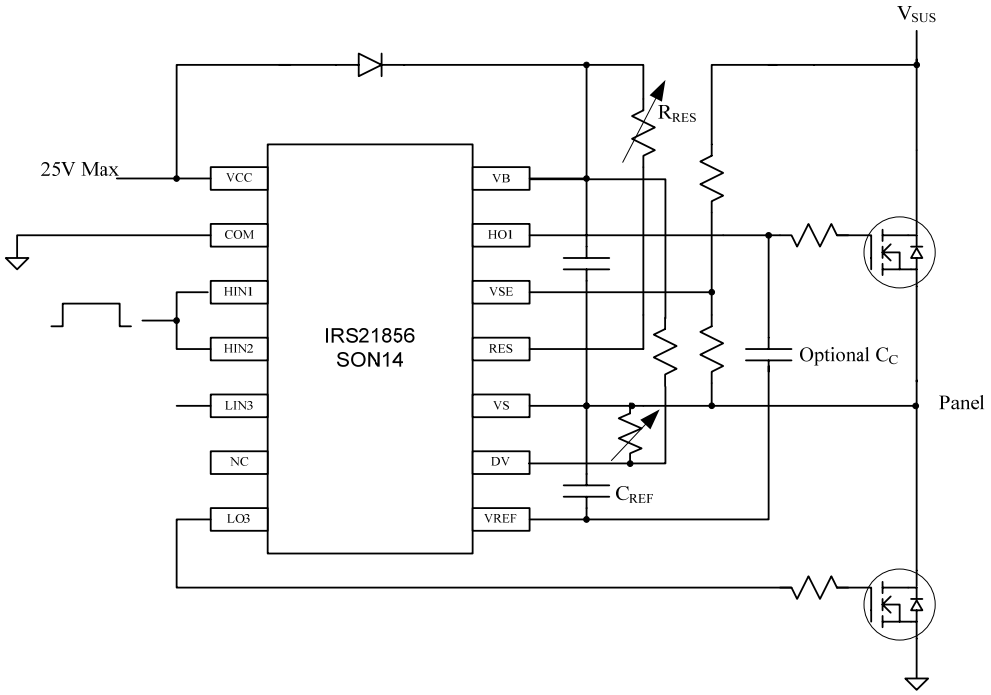
The IRS21856 is high voltage and programmable ramp slope control gate driver for MOSFET and IGBT with single high side dual mode driver and low side driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with 5V standard CMOS or LSTTL output. The output driver features a programmable slope control by external R/C and input signal. The floating channels can be used to drive an N-channel power MOSFET or IGBT in the high side configuration, which operates up to 600 volts above the COM ground.

Simplified Block Diagram

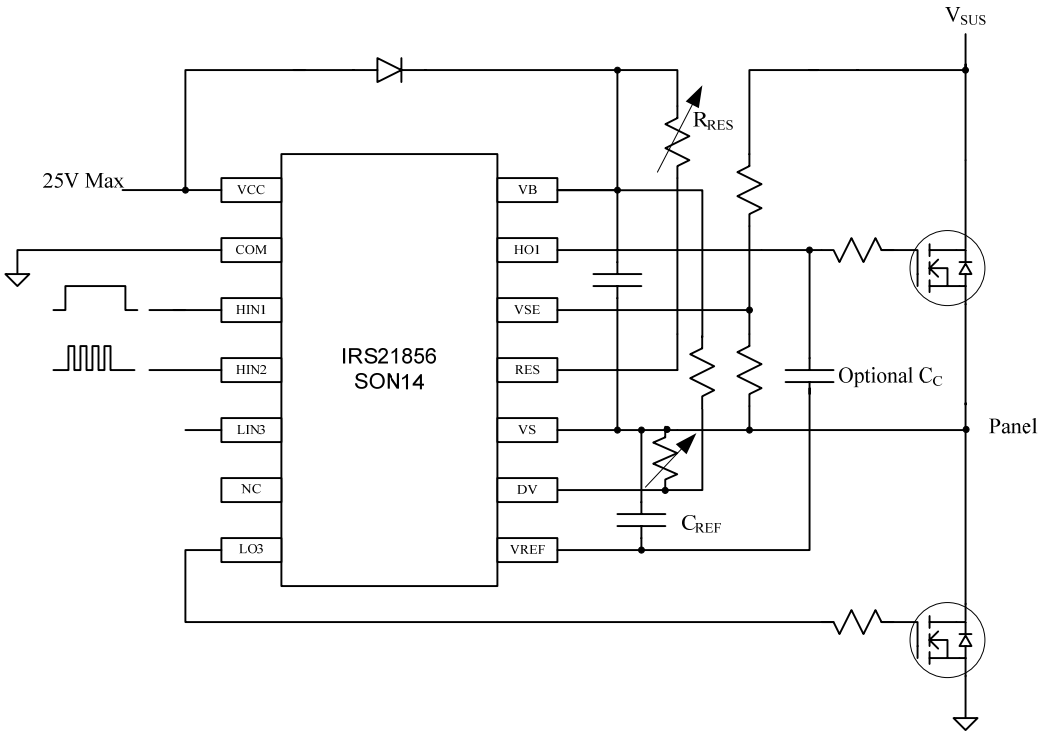


Typical Connection Diagrams

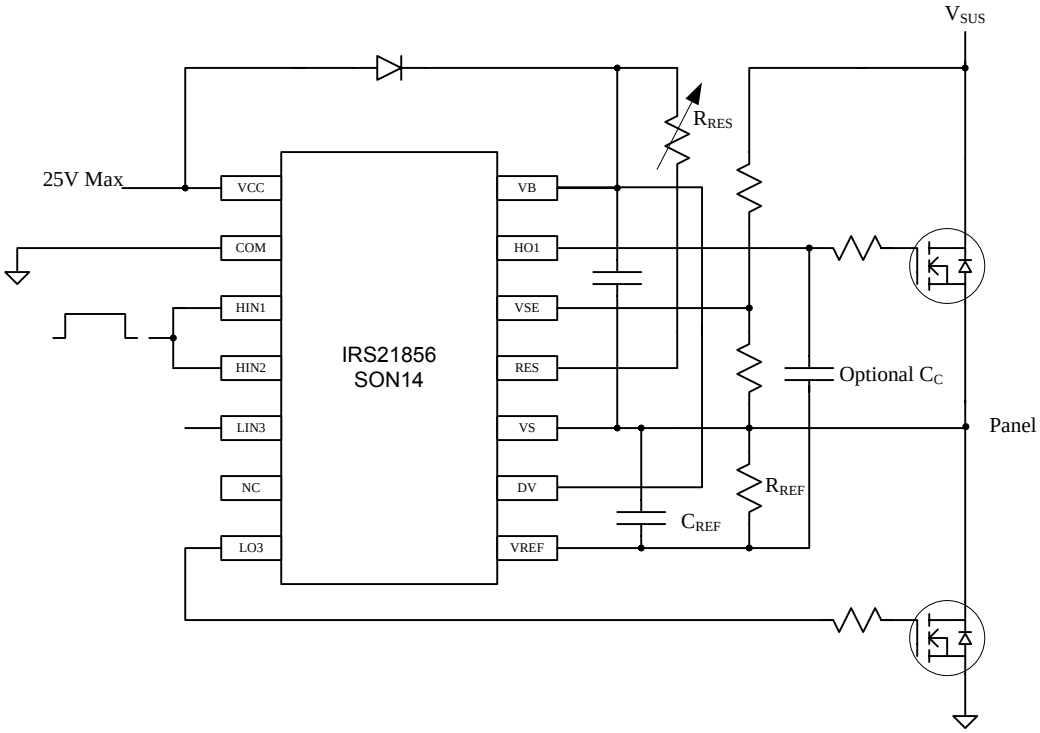
A) Linear Ramp driver's connection diagram



B) Stepwise Linear Ramp driver's connection diagram



C) Exponential Ramp driver's connection diagram



Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC14N	MSL2††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I , Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Symbol	Definition	Min	Max	Units
V_{CC}	Low side supply voltage	-0.3	25	V
V_{IN}	Logic input voltage (HIN1, HIN2, LIN3)	COM-0.3	VCC +0.3	V
V_{LO}	Low side gate drive output voltage	COM-0.3	VCC +0.3	V
V_{DV}, V_{VREF}	High side inputs voltage	VS-0.3	VB+0.3	V
V_{VSE}, V_{RES}	High side inputs voltage	VS-0.3	VB+0.3	V
V_B	High side floating well supply voltage	-0.3	625	V
V_S	High side floating well supply return voltage	VB-25	VB+0.3	V
V_{HO1}	Floating gate drive output voltage	VS-0.3	VB+0.3	V
dV_S/dt	Allowable VS offset supply transient relative to COM	-	50	V/ns
P_D	Package Power Dissipation @ TA<=+25ºC	-	1.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	-	120	ºC/W
T_J	Junction Temperature	-55	150	ºC
T_S	Storage Temperature	-55	150	ºC
T_L	Lead temperature (Soldering, 10 seconds)	-	300	ºC

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The offset rating are tested with supplies of (VCC-COM) = (VB-VS)=15V.

Symbol	Definition	Min	Max	Units
V_{CC}	Low side supply voltage	10	20	V
V_{IN}	HIN1, HIN2, LIN3 input voltage	COM	V_{CC}	V
V_{LO3}	Low side gate drive output voltage	COM	V_{CC}	V
V_B	High side floating well supply voltage	V_S+10	V_S+20	V
V_{RES}	RES input voltage	V_S	V_B	V
V_{DV}	DV input voltage	V_S	V_B	V
$V_{VREF, VSE}$	VREF and VSE input voltage	V_S	V_B -3	V
V_S	High side floating well supply offset voltage	Note2††	600	V
V_{HO1}	Floating gate drive output voltage	V_S	V_B	V
T_A	Ambient Temperature	-40	125	ºC

† V_S and V_B voltages will be tolerant to short negative transient spikes. These will be defined and specified in the future.

†† Logic operation for Vs of -5 to 600V. Logic state held for Vs of -5V to $-V_{BS}$. (Please refer to Design Tip DT97-3 for more details).

Static Electrical Characteristics

(VCC-COM) = (VB-VS)=15V. T_A = 25ºC. The V_{IN}, $V_{IN\,TH}$ and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to respective VS, COM and are applicable to the respective output leads HO1, LO3. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.1	9.0	9.9	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.5	8.3	9.1		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.1	9.0	9.9		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.5	8.3	9.1		
I_{LK}	High side floating well offset supply leakage current	---	---	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent VBS supply current	---	4.7	8.5	mA	IN1, 2 = 5V, RES=130kohm
		---	800	1400	µA	IN1, 2 = 0V, RES=130kohm
I_{QCC}	Quiescent VCC supply current	---	120	250		IN1,2,3 = 0V or 5V
V_{IH}	Logic “1” input voltage	3.5	---	---	V	
V_{IL}	Logic “0” input voltage	---	---	0.8		
I_{IN+}	Logic “1” input bias current	---	5	---	µA	V_{IN} =5V
I_{IN-}	Logic “0” input bias current	---	0	---		V_{IN} =0V
I_{O+} _ $_{HO1,LO3}$	Output high short circuit pulsed current	---	0.5	---	A	V_O=15V,V_{IN}=5V, PW<=10us
I_{O-} _ $_{HO1,LO3}$	Output low short circuit pulsed current	---	0.5	---		V_O=0V,V_{IN}=0V, PW<=10us
V_{OL} _ $_{HO1, LO3}$	Low level output voltage	---	35	150	mV	Io=2mA
V_{OH} _ $_{HO1, LO3}$	High level output voltage, Vbias-Vo	---	15	80	mV	Io=2mA
DV exp+	Positive DV input threshold for exponential ramp	---	9.5	---	V	C_{REF} =1nF, V_{SE} open R_{RES} =130K

DV / Linear (Stepwise) Mode

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
VREF, hold	DV reference voltage	0.4	0.5	0.6	V	DV=500mV, C_{REF} =1nF, V_{SE} open R_{RES} =130K,
		2.82	3	3.18		DV=3V, C_{REF} =1nF, V_{SE} open R_{RES} =130K,

Dynamic Electrical Characteristics

(VCC-COM)= (VB-VS)=15V. T_A = 25ºC. C_L = 1000pF unless otherwise specified. All parameters are reference to COM.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Internal Operational Amplifier Characteristics						
$t_{ref\_ln\_ramp}$	Linear ramp reference 10% to 90%	110	170	230	µs	C_{REF} =1nF, V_{SE} open, R_{RES} =130K, V_{DV} =VS=COM
Gm	OTA transconductance	---	12	---	mS	CL_LO=1nF, V_{DV} =V_B, R_{RES} =130K, dc bias 5V
$G_{open\ loop}$	Open loop gain	45	60	---	dB	Cc =1nF, V_{DV} =V_B, R_{RES} =130K
BW_{SS}	Small signal bandwidth	---	3.5	---	MHz	Cc =1nF V_{DV} =V_B, R_{RES} =130K
V_{OS}	Input offset voltage	---	10	---	mV	V_{DV} =V_B, R_{RES} =130K
$HO1_{SR+}$	Output positive slew rate	---	4.5	---	V/µs	CL_HO1=1nF, V_{DV} =V_B, R_{RES} =130K
CMRR	Common mode rejection ratio	55	65	---	dB	V_{DV} =V_B, R_{RES} =130K
PSRR	Power supply rejection ratio	55	65	---	dB	V_{DV} =V_B, R_{RES} =130K
Propagation Delay Characteristics						
t_{on}	Turn-on delay (HO1, LO3)	---	150	250	ns	Gate Drive Mode C_L =1nF
t_{off}	Turn-off delay (HO1, LO3)	---	160	260		
t_r	Turn-on rise from 10% to 90%	---	30	70		
t_f	Turn-off fall from 90% to 10%	---	20	70		
MT	Delay matching, HO1 & LO3 turn-on/off			50		

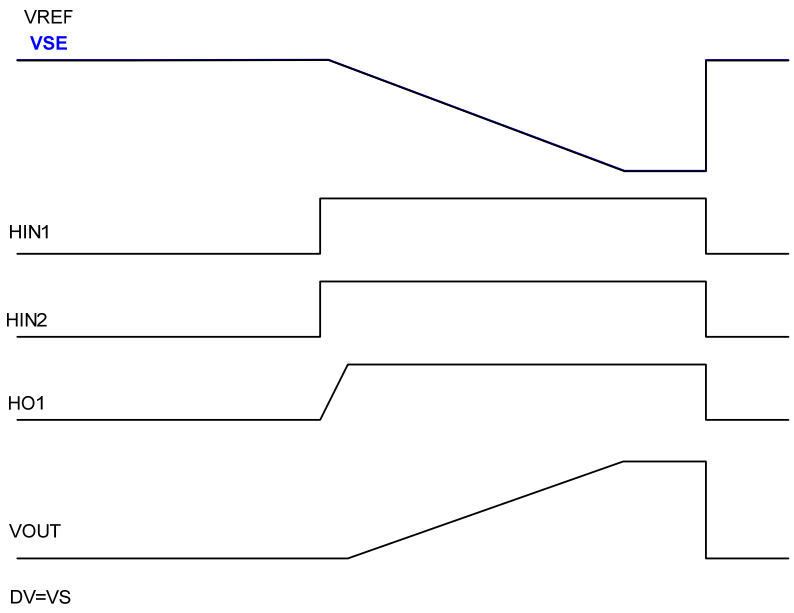


Figure 1A1 Input/Output Timing Diagram: Linear Ramp

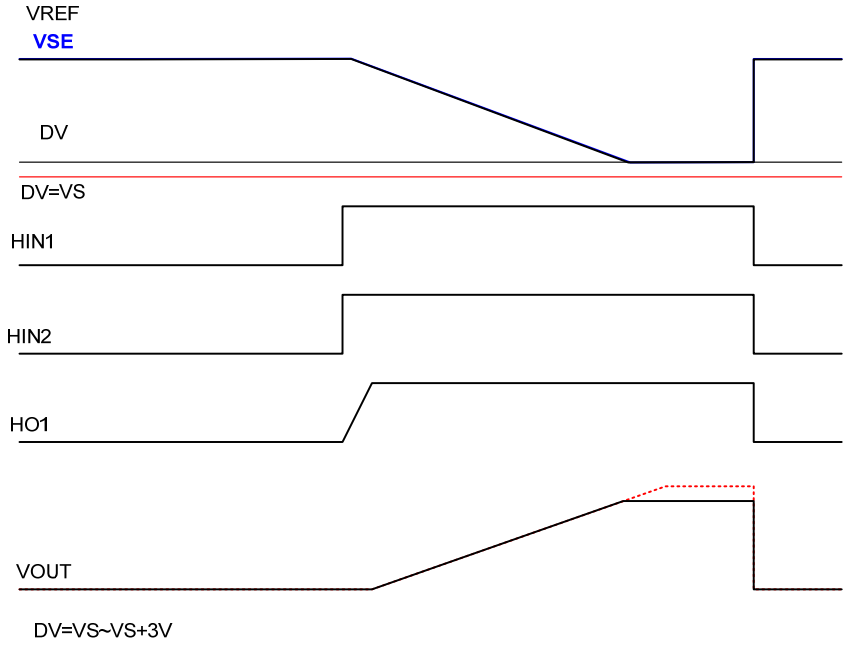


Figure 1A2 Input/Output Timing Diagram: Linear Ramp with voltage difference

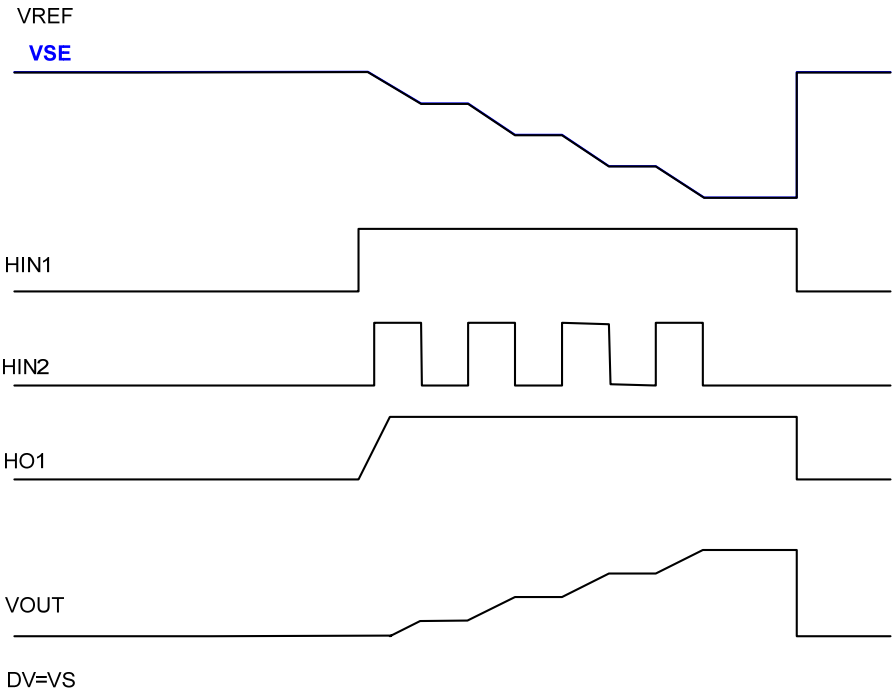


Figure 1B Input/Output Timing Diagram: Stepwise linear Ramp

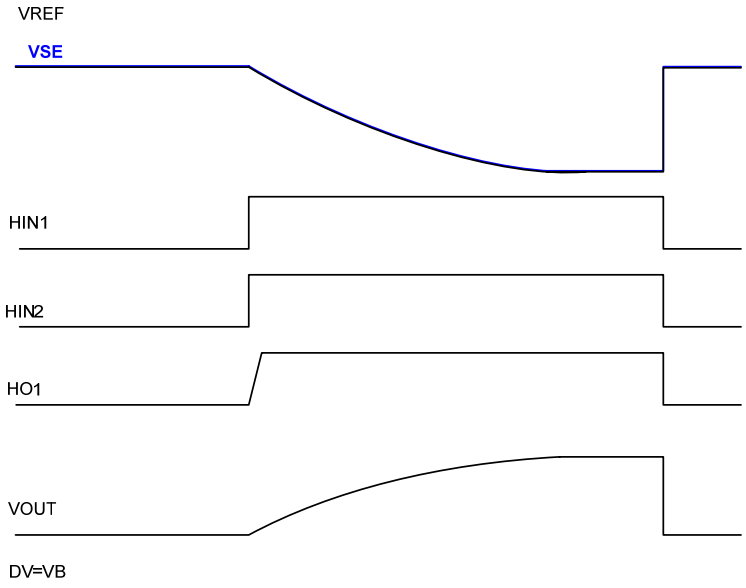


Figure 1C Input/Output Timing Diagram: Exponential Ramp

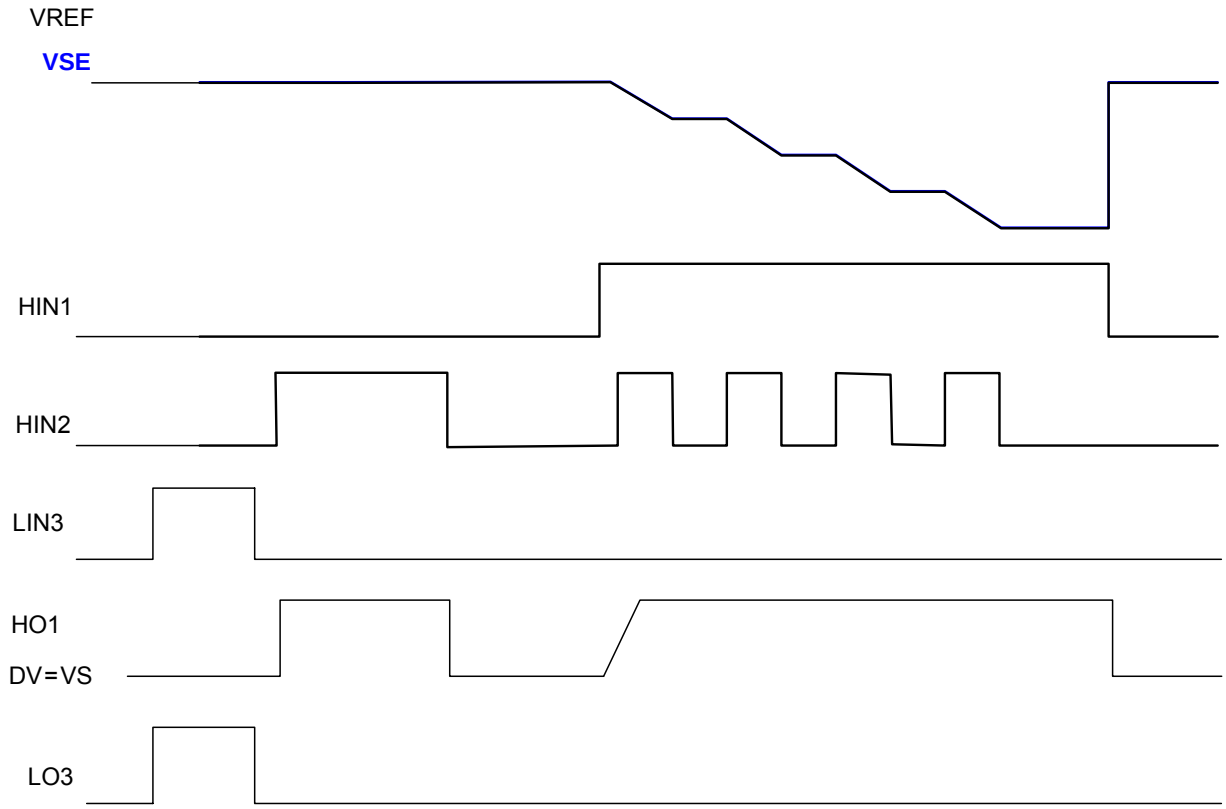


Figure 1D Input/Output Timing Diagram : HO1/LO3 outputs

Logic Truth Table

HIN1	HIN2	LIN3	LO3	OTA of HO1	Gate driver of HO1
0	0	0	0	High impedance (HIZ)	0
0	0	1	1	High impedance (HIZ)	0
0	1	0	0	High impedance (HIZ)	1
0	1	1	0	High impedance (HIZ)	0
1	1	0	0	Linear/Exp ramp depend on DV pin	High impedance (HIZ)
1	1	1	0	High impedance (HIZ)	0
1	Step(0/1)	0	0	Stepwise linear if DV pin is Vs	High impedance (HIZ)
1	Step(0/1)	1	0	High impedance (HIZ)	0

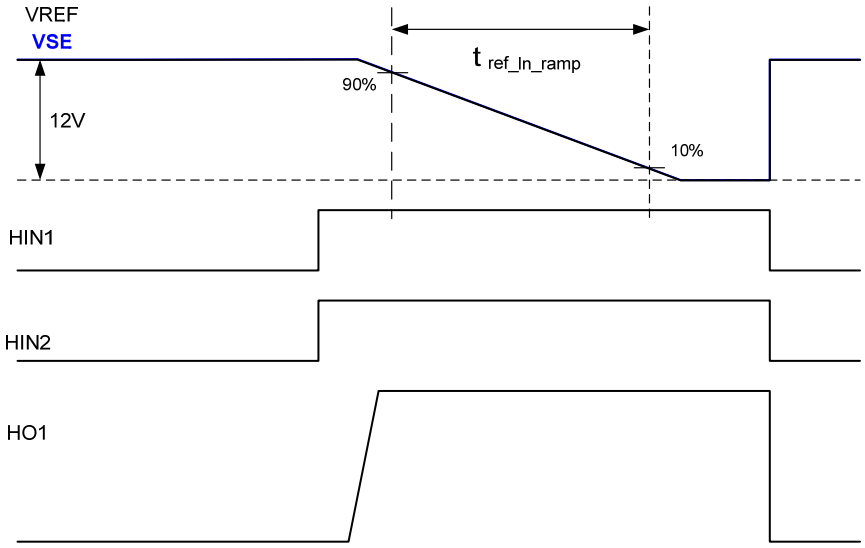


Figure 2 Timing Definitions of V_{REF}

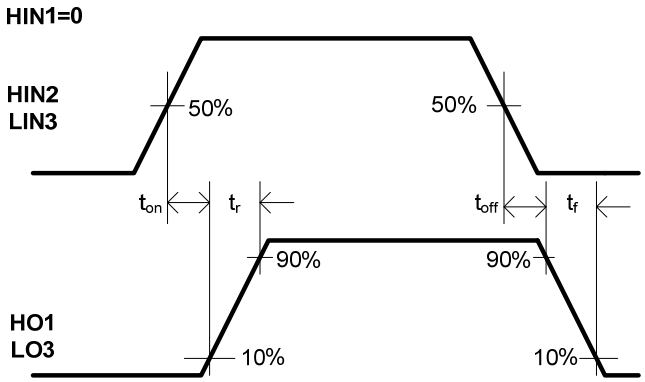


Figure 3 Switching Time Waveform Definitions of HO1 and LO3

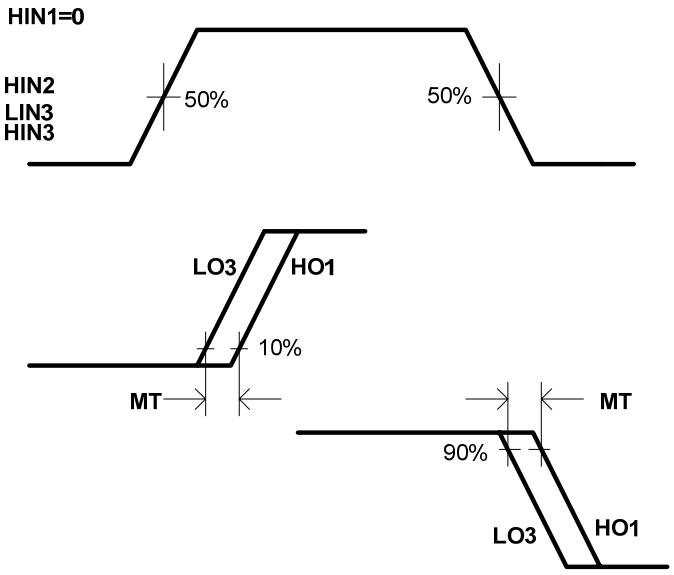
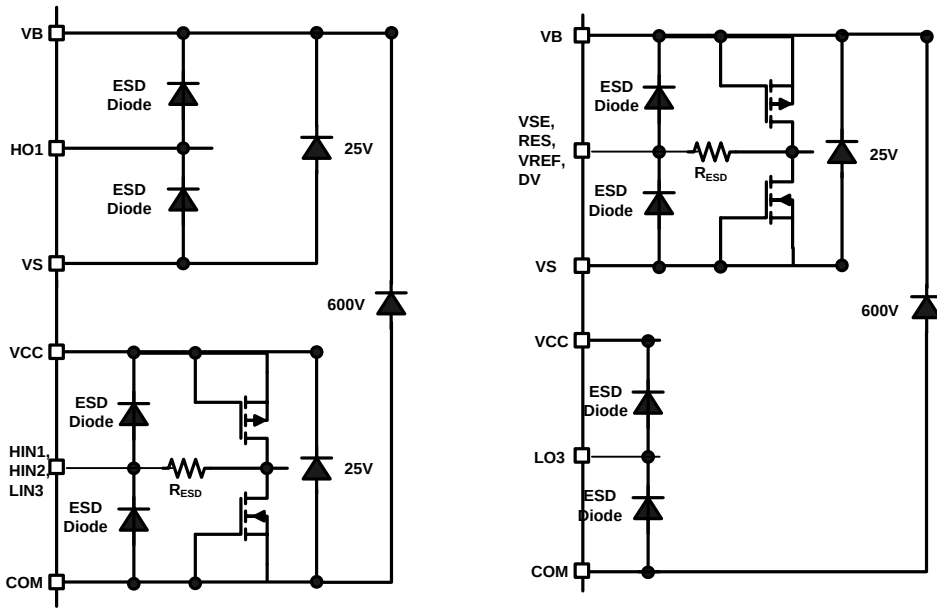


Figure 4 Delay Matching Waveform Definitions

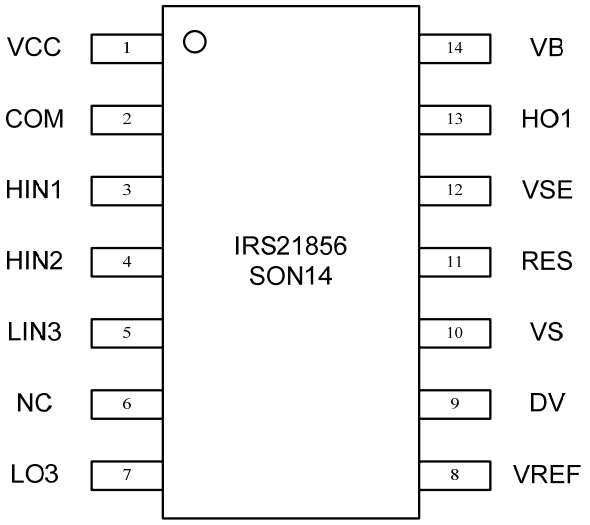
Input/Output Pin Equivalent Circuit Diagrams



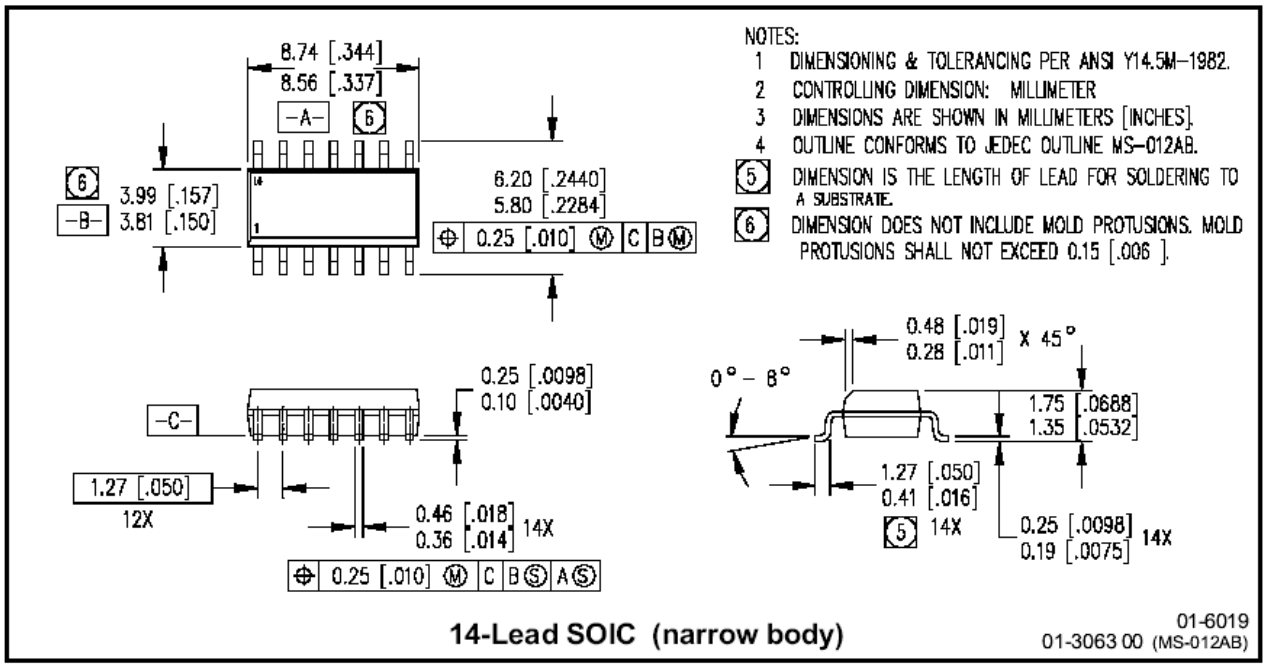
Lead Definitions

PIN#	Symbol	Description
1	VCC	Low side supply voltage
2	COM	Low side supply return
3	HIN1	Logic input for HO1 ramp reference control
4	HIN2	Logic input for high side gate driver outputs, in phase
5	LIN3	Logic input for low side gate driver output
6	NC	No Connection
7	LO3	Low side gate driver output
8	VREF	External programmable R/C input for ramp generation
9	DV	Ramp selection and programmable difference voltage (DV) input
10	VS	High side gate drive floating supply return
11	RES	Adjustable current source resistor input
12	VSE	Voltage sense input
13	HO1	High side gate driver output
14	VB	High side gate drive floating supply

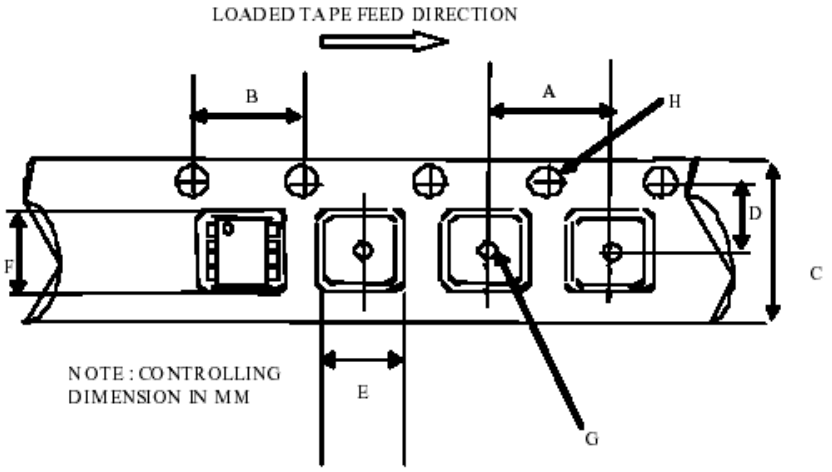
Lead Assignments



Package Details: SOIC14

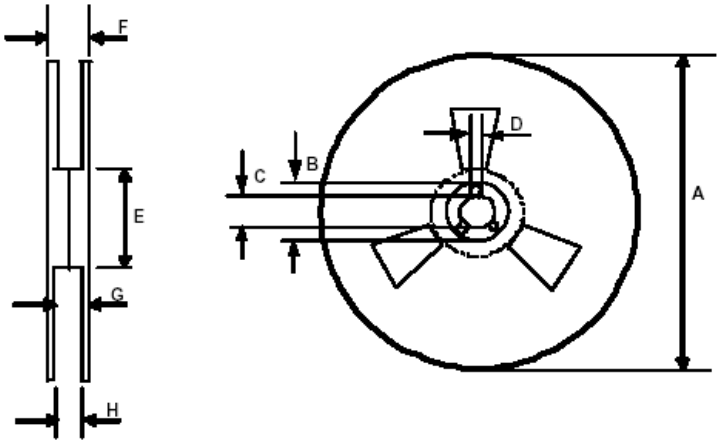


Tape and Reel Details: SOIC14



CARRIER TAPE DIMENSION FOR 14SOICN

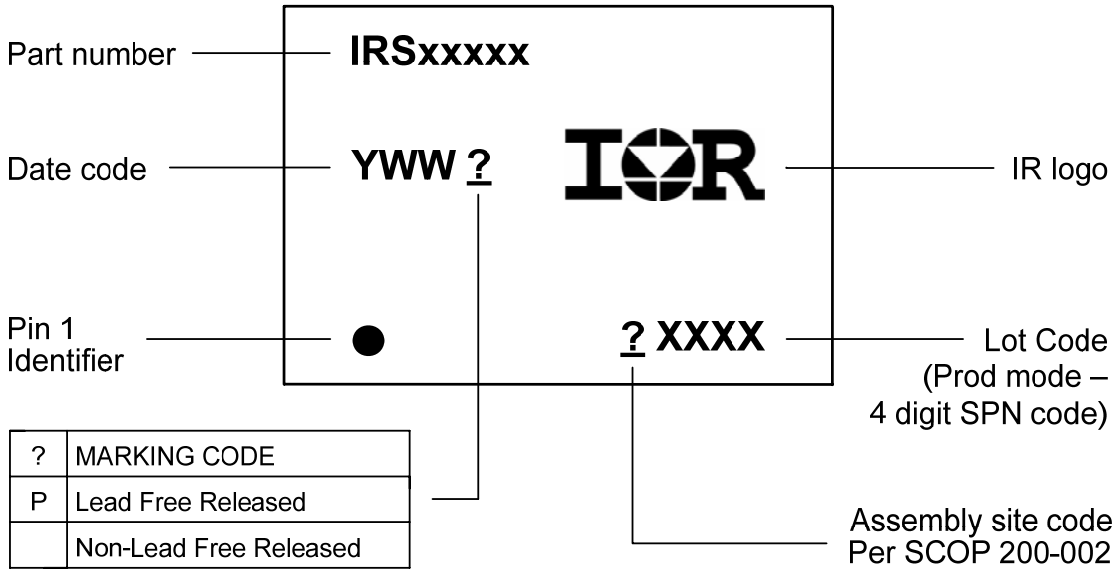
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 14SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS21856S	SOIC14	Tube/Bulk	55	IRS21856SPBF
		Tape and Reel	2500	IRS21856STRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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