



July 2014

# FDMS86202

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

120 V, 64 A, 7.2 mΩ

### Features

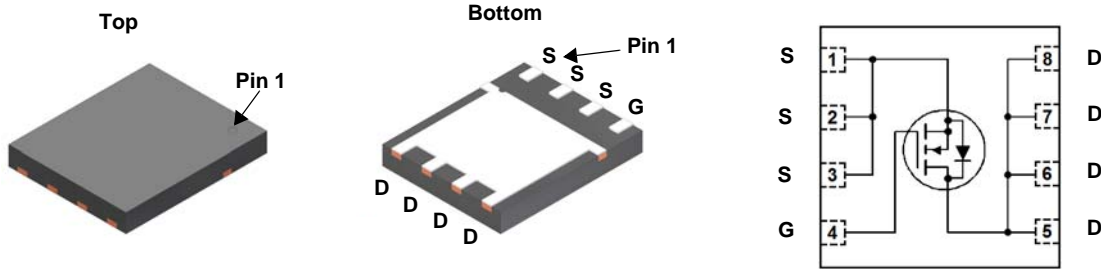
- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 7.2 mΩ at  $V_{GS} = 10$  V,  $I_D = 13.5$  A
- Max  $r_{DS(on)}$  = 10.3 mΩ at  $V_{GS} = 6$  V,  $I_D = 11.5$  A
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Application

- DC-DC Conversion



Power 56

### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	120	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	$T_C = 25^\circ\text{C}$	A
	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	
	-Pulsed	(Note 4)	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	W
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86202	FDMS86202	Power 56	13 "	12 mm	3000 units

FDMS86202 N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	120			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		103		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 96\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 13.5\text{ A}$		6.0	7.2	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 11.5\text{ A}$		8.1	10.3	
		$V_{GS} = 10\text{ V}$ , $I_D = 13.5\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		10.9	13.2	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 13.5\text{ A}$		44		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		3195	4250	pF
$C_{oss}$	Output Capacitance			449	600	pF
$C_{rss}$	Reverse Transfer Capacitance			17	30	pF
$R_g$	Gate Resistance		0.1	0.9	2.7	$\Omega$

### Switching Characteristics

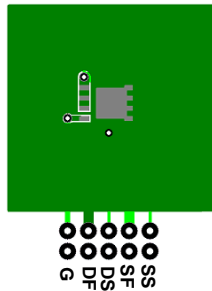
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 60\text{ V}$ , $I_D = 13.5\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		21	33	ns	
$t_r$	Rise Time			6	13	ns	
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns	
$t_f$	Fall Time			5	11	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		45	64	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 6\text{ V}$	$V_{DD} = 60\text{ V}$ , $I_D = 13.5\text{ A}$		29	41	nC
$Q_{gs}$	Gate to Source Charge				14.3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				8.7		nC

### Drain-Source Diode Characteristics

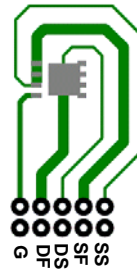
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.69	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 13.5\text{ A}$ (Note 2)		0.76	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 13.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		73	118	ns
$Q_{rr}$	Reverse Recovery Charge			117	187	nC

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $45\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $115\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

- $E_{AS}$  of 600 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 20\text{ A}$ ,  $V_{DD} = 120\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 65\text{ A}$ .

- Pulse Id limited by junction temperature,  $t_d \leq 100\text{ }\mu\text{s}$ , please refer to SOA curve for more details.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

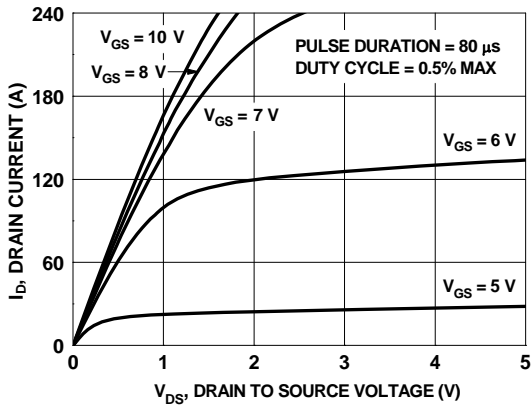


Figure 1. On Region Characteristics

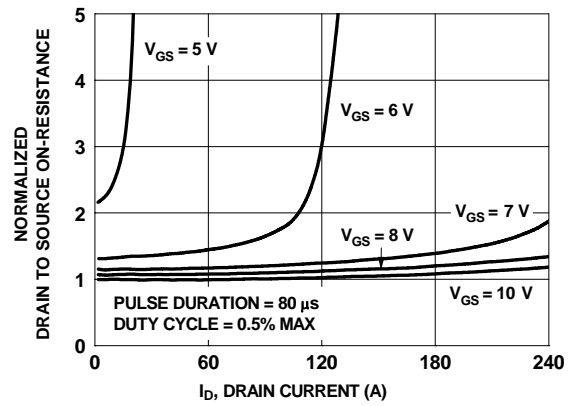


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

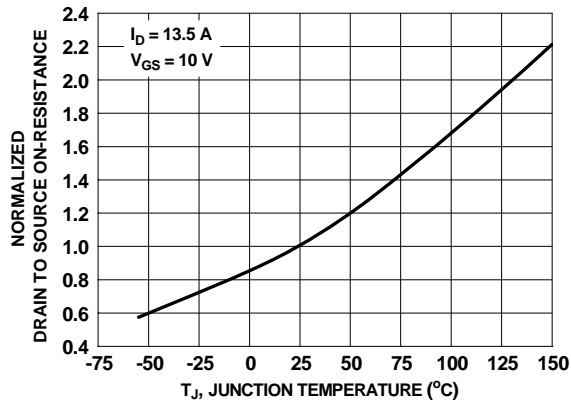


Figure 3. Normalized On Resistance vs Junction Temperature

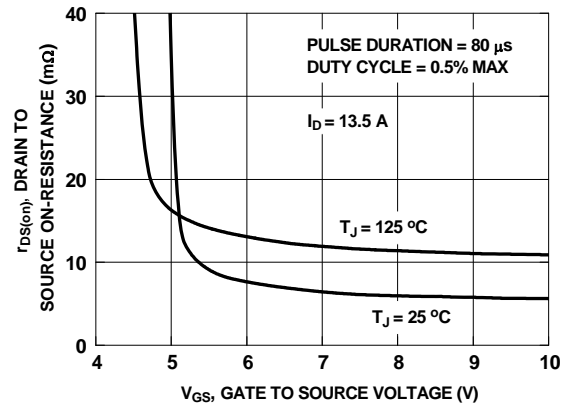


Figure 4. On-Resistance vs Gate to Source Voltage

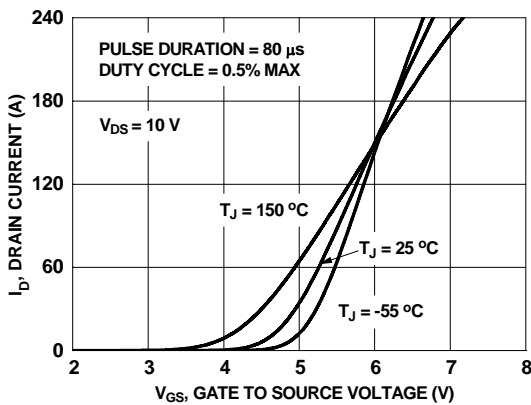


Figure 5. Transfer Characteristics

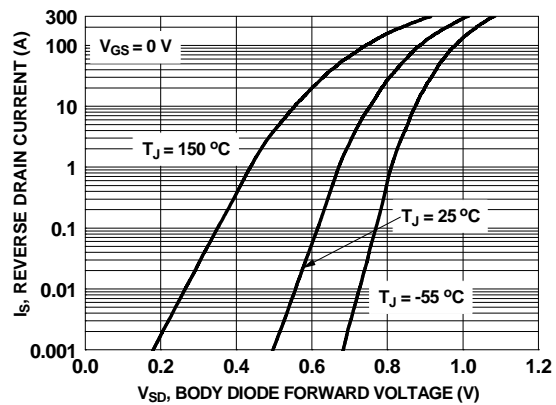
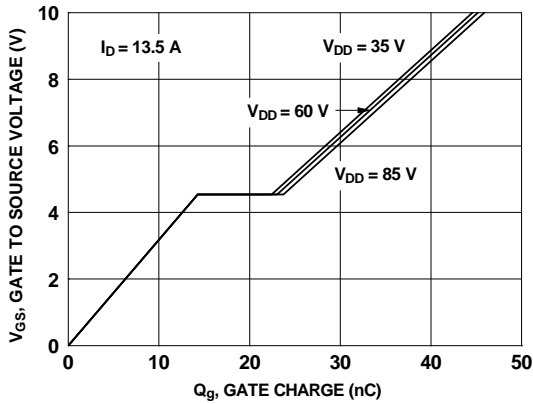
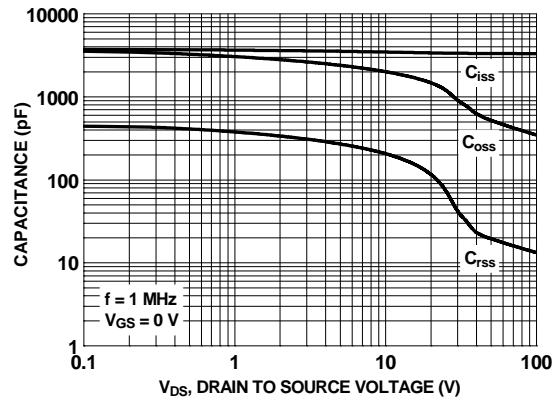


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

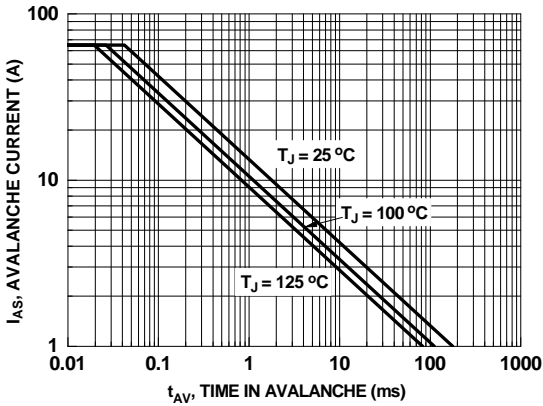
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



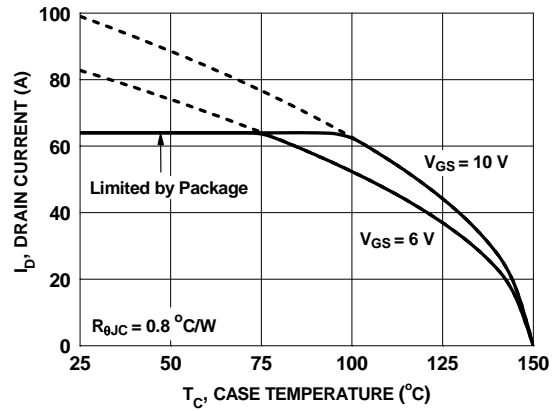
**Figure 7. Gate Charge Characteristics**



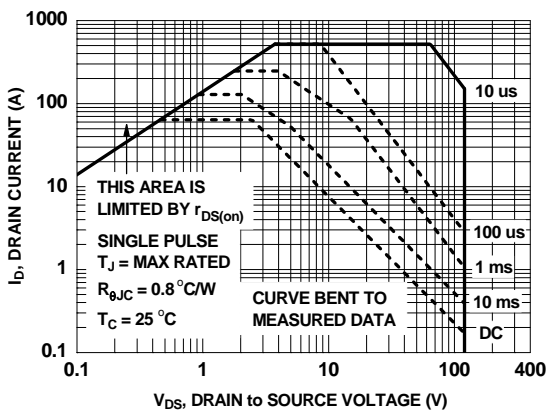
**Figure 8. Capacitance vs Drain to Source Voltage**



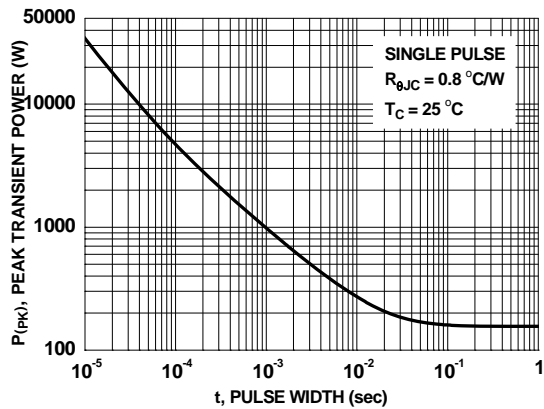
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

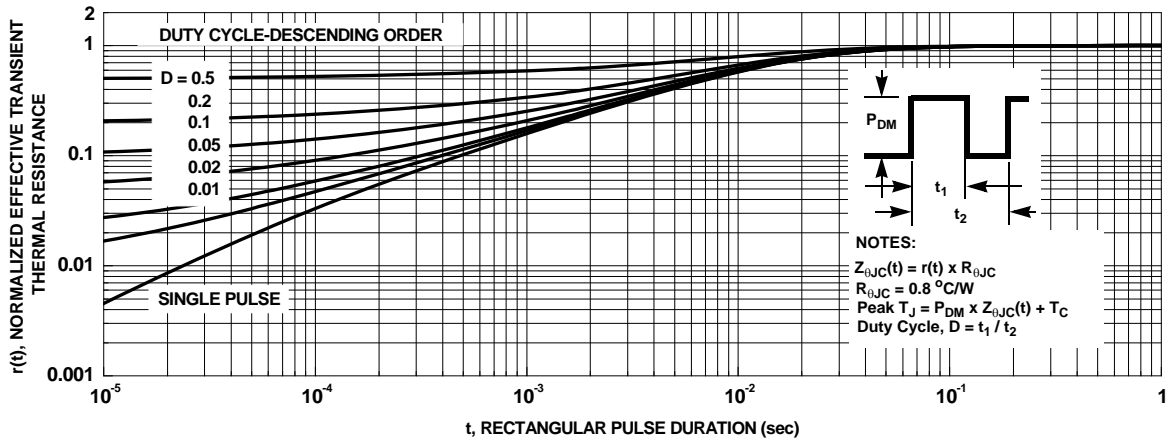


**Figure 11. Forward Bias Safe Operating Area**

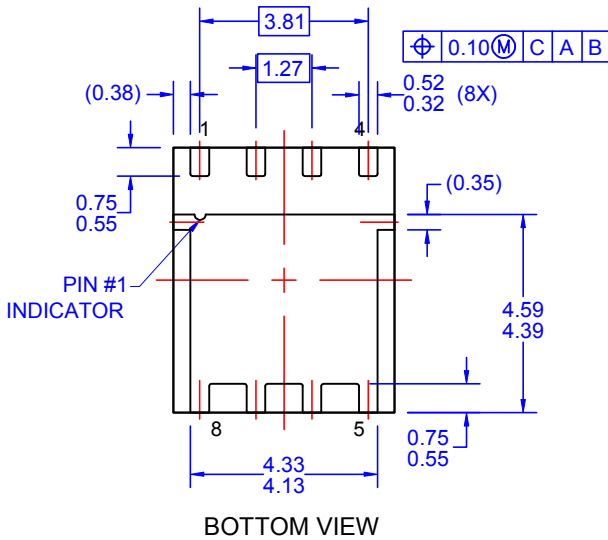
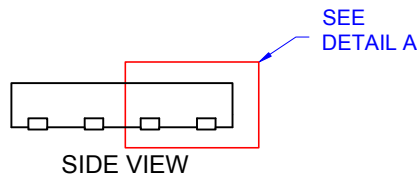
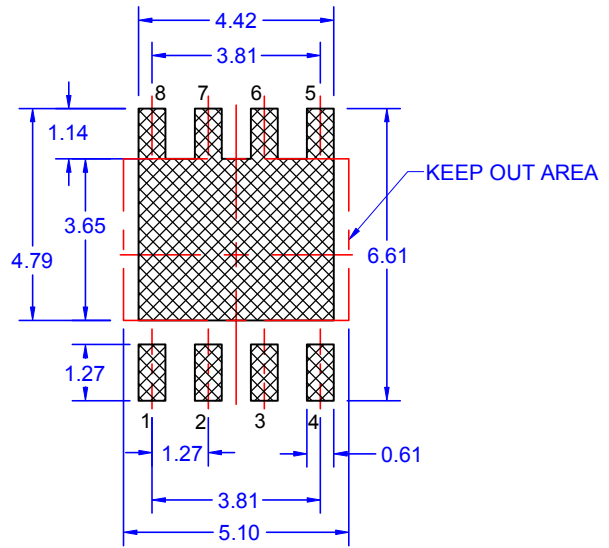
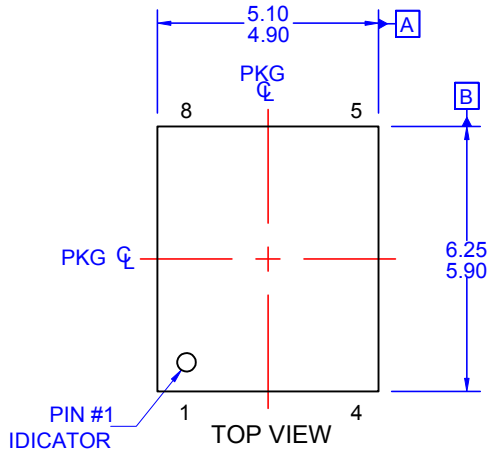


**Figure 12. Single Pulse Maximum Power Dissipation**

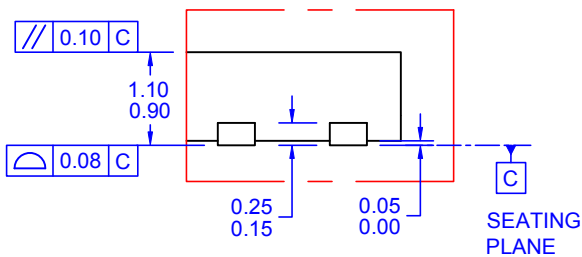
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**



- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
 D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.  
 E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.  
 F) DRAWING FILE NAME: PQFN08JREV2.  
 G) FAIRCHILD SEMICONDUCTOR








**DETAIL A**  
SCALE: 2:1



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| EcoSPARK®   | MicroFET™                                      | SMART START™  |  |
| EfficientMax™   | MicroPak™                                      | Solutions for Your Success™   | UHC®  |
| ESBC™   | MicroPak2™                                     | SPM®  | Ultra FRFET™  |
|  | MillerDrive™                                   | STEALTH™  | UniFET™   |
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| FACT®   | MTX®   | SuperSOT™-8   | XS™   |
| FAST®   | MVN®   | SupreMOS®   | Xsens™  |
| FastvCore™  | mWSaver®                                       | SyncFET™  | 仙童™   |
| FETBench™   | OptoHiT™                                       | Sync-Lock™  |   |
| FPS™  | OPTOLOGIC®                                     |   |   |

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