Application Note
December 3, 2004
PDF Name: input_filtering_an.pdf

Application Guidelines for Non-Isolated Converters
AN04-002 Input Filtering for Austin Lynx Series POL Modules

Introduction

The Austin Lynx™ and Lynx II family of non-isolated POL (point-of-load) modules use the buck converter topology shown in Fig. 1. The input current of such a converter is discontinuous, and therefore to smooth out the current drawn at the module input terminals, these converters have a small amount of input filter capacitance on board the module. In many applications, there are multiple POL converters powered from the same input bus and distributed across the customer's board. All these switching converters generate ripple and noise on the common DC input bus which should be suppressed so that operation of one converter does not adversely affect others. In addition to the input ripple created by the POL converters, in many applications the POL module is powered from another switch–mode converter which has its own output voltage ripple and noise. Additional input filter capacitance external to the module is recommended to further reduce the input ripple current seen by the source powering the modules. This application note details some of the important considerations when designing input filters to reduce input voltage ripple when using POL converters. Note that all input filtering considerations apply to the Austin Lynx and Lynx II families of modules.

Filtering the DC Input Bus

The first consideration in powering POL modules is the source impedance of the upstream converter. For stable operation of the POL module, the source impedance should be less than the input impedance of the module over a frequency range from a few Hz to about 1/5th of the switching frequency (which is around 300kHz for the Austin Lynx series of modules). In typical applications where both the upstream powering DC-DC converter and the Austin Lynx modules are co-located on the same printed circuit board, the input stability condition is usually satisfied (i.e., source impedance is much less than input impedance of the POLs) by virtue of the on-module capacitors at the output of the powering DC-DC converter and input capacitors on the Austin Lynx modules. However, if an inductor is used at the input to the Austin Lynx series module, or a long lead path is present at the input to the module contributing to increased input inductance, the higher effective source impedance as seen by the POL converter may violate the input stability condition. In this case, a small capacitor, e.g. 33 uF, should be placed on the input bus of the Austin Lynx to reduce the source impedance.

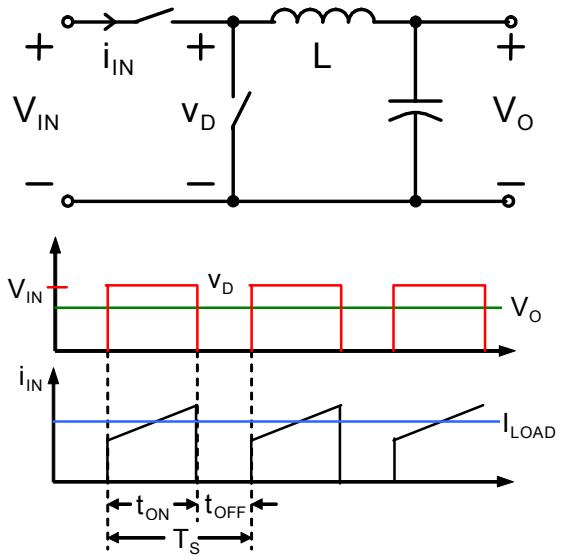

Fig. 1 Simplified circuit diagram and waveforms of a buck converter.

The input voltage feeding the POL module has a small AC component which is superimposed on a large DC voltage. The AC components are in two distinct different frequency ranges, each caused by a different mechanism. The first is AC voltage excursions on the input bus due to load transient changes at the output of POL modules. This is usually a low frequency phenomenon with settling times of the order of several hundred microseconds with equivalent frequencies in the few tens of kHz. The second source of input AC ripple and noise is the switching action of the POL buck converter as well as the input source converter. This is generally a high frequency AC ripple at the switching frequency of the POL converter and/or upstream converter to several harmonics.

The second type of AC component is created due to the switching action of the POL when it draws power from the input source in discontinuous current pulses. The frequency of this AC component is equal to the switching frequency of the POL and it has several harmonics, expanding well into the MHz frequency region. The slew rate of the current pulses is also very large, of the order of several thousand A/μs. All Tyco non-isolated POL converters have ceramic filter capacitors placed on the module which reduces the ripple and noise significantly. However, this ripple and noise can be reduced further by placing extra capacitors on the input bus of the POL converter.

Another source for high frequency noise on the DC bus is the upstream source converter. AC ripple and noise stemming from the source converter is usually much smaller than the ripple caused by the POL module. This is due to the fact that typical upstream converters have an LC filter at their output which reduces the ripple and noise significantly. Therefore, most of the ripple and noise

created on the input bus is mainly due to the POL converters.

Choosing Decoupling Capacitors for Reducing Switching Ripple

In general, the AC components on the input bus are suppressed using reactive filter components, such as capacitors and inductors. The input filter capacitors carry the AC component of the current. Most of the ripple current flows through the input ceramic capacitors already placed inside the module. However, a portion of the AC ripple current is also drawn from the input bus where most of it is supplied by the external input capacitors. It is therefore crucial not to exceed the RMS current rating of the external capacitor chosen. Aluminum electrolytic and tantalum capacitors have high ESR values and thus are generally not suitable for decoupling the switching noise and ripple of the POL module. However, they can be used in combination with ceramic capacitors for other purposes such as suppressing the lower frequency ripple caused by load transients.

Low ESL and ESR ceramic capacitors are recommended for input decoupling of the high-frequency ripple and noise since they provide the maximum attenuation in a small package size. To reduce high-frequency voltage spikes at the input of the module, 0.1 µF and 1.0 µF small-package ceramic capacitors should be placed at the input of the module. The smallest (both in value and physical size) capacitors are placed closest to the module input pins. Layout is also important in dealing with high frequency switching ripple and noise.

A generic method for placing both and input capacitors (ceramic, tantalum, polymer, aluminum electrolytic, etc.) is shown in Fig. 2. Ceramic capacitors should be placed as close as possible to the input pins of the POL module, followed by low ESR polymer capacitors and aluminum electrolytics if needed. Since the AC RMS current will be shared by the input capacitors, it is recommended that

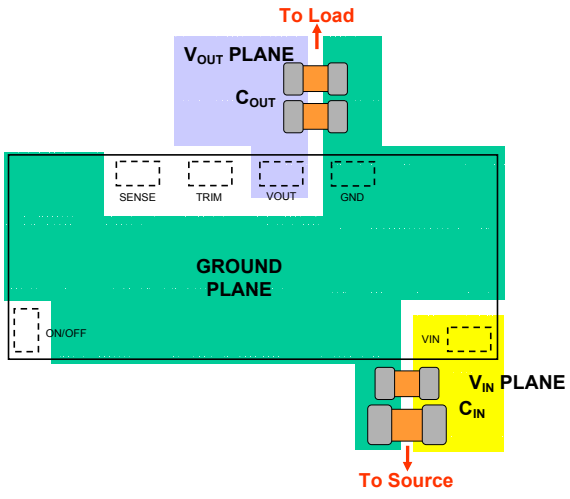

Fig. 2. Example Layout of an Austin Lynx SMT module showing location of the input capacitors.

ceramic capacitors be selected such that their impedance is substantially lower than the impedance of the tantalum and/or aluminum electrolytic capacitors at the switching frequency. This will ensure that most of the AC RMS ripple current will flow through the ceramic capacitors and not through the high ESR tantalum and/or aluminum electrolytic capacitors.

The input bus voltage ripple should be reduced sufficiently to ensure proper operation of the loads and the overall power system. A reasonable target (unless special loads are also present on the input voltage bus) is a peak-to-peak voltage ripple of 3% of the bus voltage. The designer should also take into account the static output voltage regulation of the 12V bus converter. For example, the Tyco QBK025A0B1 12V bus converter regulates its output to within ±5% which corresponds to

$$12\text{V} \times 5\% = 0.6\text{V}$$

Assuming a maximum peak-to-peak input ripple voltage of 3% voltage, and that the bus converter is to feed the Lynx II series of input modules which have a minimum input voltage of 8.3V, then the decoupling circuit should be designed in such a way that the maximum bus voltage deviation due to a load transient is limited to

$$12\text{V} - 0.6\text{V} - 0.36\text{V} - 8.3\text{V} = 2.74\text{V}$$

to guarantee proper operation of the POL converters.

For the 5V and 3.3V input bus voltage cases, the allowable ripple on the input bus is usually dictated by IC loads powered from the same input bus. Although requirements vary, maximum bus voltage p-p ripple limits of 100mV on 5V systems, and 50mV on 3.3V systems are common.

Decoupling the 12V Bus with Capacitors

For programmable DC-DC converters such as the Austin Lynx family of modules, input ripple voltage varies with:

1. Output voltage of the POL converter when the load current is kept constant; and
2. Load current at the output of the POL converter for a given voltage

Figure 3 shows the variation of input ripple voltage at full load with varying output voltages for the 12V Austin Lynx family of modules, when no external input filtering is used.

A simple and effective method for reducing the input voltage ripple is to place a couple of low ESR ceramic capacitors at the module input terminals. In Figure 4, the peak-to-peak input voltage ripple is shown for the same modules as in Fig. 3, when two 22µF, 16V, X5R ceramic capacitors (TDK part #: C4532X5R1C226M) are placed at the input terminals. The load for each module is set at its full rated value.

The input ripple voltage varies in direct proportion to the load current. An example of this behaviour is shown in

Figure 5 for the 12V Austin SuperLynx module (AXA016A0X3) with two 22 µF ceramic capacitors. This linear relationship allows estimating the ripple voltage at load current levels below the full load value and is equally applicable to all members of the Austin Lynx and Lynx II series of products.

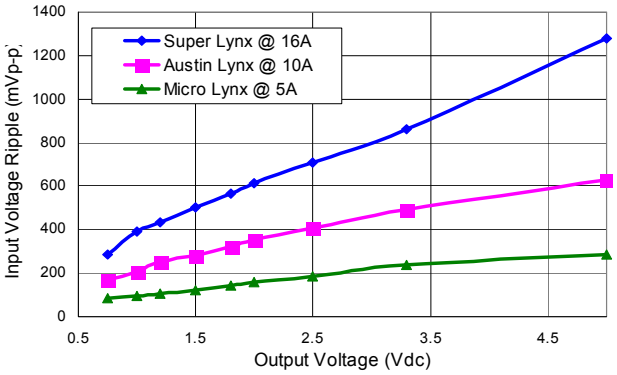

Fig. 3. Input ripple voltage of the 12V Austin Lynx family modules vs. output voltage at full rated load and no external input filtering.

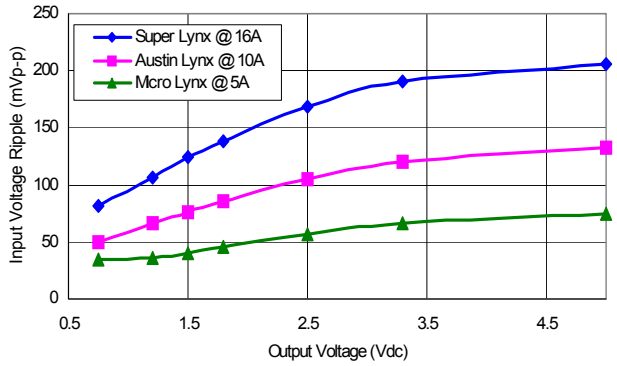

Fig. 4. Input ripple voltage vs. output voltage Vo at full rated load for the Austin SuperLynx, Lynx and MicroLynx modules, with two 22µF ceramic capacitors placed at the input of the module. The curves also apply to the Austin Lynx II series of modules.

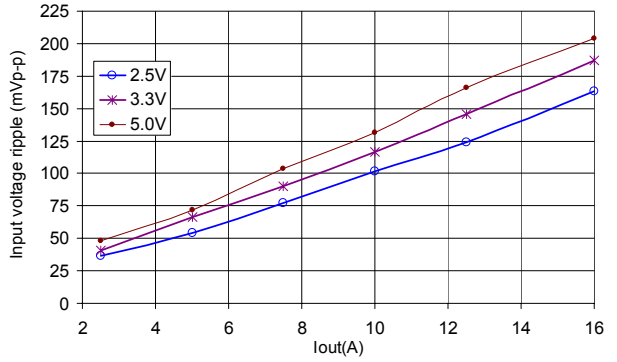

Fig. 5. Input ripple voltage of the 12V Austin Lynx/SuperLynx, Lynx II and SuperLynx II modules vs. output current.

Decoupling 5V and 3.3V Buses with Capacitors

As discussed earlier, the ripple voltage on the 5V and 3.3V buses should be reduced to levels of 100mV p-p (for 5V buses) and 50mV p-p (for 3.3V buses) in order to not affect other sensitive loads on the input bus. Figure 6 shows the amount of ceramic capacitance required to limit the input voltage ripple below 100mV p-p for a 5V input bus. As an example, the amount of capacitance required to limit the peak-to-peak input voltage ripple to less than 100 mV for an Austin SuperLynx module (AXH016A0X3) at full load of 16A, with an output voltage of 2.5V and 5V input voltage is given by Fig. 6 to be 142 µF. This can be realized by the parallel combination of 100 µF, 22 µF and 2x10 µF ceramic capacitors. Similarly, Figure 7 shows the minimum capacitance required for limiting input voltage ripple below 50mV p-p for a 3.3V input bus.

The decoupling approach described so far relies on the use of low ESR ceramic capacitors. The main benefits of capacitive decoupling are summarized below:

- It is very effective in reducing the input bus ripple with only a few extra components
- It is flexible in the sense that during initial design stage a number of component pads may be allocated for capacitors, however, if later they are found to be not necessary, the designer may choose not to populate these pads.
- Capacitive filtering on the input bus may improve the transient response of the POL converter.
- It helps reduce the likelihood of running into input

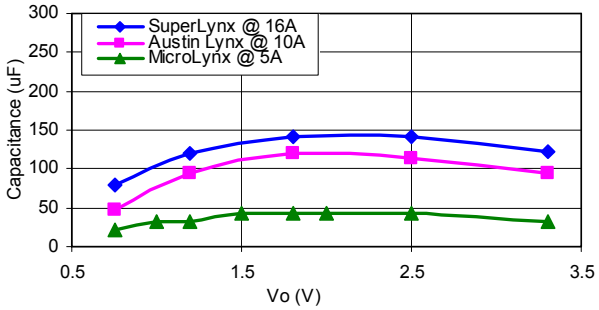

Fig. 6. Input capacitance needed to limit input ripple voltage to 100mV p-p vs. Vout with a 5V input bus.

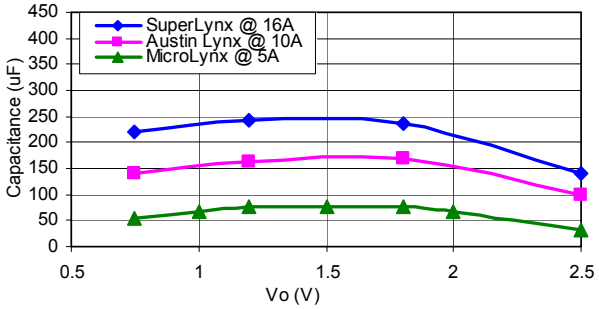

Fig. 7. Input capacitance needed to limit input ripple voltage to below 50mV p-p vs. Vout with a 3.3V input bus.

filter instability without any other drawbacks.

Decoupling The Input Bus for Extra-Low Ripple and Noise

In some applications, it may be necessary to reduce the input ripple of the POL converter to unusually low values. In such cases, the best cost and space saving approach for decoupling is to use a π–filter with the combination of a small inductor and capacitors as shown in Figure 8. The inductor in the filter circuit increases the source impedance of the input bus. This in turn may cause input filter instability if the source impedance of the bus is not substantially lower than the input impedance of the POL converter. The value of the inductor should be chosen in such a way that it does not cause input filter instability. It is recommended that the inductance be kept less than 0.5 μH.

Circuit simulation can be used to predict the input ripple voltage and RMS currents flowing through individual capacitor branches. As discussed earlier in this Application Note under the "Choosing Decoupling Capacitors" section, it is very important not to exceed the RMS current rating of the capacitors. If excessive RMS current flows through the capacitors, it may cause catastrophic component failures.

Figure 9 shows the model of the POL converter with a π–filter consisting of capacitors C1, C2, Lp, C3 and C4. In

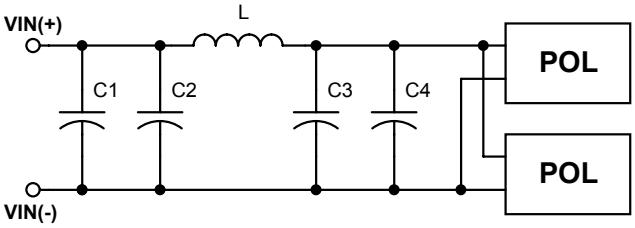

Fig. 8. Circuit diagram showing the π-filter arrangement for input-bus decoupling.

this particular example, an AXA010A0X3 module is shown. There are three 10 μF, 16V ceramic capacitors located inside the module, across the input pins. Under 12V input voltage bias, the capacitance of the ceramic capacitors declines as much as 20% from its nominal value. Therefore, in the PSpice model their value is adjusted downwards to 8 μF. The effective series inductance (ESL) of the capacitor depends on the case size and for the 1210 capacitors used in AXA010A0X3, the ESL is 0.95 nH.

The ESR of ceramic capacitors has a strong frequency dependence and usually decreases 20 dB/decade up to the self resonant frequency (SRF) of the capacitor and attains the minimum value at the SRF. For simulating the input voltage ripple, the ESR at the switching frequency of POL converter should be used in the PSpice model. The ESR of the capacitor is critical in the accuracy of the simulation. Contact and trace resistance should also be included in the model.

The current pulses drawn from the input bus by the buck converter are modelled using the current sources I1 and I2 which when combined create the trapezoidal current waveform shown in Figure 1. The shape of the current pulses depend on the input voltage, programmed output voltage, output inductor of the buck converter, output load current and the switching frequency.

The following example shows the power of PSpice simulation in designing input decoupling circuits.

Input Filter Simulation Example

In Figure 4, the input ripple voltage for the 12V, 10A Austin Lynx SIP module is plotted as a function of the programmed output voltage at full load current of 10A when two 22 μF ceramic capacitors are placed across the input terminals. From Fig. 4, the ripple voltage is 116.7mV p-p. The oscilloscope picture showing the measured ripple voltage waveform is shown in Fig. 10.

PSpice simulation of the module under the same

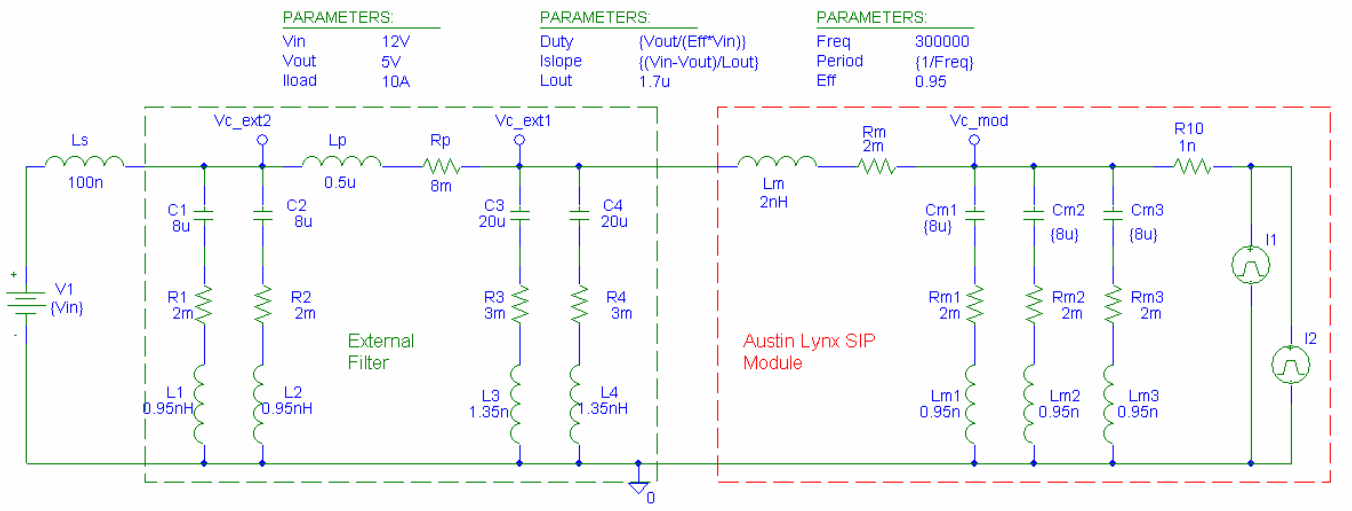

Fig. 9. PSpice simulation model of a example POL converter and input filter circuit.

operating conditions with the same decoupling circuit predicts input ripple voltage of 119.6mV, p-p as seenin the simulated input ripple waveform shown in Figure 11. Similarly, for a 1.2V output under the same conditions, the ripple is measured to be 58mV as shown in Figure 12. The simulated waveform obtained using PSpice is shown in Fig. 13, and indicates a ripple voltage of 62.3mV, p-p. These comparisons of measured and simulated waveforms show the accuracy of simulating input filter circuits using a circuit simulation program.

One of the main advantages of simulation is that it provides an accurate estimate of the RMS current flowing in each capacitor, a variable which is difficult to measure experimentally. The designer can thus check whether the maximum RMS current ratings of the capacitor are violated in the design.

In the example just discussed for the 12V Austin Lynx module with an output of 1.2V@10A and 2x22 µF input capacitors, the RMS current through each 22 µF capacitor is 1.425A. In the data sheet, the capacitor manufacturer specifies the maximum RMS current through that capacitor as 3.26A (RMS) which is well above the calculated value. Therefore, there should be no problem with the ripple current flowing through the capacitors.

Summary and Conclusions

Filtering the input bus of POL converters requires careful attention to component selection and PCB layout, both of which have been discussed in detail here. Low ESR, surface mount multi-layer ceramic capacitors are the best choice for filtering high-frequency ripple voltage. Several fgraphs to aid the circuit designer in selecting input filter capacitors to use with POLs have been provided. If other capacitor technologies such as tantalum or aluminum electrolytics are utilized for load transient suppression on the input bus, they should always be used in parallel with ceramic capacitors. An excessive amount of input RMS current may cause failure of tantalum capacitors if they are used alone due to their high ESR. Finally, circuit simulation is shown to be an effective tool in predicting ripple voltage and the RMS currents through the filter capacitors. Using simulation models, very effective filtering can be designed in a straightforward manner to meet most sets of requirements.

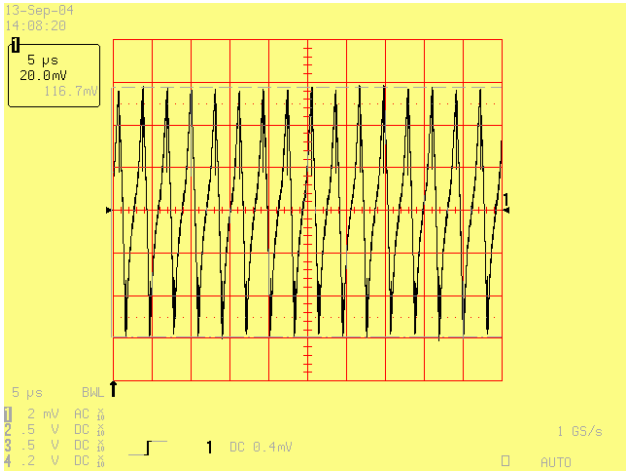

Fig. 10. Measured input ripple voltage waveforms for the AXA010A0X3 module at an output voltage of 3.3V @ 10A, with two 22µF input capacitors.

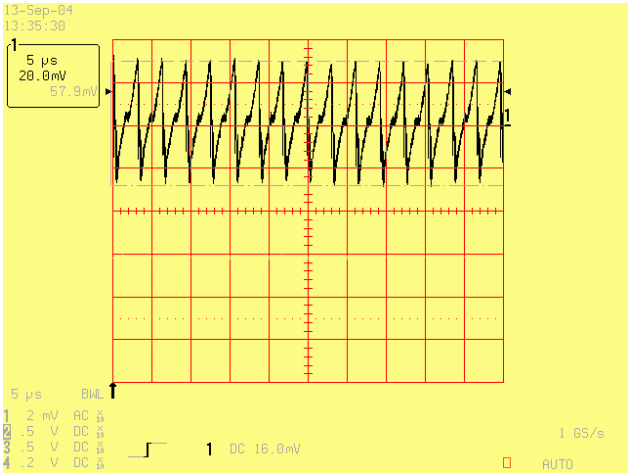

Fig. 12. Measured waveform of input ripple voltage for the AXA010A0X3 module at an output voltage of 1.2V @ 10A, with two 22µF input capacitors.

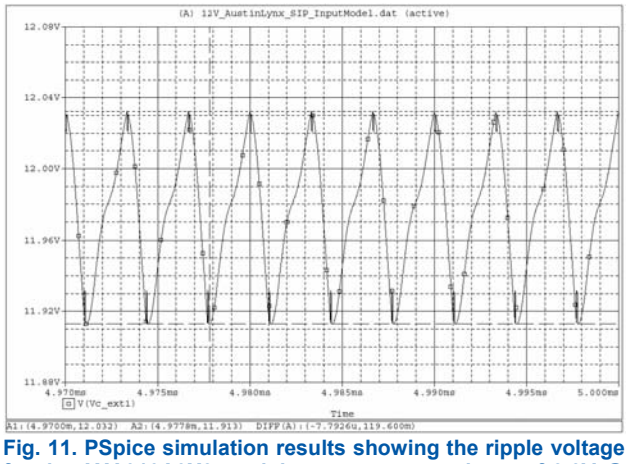

Fig. 11. PSpice simulation results showing the ripple voltage for the AXA010A0X3 module at an output voltage of 3.3V @ 10A, with two 22µF input capacitors.

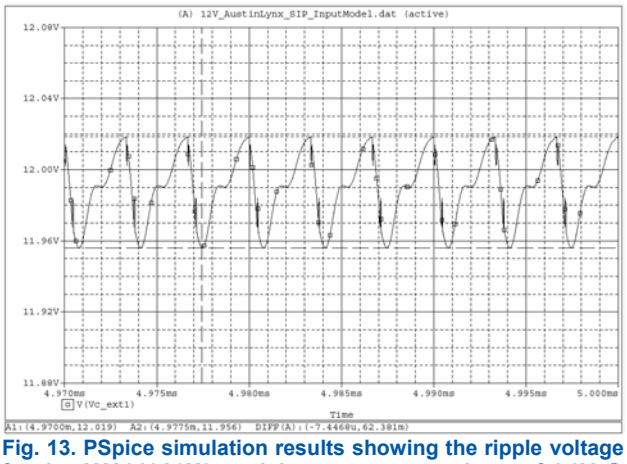

Fig. 13. PSpice simulation results showing the ripple voltage for the AXA010A0X3 module at an output voltage of 1.2V @ 10A, with two 22µF input capacitors.

Tyco Electronics, Power Systems

Tyco Electronics is a worldwide company employing over 77,000 employees in more than 51 countries.
For a complete up-to-date list of our sales offices please visit our website at www.power.tycoelectronics.com

World Wide Headquarters
Tyco Electronics Power Systems, Inc.
3000 Skyline Drive, Mesquite, TX 75149, USA
+1-800-526-7819
(Outside U.S.A.: **+1-972-284-2626**)
www.power.tycoelectronics.com
e-mail: techsupport1@tycoelectronics.com

Europe, Middle-East and Africa Headquarters
Tyco Electronics (UK) Ltd
Tel: +44 (0) 1344 469 300

Latin America, Brazil, Caribbean Headquarters
Tyco Electronics Power Systems
Tel: +56 2 209 8211

India Headquarters
Tyco Electronics Systems India Pte. Ltd.
Tel: +91 80 841 1633 x3001

Asia-Pacific Headquarters
Tyco Electronics Singapore Pte. Ltd.
Tel: +65 6416 4283

Document No: AN04-004 ver. 1.1
PDF Name: input_filtering_an.pdf