4-bit magnitude comparator 74F85

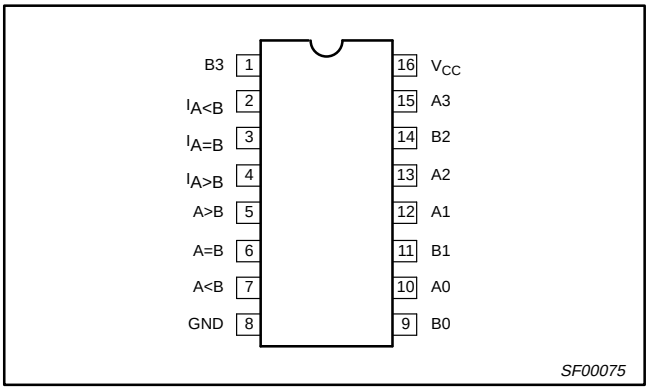
FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating

DESCRIPTION

The 74F84 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0–A3) and (B0–B3) where A3 and B3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme. The expansion inputs $I_{A>B}$, and $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the lease significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation, the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

ORDERING INFORMATION

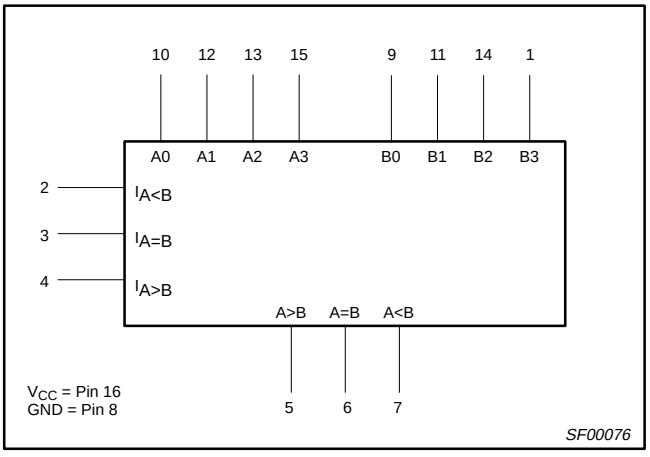
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16-pin plastic DIP	N74F85N
16-pin plastic SO	N74F85D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

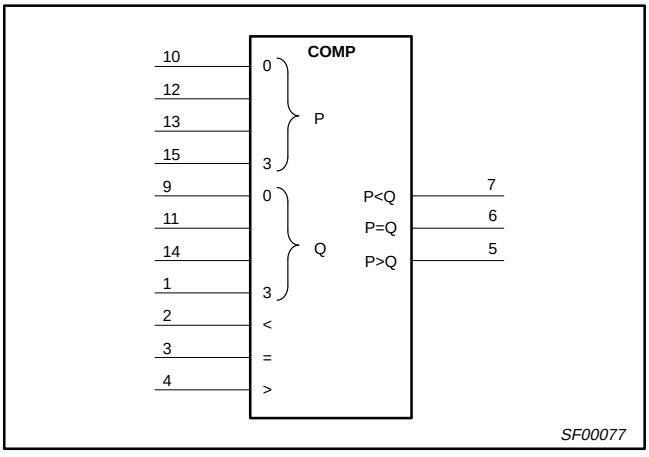
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A3	Comparing inputs	1.0/0.033	20μA/20μA
B0–B3	Comparing inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$, $I_{A>B}$	Expansion inputs (active High)	1.0/0.033	20μA/20μA
A<B, A=B, A>B	Data outputs (active High)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL

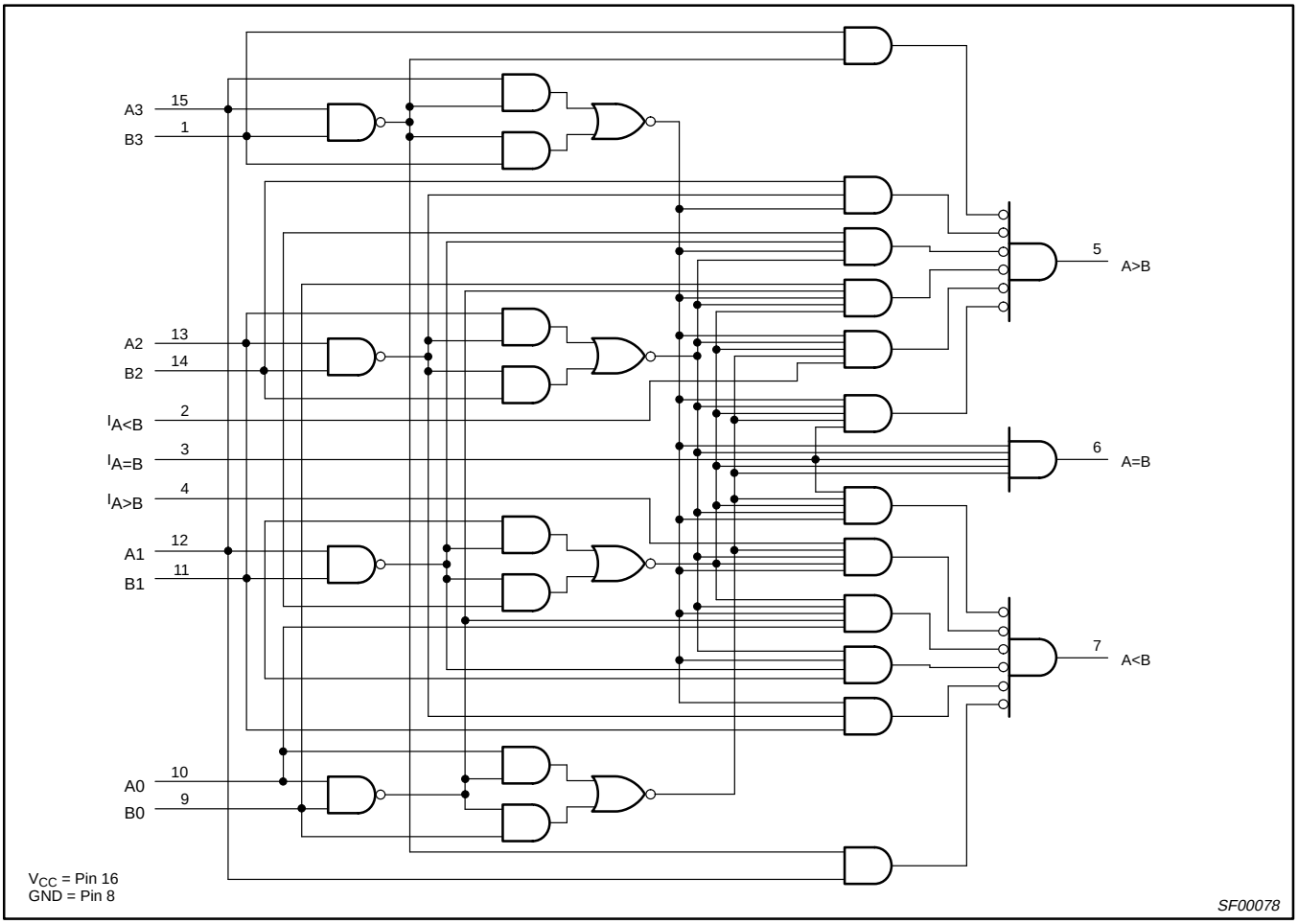


IEC/IEEE SYMBOL



4-bit magnitude comparator 74F85

LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	**A2,B2**	**A1,B1**	**A0,B0**	**$I_{A>B}$**	**$I_{A<B}$**	**$I_{A=B}$**	**A>B**	**A<B**	**A=B**
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION

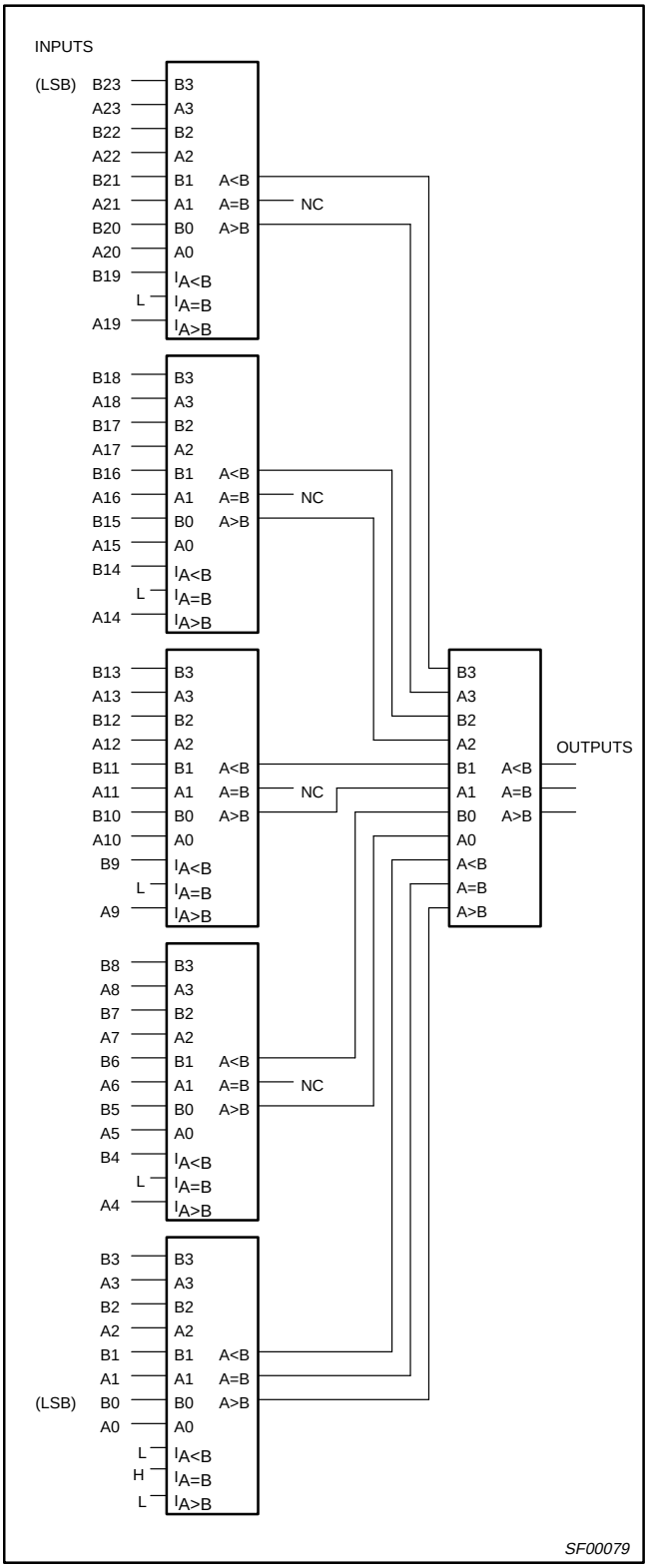


Figure 1. Comparison of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. The expansion inputs can be used as a fifth input bit position except on the least significant device, which must be connected as in the serial scheme. The expansion inputs used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ = Low. The 74F85 can be used as a 5-bit comparator only when the outputs are used to drive the (A0–A3) and (B0–B3) inputs of another 74F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1.

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 74F
1–4 bits	1	12ns
5–24 bits	2–6	22ns
25–120 bits	8–31	34ns

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} = GND		36	50	mA
	Supply current (total) I_{CCL}	V_{CC} = MAX	An = Bn = $I_{A=B}$ = GND, $I_{A>B}$= $I_{A<B}$ = 4.5V		40	54	mA

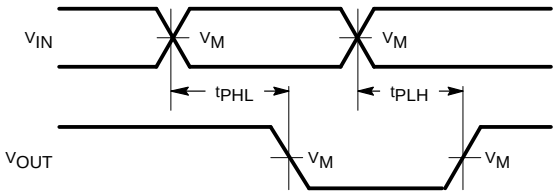
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A or B to A<B, A>B	Waveform 1 3 logic levels	6.0 7.0	8.5 9.5	11.0 14.0	5.5 6.5	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B to A=B	Waveform 1 4 logic levels	6.5 7.0	9.0 9.5	11.5 14.0	6.0 6.5	14.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ to A>B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	7.5 9.0	2.5 2.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ to A=B	Waveform 1 2 logic levels	2.5 3.5	4.5 7.5	7.0 10.0	2.0 2.5	9.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ to A<B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	8.0 9.0	3.0 2.0	9.5 9.5	ns

AC WAVEFORMS



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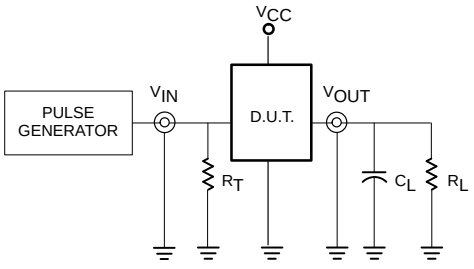
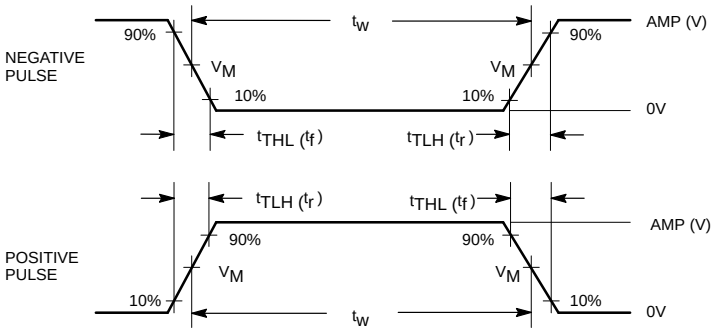
Waveform 1. Propagation Delay Input to Output

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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