Structure: Silicon Monolithic integrated circuit

Product name: I/O interface LSI for PAL-type DVD recorder

Type: BH7626KS2

Outer dimensions: Figure-1 SQFP-T52 (Plastic Mold)

Pin assignment: Figure-2

Block diagram: Figure-3

Absolute Maximum Ratings (Ta = 25℃)

Item	Symbol	Rating	Unit
Power supply voltage	VCC	7.0	V
Power dissipation	Pd	1300 ※1	mW
Operating temperature range	Topr	−25 ~ +65	℃
Storage temperature range	Tstg	−55 ~ +125	℃

※1 Deratings is done at 13mW/℃ above Ta=25℃.

Operation Range

Item	Symbol	Range	Unit
Power supply voltage	AVCC1,AVCC2, DVCC1,DVCC2	4.75~5.25	V

※ This product is not designed for protection against radioactive rays.
※ Use the same power supply for AVCC1, AVCC2, DVCC1, and DVCC2.
※ Operation faults may occur if this IC's input or output pins are connected to signal lines from another power supply unit (or to an external pin, etc.) when there is no power being supplied to this IC. Note this with caution and take measures to avoid this.
※ The I^2C bus complies with Version 2.0. (Fast mode is supported, HS mode is not supported.)

Discription

The BH7626KS2 is a 75 Ω driver compound LSI with video signal input switcher for PAL-type DVD recorders that use I^2C bus control. The I^2C bus can also be used to control the BD3826FS, an audio signal switcher LSI that can be used in combination with this LSI. (In such cases, use the same power supply as the VCC.)
The BH7626KS2 includes control functions (function switch and fast blanking) for PAL-type skirted pins, as well as one general-purpose parallel output port.

Features

- O Vcc 5V Single
- O I^2C bus control (input has high impedance when power is OFF)
- O BD3826FS control functions are built-in.
- O General-purpose parallel control pin (1 channel) is built-in.
- O Standby mode

[Playback]

O CVBS/Y
5-inputs, with five mutable B clamp circuits
1-output, 0/2.5 dB amplifier + buffer
2-outputs, 6/8 dB amplifier + 75 Ω driver
One Y/C MIX circuit

O C
2-inputs, two mutable BIAS circuits
2-outputs, 6/8 dB amplifier + 75 Ω driver (with common R)

[Recording]

O R, G, B
2-inputs, five B clamp circuits
One mutable clamp/BIAS circuit
3-outputs, 6/8 dB amplifier + 75 Ω driver
3-outputs, 0/3 dB amplifier + buffer

- O For mute circuits, switches can be set individually or all at once. (ALL MUTE)
- O Nine channels of 6 order LPF are built-in. (for playback and recording)
- O Fast blanking circuit is built-in.
- O Two function switch inputs are built-in.

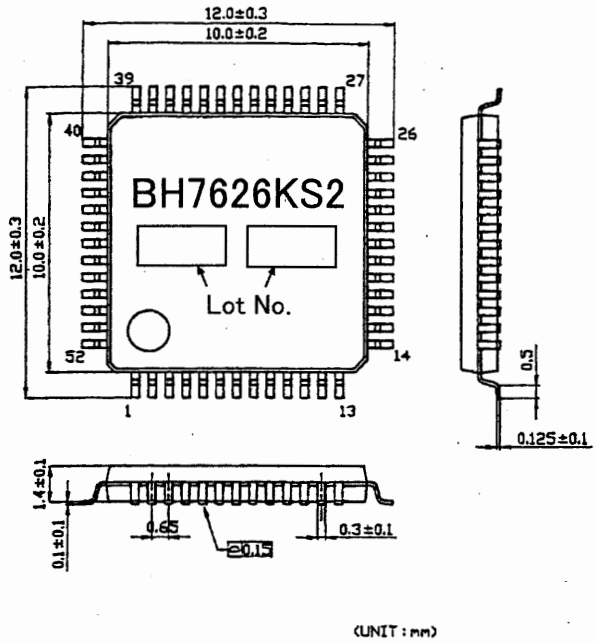


Figure-1 Outer dimensions
(SQFP-52)

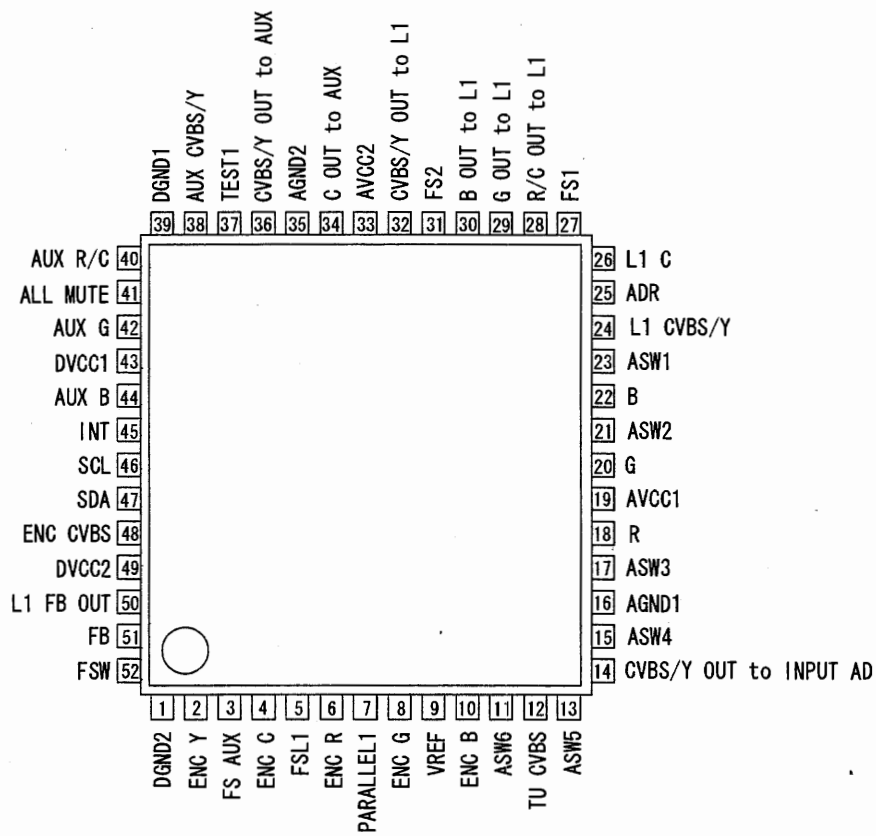
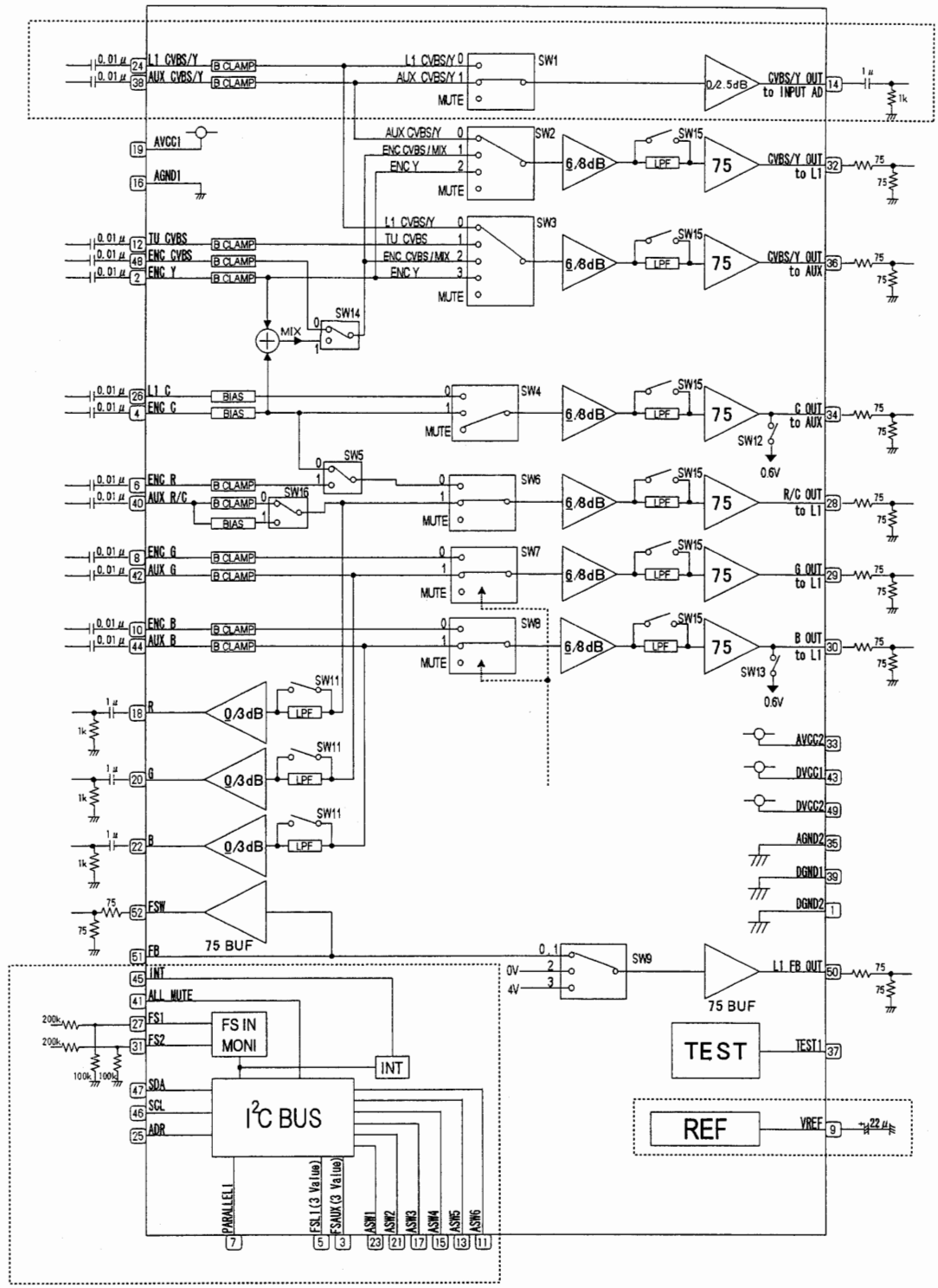


Figure-2 Pin assignment



(Note) Blocks that operate during standby mode are enclosed in broken lines.

Figure-3 Block diagram

Electrical characteristics (1/4) (Unless otherwise noted, Ta=25℃,Vcc=5.0V)

Item	Symbol	Limit MIN.	Limit TYP.	Limit MAX.	Unit	Conditions
< Device total >						
VCC Circuit current	I_{CC}	90	137	184	mA	VCC=5V, No Signal, Load=75Ω
VCC Circuit current at standby	I_{CCST}	9	15	21	mA	VCC=5V, No Signal, Load=75Ω
< SELECTOR part >						
CVBS/Y OUT to INPUT AD Voltage gain 0dB	G_0	−0.7	−0.2	0.3	dB	Vin : 1.0Vp-p, f=100kHz, 0dB
CVBS/Y OUT to INPUT AD Voltage gain 2.5dB	$G_{2.5}$	2.0	2.5	3.0	dB	Vin : 1.0Vp-p, f=100kHz, 2.5dB
R, G, B OUT Voltage gain 0dB	G_0	−0.7	−0.2	0.3	dB	Vin : 1.0Vp-p, f=100kHz, 0dB, LPF : off
R, G, B OUT Voltage gain 3dB	G_3	2.5	3.0	3.5	dB	Vin : 1.0Vp-p, f=100kHz, 3dB, LPF : off
R, G, B OUT Voltage gain 0dB LPF	G_{0LPF}	−0.8	−0.3	0.2	dB	Vin : 1.0Vp-p, f=100kHz, 0dB, LPF : on
R, G, B OUT Voltage gain 3dB LPF	G_{3LPF}	2.4	2.9	3.4	dB	Vin : 1.0Vp-p, f=100kHz, 3dB, LPF : on
CVBS/Y OUT to INPUT AD Maximum output level	V_{OM}	2.8	3.2	−	Vp-p	THD=1.0%, f=10kHz
R, G, B OUT Maximum output level	V_{OM}	2.8	3.2	−	Vp-p	THD=1.0%, f=10kHz
CVBS/Y OUT to INPUT AD Frequency characteristic	F	−1.0	0.0	1.0	dB	Vin : 1.0Vp-p, f=7MHz/100kHz
R, G, B OUT Frequency characteristic	F	−1.0	0.0	1.0	dB	Vin : 1.0Vp-p, f=7MHz/100kHz LPF : off
R, G, B OUT Frequency characteristic 1 LPF	F_1	−1.5	−0.5	0.5	dB	Vin : 1.0Vp-p, f=6.75MHz/100kHz LPF : on
R, G, B OUT Frequency characteristic 2 LPF	F_2	−	−38	−27	dB	Vin : 1.0Vp-p, f=27MHz/100kHz LPF : on
CVBS/Y OUT to INPUT AD MUTE attenuation	M_T	−	−60	−55	dB	Vin : 1.0Vp-p, f=4.43MHz
Switch difference voltage gain	G_D	−0.5	0.0	0.5	dB	Vin : 1.0Vp-p, f=100kHz
< 75Ω driver part >	CVBS/Y OUT to L1, CVBS/Y OUT to AUX, C OUT to AUX, R/C OUT to L1, G OUT to L1, B OUT to L1 common specification					
Voltage gain 6dB	G_6	5.7	6.2	6.7	dB	Vin : 1.0Vp-p, f=100kHz, 6dB LPF : off
Voltage gain 6dB LPF	G_{6LPF}	5.6	6.1	6.6	dB	Vin : 1.0Vp-p, f=100kHz, 6dB LPF : on
Voltage gain 8dB LPF	G_{8LPF}	7.6	8.1	8.6	dB	Vin : 1.0Vp-p, f=100kHz, 8dB LPF : on
Maximum output level	V_{OM}	2.8	3.2	−	Vp-p	THD=1.0%, f=10kHz
Frequency characteristic	F	−1.0	0.0	1.0	dB	Vin : 1.0Vp-p, f=7MHz/100kHz LPF : off
Frequency characteristic 1 LPF	F_1	−1.5	−0.5	0.5	dB	Vin : 1.0Vp-p, f=6.75MHz/100kHz LPF : on
Frequency characteristic 2 LPF	F_2	−	−38	−27	dB	Vin : 1.0Vp-p, f=27MHz/100kHz LPF : on
MUTE attenuation	M_T	−	−60	−55	dB	Vin : 1.0Vp-p, f=4.43MHz, 6dB R_L=(75+75)Ω, division point
Switch difference voltage gain	G_D	−0.5	0.0	0.5	dB	Vin : 1.0Vp-p, f=100kHz

Electrical characteristics (2/4) (Unless otherwise noted, Ta=25℃,Vcc=5.0V)

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
BIAS input impedance	Z_I	14	20	26	kΩ	
AUX R/C BIAS input impedance	Z_I	100	150	200	kΩ	
< I^2C-BUS Control >						
ADR input voltage H	V_{IH}	2.0	—	VCC	V	
ADR input voltage L	V_{IL}	0	—	1.0	V	
ADR input impedance	Z_I	65	100	135	kΩ	pull down resistance
< SCL, SDA >						
Input voltage H	V_{IH}	2.0	—	VCC	V	
Input voltage L	V_{IL}	0	—	1.0	V	
Input bias current	I_B	−10	0	10	uA	
ALL MUTE threshold	V_{TH}	1.0	1.5	2.0	V	Input voltage range 0V ～ VCC
PARALLEL1 output voltage H	V_{OH}	VCC −0.5	VCC −0.1	VCC	V	Pull up 100KΩ
PARALLEL1 output voltage L	V_{OL}	0	0.3	0.5	V	I_{load} = 1mA
ASW output voltage H	V_{OH}	3.5	VCC −0.1	VCC	V	No load
ASW output voltage L	V_{OL}	0	0.1	1.0	V	No load
FSL1,FSAUX output voltage H	V_{OH}	4.0	0.95 ×VCC	VCC	V	R_L=200kΩ
FSL1,FSAUX output voltage M	V_{OM}	2.0	2.5	3.0	V	R_L=200kΩ
FSL1,FSAUX output voltage L	V_{OL}	0	0.1	0.75	V	R_L=200kΩ
< Scart connector part >						
FB threshold	V_{TH}	0.4	0.7	0.9	V	
L1 FB OUT output voltage H	V_{OH}	3.8	4.2	4.6	V	R_L= 150Ω
L1 FB OUT output voltage L	V_{OL}	0	—	0.7	V	R_L= 150Ω
FSW output voltage H	V_{OH}	3.8	4.2	4.6	V	R_L= 150Ω
FSW output voltage L	V_{OL}	0	—	0.7	V	R_L= 150Ω

Electrical characteristics (3/4) (Unless otherwise noted, Ta=25°C,Vcc=5.0V)

Item	Symbol	Limit MIN.	Limit TYP.	Limit MAX.	Unit	Conditions
FS1, FS2 threshold H	V_{TH}	2.5	2.75	3	V	Maximum input voltage:VCC
FS1, FS2 threshold L	V_{TH}	0.83	1.08	1.33	V	Minimum input voltage:0V
INT output voltage H	V_{OH}	VCC −0.5	VCC −0.1	VCC	V	Pull up 100KΩ
INT output voltage L	V_{OL}	0	0.3	0.5	V	I_{load} = 1mA
< SELECTOR part >						
Crosstalk within the switch	C_{TSW}	—	−60	−55	dB	Vin : 1.0Vp-p, f=4.43MHz, 0dB
Crosstalk between channels ※ Limit A	C_{TCHA}	—	−60	−55	dB	Vin : 1.0Vp-p, f=4.43MHz, 0dB
Crosstalk between channels ※ Limit B	C_{TCHB}	—	−57	−50	dB	Vin : 1.0Vp-p, f=4.43MHz, 0dB
< 75Ω driver part >						
Crosstalk within the switch	C_{TSW}	—	−60	−55	dB	Vin : 1.0Vp-p, f=4.43MHz, 6dB R_L =(75 +75)Ω, division point
Crosstalk between channels ※ Limit A	C_{TCHA}	—	−60	−55	dB	Vin : 1.0Vp-p, f=4.43MHz, 6dB R_L =(75 +75)Ω, division point
Crosstalk between channels ※ Limit B	C_{TCHB}	—	−57	−50	dB	Vin : 1.0Vp-p, f=4.43MHz, 6dB R_L =(75 +75)Ω, division point

※ See the following limit table concerning crosstalk within the switch or between channels.

Limit table for crosstalk between channels

													MONITOR PIN No. 14 CVBS/Y_INPUT_AD	18 R	20 G	22 B	28 L1_R/C	29 L1_G	30 L1_B	32 CVBS/Y_L1	34 C_AUX	36 CVBS/Y_AUX
No.	PIN No.	Output	PIN No.	Input	note	ADR	D1	D2	D3	D4	D5	D6										
1	14	CVBS/Y_INPUT_AD	24	L1_CVBS/Y		90	9F	FF	00	00	00	00		A	A	A	A	A	A	A	A	A
2			38	AUX_CVBS/Y		90	BF	FF	00	00	00	00		A	A	A	A	A	A	A	A	A
3	18	R	40	AUX_R/C		90	FF	FF	00	00	00	00	A		A	A	A	A	A	A	A	A
4	20	G	42	AUX_G		90	FF	FF	00	00	00	00	A	A		A	A	A	A	A	A	A
5	22	B	44	AUX_B		90	FF	FF	00	00	00	00	A	A	A		A	A	A	A	A	A
6	28	L1_R/C	4	ENC_C		90	FF	CF	00	00	00	00	A	A	A	A		B	A	A	A	A
7			6	ENC_R		90	FF	CF	80	00	00	00	A	A	A	A		B	A	A	A	A
8	28, 18	L1_R/C, R	40	AUX_R/C	CLAMP	90	FF	DF	00	00	00	00	A		A	A		B	A	A	A	A
9			40	AUX_R/C	BIAS	90	FF	DF	02	00	00	00	A		A	A		B	A	A	A	A
10	29	L1_G	8	ENC_G		90	FF	F3	00	00	00	00	A	A	A	A	B		A	A	A	A
11	29, 20	L1G, G	42	AUX_G		90	FF	F7	00	00	00	00	A	A		B	B		A	A	A	A
12	30	L1_B	10	ENC_B		90	FF	F3	00	00	00	00	A	A	A	A	A	A		A	A	A
13	30, 22	L1B, B	44	AUX_B		90	FF	F7	00	00	00	00	A	A	B		A	A		A	A	A
14	32	CVBS/Y_L1	38	AUX_CVBS/Y		90	E7	FF	00	00	00	00	A	A	A	A	A	A	A		A	A
15			48	ENC_CVBS		90	EF	FF	00	00	00	00	A	A	A	A	A	A	A		A	A
16			2	ENC_Y		90	F7	FF	00	00	00	00	A	A	A	A	A	A	A		A	A
17			2	ENC_Y	MIX	90	EF	FF	00	08	00	00	A	A	A	A	A	A	A		A	A
18			4	ENC_C	MIX	90	EF	FF	00	08	00	00	A	A	A	A	A	A	A		A	A
19	34	C_AUX	26	L1_C		90	FF	3F	00	00	00	00	A	A	A	A	A	A	A	A		A
20			4	ENC_C		90	FF	7F	00	00	00	00	A	A	A	A	A	A	A	A		A
21	36	CVBS/Y_AUX	24	L1_CVBS/Y		90	F8	FF	00	00	00	00	A	A	A	A	A	A	A	A	A	
22			12	TU_CVBS		90	F9	FF	00	00	00	00	A	A	A	A	A	A	A	A	A	
23			48	ENC_CVBS		90	FA	FF	00	00	00	00	A	A	A	A	A	A	A	A	A	
24			2	ENC_Y		90	FB	FF	00	00	00	00	A	A	A	A	A	A	A	A	A	
25			2	ENC_Y	MIX	90	FA	FF	00	08	00	00	A	A	A	A	A	A	A	A	A	
26			4	ENC_C	MIX	90	FA	FF	00	08	00	00	A	A	A	A	A	A	A	A	A	

Electrical characteristics (4/4) <Guaranteed design parameters> (Unless otherwise noted, Ta=25℃,Vcc=5.0V)

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
< SELECTOR part >						
CVBS/Y OUT to INPUT AD DG 0dB	D_{G0}	—	0.5	—	%	10step signal, Vout : 1.0Vp-p
CVBS/Y OUT to INPUT AD DG 2.5dB	$D_{G2.5}$	—	0.5	—	%	10step signal, Vout : 1.0Vp-p
R, G, B OUT DG 0dB	D_{G0}	—	0.5	—	%	10step signal, Vout : 1.0Vp-p
R, G, B OUT DG 3dB	D_{G3}	—	0.5	—	%	10step signal, Vout : 1.0Vp-p
R, G, B OUT DG 0dB LPF	D_{G0LPF}	—	0.5	—	%	10step signal, Vout : 1.0Vp-p
R, G, B OUT DG 3dB LPF	D_{G3LPF}	—	0.5	—	%	10step signal, Vout : 1.0Vp-p
CVBS/Y OUT to INPUT AD DP 0dB	D_{P0}	—	0.2	—	deg	10step signal, Vout : 1.0Vp-p
CVBS/Y OUT to INPUT AD DP 2.5dB	$D_{P2.5}$	—	0.2	—	deg	10step signal, Vout : 1.0Vp-p
R, G, B OUT DP 0dB	D_{P0}	—	0.2	—	deg	10step signal, Vout : 1.0Vp-p
R, G, B OUT DP 3dB	D_{P3}	—	0.2	—	deg	10step signal, Vout : 1.0Vp-p
R, G, B OUT DP 0dB LPF	D_{P0LPF}	—	0.2	—	deg	10step signal, Vout : 1.0Vp-p
R, G, B OUT DP 3dB LPF	D_{P3LPF}	—	0.2	—	deg	10step signal, Vout : 1.0Vp-p
CVBS/Y OUT to INPUT AD S/N 0dB	S_{N0}	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p
CVBS/Y OUT to INPUT AD S/N 2.5dB	$S_{N2.5}$	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p
R, G, B OUT S/N 0dB	S_{N0}	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p
R, G, B OUT S/N 3dB	S_{N3}	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p
R, G, B OUT S/N 0dB LPF	S_{N0LPF}	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p
R, G, B OUT S/N 3dB LPF	S_{N3LPF}	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p
< 75Ω driver part >	CVBS/Y OUT to L1, CVBS/Y OUT to AUX, C OUT to AUX, R/C OUT to L1, G OUT to L1, B OUT to L1 common specification					
DG 6dB	D_{G6}	—	1.0	—	%	10step signal, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
DG 6dB LPF	D_{G6LPF}	—	1.0	—	%	10step signal, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
DG 8dB LPF	D_{G8LPF}	—	1.0	—	%	10step signal, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
DP 6dB	D_{P6}	—	0.4	—	deg	10step signal, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
DP 6dB LPF	D_{P6LPF}	—	0.4	—	deg	10step signal, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
DP 8dB LPF	D_{P8LPF}	—	0.4	—	deg	10step signal, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
S/N 6dB	S_{N6}	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
S/N 6dB LPF	S_{N6LPF}	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
S/N 8dB LPF	S_{N8LPF}	—	−70	—	dB	50% Flat Field, Vout : 1.0Vp-p R_L=(75+75)Ω, division point
Output impedance	Z_0	—	1	—	Ω	R_L=150Ω
< Scart connector part >						
L1FBOUT output impedance	Z_0	—	4	—	Ω	R_L=150Ω

■ I²C−BUS Control input Specifications

○ I²C -BUS Format (WRITE MODE)

S	SLAVE ADDRESS	A	DATA1	A	DATA2	A	DATA3	A	DATA4	A	DATA5	A	DATA6	A	P

S : Start Condition
A : Acknowledge
P : Stop Condition

	b7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	0	0	1	0	0	ADR	R/W
DATA1	#	ADSW		L1SW		YAUXSW		
DATA2	CAUXSW		RSW		GBSW		#	#
DATA3	CRSW	FBSW		#	AMP6/8	RGB_FLT	CL/BI SEL	AD0/2_5
DATA4	INT_EN	OUTCTL1	OUTCTL2	Standby	MIXSW	DRV_FLT	ASW5	ASW6
DATA5	PARALLEL1	RGB0/3	#	#	ASW1	ASW2	ASW3	ASW4
DATA6	FSL		FSA		#	#	#	#

Don't Care

○ Switch I/O selection mode setting (* indicates status when power is on. [Initial condition])

ADR: Sets slave address via ADR pin (Write mode)
0: When ADR pin's input = L, address is "90H".
1: When ADR pin's input = H, address is "92H".

R/W: Selects Read or Write mode
0 : WRITE
1 : READ

ADSW: Selects SW1 input. Selects signal output for "CVBS/Y to INPUT AD".
00 : L1 CVBS/Y
01 : AUX CVBS/Y *
10 : MUTE
11 : MUTE

L1SW: Selects SW2 input. Selects signal output for "CVBS/Y to L1".
00 : AUX CVBS/Y *
01 : ENC CVBS or Y/C MIX
10 : ENC Y
11 : MUTE

YAUXSW: Selects SW3 input. Selects signal output for "CVBS/Y to AUX".
000 : L1 CVBS/Y *
001 : TU CVBS
010 : ENC CVBS or Y/C MIX
011 : ENC Y
1XX : MUTE

CAUXSW: Selects SW4 input. Selects signal output for "C OUT to AUX".
00 : L1 C
01 : ENC C
10 : MUTE (Output voltage=0.2V Typ.)
11 : MUTE * (Output voltage =2.1V Typ.)

(Note) CAUXSW; DATA2[7,6] = "10" or "11" (bias output voltage changes during mute mode)
When Mute is selected, use DATA2[7,6] = "11".

RSW: Selects SW6 input. Selects signal output for "R/C OUT to L1".
00 : ENC C or ENC R
01 : AUX R/C *
1X : MUTE

GBSW: Selects SW7 and SW8 inputs. Selects signal output for "G OUT to L1" and "B OUT to L1".
00 : ENC G, ENC B
01 : AUX G, AUX B *
1X : MUTE

CRSW: Selects SW5 input. Selects signal to be input to RSW.
0 : ENC C *
1 : ENC R

FBSW: Selects SW9 output. Selects output for "L1 FB OUT".
0X : FB (Through) *
10 : 0V
11 : 4V

AMP6/8: Sets 75 Ω driver's output AMP gain.
0 : 6dB *
1 : 8dB

(Note) This is valid only when ENC input has been selected. (See page 14.)

RGB_FLT: Selects SW11 input. Selects whether to output R, G, and B output signals via a filter.
0: Without filter *
1: With filter

CL/BI SEL: Selects SW16 input. Sets input type for "AUX R/C".
0 : B CLAMP *
1 : BIAS

AD0/2_5: Sets AMP gain for "CVBS/Y to INPUT AD" pin.
0 : 0dB *
1 : 2.5dB

INT_EN: Controls output of INT signal
0 : Enable *
1 : Disable

(Note) The INT signal is cleared when switching from Enable to Disable. After the power is turned on, first use the INT clear signal to reset from "INT_EN" or I^2C-BUS "read mode".

OUTCTL1: Selects SW12 output. Controls output for "C OUT to AUX".
0 : Normal (Normal output mode)
1 : MUTE * (Input mode)

OUTCTL2: Selects SW13 output. Controls output for "B OUT to L1".
0 : Normal * (Normal output mode)
1 : MUTE (Input mode)

(Note) During video input mode set when OUTCTL1 ; DATA4[6] = "1" and OUTCTL2 ; DATA4[5] = "1", output pins (pins 30 and 34) become DC output pins (0.6 V Typ.).
If there is not sink ability of the 75 Ω driver connected to this IC, the IC may not operate correctly.
Note with caution that the countermeasure shown in the figure below (Figure 4) will be required.

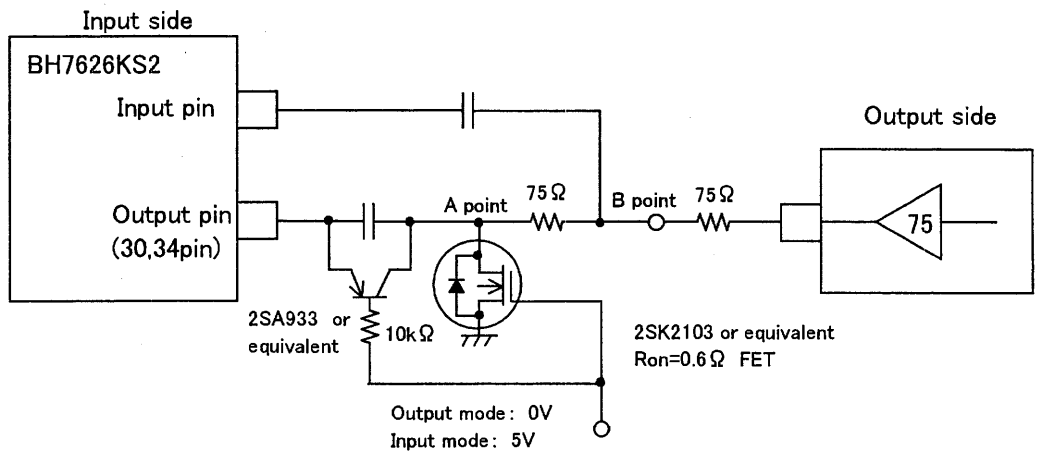


Figure-4. Example of external Circuit for Video I/O Switching

Standby: Sets Normal mode or Standby mode.
0 : Normal *
1 : Standby
(Note) See the block diagram on page 4 for description of the blocks during Standby mode.

MIXSW: Selects SW14 input. Selects signal to be input to L1SW (SW2) and YAUXSW (SW3).
0 : ENC CVBS *
1 : Y/C MIX

DRV_FLT: Selects SW15 input. Selects whether or not 75 Ω driver output signal is output via a filter.
0 : Without filter *
1 : With filter
(Note) The ENC input setting is fixed as "1: With filter". (See page 14.)

PARALLEL1: Sets PARALLEL1 pin's output.
0 : Low *
1 : Hi

RGB0/3: Sets AMP gain individually for R, G, and B output pins.
0 : 0dB *
1 : 3dB

ASW 1 to 6: Sets ASW pin's output.
0 : Low
1 : Hi
(Note) Initial condition : ASW1:H ASW 2:L ASW 3:H ASW 4:L ASW 5:L ASW6:L *

FSL: Sets FSL1's output
00 : Low, FS1 input mode *
01 : Low
10 : MID
11 : HI

FSA : Sets FSAUX's output
00 : Low , FS2 input mode *
01 : Low
10 : MID
11 : HI

(Note) For description of the input mode, see page 15.

FSL	FS1	FSA	FS2
00	Input mode is valid	00	Input mode is valid
01	Input mode is invalid	01	Input mode is invalid
10	↓	10	↓
11	↓	11	↓

○ I^2C -BUS Format (READ MODE)

S	SLAVE ADDRESS	A	DATA1	A/N	DATA2	A/N	DATA3	A/N	DATA4	A/N	DATA5	A/N	DATA6	A/N	P

S : Start Condition
A/N : NO acknowledge
P : Stop Condition

	b7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	0	0	1	0	0	ADR	R/W
DATA1	HI	ADSW		L1SW		YAUXSW		
DATA2	CAUXSW		RSW		GBSW		HI	HI
DATA3	CRSW	FBSW		HI	AMP6/8	RGB_FLT	CL/BI SEL	AD0/2_5
DATA4	INT_EN	OUTCTL1	OUTCTL2	Standby	MIXSW	DRV_FLT	ASW5	ASW6
DATA5	PARALLEL1	RGB0/3	HI	HI	ASW1	ASW2	ASW3	ASW4
DATA6	FSL		FSA		FS1		FS2	

Don't Care

ADR: Sets slave address via ADR pin. (Read mode)
0: When ADR pin's input = L, address is "91H".
1: When ADR pin's input = H, address is "93H".

R/W: Selects Read or Write mode
0 : WRITE
1 : READ

FS1: Outputs status of FS1
00 : Low
10 : MID
11 : HI

FS2 : Outputs status of FS2
00 : Low
10 : MID
11 : HI

○ I²C−BUS operating conditions

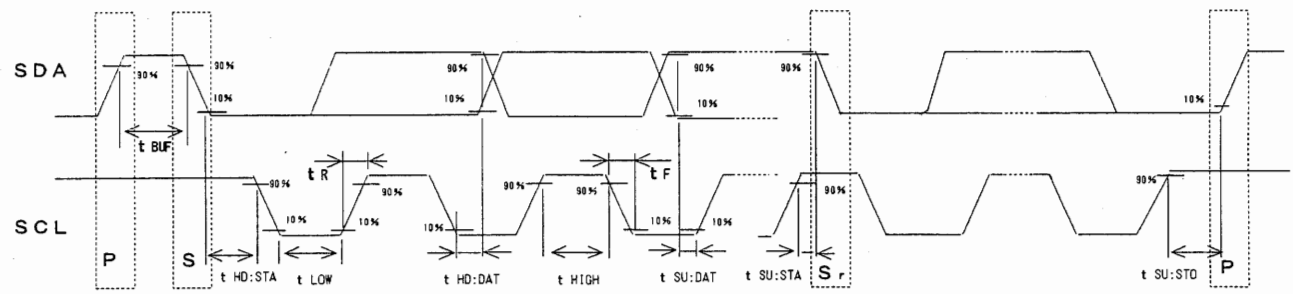
The I²C-BUS supports the Version 2.0 Fast mode. It does not support HS mode.

Item	Symbol	limit		Unit
		Min.	Max.	
SCL CLK frequency	f_{SCL}	0	400	kHz
Data transfer waiting time	t_{BUF}	1.3	−	μS
Beginning hold time	$t_{HD:STA}$	0.6	−	μS
SCL「L」hold time	t_{LOW}	1.3	−	μS
SCL「H」hold time	t_{HIGH}	0.6	−	μS
Beginning setup time	$t_{SU:STA}$	0.6	−	μS
Data hold time	$t_{HD:DAT}$	0 ※1	−	nS
Data setup time	$t_{SU:DAT}$	100	−	nS
Signal rise time	t_R	−	3.0 ※2	μS
Signal fall time	t_F	−	300	nS
Stop setup time	$t_{SU:STO}$	0.6	−	μS

※1 The signal fall time may change, depending on the wire delay or capacitance load during SCL's falling edge, Set the data hold time (up to 300 ns) on the transmitting side.

※2 If the signal rise time increases, note with caution that restrictions may apply at the SCL clock's maximum frequency, so the rate minimum values must be met for each rating parameter set between the SCL and SDA signals. Be sure to evaluate with an actual device before using.

I²C−BUS control signal



■ Selects 75 Ω driver's output AMP gain (AMP6/8) and filter settings (DRV_FLT)

○ Gain settings made via AMP6/8 are valid only when ENC input has been selected via the various output pins.
Therefore, when any output other than ENC input is selected, the setting made via AMP6/8 is ignored (fixed at 6 dB).
The filter setting by DRV_FLT becomes fixed as "with filter" when ENC input has been selected via the various output pins.
(ENC input: ENC CVBS/Y, Y/C MIX, ENC Y, ENC C, ENC R, ENC G, ENC B)

Setting of 75 Ω driver output under various switch modes

○ CVBS/Y OUT to L1

L1SW	Selected input PIN	AMP6/8		DRV_FLT	
		0(6dB)	1(8dB)	0(Without)	1(With)
00	AUX CVBS/Y	6dB	6dB	Without	With
01	ENC CVBS/Y or Y/C MIX	6dB	8dB	With	With
10	ENC Y	6dB	8dB	With	With
11	MUTE	–	–	–	–

○ CVBS/Y OUT to AUX

YAUXSW	Selected input PIN	AMP6/8		DRV_FLT	
		0(6dB)	1(8dB)	0(Without)	1(With)
000	L1 CVBS/Y	6dB	6dB	Without	With
001	TU CVBS	6dB	6dB	Without	With
010	ENC CVBS/Y or Y/CMIX	6dB	8dB	With	With
011	ENC Y	6dB	8dB	With	With
1xx	MUTE	–	–	–	–

○ C OUT to AUX

CAUXSW	Selected input PIN	AMP6/8		DRV_FLT	
		0(6dB)	1(8dB)	0(Without)	1(With)
00	L1 C	6dB	6dB	Without	With
01	ENC C	6dB	8dB	With	With
1x	MUTE	–	–	–	–

○ R/C OUT to L1

RSW	Selected input PIN	AMP6/8		DRV_FLT	
		0(6dB)	1(8dB)	0(Without)	1(With)
00	ENC C or ENC R	6dB	8dB	With	With
01	AUX R/C	6dB	6dB	Without	With
1x	MUTE	–	–	–	–

○ G OUT to L1
B OUT to L1

GBSW	Selected input PIN	AMP6/8		DRV_FLT	
		0(6dB)	1(8dB)	0(Without)	1(With)
00	ENC G,ENC B	6dB	8dB	With	With
01	AUX G,AUX B	6dB	6dB	Without	With
10	MUTE	–	–	–	–

■ INT signal (pin 45)

○ The INT signal is used to monitor the status of FS1 and FS2, and High (high impedance) output is set when this status changes. This monitoring of FS1 and FS2 occurs when "Input mode" has been set via the I²C bus.

Mode		Monitoring
FS1	FS2	
Input mode	Input mode	Both
Input mode	The other	FS1 only
The other	Input mode	FS2 only
The other	The other	No monitoring

○ The INT signal is cleared each time data is read via the I²C bus (i.e., during read mode), if the slave address matches.

○ INT signal output control

Control can be performed via the I²C bus. When switching from Enable to Disable, the INT signal is cleared.

(Note) After the power is turned on, first use the INT clear signal to reset from "INT_EN" or "read mode".

■ Standby mode

○ Standby mode can be set via the I²C bus. During Standby mode, the only blocks that operate are those enclosed in broken lines in Figure 3's block diagram.

■ ALL MUTE

○ The output pins for CVBS/Y, C, R/C, G, and B (pins 14, 28, 29, 30, 32, 34, and 36) are all muted.
Mute control of individual outputs is performed via the I²C bus.

ALL MUTE	Mode
H	Nomal
L	Mute

■ Bias output during Mute mode

○ During MUTE mode, bias output at the no signal time is set.

(Note)

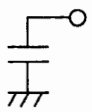
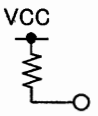
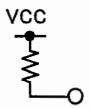
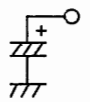
1) R/C OUT to L1 pin (pin 28)
During Mute mode, the bias output selected by "CL/BI SEL" is set.

2) C OUT to AUX pin (pin 34)
During Mute mode, the bias output varies according to whether CAUXSW;DATA2[7,6] = "10" or "11".

10 : MUTE (Output voltage=0.2V Typ.)
11 : MUTE (Output voltage=2.1V Typ.)

When MUTE has been selected, use DATA2[7,6] = "11".
During ALL_MUTE mode, the output voltage becomes 2.1 V (Typ.).

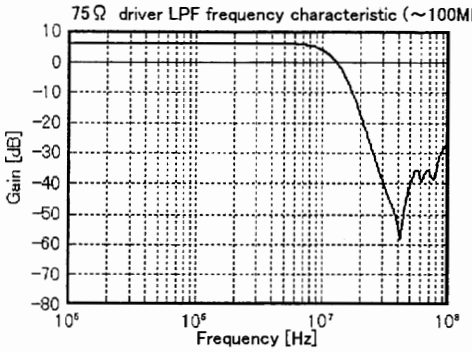
■ Handling of unused pins

Pin name	Pin handling	Pin name	Pin handling
19. AVCC1 33. AVCC2 43. DVCC1 49. DVCC2	—	45. INT	— (OPEN)
16. AGND1 35. AGND2 39. DGND1 1. DGND2		3. FS AUX 5. FS L1	— (OPEN)
4. ENC C 26. L1 C		37. TEST1	
40. AUX R/C		41. ALL MUTE	
2. ENC Y 6. ENC R 8. ENC G 10. ENC B 12. TU CVBS 24. L1 CVBS/Y 38. AUX CVBS/Y 42. AUX G 44. AUX B 48. ENC CVBS	 or —(OPEN) If a pin has been not set for input, it can be left unconnected (OPEN); otherwise connect the coupling to GND.	25. ADR	
14. CVBS/Y OUT to INPUT AD 18. R 20. G 22. B	— (OPEN)	7. PARALLEL1	— (OPEN)
30. B OUT to L1 29. G OUT to L1 28. R/C OUT to L1 36. CVBS/Y OUT to AUX 34. C OUT to AUX 32. CVBS/Y OUT to L1		46. SCL	
50. L1 FB OUT		47. SDA	
52. FSW		9. VREF	
51. FB		27. FS1 31. FS2	
23. ASW1 21. ASW2 17. ASW3 15. ASW4 13. ASW5 11. ASW6	— (OPEN)		

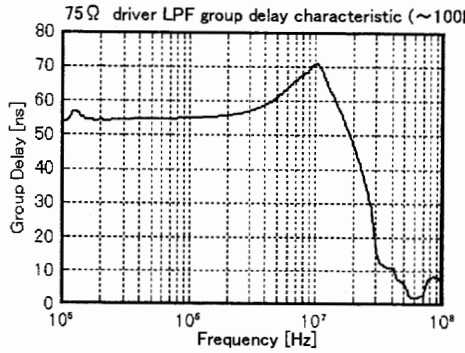
■ Electrical characteristics curve (Reference)

Conditions : Ta=25°C, VCC=5V, Vin=1Vpp

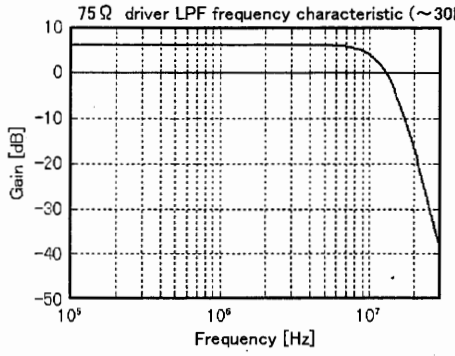
75Ω driver LPF frequency characteristic (~100MHz)



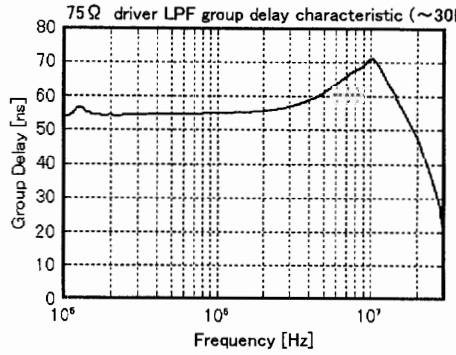
75Ω driver LPF group delay characteristic (~100MHz)



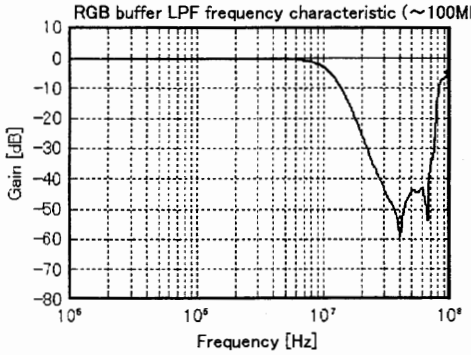
75Ω driver LPF frequency characteristic (~30MHz)



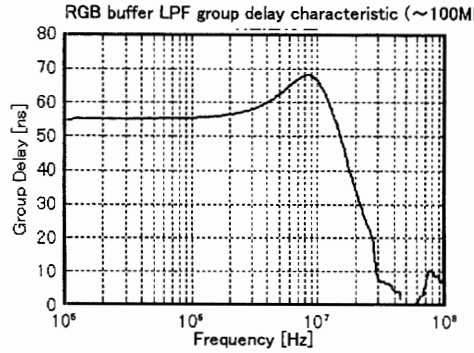
75Ω driver LPF group delay characteristic (~30MHz)



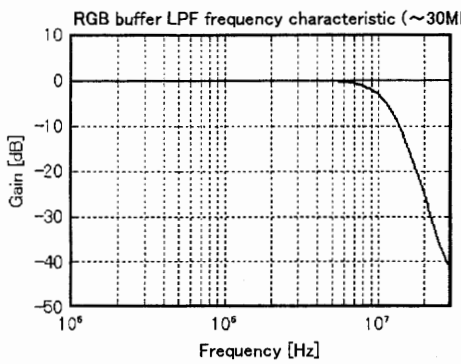
RGB buffer LPF frequency characteristic (~100MHz)



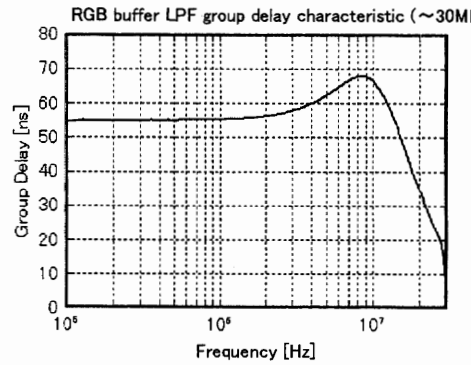
RGB buffer LPF group delay characteristic (~100MHz)



RGB buffer LPF frequency characteristic (~30MHz)



RGB buffer LPF group delay characteristic (~30MHz)



The above data is provided for reference only and is not guaranteed.
Be sure to conduct a thorough evaluation using an actual device before use.

■ Cautions on use

(1) Absolute maximum ratings

This LSI may be damaged if the absolute maximum ratings for the applied voltage, temperature range, or other parameters are exceeded. Therefore, avoid using a voltage or temperature that exceeds the absolute maximum ratings.
If it is possible that absolute maximum ratings will be exceeded, use fuses or other physical safety measures and determine ways to avoid exceeding the LSI's absolute maximum ratings.

(2) GND potential

Try to set the minimum voltage for the GND pin potential, regardless of the operation mode.
Check that the voltage of each pin does not go below the GND pin's voltage, including transient phenomena.

(3) Shorting between pins and mounting errors

When mounting the LSI chip on a board, be very careful to set the chip's orientation and position precisely.
When the power is turned on, the LSI may be damaged if it is not mounted correctly. The LSI may also be damaged if a short occurs (due to a foreign object, etc.) between two pins, between a pin and the power supply, or between a pin and the GND.

(4) Operation in strong magnetic fields

Note with caution that operation faults may occur when this LSI operates in a strong magnetic field.

(5) Operating power supply voltage

Although operation of basic circuit functions is guaranteed when within the rated operating power supply voltage range (4.75 V to 5.25 V), be sure to confirm the voltage setting along with settings for constants and elements before use.

(6) Operation temperature range

Although operation of basic circuit functions is guaranteed when within the rated operation temperature range (−25℃ to +65℃), be sure to check this in the thermal design.
In the set design, check the placement of fans and the board layout to make sure there is adequate circulation of air around the IC, and implement any additional heat dissipation measures that are needed.