

FEATURES

- 5V Supply Voltage
- FOUT/PWMOUT Output Period Range:
 - $40\mu s \leq t_{FOUT} \leq 1.398\text{min}$
 - $RSET = 4.32M\Omega$
- PWMOUT Output Duty Cycle:
 - 75% for $FDIV2:0 = 000$
 - CPWM = 100pF
- PWMOUT Duty Cycle Reduction
 - 1MΩ Potentiometer
- Fully Assembled and Tested
- 2in x 2in 2-layer circuit board

COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION
C1	1	100pF ±10% capacitor (0805)
C2	1	4.7µF ±10% capacitor (0805)
R2	1	10MΩ ± 1% (0805)
R1	1	4.32MΩ ± 1% (0805)
PWM_ADJ	1	1MΩ Potentiometer
U1	1	TS3004
VDD,F_OUT, PWM_OUT	3	Test points
J1, FDIV0, FDIV1, FDIV2	3	Jumper

DESCRIPTION

The TS3004 is a single-supply, second-generation Touchstone Semi oscillator/timer fully specified to operate at a supply voltage range of 1.55V to 5.25V while consuming less than 2.4µA(max) supply current. Requiring only a resistor to set the base output frequency (or output period) at 25kHz (or 40µs) with a 50% duty cycle, the TS3004 timer/oscillator is compact, easy-to-use, and versatile. Optimized for ultra-long life, low frequency, battery-powered/portable applications, the TS3004 joins the TS3001, TS3002, TS3003 and TS3006 in Touchstone's CMOS timer family in its "NanoWatt Analog™" series of high-performance analog integrated circuits.

The TS3004 requires only an $RSET = 4.32M\Omega$ resistor to set the FOUT/PWMOUT output period range to between 40µs and 1.398 minutes. To change the output period, an FDIV2:0 combination can be selected. With an on-board 100pF CPWM capacitor, the duty cycle of PWMOUT is set at approximately 75%. Further reduction of the duty cycle is available with an on-board 1MΩ potentiometer. The complete circuit is designed at a supply voltage of 5V. The TS3004 is fully specified over the -40°C to +85°C temperature range and is available in a low-profile, 10-pin 3x3mm TDFN package with an exposed back-side paddle.

Product datasheet and additional documentation can be found on the factory web site at www.touchstonesemi.com.

ORDERING INFORMATION

Order Number	Description
TS3004DB	TS3004 Demo Board

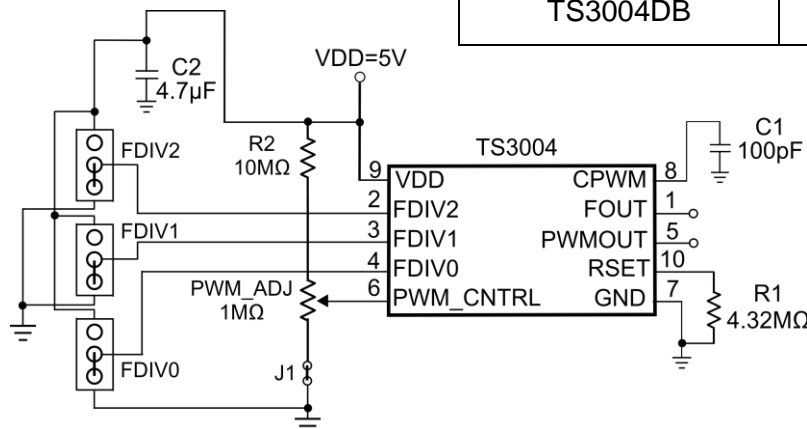


Figure 1. TS3004 Demo Board Circuit

DESCRIPTION

The TS3004 requires only an RSET = 4.32MΩ resistor to set the FOUT/PWMOUT output period between 40μs and 1.398 minutes. To change the output period, an FDIV2:0 combination can be selected. With an on-board 100pF CPWM capacitor, the duty cycle of PWMOUT is set at approximately 75%. Further reduction of the duty cycle is available with an on-board 1MΩ potentiometer. The complete circuit is designed at a supply voltage of 5V and it is shown in Figure 1.

The TS3004 is a user-programmable oscillator where the period of the square wave at its FOUT terminal is generated by an external resistor connected to the RSET pin. The output period is given by:

$$t_{FOUT} (s) = \frac{8^{FDIV2:0} \times RSET}{1.08E11}$$

Equation 1. FOUT Frequency Calculation where FDIV2:0 = 0 to 7

With RSET = 4.32MΩ and FDIV2:0=000(0), the FOUT period is approximately 40μs with a 50% duty cycle. As design aids, Tables 1 lists TS3004's typical FOUT period for various standard values for RSET and FDIV2:0 = 111(7).

RSET (MΩ)	tFOUT(s)
0.360	6.99
1	19.42
2.49	48.35
4.32	83.89
6.81	132.27
9.76	189.39
12	233

Table 1: tFOUT vs RSET for FDIV2:0 = 111(7)

The TS3004 also provides a separate PWM output signal at its PWMOUT terminal that is anti-phase with respect to FOUT. To adjust the pulse width of the PWMOUT output, a single capacitor can be placed at the CPWM pin. To determine the capacitance needed for a desired pulse width, the following equation is to be used:

$$CPWM(F) = \frac{\text{Pulse Width(s)} \times I_{CPWM}}{V_{CPWM} \cong 300mV}$$

Equation 2. CPWM Capacitor Calculation

where ICPWM and VCPWM is the current supplied and voltage applied to the CPWM capacitor, respectively. The pulse width is determined based on the period of FOUT and should never be greater than the period at FOUT. Make sure the PWM_CNTRL pin is set to at least 400mV when calculating the pulse width of PWMOUT. Note VCPWM is approximately 300mV, which is the RSET voltage. Also note that ICPWM is either 1μA or 100nA. Refer to Table 2 for the output period range available with a 10MΩ RSET resistor.

FDIV 2:0	tFOUT	ICPWM (A)
000	40μs	1μ
001	320μs	1μ
010	2560μs	100n
011	20.48ms	100n
100	163.84ms	100n
101	1.310s	100n
110	10.486s	100n
111	1.398min	100n

Table 2: FOUT and PWMOUT Frequency Range per FDIV2:0 Combination for RSET= 4.32MΩ

The PWMOUT output pulse width can be adjusted further after selecting a CPWM capacitor. This can be achieved by applying a voltage to the PWM_CNTRL pin between VRSET and GND. With a voltage of at least VRSET, the pulse width is set based on Equation 2. For example, with a period of 40μs and a 0.1μF capacitor at the CPWM pin generates a pulse width of approximately 30ms. This can be calculated using Equation 2. By reducing the PWM_CNTRL voltage from VRSET ≅ 300mV to GND, the pulse width can be reduced further. Note that VRSET can be set up to VDD.

QUICK START PROCEDURE

Required Equipment

- TS3004 Demo Board
- DC Power Supply
- Oscilloscope Model Agilent DSO1014A or equivalent
- Two 10X, 15pF//10MΩ oscilloscope probes
- Potentiometer screwdriver

To evaluate the TS3004 silicon timer, the following steps are to be performed:

- 1) Before connecting the DC power supply to the demo board, turn on the power supply, set the DC voltage to 5V, and then turn it off.
- 2) Connect the DC power supply positive terminal to the test point labeled VDD. Connect the negative terminal of the DC power supply to the test point labeled GND.
- 3) To monitor the FOUT output signal, connect the signal terminal of an oscilloscope probe to the test point labeled FOUT and the ground terminal to the test point labeled GND.
- 4) To monitor the PWMOUT output signal, connect the signal terminal of a second oscilloscope probe to the test point labeled PWM_OUT and the ground terminal to the test point labeled GND.

- 5) Select two channels on the oscilloscope and set the vertical voltage scale and the vertical position on each channel to 2V/DIV and 0V, respectively. Set the horizontal time scale to 5 μ s/DIV. The coupling should be DC coupling. Turn on the power supply.

The supply current will vary depending on the load on the output. Given the default set-up on the board, the FOUT/PWMOUT output period is approximately 40 μ s. The PWMOUT duty cycle is set to approximately 75%. With an output load of 15pF on both FOUT and PWMOUT outputs due to the oscilloscope probes, the supply current should be less than 8 μ A.

- 6) To change the period, change the combination of FDIV2:0 via jumpers FDIV2, FDIV1, and FDIV0. Refer to Table 2.
- 7) If further reduction of the duty cycle of the PWMOUT output is desired, turn the potentiometer clockwise. If jumper J1 is removed, the PWM_CNTRL pin is tied to VDD and the potentiometer will not change the PWMOUT output duty cycle.

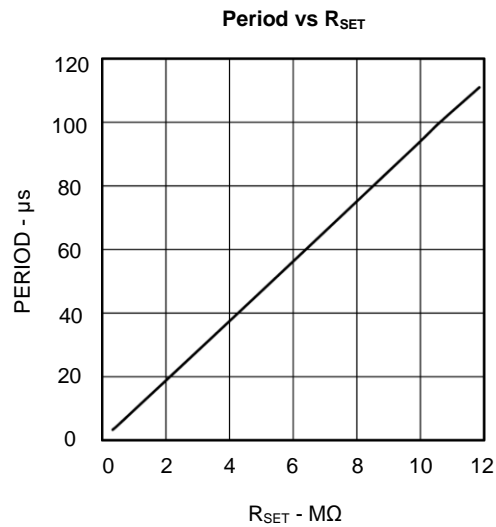


Figure 2. FOUT/PWMOUT Period vs R_{SET}

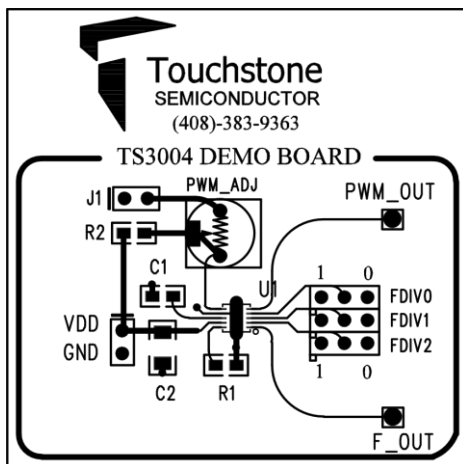


Figure 3. Top Layer View #1

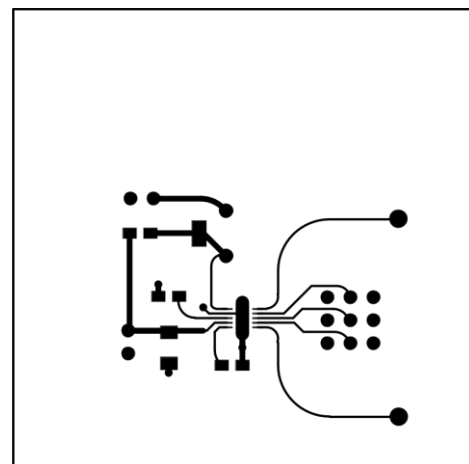


Figure 4. Top Layer View #2

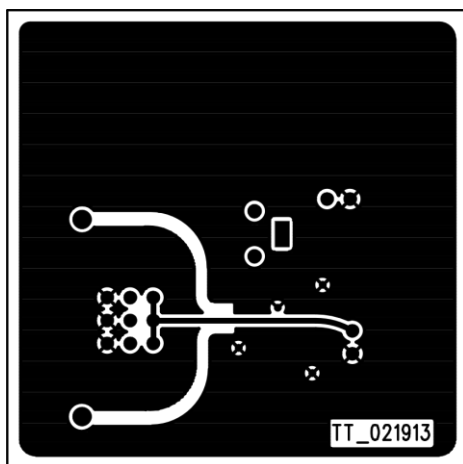


Figure 5. Bottom Layer (GND) #1

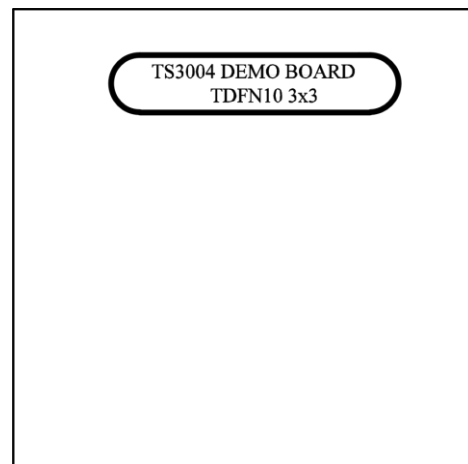


Figure 6. Bottom Layer (GND) #2