

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4557B

LSI

1-to-64 bit variable length shift register

Product specification
File under Integrated Circuits, IC04

January 1995

1-to-64 bit variable length shift register

HEF4557B LSI

DESCRIPTION

The HEF4557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled length control inputs ($L_1, L_2, L_4, L_8, L_{16}$ and L_{32}) plus one. Serial data may be selected from the D_A or D_B data inputs with the A/\bar{B} select input. This feature is useful for recirculation

purposes. Information on D_A or D_B is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP_0 while $\overline{CP_1}$ is LOW or on the HIGH to LOW transition of $\overline{CP_1}$ while CP_0 is HIGH. A HIGH on master reset (MR) resets the register and forces O to LOW and \bar{O} to HIGH, independent of the other inputs.

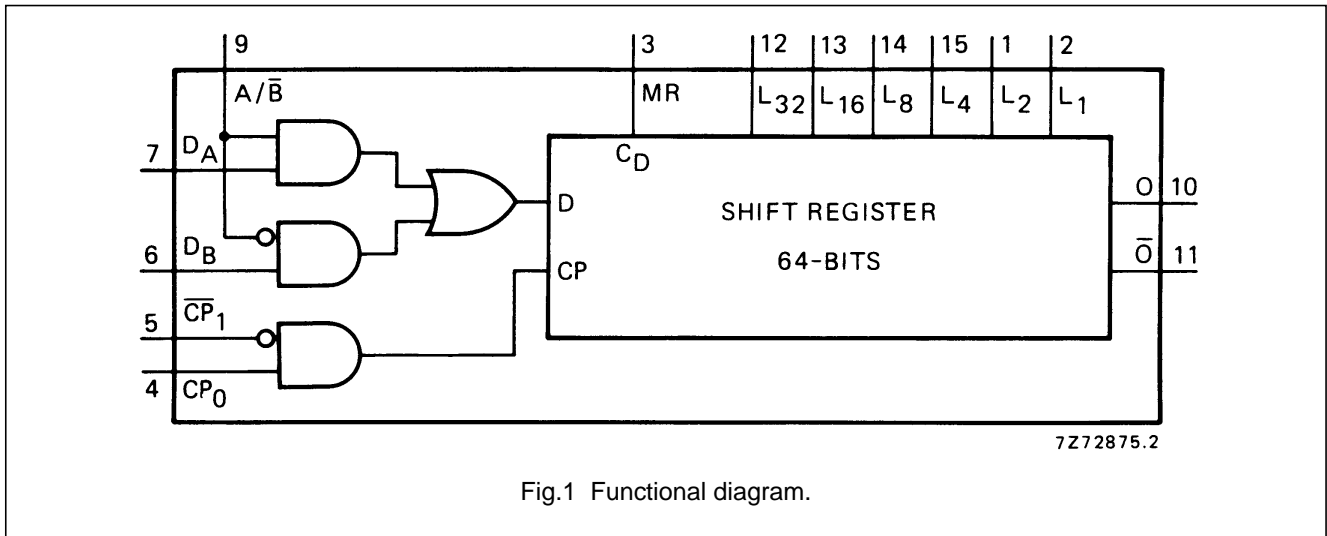


Fig.1 Functional diagram.

PINNING

- D_A, D_B data inputs
- A/\bar{B} select data input
- CP_0 clock input
- $\overline{CP_1}$ clock enable input
- MR asynchronous master reset
- L_1 to L_{32} bit-length control inputs
- O, \bar{O} buffered outputs

- HEF4557BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4557BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4557BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

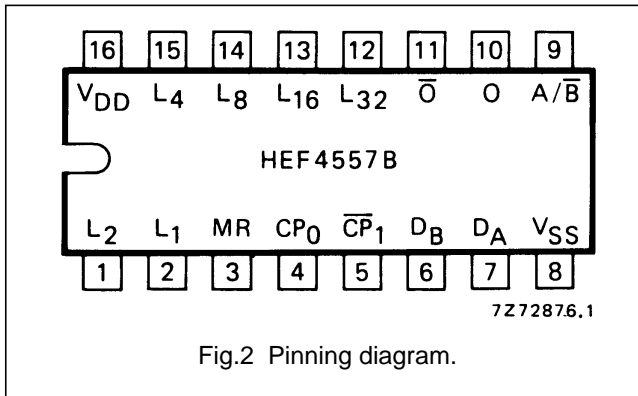


Fig.2 Pinning diagram.

FAMILY DATA, I_{DD} LIMITS category LSI

See Family Specifications

1-to-64 bit variable length shift register

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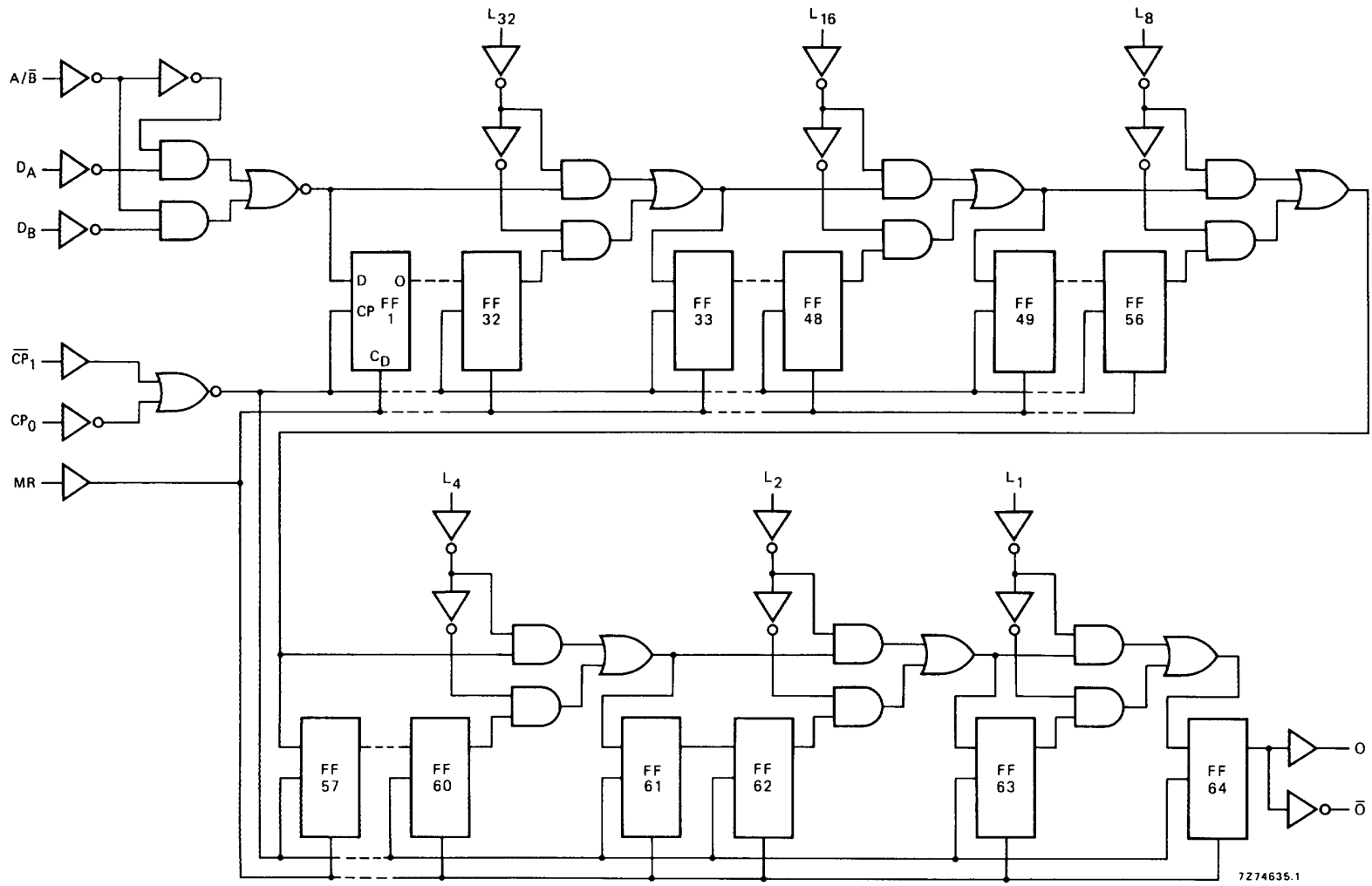


Fig.3 Logic diagram.

1-to-64 bit variable length shift register

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FUNCTION TABLE

INPUTS						OUTPUT
MR	A/B	D _A	D _B	CP _O	CP ₁	O ⁽¹⁾
L	L	D ₁	D ₂	↗	L	D ₂
L	H	D ₁	D ₂	↗	L	D ₁
L	L	D ₁	D ₂	H	↘	D ₂
L	H	D ₁	D ₂	H	↘	D ₁
H	X	X	X	X	X	L

Notes

1. The moment D_n appears at O depends on the bit-length shown in the table below.
2. H = HIGH state (the more positive voltage)
3. L = LOW state (the less positive voltage)
4. X = state is immaterial
5. ↗ = positive-going transition
6. ↘ = negative-going transition
7. D_n = either HIGH or LOW

BIT-LENGTH SELECT FUNCTION TABLE

L ₃₂	L ₁₆	L ₈	L ₄	L ₂	L ₁	REGISTER LENGTH
L	L	L	L	L	L	1-bit
L	L	L	L	L	H	2-bits
L	L	L	L	H	L	3-bits
L	L	L	L	H	H	4-bits
L	L	L	H	L	L	5-bits
L	L	L	H	L	H	6-bits
L	L	L	H	H	L	7-bits
L	L	L	H	H	H	8-bits
↓	↓	↓	↓	↓	↓	↓
L	H	H	H	H	H	32-bits
H	L	L	L	L	L	33-bits
H	L	L	L	L	H	34-bits
↓	↓	↓	↓	↓	↓	↓
H	H	H	H	L	L	61-bits
H	H	H	H	L	H	62-bits
H	H	H	H	H	L	63-bits
H	H	H	H	H	H	64-bits

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	3 500 f _i + ∑ (f _o C _L) × V _{DD} ² 15 000 f _i + ∑ (f _o C _L) × V _{DD} ² 37 000 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

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AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $CP_0, \overline{CP}_1 \rightarrow O, \overline{O}$ HIGH to LOW	5	t_{PHL}	240	480	ns	$213\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		90	180	ns	$79\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		65	130	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	240	480	ns	$213\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		90	180	ns	$79\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		65	130	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$
	$MR \rightarrow O$ HIGH to LOW	5	t_{PHL}	170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		80	160	ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
	$MR \rightarrow \overline{O}$ LOW to HIGH	5	t_{PLH}	140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		55	110	ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

Interpolation table (see note next page)

LENGTH CONTROL INPUTS						MINIMUM NUMBER OF BITS SELECTED	SET-UP, HOLD, RECOVERY TIMES
L_1	L_2	L_4	L_8	L_{16}	L_{32}		
L	L	L	L	L	L	1	specified
H	L	L	L	L	L	2	
X	H	L	L	L	L	3	
X	X	H	L	L	L	5	six equal steps
X	X	X	H	L	L	9	
X	X	X	X	H	L	17	
X	X	X	X	X	H	33	specified

Notes

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

1-to-64 bit variable length shift register

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LSI**AC CHARACTERISTICS** $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns; see also waveforms Fig.4

	V_{DD} V	SYMBOL	MIN.	TYP.		
Minimum clock pulse width; LOW for CP_0 or HIGH for \overline{CP}_1	5	t_{WCPL}	180	90 ns	see note	
	10	or	60	30 ns		
	15	t_{WCPH}	40	20 ns		
Minimum reset pulse width; HIGH	5	t_{WMRH}	150	75 ns		
	10		70	35 ns		
	15		50	25 ns		
Set-up times $D_A, D_B, A/\overline{B} \rightarrow CP_0,$ \overline{CP}_1 L_1 to $L_{32} = \text{LOW}$	5	t_{su}	360	180 ns		
	10		140	70 ns		
	15		90	45 ns		
	$L_{32} = \text{HIGH}$	5	t_{su}	40		-20 ns
		10		35		-10 ns
		15		30		-5 ns
Hold times $D_A, D_B, A/\overline{B} \rightarrow CP_0,$ \overline{CP}_1 L_1 to $L_{32} = \text{LOW}$	5	t_{hold}	-40	-110 ns		
	10		-10	-45 ns		
	15		0	-30 ns		
	$L_{32} = \text{HIGH}$	5	t_{hold}	90	30 ns	
		10		60	20 ns	
		15		50	15 ns	
Recovery times for MR L_1 to $L_{32} = \text{LOW}$	5	t_{RMR}	500	250 ns		
	10		250	125 ns		
	15		150	75 ns		
	$L_{32} = \text{HIGH}$	5	t_{RMR}	110	50 ns	
		10		70	30 ns	
		15		60	25 ns	
Minimum clock pulse frequency	5	f_{max}	2,5	5 MHz		
	10		7	14 MHz		
	15		10	20 MHz		

Note

1. The set-up, hold and recovery times vary with the minimum number of bits selected. For other values as specified one may interpolate as shown in the table (see previous page).

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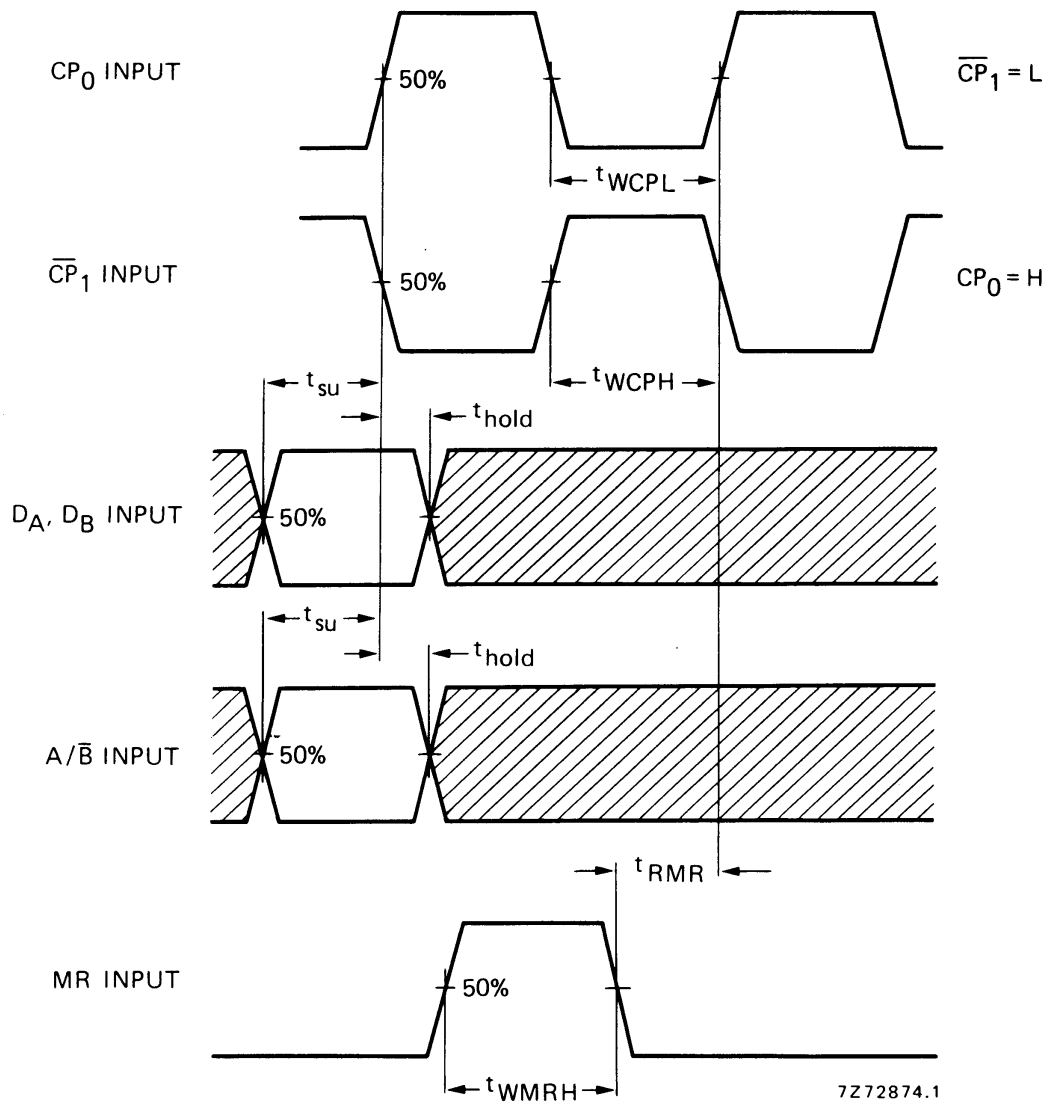
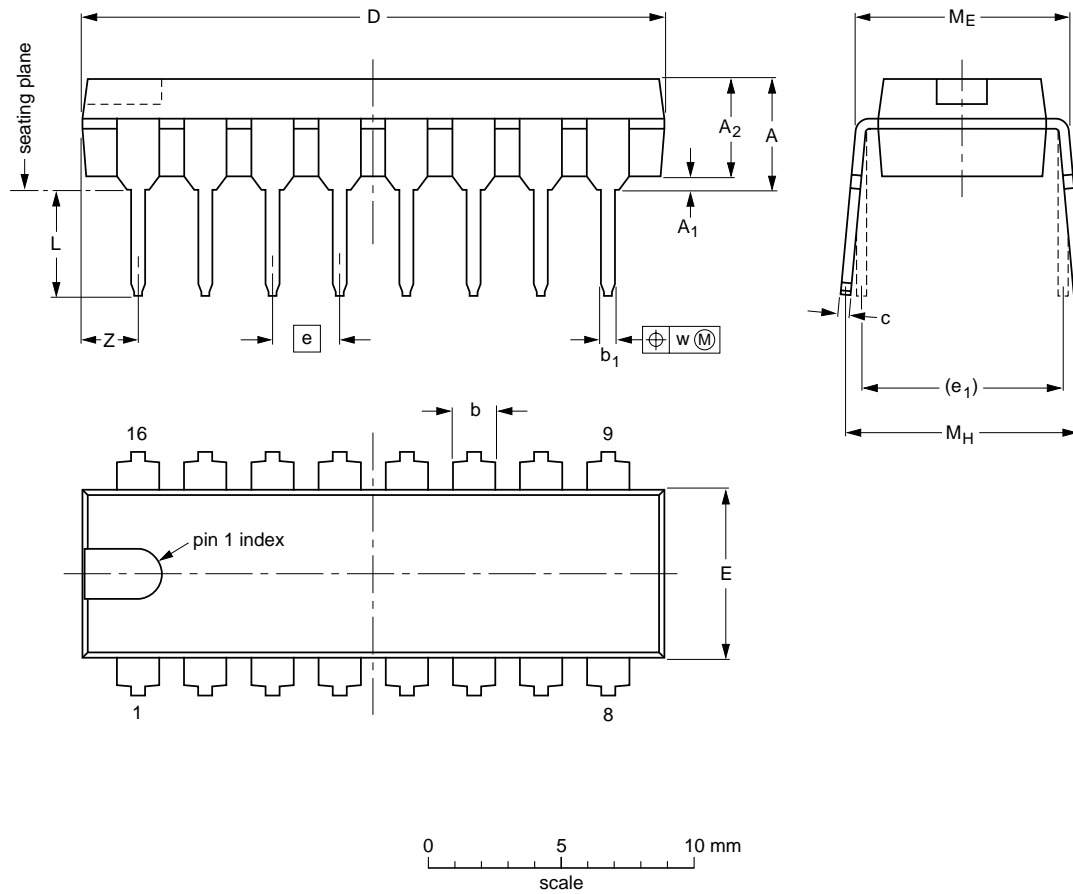


Fig.4 Waveforms showing recovery time for MR and minimum CP_0 , \overline{CP}_1 and MR pulse widths, set-up and hold times for D_A , D_B and A/\overline{B} to CP_0 and \overline{CP}_1 . Set-up and hold times are shown as positive values but may be specified as negative values.

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

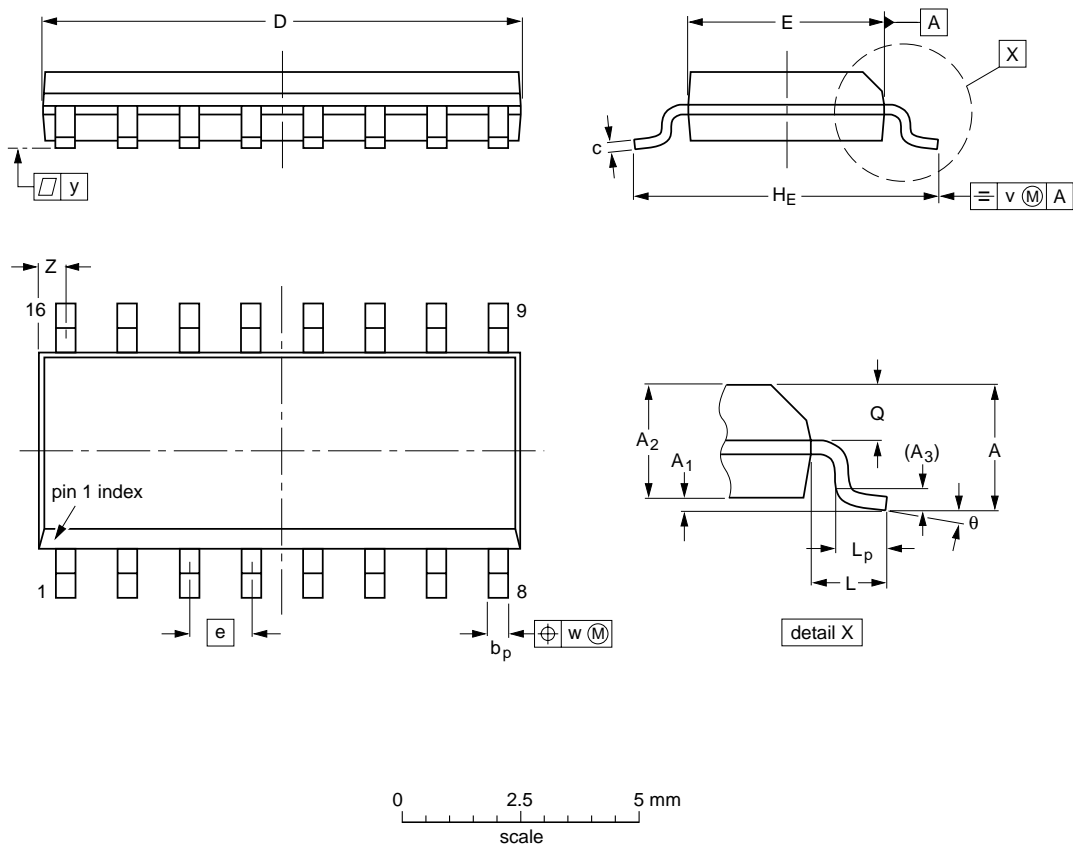
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				92-10-02 95-01-19

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22