

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4514B

MSI

1-of-16 decoder/demultiplexer with input latches

Product specification
File under Integrated Circuits, IC04

January 1995

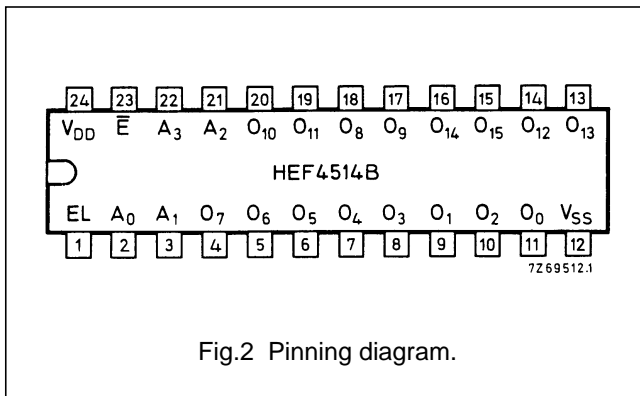
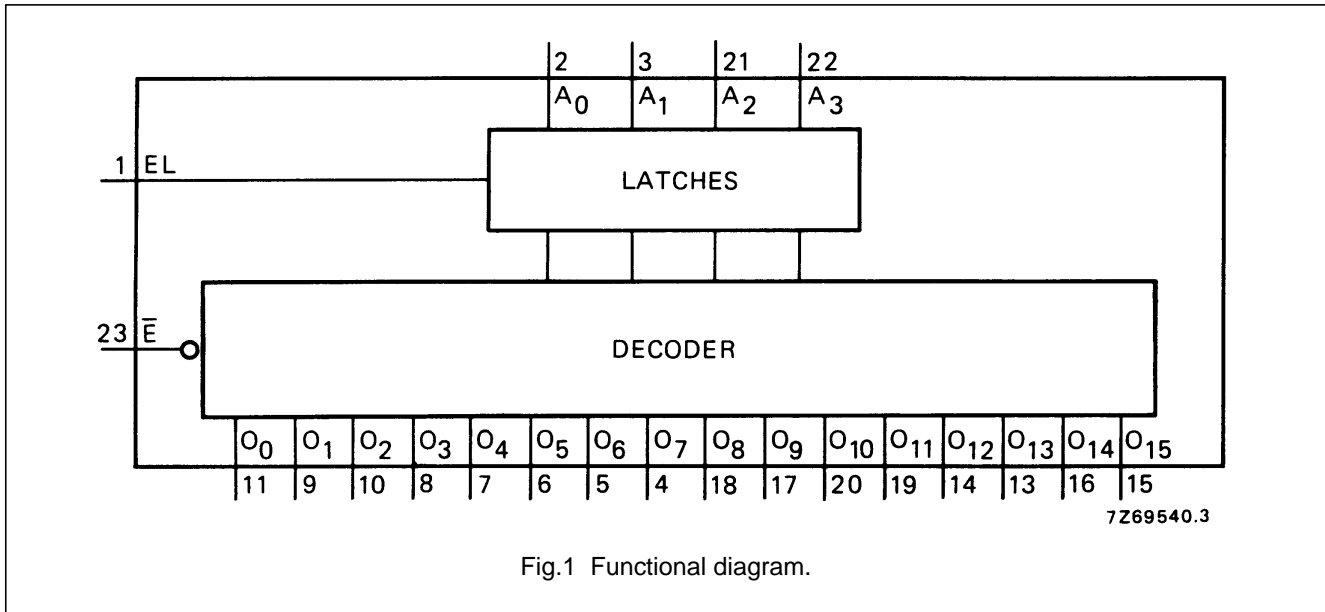
1-of-16 decoder/demultiplexer with input latches

HEF4514B
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DESCRIPTION

The HEF4514B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input (\bar{E}). The 16 outputs (O_0 to O_{15}) are mutually exclusive active HIGH. When EL is HIGH, the selected output is determined by the data on A_n . When EL goes LOW, the

last data present at A_n are stored in the latches and the outputs remain stable. When \bar{E} is LOW, the selected output, determined by the contents of the latch, is HIGH. At \bar{E} HIGH, all outputs are LOW. The enable input (\bar{E}) does not affect the state of the latch. When the HEF4514B is used as a demultiplexer, \bar{E} is the data input and A_0 to A_3 are the address inputs.



PINNING

- A_0 to A_3 address inputs
- \bar{E} enable input (active LOW)
- EL latch enable input
- O_0 to O_{15} outputs (active HIGH)

- HEF4514BP(N): 24-lead DIL; plastic (SOT101-1)
- HEF4514BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
- HEF4514BT(D): 24-lead SO; plastic (SOT137-1)
- (): Package Designator North America

APPLICATION INFORMATION

Some examples of applications for the HEF4514B are:

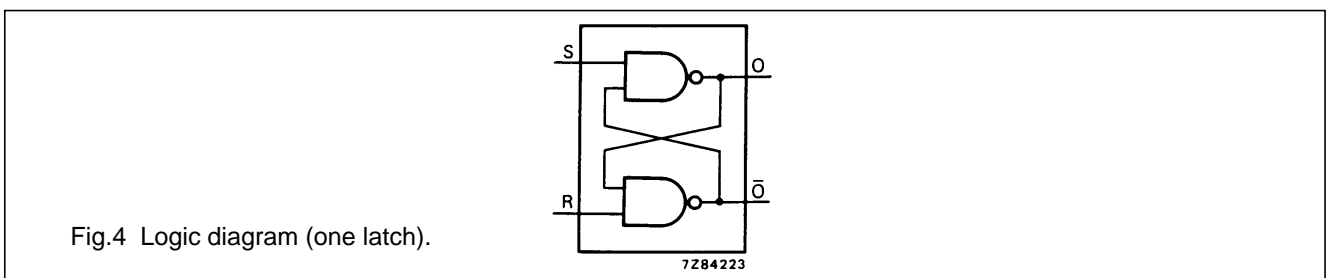
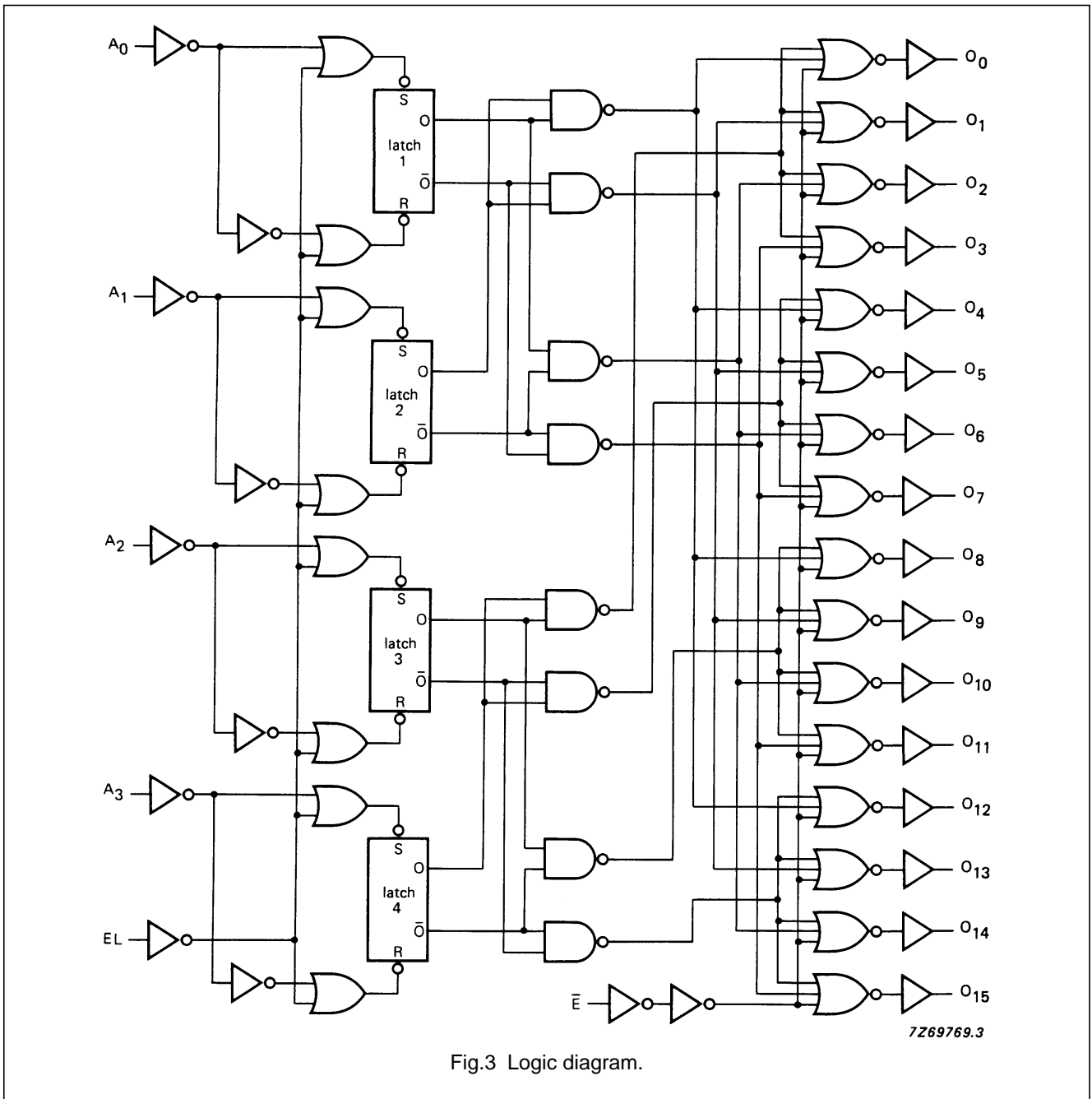
- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

1-of-16 decoder/demultiplexer with input latches

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TRUTH TABLE

INPUTS					OUTPUTS															
\bar{E}	A ₀	A ₁	A ₂	A ₃	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈	O ₉	O ₁₀	O ₁₁	O ₁₂	O ₁₃	O ₁₄	O ₁₅
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

Notes

- EL = HIGH; H = HIGH state (the more positive voltage);
L = LOW state (the less positive voltage); X = state is immaterial

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays A _n , EL → O _n HIGH to LOW	5	t _{PHL}	260	520	ns	233 ns + (0,55 ns/pF) C _L	
	10		95	190	ns	84 ns + (0,23 ns/pF) C _L	
	15		65	130	ns	57 ns + (0,16 ns/pF) C _L	
	LOW to HIGH	5	t _{PLH}	270	550	ns	243 ns + (0,55 ns/pF) C _L
		10		95	190	ns	84 ns + (0,23 ns/pF) C _L
		15		65	130	ns	57 ns + (0,16 ns/pF) C _L
\bar{E} → O _n HIGH to LOW	5	t _{PHL}	175	350	ns	148 ns + (0,55 ns/pF) C _L	
	10		65	130	ns	54 ns + (0,23 ns/pF) C _L	
	15		45	90	ns	37 ns + (0,16 ns/pF) C _L	
	LOW to HIGH	5	t _{PLH}	200	400	ns	173 ns + (0,55 ns/pF) C _L
		10		70	140	ns	59 ns + (0,23 ns/pF) C _L
		15		50	100	ns	42 ns + (0,16 ns/pF) C _L

1-of-16 decoder/demultiplexer with input latches

HEF4514B
MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Output transition times HIGH to LOW LOW to HIGH	5	t_{THL}	90	180	ns	$40\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		35	65	ns	$14\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		25	50	ns	$11\text{ ns} + (0,28\text{ ns/pF}) C_L$
	5	t_{TLH}	85	170	ns	$35\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		35	70	ns	$14\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		25	50	ns	$11\text{ ns} + (0,28\text{ ns/pF}) C_L$
Set-up time $A_n \rightarrow \text{EL}$	5	t_{su}	120	60	ns	see also waveforms Fig.5
	10		40	20	ns	
	15		30	15	ns	
Hold time $A_n \rightarrow \text{EL}$	5	t_{hold}	0	60	ns	
	10		0	20	ns	
	15		0	15	ns	
Minimum EL pulse width; HIGH	5	t_{WELH}	120	60	ns	
	10		40	20	ns	
	15		30	15	ns	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1100 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5500 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$16\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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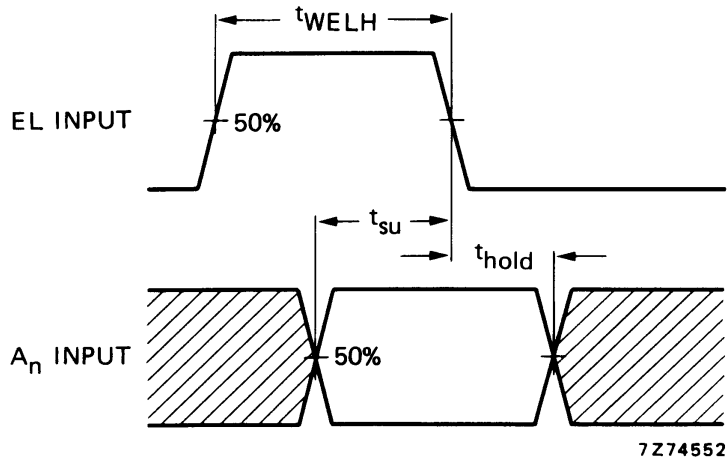
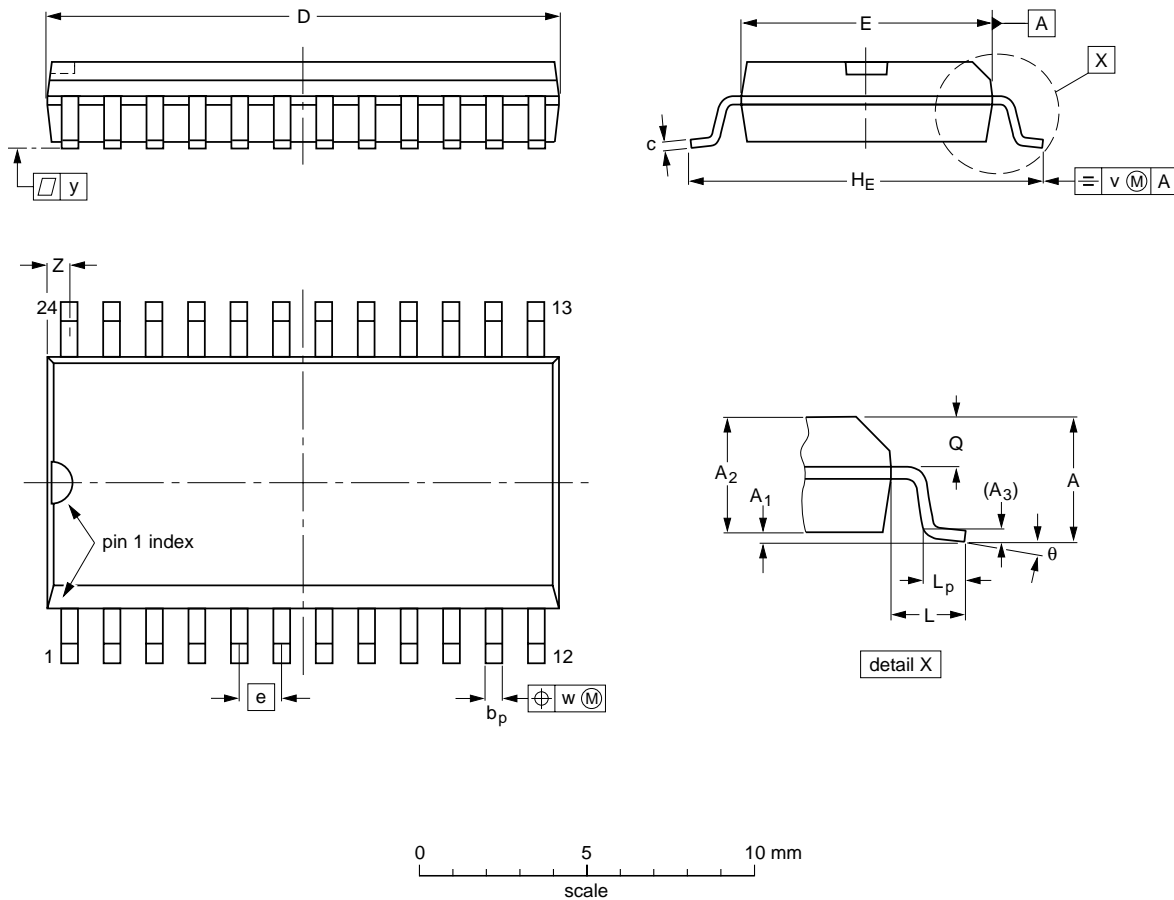


Fig.5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as negative values.

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

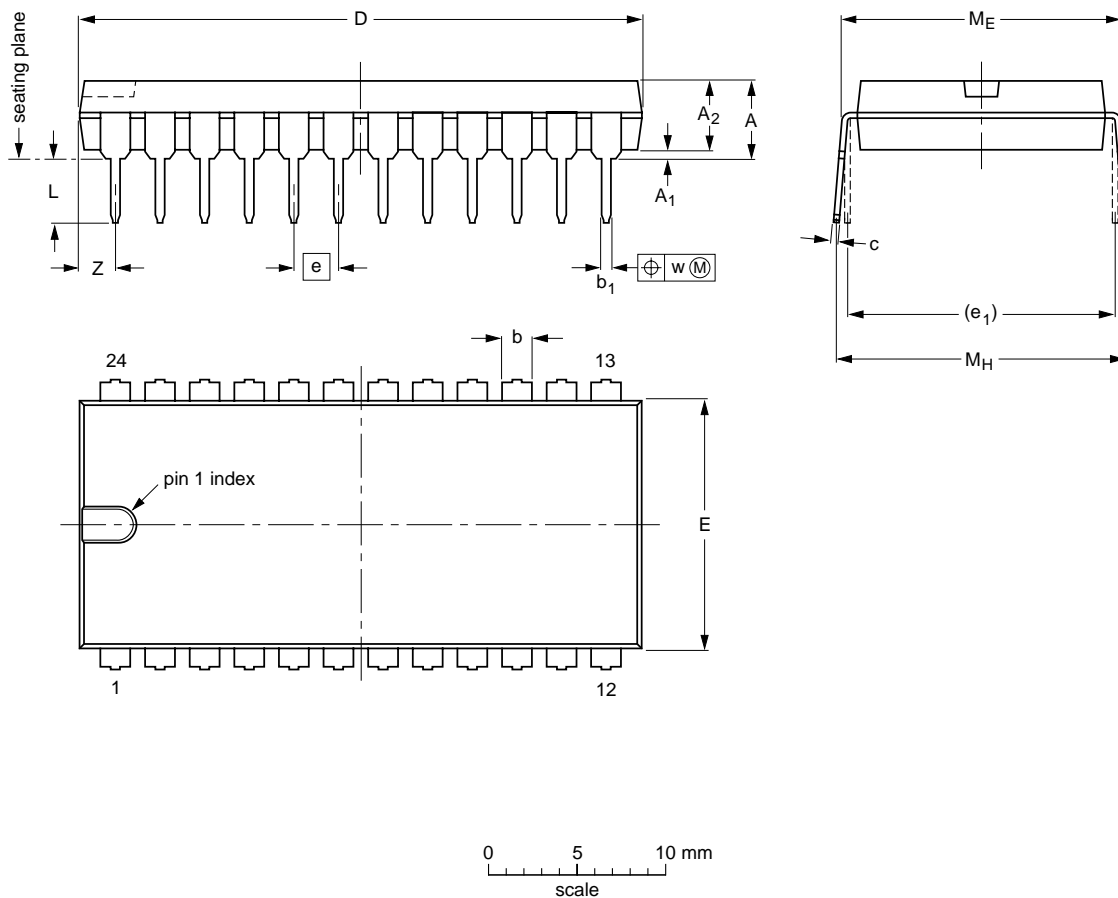
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

DIP24: plastic dual in-line package; 24 leads (600 mil)

SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				92-11-17 95-01-23