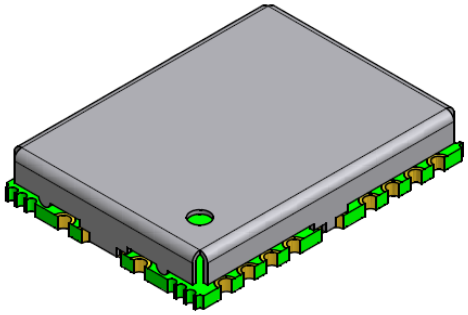

REV 1.2

TECHNICAL DESCRIPTION

Fastrax IT321 OEM GPS Receiver

This document describes the electrical connectivity and main functionality of the Fastrax IT321 OEM GPS Receiver.

November 19, 2007

Fastrax Ltd.

TRADEMARKS

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CHANGE LOG

Rev.	Notes	Date
1.0	Initial documentation	2007-08-24
1.1	Module name change to IT321, abs. max power dissipation 300mW, oper. temp. range -30C… +85C, GPIO6 & 13 added to HW rev. B, added VDD ripple specification, added ON_OFF timing, removed solder profile picture, added tape and reel spec, changed Application Board documents to rev C.	2007-10-11
1.2	GPIO13 changed to GPIO2 (IT321 PCB rev. C). Updated protocol configuration Table 3.	2007-11-19

CONTENTS

COMPLEMENTARY READING

The following Fastrax reference documents are complementary reading for this document. All operating and firmware related documentation is also available at ***www.fastrax.fi***

Ref. #	File name	Document name

The following SiRF reference documents are also complementary reading for this document. All operating and firmware related documentation is available from SiRF Technology, Inc.

Ref. #	File name	Document name
I	GSC3LTProductInsert.pdf	GSC3LT Brochure
II	NMEA Reference Manual.pdf	NMEA Reference Manual
III	SiRF Binary Protocol Reference Manual.pdf	SiRF Binary Protocol Reference Manual

1. GENERAL DESCRIPTION

The Fastrax IT321 is an OEM GPS receiver module, which provides the SiRFstarIII receiver *(ref I)* functionality using the state of the art SiRF GSC3LT chip. The module has tiny form factor 10.4x14.0mm, height is 2.3mm nominal (2.6mm max). The Fastrax IT321 receiver provides low power and very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations.

The module is available with two versions:

- SiRF ROM code version
- Early samples can be provided with embedded flash version (4Mbit in GSC3LTf) for evaluation with GSWLT3 firmware.

The module provides complete signal processing from antenna input to serial data output in either NMEA messages *(ref II)* or in SiRF binary protocol *(ref III)*. The module requires a main power supply VDD, which can be powered directly from a raw battery voltage. The Fastrax IT321 module interfaces to the customer's application via one serial port. Serial data and I/O signal levels are 1.8V or 1.2V CMOS compatible.

The antenna input supports passive and active antennas and provides also an internally generated antenna bias supply.

This document describes the electrical connectivity and main functionality of the Fastrax IT321 OEM GPS Receiver module.

1.1 Block diagram

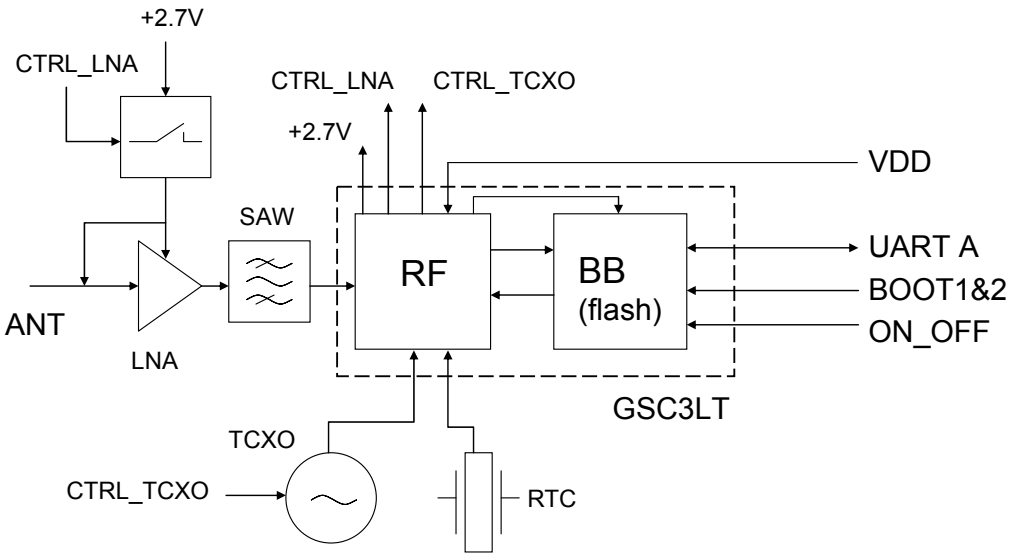


Figure 1 Block diagram

1.2 Frequency Plan

Clock frequencies generated internally at the Fastrax IT321 receiver:

- 32768 Hz real time clock (RTC)
- 16.369 MHz master clock (TCXO)
- 1571.424 MHz local oscillator of the RF down-converter

2. SPECIFICATIONS

2.1 General

Table 1 General Specifications

Receiver	GPS L1 C/A-code, SPS
Chip set & Navigation sensitivity	SiRF GSC3LT -159dBm
Channels	20 physical (12 in tracking, firmware limited)
Update rate	1 Hz default (fix rate configurable with SiRF TricklePower)
Supply voltage, VDD	+3.25V…+5.5 V (can be raw battery supply)
Supply voltage, VDD ripple max	300mVpp @ f<10kHz & 3mVpp @ f>100kHz
Power consumption, VDD	90 mW typical @ 3.3V (without Antenna bias)
Power consumption, VDD	65 uW typical @ 3.3V (during Hibernate state)
Antenna net gain range	0…+25dB (+10… +20dB suggested for optimum performance)
Antenna bias voltage	+2.7V (+0.3/-0.5V)
Antenna bias current	15 mA max
Storage temperature	-40ºC…+85ºC
Operating temperature (*note 1*)	-30ºC…+85ºC
Serial port configuration	NMEA (configurable to SiRF binary)
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed	4800 baud (configurable)
I/O signal levels, VCC = 1.8V or 1.2V	CMOS compatible: low state 0…0.25xVCC; high state 0.75…1.0xVCC
I/O sink/source capability	+/- 2 mA max.
PPS output	+/-1us accuracy

Note 1: Operation in the storage temperature range –40°C… +85°C is allowed but Time-to-First-Fix and other GPS performance may be degraded.

2.2 Absolute maximum ratings

Table 2 Absolute maximum ratings

Item	Min	Max	unit
Operating and storage temperature	-40	+85	ºC
Power dissipation	-	300	mW
Supply voltage, VDD	-0.3	+5.5	V
Input voltage on any input connection, VCC = 1.2V or 1.8V	-0.3	VCC+0.3V	V
RF input level	-	+15	dBm

3. OPERATION

3.1 Operating modes

After power up the IT321 module (with Flash version) boots from the internal ROM or from flash memory depending on the BOOT1 and BOOT2 control inputs (see Table 4).

With ROM code version the BOOT1 & 2 inputs can be left unconnected but the inputs GPIO6 & 2 determine baud rate and protocol selection (see Table 3). Modes of operation:

- Normal mode (Navigation)
    - Power management system modes
- Hibernate mode
- Programming mode

3.2 Normal mode

The IT321 receiver will start navigation automatically after power up using all (if any) aiding information on GPS time, satellite ephemeris and Last Known Good (LKG) position information provided by the non-volatile back up block (RTC & RAM). The power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as *Full Power* or *Navigation* state.

Navigation is available and any configuration settings are valid as long as the VDD power supply is active. When the VDD is powered off, settings are reset to factory configuration and receiver performs a cold start on next power up.

3.2.1 Output configuration

With ROM code version user can select the data output configuration by setting the GPIO 6 and 2, which are read at power up. Configuration is selected by setting GPIO 6 and 13 to low or high state according to the following table.

Table 3 Output configurations

Configuration	1	2	3
GPIO6 input	low	high	low
GPIO2 input	low	low	high
Protocol	NMEA 3.01	SiRF binary	NMEA 3.01
Baud rate	4800,n,8,1	57600,n,8,1	57600,n,8,1
NMEA messages @1s	GGA, GSA, GSV@5s, RMC, VTG	-	GGA, GSA, GSV, RMC, VTG, (EE)
Binary messages @1s		2, 4, 9, 13, 18, 41, (EE)	
GPIO1 output, no navigation	high	high	high
GPIO1 output, navigation	100ms high @ 1Hz	100ms high @ 1Hz	100ms high @ 1Hz
DGPS/SBAS	Disabled	Enabled	Enabled
Static navigation filter	Disabled	Disabled	Enabled
Track smoothing filter	Enabled	Enabled	Enabled
Internal DR	Disabled	Disabled	Enabled
Extended Ephemeris	Disabled	Enabled	Enabled

3.2.2 Power management system modes

The IT321 module supports also SiRF operating modes for reduced average power consumption (*ref III*) like Adaptive TricklePower™ and Push-to-Fix™ modes:

1. *Adaptive TricklePower:* In this mode the receiver stays at Full Power for 200… 900ms and provides a valid fix. Between fixes with 1… 10 sec interval the receiver stays in a low power mode to reduce power drain. TricklePower mode is configurable with

SiRF binary protocol message ID151 (*ref III*). The receiver stays once in while in Full Power automatically to collect new ephemeris and almanac data from rising satellites.

2. *Push-to-Fix*: In this mode the receiver is configured to wake up periodically, typically every 1800 sec, to collect new ephemeris data from rising satellites. Rest of the time the receiver stays in a low power mode. The host wakes up the receiver by ON_OFF control input interrupt (pulse low-high-low >62us) after which the receiver performs Hot start and a valid fix is available within few seconds. This mode is configurable with SiRF binary protocol message ID151 (*ref III*).

Note that position accuracy is somewhat degraded in power management modes when compared to full power operation.

3.3 Hibernate mode

Hibernate mode means a low quiescent power state where only the internal non-volatile RTC and RAM block is powered on. The main supply input VDD is kept active all the time, even during Hibernate mode. The Hibernate mode is entered by host interrupt at ON_OFF control input (pulse low-high-low >62us).

Other internal blocks like digital baseband and I/O block are internally powered off, thus output levels are at low state and any inputs, excluding ON_OFF input, like UART RXA should be disconnected or forced to low state.

The receiver wakes up from Hibernate mode and returns to Normal mode after next ON_OFF interrupt (pulse low-high-low >62us) allowing fast TTFF with either Hot or Warm start.

3.4 Programming mode

Programming mode is only available with the flash version (GSC3LTf) with the embedded 4Mbit flash memory. The ROM code version does not support programming.

Programming via HW-booting mode is utilized by forcing the BOOT1 and BOOT2 control inputs for high state (Flash programming, following table) during power up. Now the GPS module boots for the UART and waits for the boot loader commands from the host (an application running on the host, SiRFFlash). It is suggested that all applications using embedded flash version should support the HW-booting by ac-

cess to UART (TXA & RXA), BOOT1 and BOOT2 input signals and VDD On/Off control.

Note that during the flash update process the serial data speed is changed and thus the serial line connection should be a direct line to the host without any transferring utilities that may cause failure during speed change.

Table 4 BOOT modes

BOOT mode	**BOOT2** (internal pull up)	**BOOT1** (internal pull down)
Flash (Normal mode)	0	0
Reserved	0	1
Flash programming UART A	1	1
ROM (Normal mode) (Default)	1	0

3.5 Procedure for re-programming the flash firmware

1. Connect UART (RXA and TXA signals) to PC via RS232 converter.

2. Set the module to UART boot mode: Power up the module to Flash programming mode according to Table 4. when using Fastrax Evaluation kit power up the kit and toggle Prog/Reset switch to Prog position.

3. Start SiRFFlash application on PC.

4. Browse for the flash *.s file.

5. Check the Communication setting from the SiRFFlash to meet your PC serial port.

6. Press Execute at SiRFFlash. Now the flashing starts.

7. After flashing has finished, recover normal operation by toggling power VDD off-on and setting boot mode to Flash mode according to Table 4.

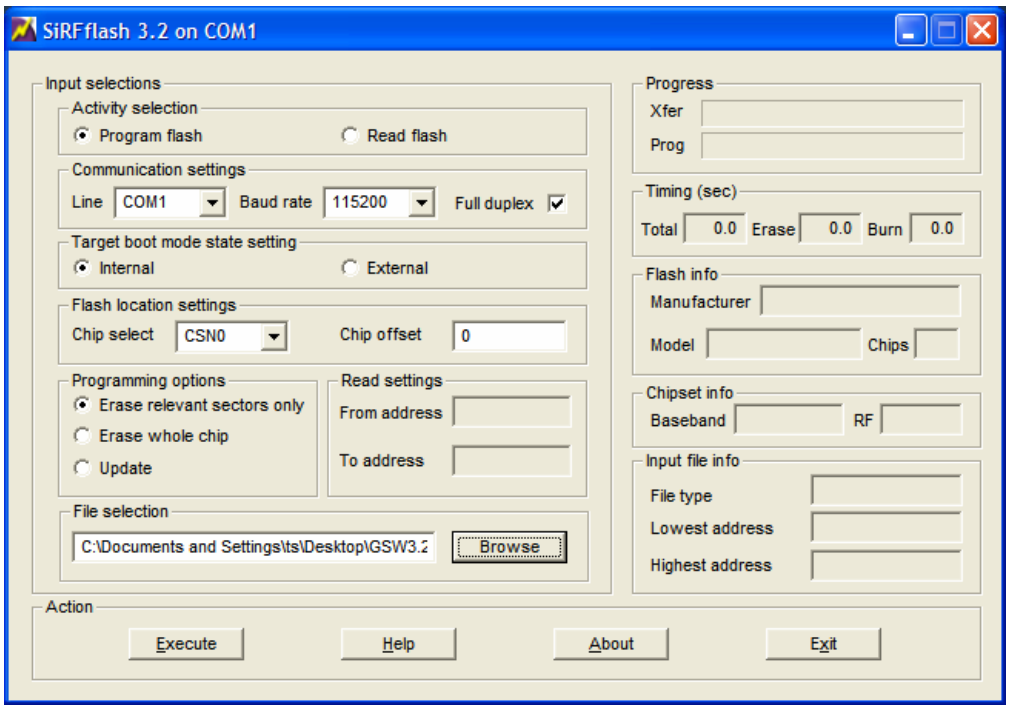


Figure 2 SiRFFlash utility settings

4. CONNECTIVITY

4.1 Connection assignments

The I/O connections are available as soldering pads on the bottom side of the module. These pads are also used to attach the module on the motherboard in application. All unconnected I/O should be left open (floating) unless instructed to use pull external up or pull down.

Table 5 Connections

Contact	Signal name	I/O	Alternative signal name	Signal description
1	ANT	I/O	-	Antenna signal input 50 ohm, Antenna bias voltage +2.7V output
2	GND	-	-	Ground
3	GND	-	-	Ground
4	GND	-	-	Ground
5	GND	-	-	Ground
6	GPIO6	I	-	Control input for protocol configuration. VCC=1.8V. For default pull low.
7	ON_OFF	I	-	Interrupt toggle (pulse low-high-low 100ms) for switching between Hibernate/Normal mode. VCC=1.2V. Pull to low state with e.g. 10kohm if not used.
8	GND	-	-	Ground
9	VDD	-	-	Power supply, can be raw battery voltage. Note ripple voltage spec.
10	BOOT1	I	-	BOOT select 1. Can be left unconnected with ROM version. With flash version connect to BOOT2 signal and pull low with R<5kohm. Has internal pull down resistor 100kohm. VCC=1.8V.

11	GND	-	-	Ground
12	TSYNC	I/O	GPIO8	Option for Timing pulse input in A-GPS version. Pull low when not used with e.g. 10kohm. VCC=1.8V.
13	GPIO2	I	-	Control input for protocol configuration. VCC=1.8V. For default pull low.
14	GND	-	-	Ground
15	GPIO1	O	-	Valid fix indicator output. Can be left unconnected. VCC=1.8V
16	ECLK	I	-	Option for external clock input in A-GPS version. Pull low state with e.g. 10kohm if not used. VCC=1.8V.
17	GND	-	-	Ground
18	RXA	I	-	UART A async. Input. Has internal pull up resistor 100kohm. VCC=1.8V.
19	TXA	O	-	UART A async. Output. VCC=1.8V.
20	PPS	O	-	1PPS signal output. VCC=1.8V.
21	GND	-	-	Ground
22	BOOT2	I	-	BOOT select 2. Can be left unconnected with ROM version. With flash version connect to BOOT1 signal and pull low with R<5kohm. Has internal pull up resistor 100kohm. VCC=1.8V.
23	GND	-	-	Ground
24	GND	-	-	Ground
Contact	Signal name	I/O	Alternative signal name	Signal description

4.2 Power supply

The IT321 module requires only one power supply VDD, which can be supplied directly from a battery since the module has internal regulators. Keep the supply active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Main power supply VDD current varies according to the processor load and satellite acquisition. Typical VDD peak current is 45mA during acquisition. Typical VDD current in low power Hibernate mode is 20uA.

The IT321 allows about 300mVpp ripple voltage at the supply VDD below 10kHz frequency. The ripple voltage should be reduced further at VDD supply below 3mVpp at 100kHz frequency or higher. E.g. if the battery that provides the supply for VDD is connected to a switched mode regulator operating at 100kHz, the resulting voltage ripple shall be reduced below 3mVpp by a suitable by-pass capacitor or by external low pass filter prior VDD supply input.

4.3 Configuration select: GPIO 6 & 2

The data output protocol configuration is defined using the GPIO 6 and 13 control inputs. After power up the value is read and the configuration is processed according the Table 3 (in previous chapter).

The GPIO 6&2 inputs should be kept valid after power up for at least 500 ms to allow the internal power-on-reset delay to settle. I/O levels are CMOS 1.8V compatible.

4.4 Boot Control inputs

The boot source is defined in the internal boot ROM sector by using the BOOT1 and BOOT2 control inputs. After power up the value is read and the boot is processed according the Table 4 (in previous chapter).

The BOOT inputs should be kept valid after power up for at least 500 ms to allow the internal power-on-reset delay to settle. I/O levels are CMOS 1.8V compatible.

NOTE

With ROM code version the BOOT inputs can left unconnected (floating) since internal pull ups are configured to ROM mode as default.

NOTE

With embedded flash version the BOOT1 and BOOT2 input can be connected to the same boot control source from host. Normal operation requires external pull-down resistors connected to the common input, e.g. 0 ohm… 4.7kohm.

4.5 ON_OFF control input

The ON_OFF control input can be used to control the receiver between Normal or Hibernate modes and also to generate interrupt in Push-to-Fix operation.

The ON_OFF interrupt is generated by a low-high-low toggle, which should be longer than 62us and less than 1s (suggestion is abt. 100ms pulse length). Input level is CMOS 1.2V compatible. Do not generate ON_OFF interrupts less than 1 sec intervals. Especially take care that any multiple switch bounce pulses are filtered out.

After power up the first ON_OFF interrupt sets the module to Hibernate mode. Next ON_OFF interrupt wakes up the module for Normal (Navigation) operation. Consequent ON_OFF interrupts switch the operation mode between Hibernate and Normal modes.

During Hibernate mode internal I/O supply is internally powered off, thus output levels are at low state and any inputs, excluding ON_OFF input, like UART RXA should be disconnected or forced to low state.

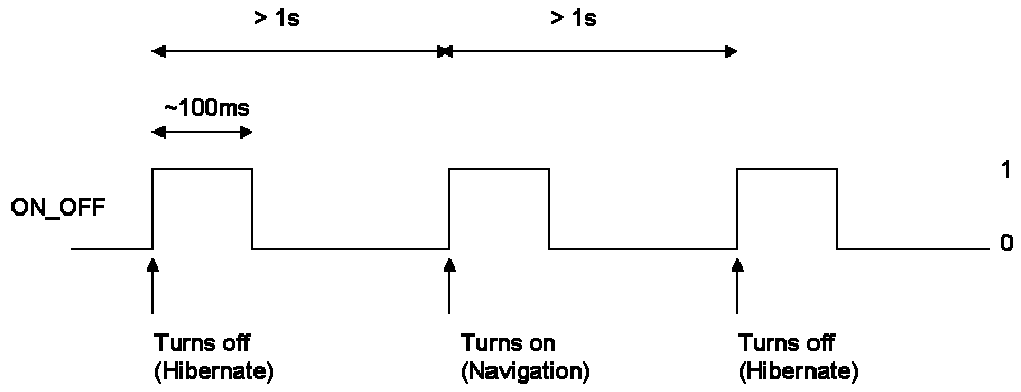


Figure 3 Suggested ON_OFF Hibernate control timing diagram.

NOTE

If not used, pull ON_OFF signal to low state with e.g. 10kohm pull down resistor.

If used, note that the input is CMOS 1.2V compatible. Use e.g. a resistive divider to reduce input voltage to 1.2V when using 1.8V or 3.3V host control source.

Do not generate multiple ON_OFF interrupts less than 1 sec intervals. Especially filter out multiple pulses generated by a mechanical switch bounce.

4.6 Antenna input

The module supports passive and active antennas. The antenna input impedance is 50 ohms. During Normal (navigating) operation, the input provides also a bias supply (+2.7V typ.). When the navigation is stopped, the antenna bias is switched off automatically.

NOTE

Passive antennas with a short-circuit to GND should be DC blocked externally with a 18pF…1nF serial capacitor.

4.6.1 Active GPS antenna

The customer may use an external active GPS antenna for e.g. in mobile or indoor usage. It is suggested the active antenna has a net gain *including cable loss* in the range from +10 dB to +25 dB.

NOTE

Max antenna bias current is 15mA. Antenna bias circuit has internal short circuit protection. At short circuit condition the antenna bias current is limited to abt. 60mA and the navigation data output will be stopped. Navigation will recover automatically when short circuit is removed.

4.7 UART

The device supports UART communication via one serial port A.

The default configuration for baud rates and respective protocols can be changed by commands via NMEA or SiRF binary protocols *(ref II & III)*. Any custom configuration stays active as long as supply VDD is active.

I/O levels form the serial port is CMOS 1.8V compatible, not RS232 compatible. Use an external level converter to provide CMOS 3.3V or RS232 levels when needed. The RXA input can be left unconnected when not needed since it has internal pull up resistor.

4.8 PPS

The pulse-per-second (PPS) output provides a pulse signal for timing purposes. Pulse length (high state) is about 1us synchronized to full UTC second. I/O level is CMOS 1.8V compatible.

4.9 ELCK

The ECLK is available optionally for external clock input with special ROM version for A-GPS frequency aiding. Pull down (e.g. 10kohm) if not used. I/O level is CMOS 1.8V compatible.

NOTE

Pull ECLK signal to low state e.g. with 10kohm resistor.

4.9.1 GPIO1 Valid fix indicator

GPIO1 is available as a valid fix indicator. Prior navigation the output stays at high state. During valid fix the output sends 100ms high state pulses at 1Hz rate. The I/O level is CMOS 1.8V compatible.

4.9.2 TSYNC/GPIO8

Optional input TSYNC input is intended for external time aiding with a special ROM version used for A-GPS. GPIO8 is available only for custom purposes with embedded flash version. I/O level is CMOS 1.8V compatible. Pull low with e.g. 10kohm when not used.

4.10 Mechanical dimensions and contact numbering

Module size is 10.4mm (width) x 14.0mm (length) x 2.3mm (height 2.6mm max). General tolerance is ±0.3mm.

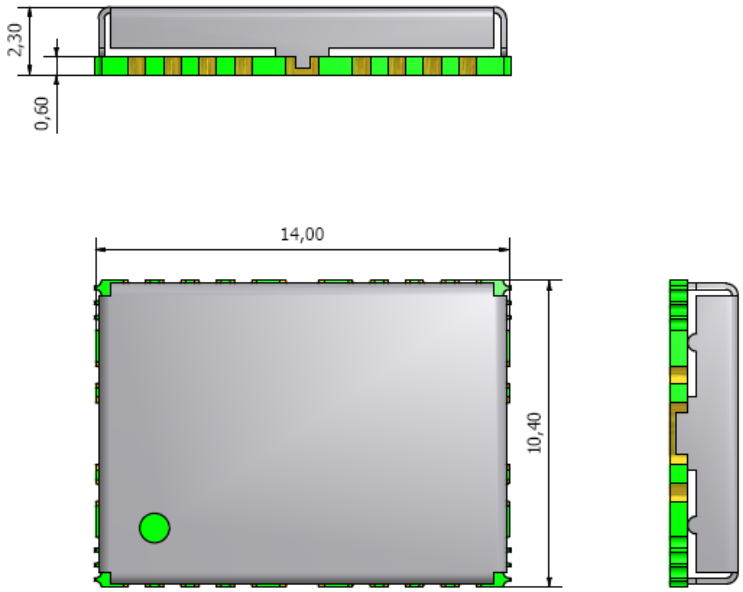


Figure 4 Dimensions

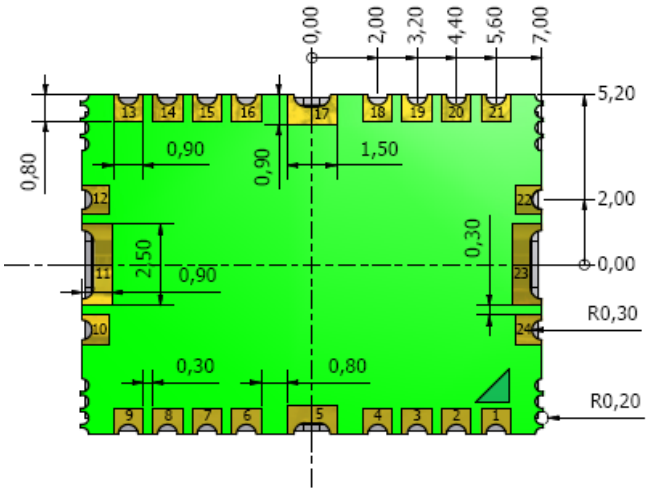


Figure 5 I/O pad numbering and dimensions, bottom view.

4.11 Suggested pad layout and pin out

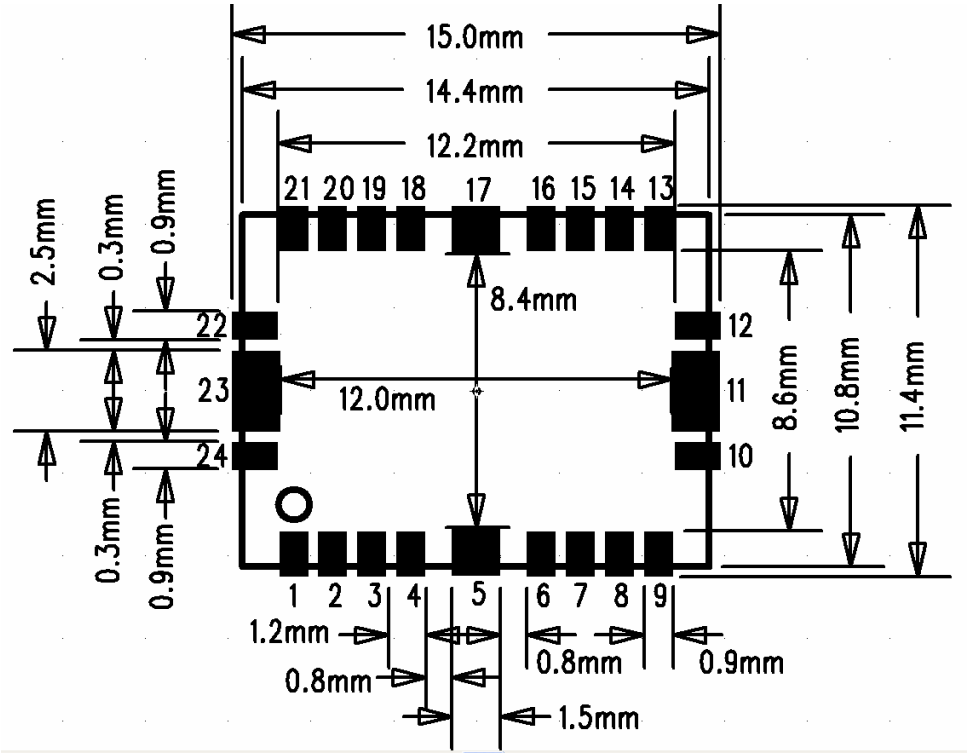


Figure 6 Suggested pad layout, occupied area and pin out, top view.

5. MANUFACTURING

5.1 Assembly

The IT321 module supports only assembly and soldering in a reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume.

5.2 Suggested Reflow soldering profile

Suggested peak reflow temperature is 250C for ten seconds (Pb-free paste). Absolute max reflow temperature is 260C for ten seconds.

5.3 Moisture sensitivity

Note that the IT321 is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be re-packed or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

5.4 Tape and reel

One reel contains 500, 1000, or 1500 modules.

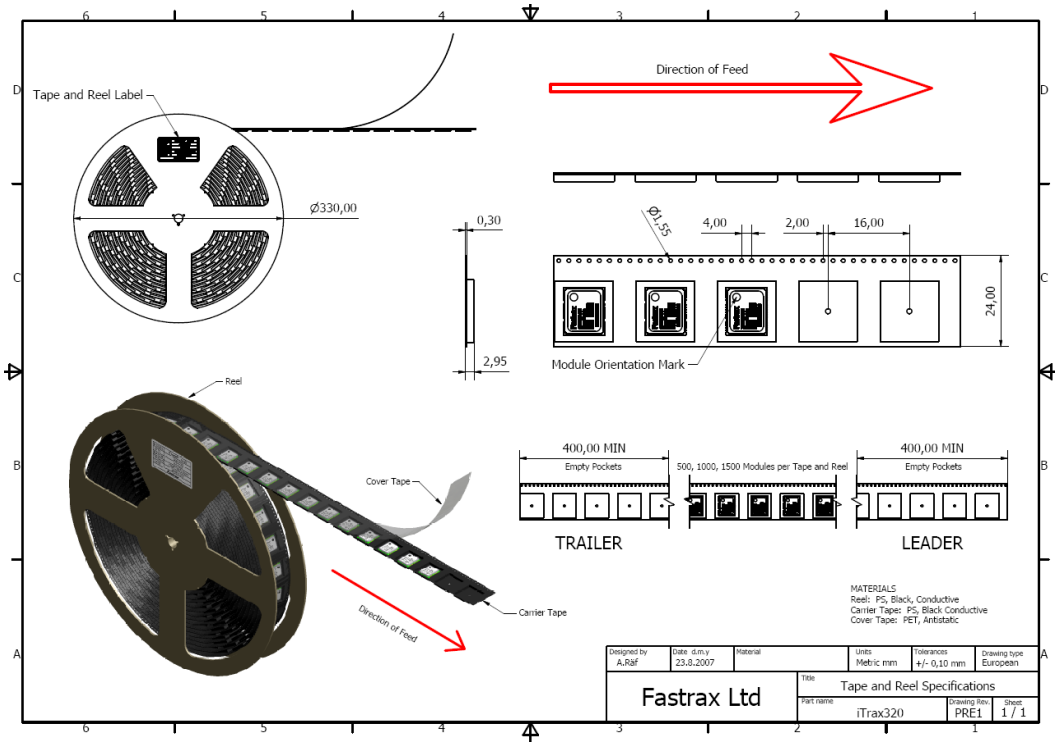


Figure 7 Tape and reel specification

6. REFERENCE DESIGN

The idea of the reference design is to give a guideline for the applications using the OEM GPS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing the GPS receiver in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB layout itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

6.1 Reference circuit diagram

The following picture describes a minimum connectivity for a typical autonomous navigation application. It consists of the IT321 module, which is powered by the main VDD supply (+3.3V… +5.5V). The VDD supply can be raw battery connection given that the VDD ripple voltage specification is not exceeded. With a high ripple power supply use an external by-pass capacitor(s) or a low pass filter for VDD supply input.

Serial port TXA is connected to host UART input. RXA connection to host UART output is required when sending commands to IT321.

Optional connectivity for host includes PPS signal for timing purposes, BOOT control inputs for e.g. re-programming the firmware with flash version and ON_OFF control input for Normal/Hibernate (ON/OFF) mode control.

No back up supply is required. Instead keep the main supply VDD active all the time and use the ON_OFF control input to switch between Navigation and Hibernate operation mode.

Note that all I/O signal levels are CMOS 1.8V compatible, except ON_OFF input, which is CMOS 1.2V compatible.

Standard operation does not support ELCK or Timesync operation and these inputs should be pulled to low state.

Note that there is a DC bias voltage present at the RF input, when the module is operating in Navigating mode. If a passive antenna with a short-circuit to the GND is used, an external series DC block capacitor (18pF…1nF) must be used for the antenna input.

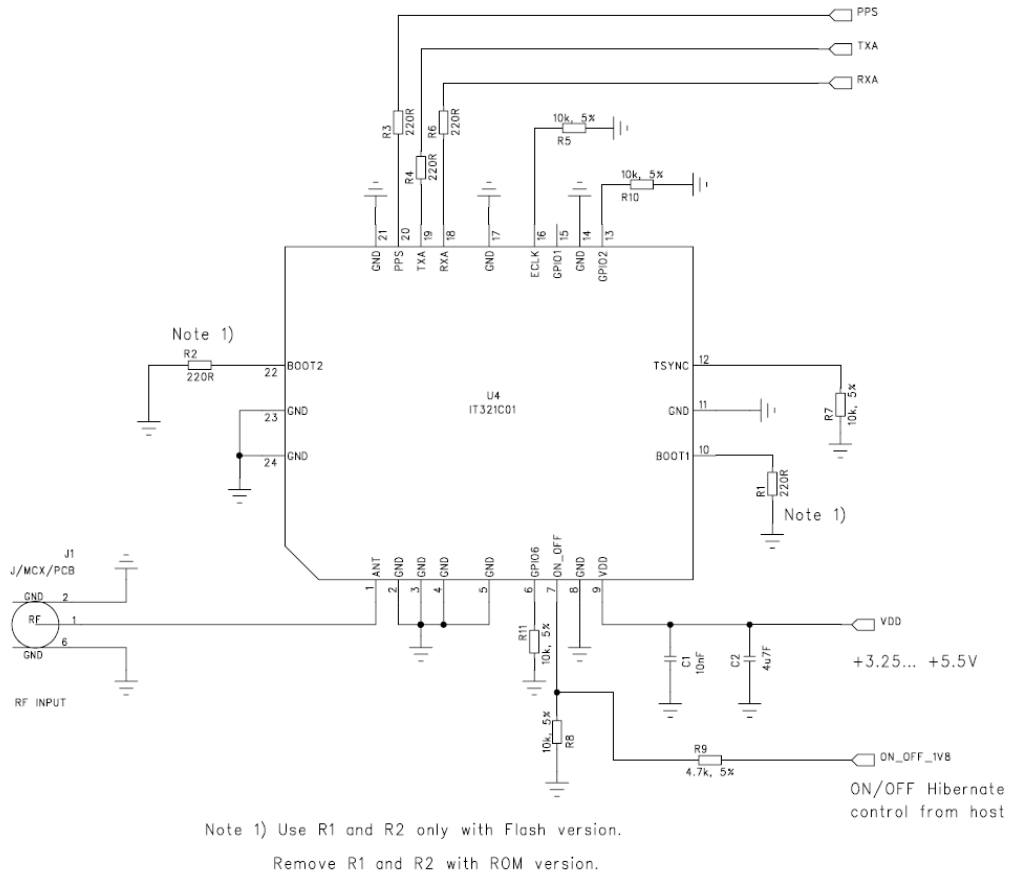


Figure 8 Reference Circuit Drawing

6.2 PCB layout issues

The suggested 4-layer PCB build up is presented in the following table.

Table 6 Suggested PCB build up

Layer	Description
1	Signal + Ground with copper keep-out below IT321
2	Ground plane
3	Signals

4	Ground plane

Routing signals directly under the module should be avoided. This area should be dedicated to keep-out to both traces and to ground (copper), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first inner layer below the IT321 is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should placed very near to the IT321 module. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C1 and C2 should be connected very close to the module with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the IT321 to ground plane with short traces to via holes, which are connected to the ground plane. Use preferably two via holes for each GND pad.

The RF input should be routed clearly away form other signals, this minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

7. IT321 APPLICATION BOARD

The Fastrax IT321 Application Board provides the IT321 connectivity to the Fastrax Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the IT321 module, a controllable switch for VDD supply, a 1.8V regulator, a 4 channel level translator for 1.8V I/O to 3.3V conversion, an MCX antenna connector, and a 2x20 pin Card Terminal connector.

7.1 Card Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the Fastrax Evaluation Kit pin header J4. Note that UART Port A maps to serial Port 0 at the Fastrax Evaluation Kit. I/O signal levels are CMOS 3.3V compatible unless stated otherwise.

Table 7 IT321 Application Board connectivity

Pin	Signal name	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit
1	-	-	-	Not connected
2	GND	-	-	Ground
3	-	-	-	Not connected
4	GND	-	-	Ground
5	TXA_CON	O	-	UART 0 async. output
6	GND	-	-	Ground
7	RXA_CON	I	-	UART 0 async. input
8	GND	-	-	Ground
9	VDD_CON	I	-	Power supply input +3.3V
10	GND	-	-	Ground
11	PPS_CON	O	-	1PPS signal output
12	GND	-	-	Ground
13	XRESET_CON	I	-	Active low async. system reset used to switch VDD supply
14	-	-	-	Not connected

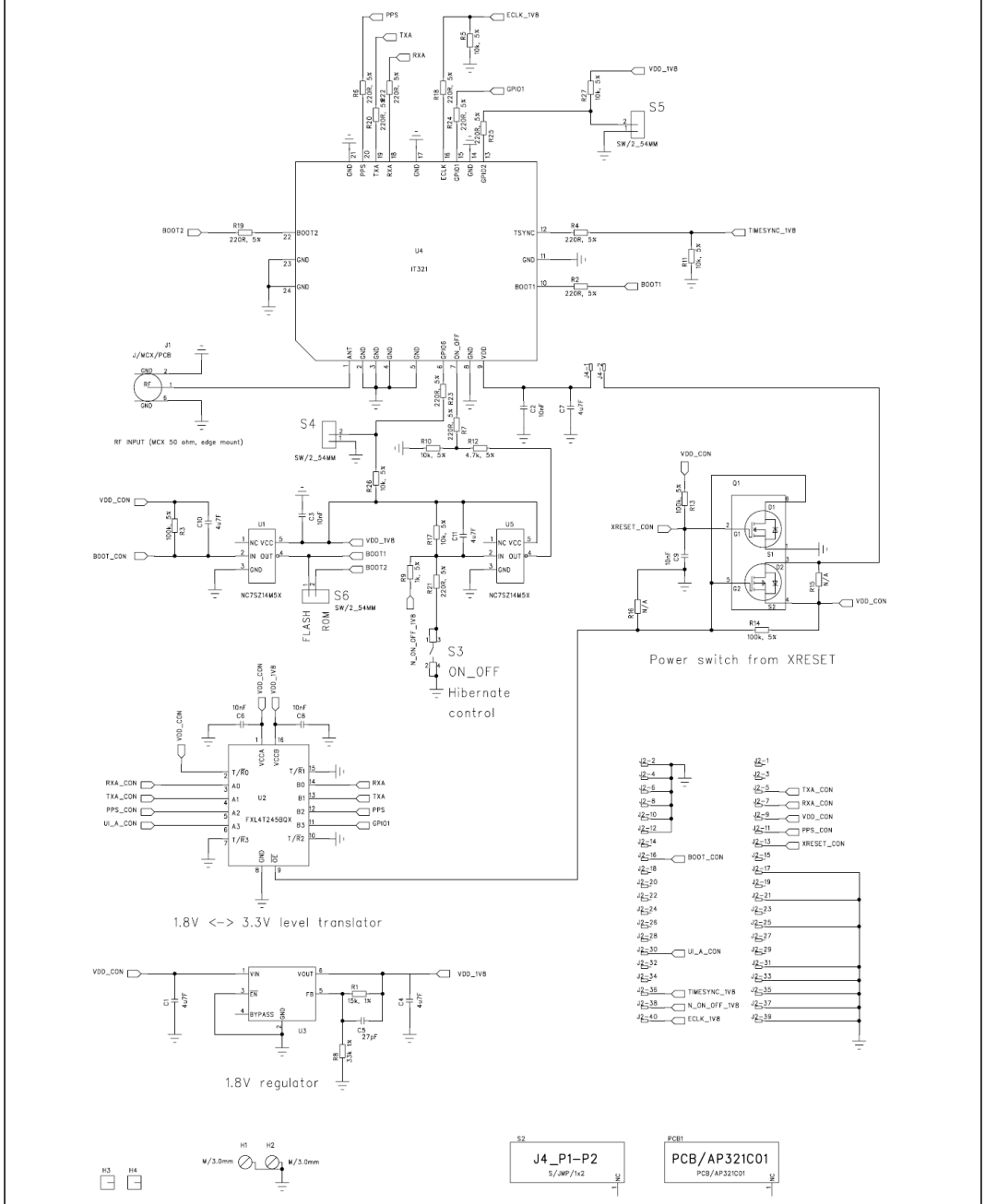
15	-	-	-	Not connected
16	BOOT_CON	I	-	Boot Select UART/Flash
17	GND	-	-	Ground
18	-	-	-	Not connected
19	-	-	-	Not connected
20	-	-	-	Not connected
21	GND	-	-	Ground
22	-	-	-	Not connected
23	-	-	-	Not connected
24	-	-	-	Not connected
25	GND	-	-	Ground
26	-	-	-	Not connected
27	-	-	-	Not connected
28	-	-	-	Not connected
29	-	-		Not connected
30	UI_A_CON	O	GPIO1	UI indicator A output
31	GND	-	-	Ground
32	-	-	-	Not connected
33	GND	-	-	Ground
34	-	-	-	Not connected
35	GND	-	-	Ground
36	TIMESYNC_1V8	I	GPIO8	Timesync timing input, VCC 1.8V
37	GND	-	-	Ground
38	N_ON_OFF_1V8	I	-	Inverted ON_OFF control input, VCC 1V8
39	GND	-	-	Ground
40	ECLK_1V8	I	-	ECLK clock input, VCC 1.8V
Pin	Signal name	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit

7.2 Bill of materials, PCB rev C

Reference	Part Name	Description
C5	27pF	Capacitor chip, 27pF 50V 5% NP0 0402
C2-3 C6 C8-9	10nF	10nF 50V 10% X7R 0402
C1 C4 C7 C10-11	4u7F	4,7uF 6,3V X5R 0805 +20%
H3-4	FIDUCIAL	FIDUCIAL, Circle, rectangle, triangle
H1-2	HOLE	HOLE 3.2mm
U4	IT321	IT321 MODULE
J4	1x2P2.54	1x2 pin-header, straight, pitch 2.54mm
J2	2x20 edge	EDGE MOUNT SOCKET STRIP 40 PINS
J1	CON/MCX	50 Ohm male MCX connector PCB
PCB1	PCB/AP321C01	PCB AP321C01
Q1	FDG6321C	TRANSISTOR Dual P/N FET FDG6321C SOT323
R15-16	N/A	Resistor chip, 0R 0402
R3 R13-14	100k, 5%	Resistor chip, 100k 5% 0402 63mW
R5 R10-11 R17 R26-27	10k, 5%	Resistor chip, 10k 5% 0402 63mW
R1	15k, 1%	Resistor chip, 15k 1% 0402 63mW
R9	1k, 5%	Resistor chip, 1k 5% 0402 63mW
R2 R4 R6-7 R18-25	220R, 5%	Resistor chip, 220R 5% 0402 63mW
R8	33k 1%	Resistor chip, 33k 1% 0402 63mW
R12	4.7k, 5%	Resistor chip, 4.7k 5% 0402 63mW
S2	J4_P1-P2	Jumper, Pitch, 2.54mm, Red colour
S4-6	SW JMP 2P54	Switch, on-off
S3	SW	Switch, SMD PUSH BUTTON
U2	FXL4T245BQX	Dual supply 4 bit translator
U1 U5	NC7SZ14M5X	Schmit-Trigger inverter
U3	TPS79101	REGULATOR TPS79101

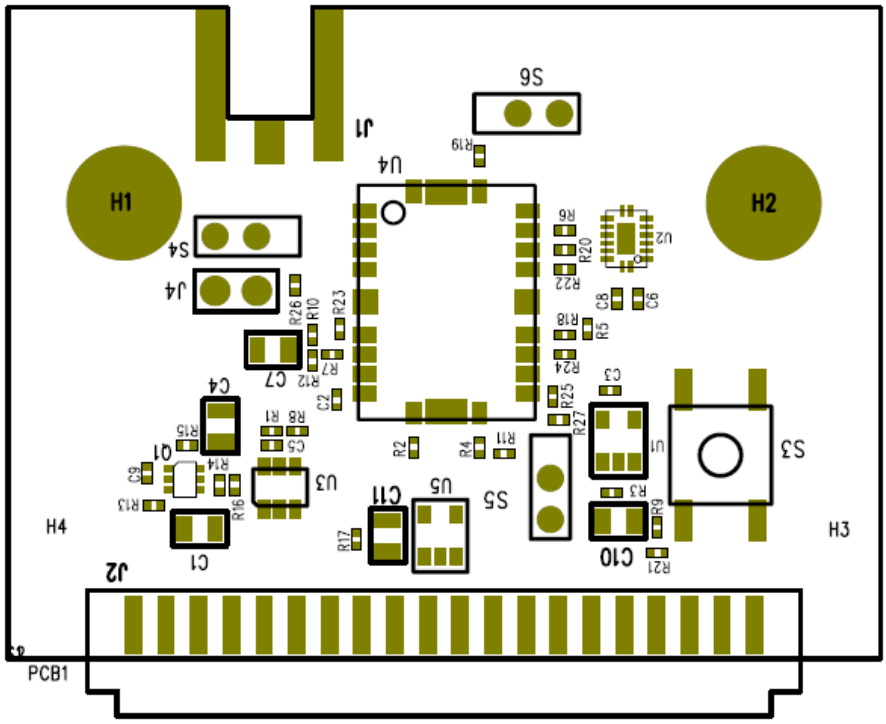
7.3 Circuit drawing, rev C

Ltr	Qty	Change	Reason / ECO no	Design	Date Review	Date Appr
C		Added GPIO6 & 13 config, UI_A and ON_OFF control		TS		
C02		Changed GPIO13 to GPIO2 (silk screen labels)		TS		

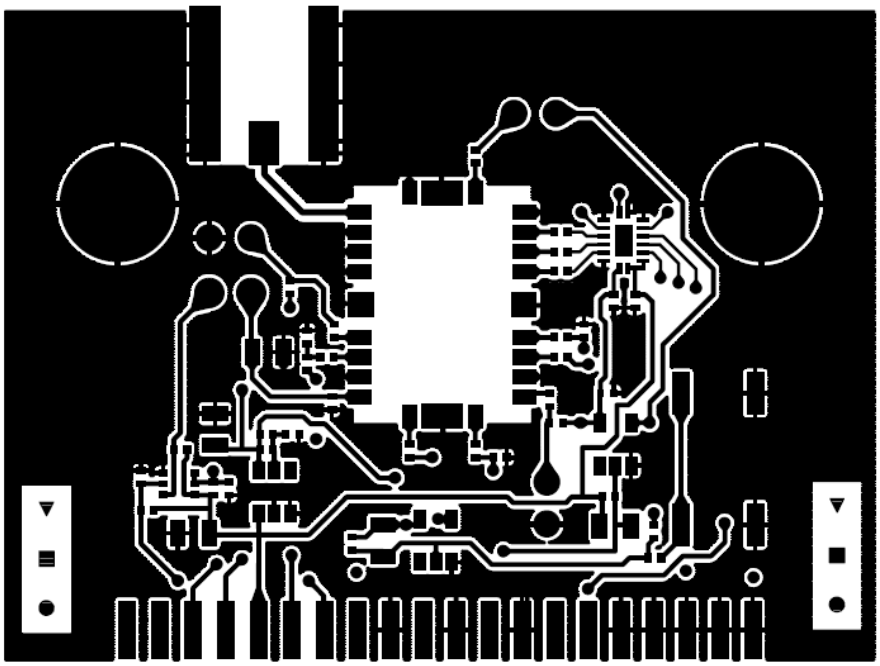


Drawn 2007-11-09	Arch Id F	Serial no	Sheet 1/1	Cooperator's doc no
Review				
Appr				
Design TS	Scale 1:1	Application Board IT321	FASTRAX	
Replaces		CIRCUIT DIAGRAM	Dwg no AP321C02	Rev C
Replaced by				

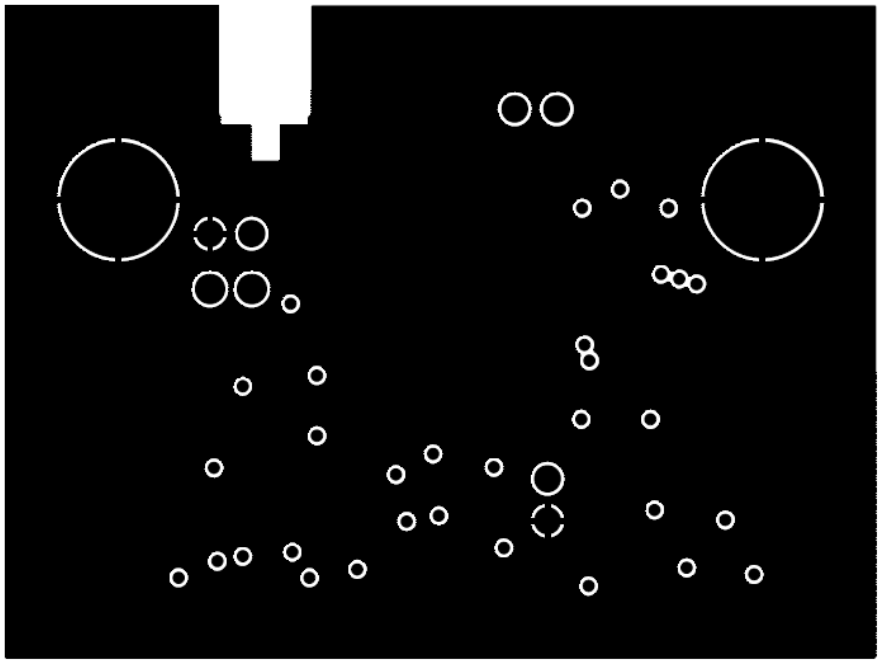
7.4 Assembly drawing, Top side, rev C



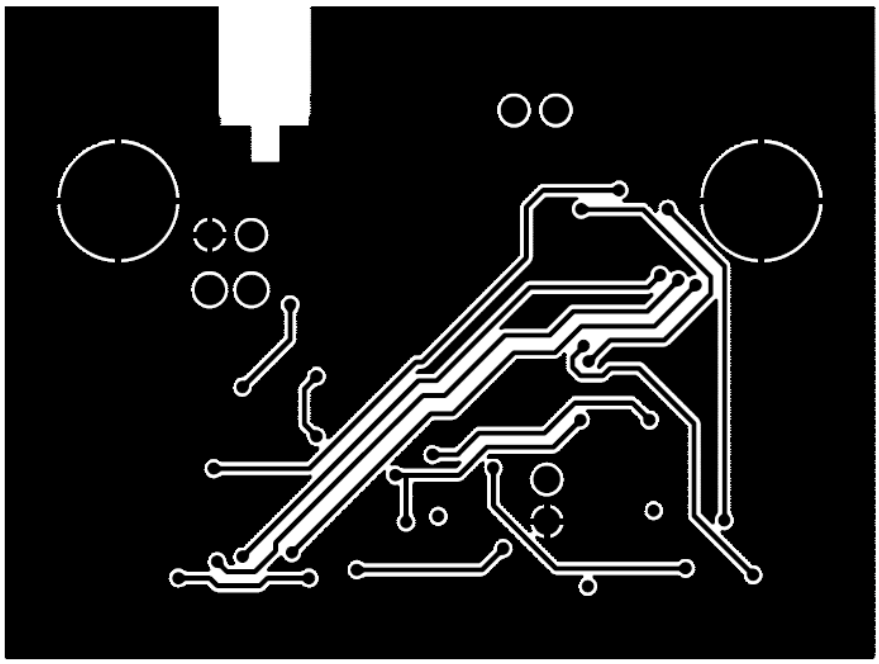
7.5 Artwork, layer 1 (Top), rev C



7.6 Artwork, layer 2, rev C



7.7 Artwork, layer 3, rev C



7.8 Artwork, layer 4 (Bottom), rev C