16-/14-/12-Bit Rail-to-Rail DACs with I²C Interface

FEATURES

- **Smallest Pin-Compatible Single DACs:**
  LTC2606: 16 Bits
  LTC2616: 14 Bits
  LTC2626: 12 Bits
- **Guaranteed 16-Bit Monotonic Over Temperature**
- **27 Selectable Addresses**
- 400kHz I²C Interface
- Wide 2.7V to 5.5V Supply Range
- Low Power Operation: 270μA at 3V
- Power Down to 1μA, Max
- High Rail-to-Rail Output Drive (±15mA, Min)
- Double-Buffered Data Latches
- Asynchronous DAC Update Pin
- LTC2606/LTC2616/LTC2626: Power-On Reset to Zero Scale
- LTC2606-1/LTC2616-1/LTC2626-1: Power-On Reset to Mid-Scale
- Tiny (3mm × 3mm) 10-Lead DFN Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

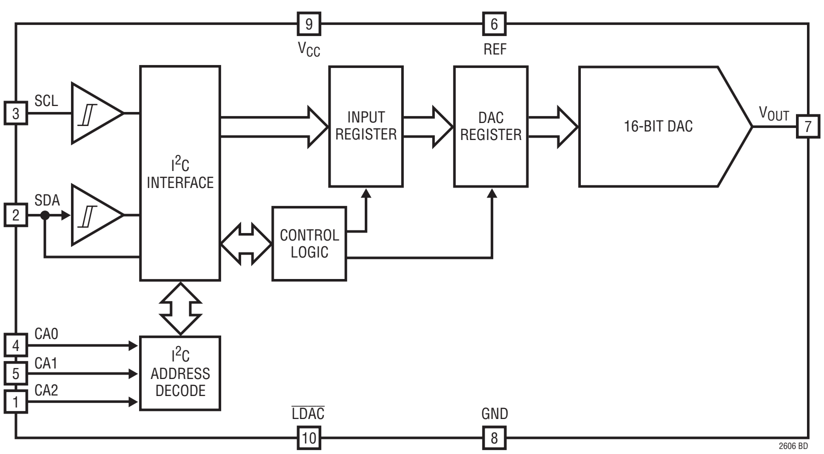
The LTC®2606/LTC2616/LTC2626 are single 16-, 14- and 12-bit, 2.7V-to-5.5V rail-to-rail voltage output DACs in a 10-lead DFN package. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish new board-density benchmarks for 16- and 14-bit DACs and advance performance standards for output drive and load regulation in single-supply, voltage-output DACs.

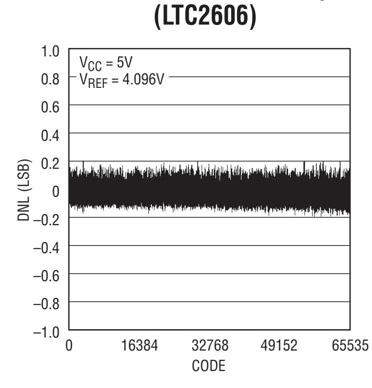
The parts use a 2-wire, I²C compatible serial interface. The LTC2606/LTC2616/LTC2626 operate in both the standard mode (clock rate of 100kHz) and the fast mode (clock rate of 400kHz). An asynchronous DAC update pin ($\overline{\text{LDAC}}$) is also included.

The LTC2606/LTC2616/LTC2626 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale; and after power-up, they stay at zero scale until a valid write and update take place. The power-on reset circuit resets the LTC2606-1/LTC2616-1/LTC2626-1 to mid-scale. The voltage outputs stay at mid-scale until a valid write and update take place.

TYPICAL APPLICATION



Differential Nonlinearity (LTC2606)



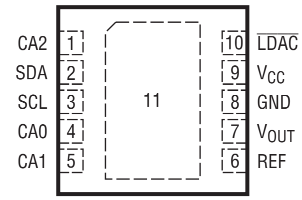
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Any Pin to GND .... –0.3V to 6V
Any Pin to V_{CC} .... –6V to 0.3V
Maximum Junction Temperature........................... 125°C
Storage Temperature Range................... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C
Operating Temperature Range:
  LTC2606C/LTC2616C/LTC2626C
  LTC2606-1C/LTC2616-1C/LTC2626-1C ...... 0°C to 70°C
  LTC2606I/LTC2616I/LTC2626I
  LTC2606-1I/LTC2616-1I/LTC2626-1I......–40°C to 85°C

PIN CONFIGURATION

TOP VIEW



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2606CDD#PBF	LTC2606CDD#TRPBF	LAJX	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2606IDD#PBF	LTC2606IDD#TRPBF	LAJX	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2606CDD-1#PBF	LTC2606CDD-1#TRPBF	LAJW	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2606IDD-1#PBF	LTC2606IDD-1#TRPBF	LAJW	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2616CDD#PBF	LTC2616CDD#TRPBF	LBPQ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2616IDD#PBF	LTC2616IDD#TRPBF	LBPQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2616CDD-1#PBF	LTC2626CDD-1#TRPBF	LBPR	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2616IDD-1#PBF	LTC2626IDD-1#TRPBF	LBPR	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2626CDD#PBF	LTC2626CDD#TRPBF	LBPS	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2626IDD#PBF	LTC2626IDD#TRPBF	LBPS	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2626CDD-1#PBF	LTC2626CDD-1#TRPBF	LBPT	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2626IDD-1#PBF	LTC2626IDD-1#TRPBF	LBPT	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LEAD FREE FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2606CDD	LTC2606CDD#TR	LAJX	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2606IDD	LTC2606IDD#TR	LAJX	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2606CDD-1	LTC2606CDD-1#TR	LAJW	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2606IDD-1	LTC2606IDD-1#TR	LAJW	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2616CDD	LTC2616CDD#TR	LBPQ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2616IDD	LTC2616IDD#TR	LBPQ	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2616CDD-1	LTC2616CDD-1#TR	LBPR	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2616IDD-1	LTC2616IDD-1#TR	LBPR	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2626CDD	LTC2626CDD#TR	LBPS	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2626IDD	LTC2626IDD#TR	LBPS	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2626CDD-1	LTC2626CDD-1#TR	LBPT	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2626IDD-1	LTC2626IDD-1#TR	LBPT	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2626/LTC2626-1 MIN	TYP	MAX	LTC2616/LTC2616-1 MIN	TYP	MAX	LTC2606/LTC2606-1 MIN	TYP	MAX	UNITS
DC Performance													
	Resolution		●	12			14			16			Bits
	Monotonicity	(Note 2)	●	12			14			16			Bits
DNL	Differential Nonlinearity	(Note 2)	●			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	(Note 2)	●		±1	±4		±4	±16		±14	±64	LSB
	Load Regulation	V_{REF} = V_{CC} = 5V, Mid-Scale I_{OUT} = 0mA to 15mA Sourcing I_{OUT} = 0mA to 15mA Sinking	 ● ●		 0.025 0.05	 0.125 0.125		 0.1 0.2	 0.5 0.5		 0.5 0.7	 2 2	 LSB/mA LSB/mA
		V_{REF} = V_{CC} = 2.7V, Mid-Scale I_{OUT} = 0mA to 7.5mA Sourcing I_{OUT} = 0mA to 7.5mA Sinking	 ● ●		 0.05 0.1	 0.25 0.25		 0.2 0.4	 1 1		 0.9 1.5	 4 4	 LSB/mA LSB/mA
ZSE	Zero-Scale Error	Code = 0	●		1	9		1	9		1	9	mV
V_{OS}	Offset Error	(Note 5)	●		±1	±9		±1	±9		±1	±9	mV
	V_{OS} Temperature Coefficient				±5			±5			±5		μV/°C
GE	Gain Error		●		±0.1	±0.7		±0.1	±0.7		±0.1	±0.7	%FSR
	Gain Temperature Coefficient				±8.5			±8.5			±8.5		ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), V_{OUT} unloaded, unless otherwise noted. (Note 11)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSR	Power Supply Rejection	V_{CC} = ±10%			–81		dB
R_{OUT}	DC Output Impedance	V_{REF} = V_{CC} = 5V, Mid-Scale; –15mA ≤ I_{OUT} ≤ 15mA V_{REF} = V_{CC} = 2.7V, Mid-Scale; –7.5mA ≤ I_{OUT} ≤	● ●		0.05 0.06	0.15 0.15	Ω Ω
I_{SC}	Short-Circuit Output Current	V_{CC} = 5.5V, V_{REF} = 5.5V Code: Zero-Scale; Forcing Output to V_{CC} Code: Full-Scale; Forcing Output to GND	 ● ●	 15 15	 34 36	 60 60	 mA mA
		V_{CC} = 2.7V, V_{REF} = 2.7V Code: Zero-Scale; Forcing Output to V_{CC} Code: Full-Scale; Forcing Output to GND	 ● ●	 7.5 7.5	 22 29	 50 50	 mA mA
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Normal Mode	●	88	124	160	kΩ
	Capacitance				15		pF
I_{REF}	Reference Current, Power Down Mode	DAC Powered Down	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3) V_{CC} = 3V (Note 3) DAC Powered Down (Note 3) V_{CC} = 5V DAC Powered Down (Note 3) V_{CC} = 3V	● ● ● ●		0.340 0.27 0.35 0.10	0.5 0.4 1 1	mA mA µA µA
Digital I/O (Note 11)							
V_{IL}	Low Level Input Voltage (SDA and SCL)		●	–0.5		$0.3V_{CC}$	V
V_{IH}	High Level Input Voltage (SDA and SCL)	(Note 8)	●	$0.7V_{CC}$			V
$V_{IL(\overline{LDAC})}$	Low Level Input Voltage ($\overline{LDAC}$)	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 5.5V	● ●			0.8 0.6	V V
$V_{IH(\overline{LDAC})}$	High Level Input Voltage ($\overline{LDAC}$)	V_{CC} = 2.7V to 5.5V V_{CC} = 2.7V to 3.6V	● ●	2.4 2.0			V V
$V_{IL(CAn)}$	Low Level Input Voltage on CA*n* (*n* = 0, 1, 2)	See Test Circuit 1	●			$0.15V_{CC}$	V
$V_{IH(CAn)}$	High Level Input Voltage on CA*n* (*n* = 0, 1, 2)	See Test Circuit 1	●	$0.85V_{CC}$			V
R_{INH}	Resistance from CA*n* (*n* = 0, 1, 2) to V_{CC} to Set CA*n* = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CA*n* (*n* = 0, 1, 2) to GND to Set CA*n* = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA*n* (*n* = 0, 1, 2) to V_{CC} or GND to Set CA*n* = Float	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current = 3mA	●	0		0.4	V
t_{OF}	Output Fall Time	V_O = $V_{IH(MIN)}$ to V_O = $V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 9)	●	20 + $0.1C_B$		250	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	$0.1V_{CC}$ ≤ V_{IN} ≤ $0.9V_{CC}$	●			1	µA
C_{IN}	I/O Pin Capacitance	(Note 4)	●			10	pF
C_B	Capacitive Load for Each Bus Line		●			400	pF
C_{CAX}	External Capacitive Load on Address Pins CA*n* (*n* = 0, 1, 2)		●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF = 4.096V (V_{CC} = 5V), REF = 2.048V (V_{CC} = 2.7V), V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC2626/LTC2626-1 MIN	TYP	MAX	LTC2616/LTC2616-1 MIN	TYP	MAX	LTC2606/LTC2606-1 MIN	TYP	MAX	UNITS
AC Performance												
t_S	Settling Time (Note 6)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		7			7 9			7 9 10		µs µs µs
	Settling Time for 1LSB Step (Note 7)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		2.7			2.7 4.8			2.7 4.8 5.2		µs µs µs
	Voltage Output Slew Rate			0.75			0.75			0.75		V/µs
	Capacitive Load Driving			1000			1000			1000		pF
	Glitch Impulse	At Mid-Scale Transition		12			12			12		nV•s
	Multiplying Bandwidth			180			180			180		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz		120 100			120 100			120 100		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz		15			15			15		μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Figure 1) (Notes 10, 11)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 2.7V to 5.5V							
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time of Both SDA and SCL Signals	(Note 9)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time of Both SDA and SCL Signals	(Note 9)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs
t_1	Falling Edge of 9th Clock of the 3rd Input Byte to $\overline{\text{LDAC}}$ High or Low Transition		●	400			ns
t_2	$\overline{\text{LDAC}}$ Low Pulse Width		●	20			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Linearity and monotonicity are defined from code k_L to code $2^N - 1$, where N is the resolution and k_L is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For V_{REF} = 4.096V and N = 16, k_L = 256 and linearity is defined from code 256 to code 65,535.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: Guaranteed by design and not production tested.

Note 5: Inferred from measurement at code 256 (LTC2606/LTC2606-1), code 64 (LTC2616/LTC2616-1) or code 16 (LTC2626/LTC2626-1) and at full-scale.

Note 6: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped 1/4-scale to 3/4-scale and 3/4-scale to 1/4-scale. Load is 2k in parallel with 200pF to GND.

Note 7: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped ±1LSB between half scale and half scale – 1. Load is 2k in parallel with 200pF to GND.

Note 8: Maximum $V_{IH} = V_{CC(MAX)} + 0.5V$

Note 9: C_B = capacitance of one bus line in pF.

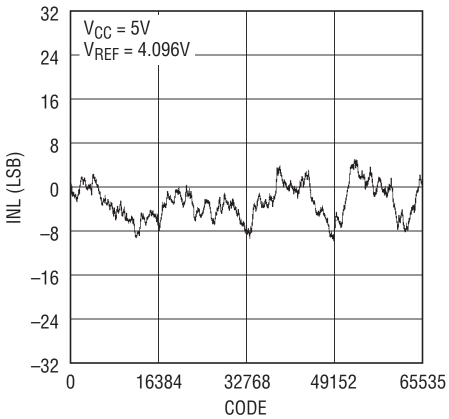
Note 10: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 11: These specifications apply to LTC2606/LTC2606-1, LTC2616/LTC2616-1, LTC2626/LTC2626-1.

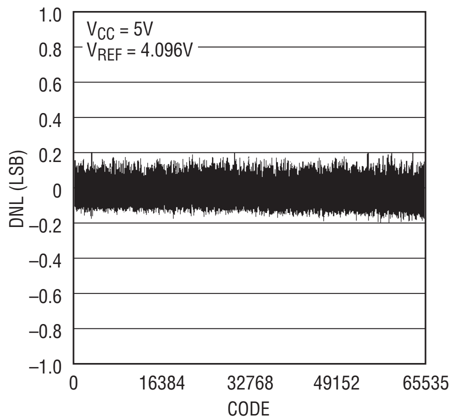
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2606

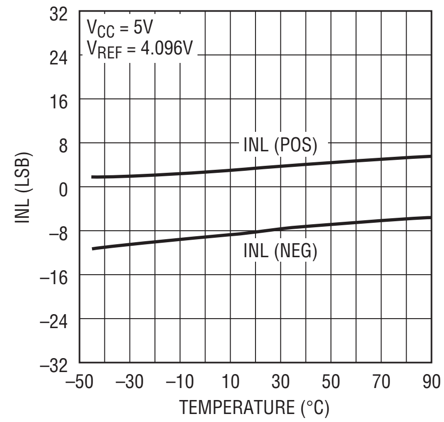
Integral Nonlinearity (INL)



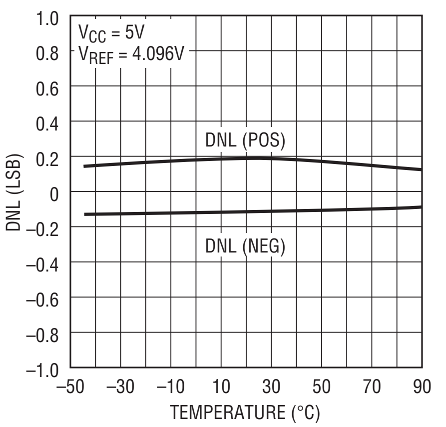
Differential Nonlinearity (DNL)



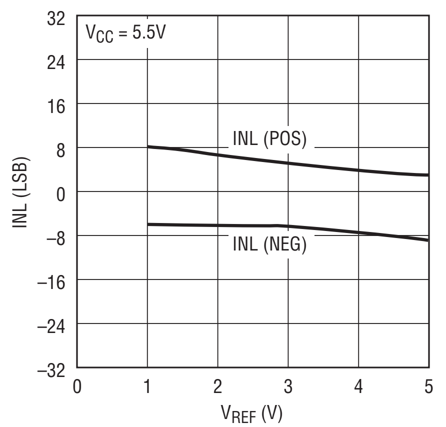
INL vs Temperature



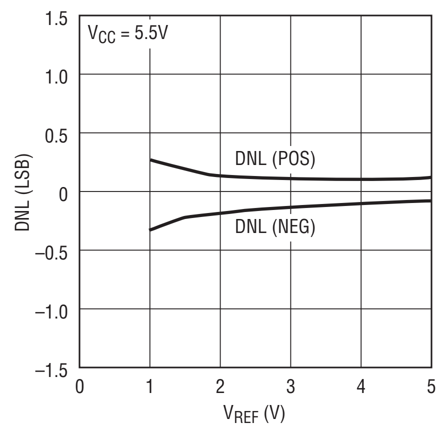
DNL vs Temperature



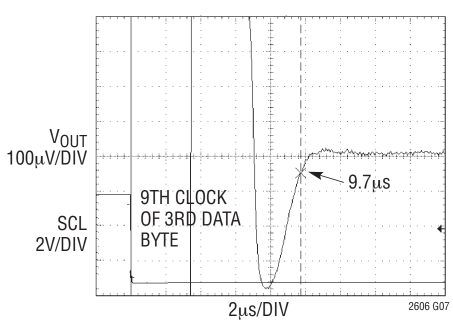
INL vs V_{REF}



DNL vs V_{REF}

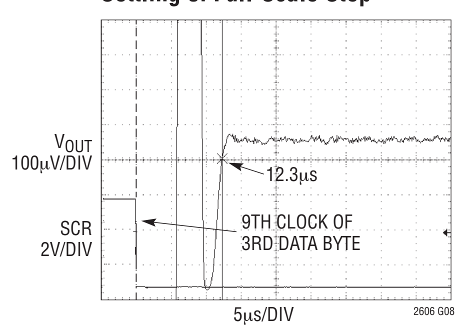


Settling to ±1LSB



V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

Settling of Full-Scale Step

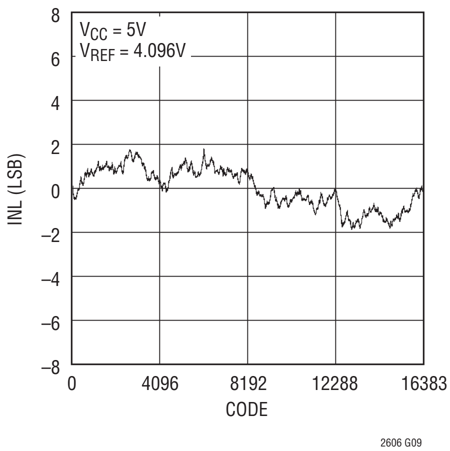


SETTLING TO ±1LSB
V_{CC} = 5V, V_{REF} = 4.096V
CODE 512 TO 65535 STEP
AVERAGE OF 2048 EVENTS

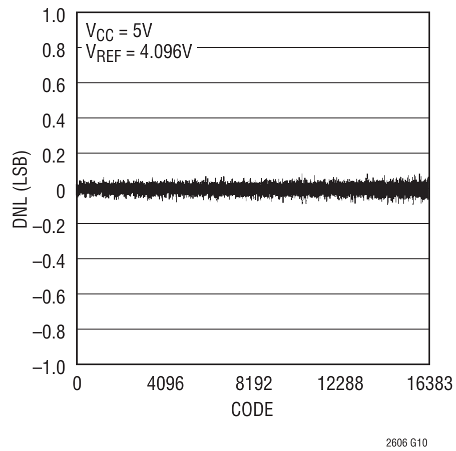
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2616

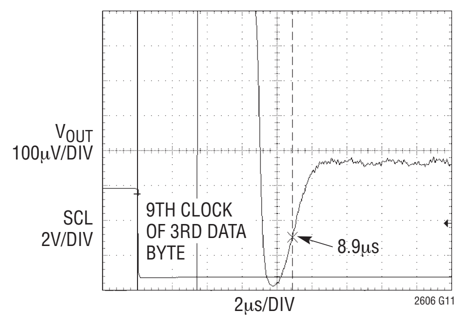
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



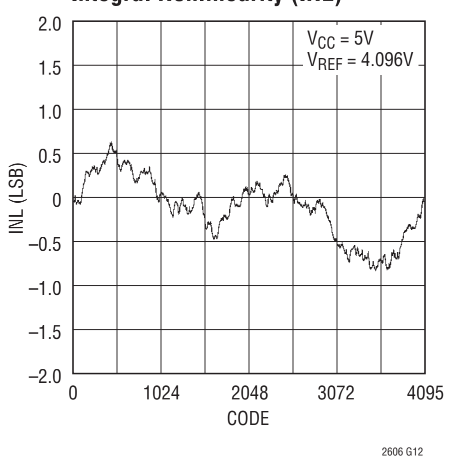
Settling to ±1LSB



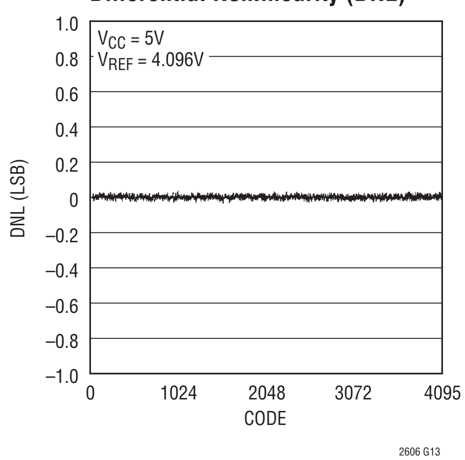
V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

LTC2626

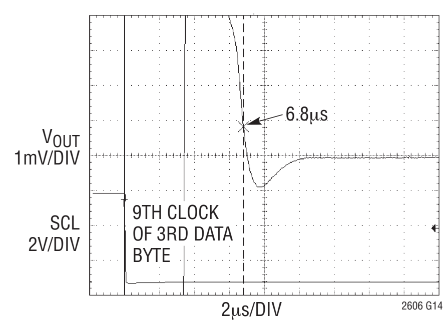
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



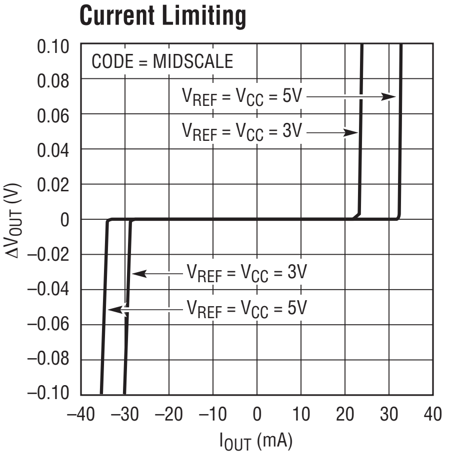
Settling to ±1LSB



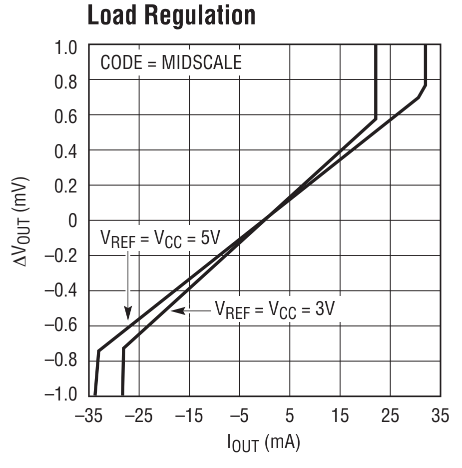
V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

LTC2606/LTC2616/LTC2626

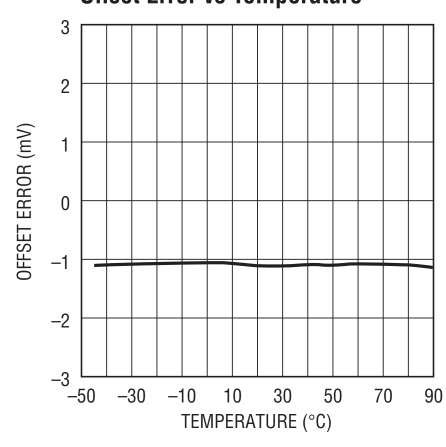
Current Limiting



Load Regulation



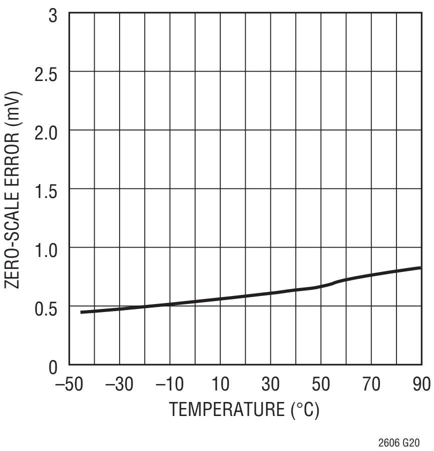
Offset Error vs Temperature



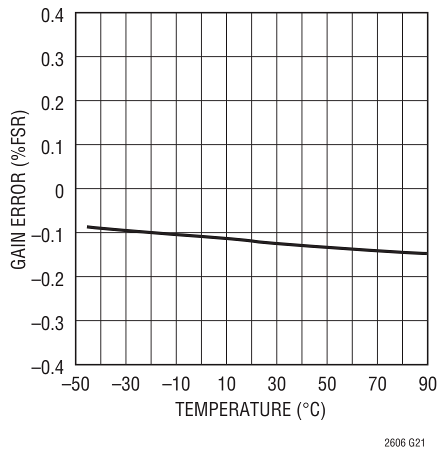
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2606/LTC2616/LTC2626

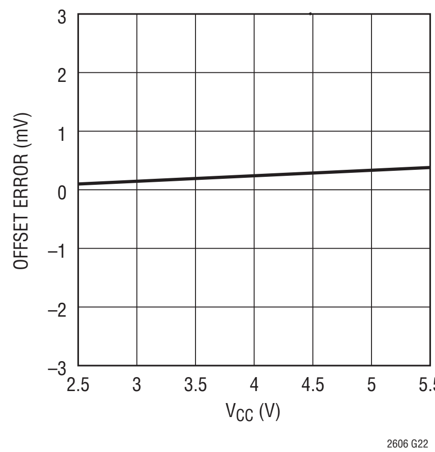
Zero-Scale Error vs Temperature



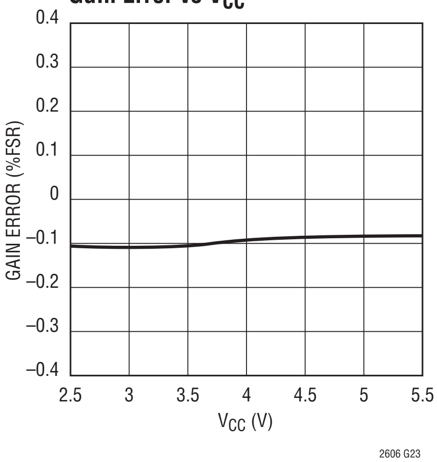
Gain Error vs Temperature



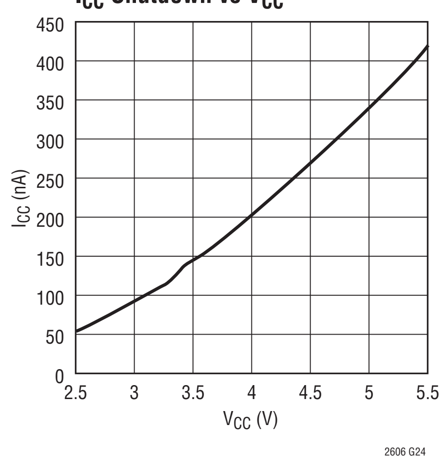
Offset Error vs V_{CC}



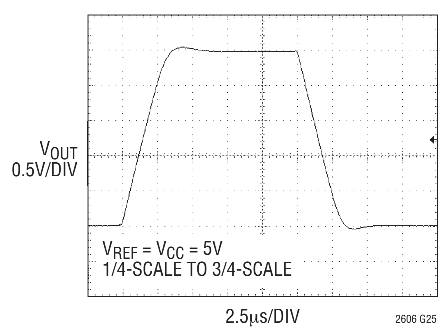
Gain Error vs V_{CC}



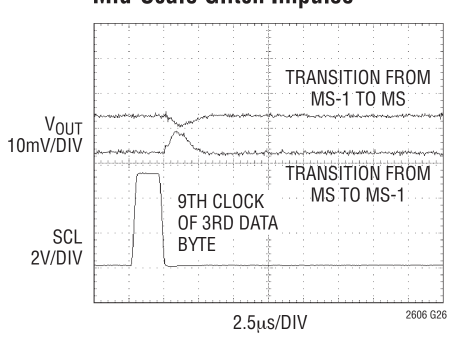
I_{CC} Shutdown vs V_{CC}



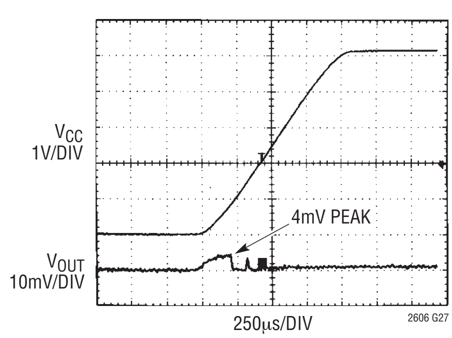
Large-Signal Response



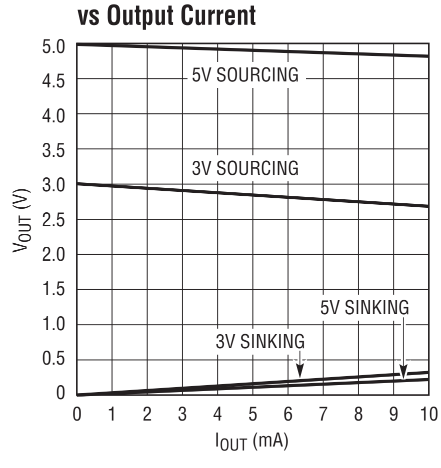
Mid-Scale Glitch Impulse



Power-On Reset Glitch



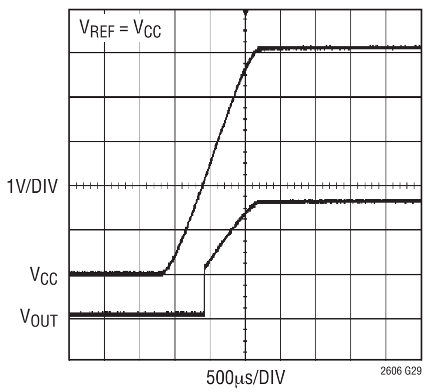
Headroom at Rails vs Output Current



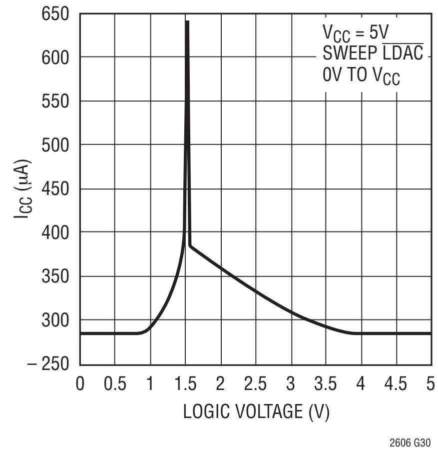
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2606/LTC2616/LTC2626

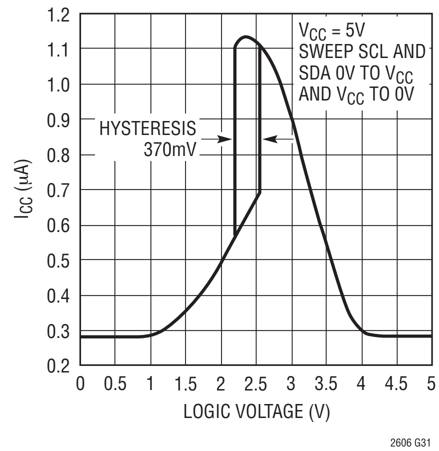
Power-On Reset to Mid-Scale



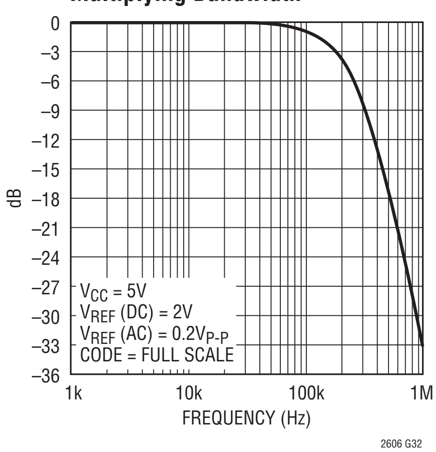
Supply Current vs Logic Voltage



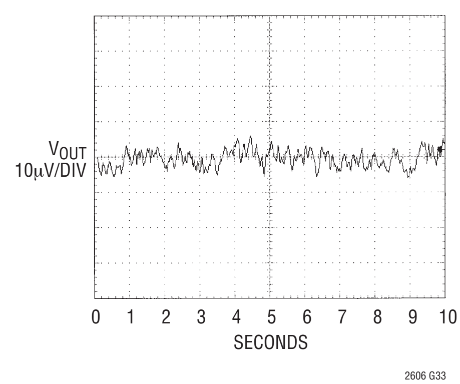
Supply Current vs Logic Voltage



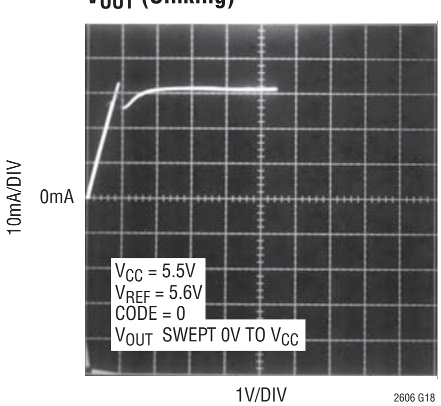
Multiplying Bandwidth



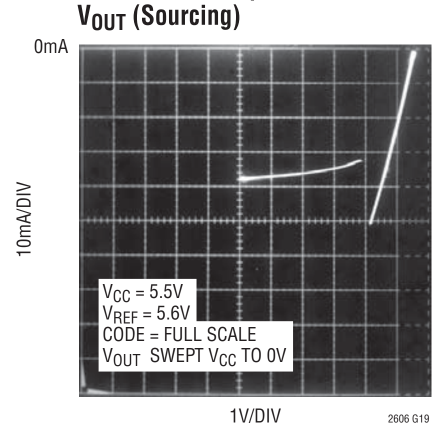
Output Voltage Noise, 0.1Hz to 10Hz



Short-Circuit Output Current vs V_{OUT} (Sinking)



Short-Circuit Output Current vs V_{OUT} (Sourcing)



PIN FUNCTIONS

CA2 (Pin 1): Chip Address Bit 2. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 1).

SDA (Pin 2): Serial Data Bidirectional Pin. Data is shifted into the SDA pin and acknowledged by the SDA pin. This pin is high impedance while data is shifted in. Open-drain N-channel output during acknowledgment. SDA requires a pull-up resistor or current source to V_{CC}.

SCL (Pin 3): Serial Clock Input Pin. Data is shifted into the SDA pin at the rising edges of the clock. This high impedance pin requires a pull-up resistor or current source to V_{CC}.

CA0 (Pin 4): Chip Address Bit 0. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 1).

CA1 (Pin 5): Chip Address Bit 1. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 1).

REF (Pin 6): Reference Voltage Input. $0V \le V_{REF} \le V_{CC}$.

V_{OUT} (Pin 7): DAC Analog Voltage Output. The output range is 0V to V_{REF}.

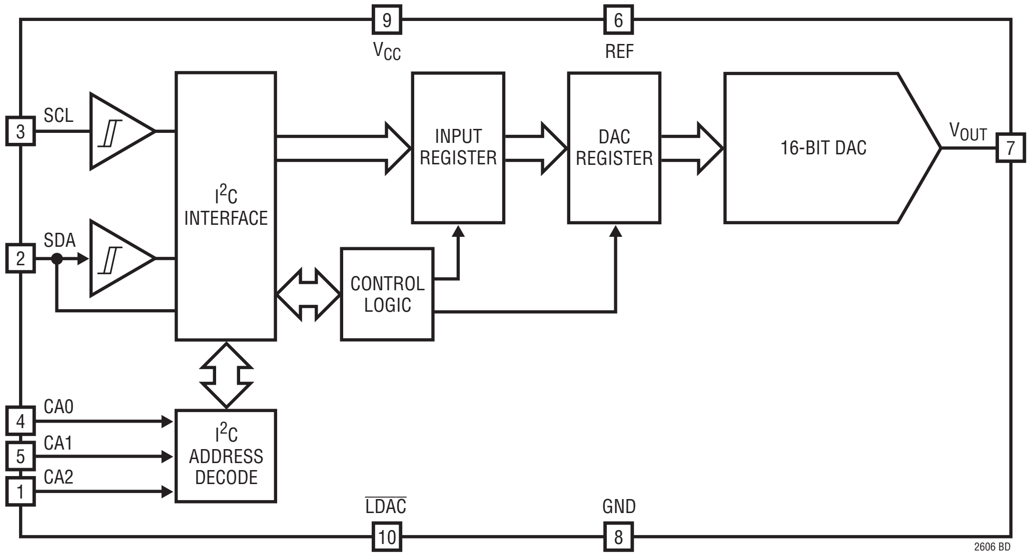
GND (Pin 8): Analog Ground.

V_{CC} (Pin 9): Supply Voltage Input. $2.7V \le V_{CC} \le 5.5V$.

$\overline{LDAC}$ (Pin 10): Asynchronous DAC Update. A falling edge on this input after four bytes have been written into the part immediately updates the DAC register with the contents of the input register. A low on this input without a complete 32-bit (four bytes including the slave address) data write transfer to the part does not update the DAC output. Software power-down is disabled when $\overline{LDAC}$ is low.

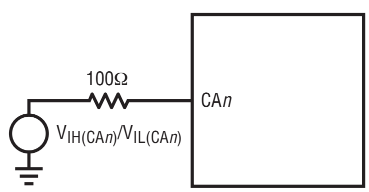
Exposed Pad (Pin 11): Ground. Must be soldered to PCB ground.

BLOCK DIAGRAM

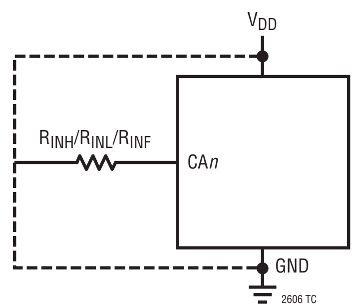


TEST CIRCUITS

Test Circuit 1



Test Circuit 2



TIMING DIAGRAMS

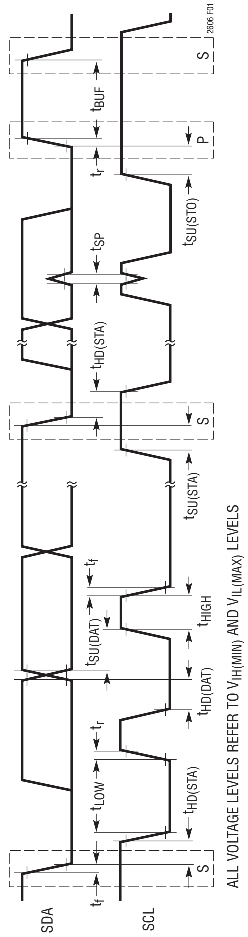


Figure 1

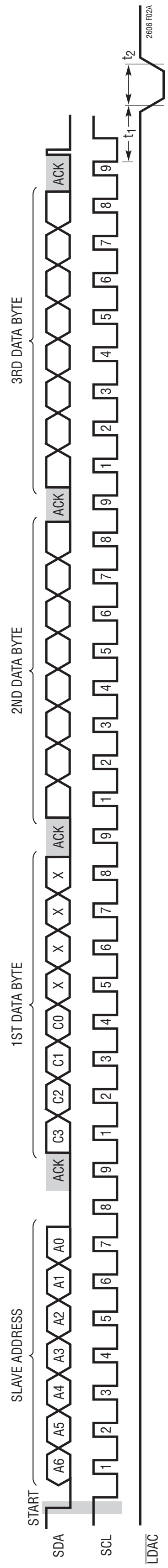


Figure 2a

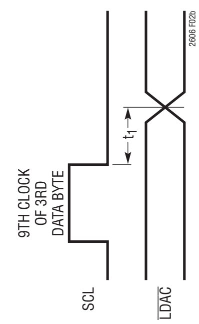


Figure 2b

OPERATION

Power-On Reset

The LTC2606/LTC2616/LTC2626 clear the outputs to zero-scale when power is first applied, making system initialization consistent and repeatable. The LTC2606-1/LTC2616-1/LTC2626-1 set the voltage outputs to mid-scale when power is first applied.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2606/LTC2616/LTC2626 contain circuitry to reduce the power-on glitch; furthermore, the glitch amplitude can be made arbitrarily small by reducing the ramp rate of the power supply. For example, if the power supply is ramped to 5V in 1ms, the analog outputs rise less than 10mV above ground (typ) during power-on. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 9) is in transition.

Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and V_{REF} is the voltage at REF (Pin 6).

Serial Digital Interface

The LTC2606/LTC2616/LTC2626 communicate with a host using the standard 2-wire I^2C interface. The Timing Diagrams (Figures 1 and 2) show the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The value of these pull-up resistors is dependent on the power supply and can be obtained from the I^2C specifications. For an I^2C bus operating in the fast mode, an active pull-up will be necessary if the bus capacitance is greater than 200pF. The V_{CC} power should not be removed from the LTC2606/LTC2616/LTC2626 when the I^2C bus is active to avoid loading the I^2C bus lines through the internal ESD protection diodes.

The LTC2606/LTC2616/LTC2626 are receive-only (slave) devices. The master can write to the LTC2606/LTC2616/LTC2626. The LTC2606/LTC2616/LTC2626 do not respond to a read from the master.

The START (S) and STOP (P) Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high.

When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock pulse. The slave-receiver must pull down the SDA bus line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse. The LTC2606/LTC2616/LTC2626 respond to a write by a master in this manner. The LTC2606/LTC2616/LTC2626 do not acknowledge a read (retains SDA HIGH during the period of the Acknowledge clock pulse).

OPERATION

Chip Address

The state of CA0, CA1 and CA2 decides the slave address of the part. The pins CA0, CA1 and CA2 can be each set to any one of three states: V_{CC}, GND or float. This results in 27 selectable addresses for the part. The slave address assignments are shown in Table 1.

Table 1. Slave Address Map

CA2	CA1	CA0	A6	A5	A4	A3	A2	A1	A0
GND	GND	GND	0	0	1	0	0	0	0
GND	GND	FLOAT	0	0	1	0	0	0	1
GND	GND	V_{CC}	0	0	1	0	0	1	0
GND	FLOAT	GND	0	0	1	0	0	1	1
GND	FLOAT	FLOAT	0	1	0	0	0	0	0
GND	FLOAT	V_{CC}	0	1	0	0	0	0	1
GND	V_{CC}	GND	0	1	0	0	0	1	0
GND	V_{CC}	FLOAT	0	1	0	0	0	1	1
GND	V_{CC}	V_{CC}	0	1	1	0	0	0	0
FLOAT	GND	GND	0	1	1	0	0	0	1
FLOAT	GND	FLOAT	0	1	1	0	0	1	0
FLOAT	GND	V_{CC}	0	1	1	0	0	1	1
FLOAT	FLOAT	GND	1	0	0	0	0	0	0
FLOAT	FLOAT	FLOAT	1	0	0	0	0	0	1
FLOAT	FLOAT	V_{CC}	1	0	0	0	0	1	0
FLOAT	V_{CC}	GND	1	0	0	0	0	1	1
FLOAT	V_{CC}	FLOAT	1	0	1	0	0	0	0
FLOAT	V_{CC}	V_{CC}	1	0	1	0	0	0	1
V_{CC}	GND	GND	1	0	1	0	0	1	0
V_{CC}	GND	FLOAT	1	0	1	0	0	1	1
V_{CC}	GND	V_{CC}	1	1	0	0	0	0	0
V_{CC}	FLOAT	GND	1	1	0	0	0	0	1
V_{CC}	FLOAT	FLOAT	1	1	0	0	0	1	0
V_{CC}	FLOAT	V_{CC}	1	1	0	0	0	1	1
V_{CC}	V_{CC}	GND	1	1	1	0	0	0	0
V_{CC}	V_{CC}	FLOAT	1	1	1	0	0	0	1
V_{CC}	V_{CC}	V_{CC}	1	1	1	0	0	1	0
GLOBAL ADDRESS			1	1	1	0	0	1	1

In addition to the address selected by the address pins, the parts also respond to a global address. This address allows a common write to all LTC2606, LTC2616 and LTC2626 parts to be accomplished with one 3-byte write transaction on the I^2C bus. The global address is a 7-bit on-chip hardwired address and is not selectable by CA0, CA1 and CA2.

The addresses corresponding to the states of CA0, CA1 and CA2 and the global address are shown in Table 1. The maximum capacitive load allowed on the address pins (CA0, CA1 and CA2) is 10pF, as these pins are driven during address detection to determine if they are floating.

Write Word Protocol

The master initiates communication with the LTC2606/LTC2616/LTC2626 with a START condition and a 7-bit slave address followed by the Write bit (W) = 0. The LTC2606/LTC2616/LTC2626 acknowledges by pulling the SDA pin low at the 9th clock if the 7-bit slave address matches the address of the parts (set by CA0, CA1 and CA2) or the global address. The master then transmits three bytes of data. The LTC2606/LTC2616/LTC2626 acknowledges each byte of data by pulling the SDA line low at the 9th clock of each data byte transmission. After receiving three complete bytes of data, the LTC2606/LTC2616/LTC2626 executes the command specified in the 24-bit input word.

If more than three data bytes are transmitted after a valid 7-bit slave address, the LTC2606/LTC2616/LTC2626 do not acknowledge the extra bytes of data (SDA is high during the 9th clock).

The format of the three data bytes is shown in Figure 3. The first byte of the input word consists of the 4-bit command and four don't care bits. The next two bytes consist of the 16-bit data word. The 16-bit data word consists of the 16-, 14- or 12-bit input code, MSB to LSB, followed by 0, 2 or 4 don't care bits (LTC2606, LTC2616 and LTC2626 respectively). A typical LTC2606 write transaction is shown in Figure 4.

The command assignments (C3-C0) are shown in Table 2. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register. In an update operation, the data word is copied from the input register to the DAC register and converted to an analog voltage at the DAC output. The update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

OPERATION

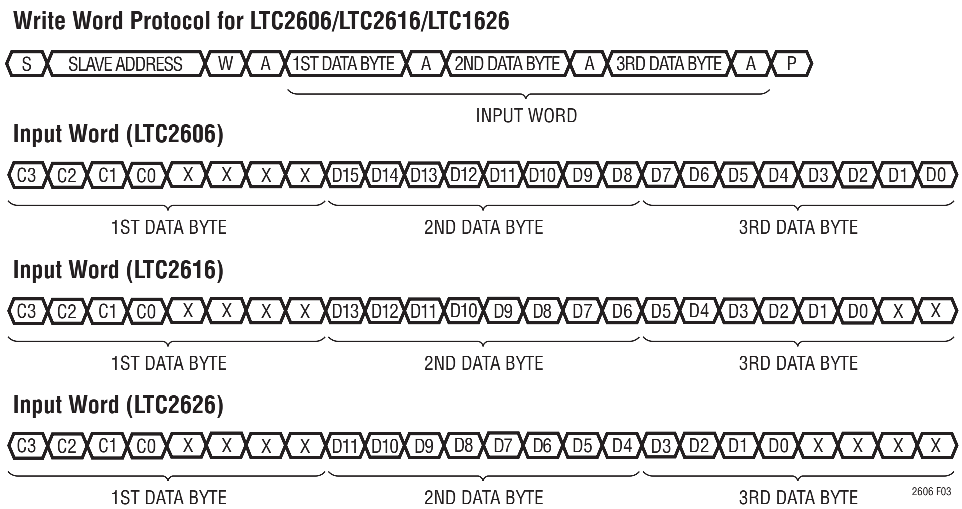


Figure 3

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever the DAC output is not needed. When in power-down, the buffer amplifier, bias circuit and reference input is disabled and draws essentially zero current. The DAC output is put into a high impedance state, and the output pin is passively pulled to ground through 90k resistors. Input- and DAC-register contents are not disturbed during power-down.

Table 2

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register
0	0	0	1	Update (Power Up) DAC Register
0	0	1	1	Write to and Update (Power Up)
0	1	0	0	Power Down
1	1	1	1	No Operation

*Command codes not shown are reserved and should not be used.

The DAC channel can be put into power-down mode by using command 0100_b. The 16-bit data word is ignored. The supply and reference currents are reduced to almost zero when the DAC is powered down; the effective resistance at REF becomes a high impedance input (typically >1GΩ).

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 2 or performing an asychronous update ($\overline{\text{LDAC}}$) as described in the next section. The DAC is powered up as its voltage output is updated. When the DAC in powered-down state is powered up and updated, normal settling is delayed. The main bias generation circuit block has been automatically shut down in addition to the DAC amplifier and reference input and so the power-up delay time is:

12μs (for V_{CC} = 5V) or 30μs (for V_{CC} = 3V)

Asynchronous DAC Update Using LDAC

In addition to the update commands shown in Table 2, the $\overline{\text{LDAC}}$ pin asynchronously updates the DAC register with the contents of the input register. Asynchronous update is disabled when the input word is being clocked into the part.

If a complete input word has been written to the part, a low on the $\overline{\text{LDAC}}$ pin causes the DAC register to be updated with the contents of the input register.

If the input word is being written to the part, a low going pulse on the $\overline{\text{LDAC}}$ pin before the completion of three bytes of data powers up the DAC but does not cause the output to be updated. If $\overline{\text{LDAC}}$ remains low after a complete input word has been written to the part, then $\overline{\text{LDAC}}$ is recognized, the command specified in the 24-bit word just transferred is executed and the DAC output is updated.

OPERATION

The DAC is powered up when $\overline{LDAC}$ is taken low, independent of any activity on the I^2C bus.

If $\overline{LDAC}$ is low at the falling edge of the 9th clock of the 3rd byte of data, it inhibits any software power-down command that was specified in the input word.

Voltage Output

The rail-to-rail amplifier has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifiers' DC output impedance is 0.050Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 25Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 25Ω • 1mA = 25mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 1000pF.

Board Layout

The excellent load regulation performance is achieved in part by keeping "signal" and "power" grounds separated internally and by reducing shared internal resistance.

The GND pin functions both as the node to which the reference and output voltages are referred and as a return path for power currents in the device. Because of this, careful thought should be given to the grounding scheme and board layout in order to ensure rated performance.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin of the part should be connected to analog ground. Resistance from the GND pin to system star ground should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.050Ω). Note that the LTC2606/LTC2616/LTC2626 are no more susceptible to these effects than other parts of their type; on the contrary, they allow layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the device cannot go below ground, it may limit for the lowest codes as shown in Figure 5b. Similarly, limiting can occur near full-scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 5c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

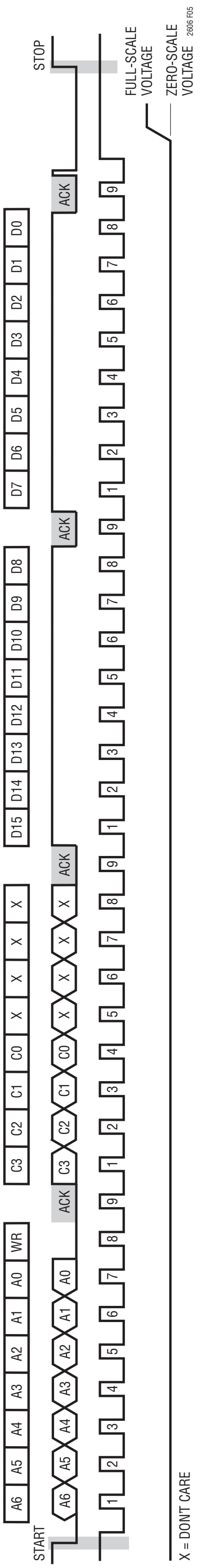


Figure 4. Typical LTC2606 Input Waveform—Programming DAC Output for Full Scale

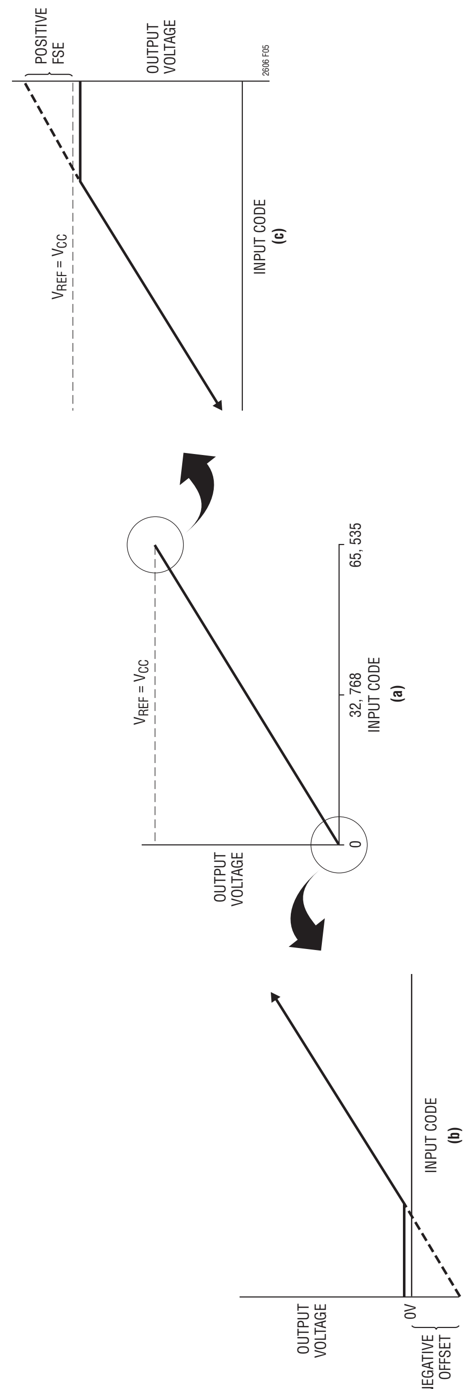
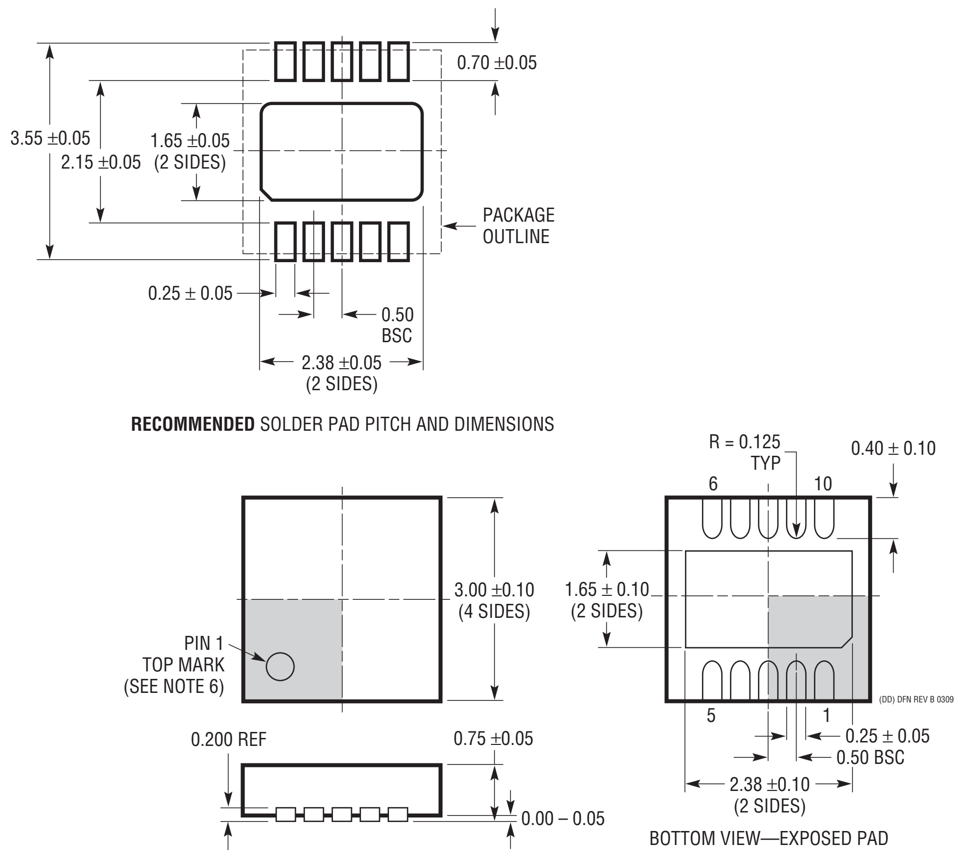


Figure 5. Effects of Rail-to-Rail Operation on a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Codes Near Full Scale

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev B)



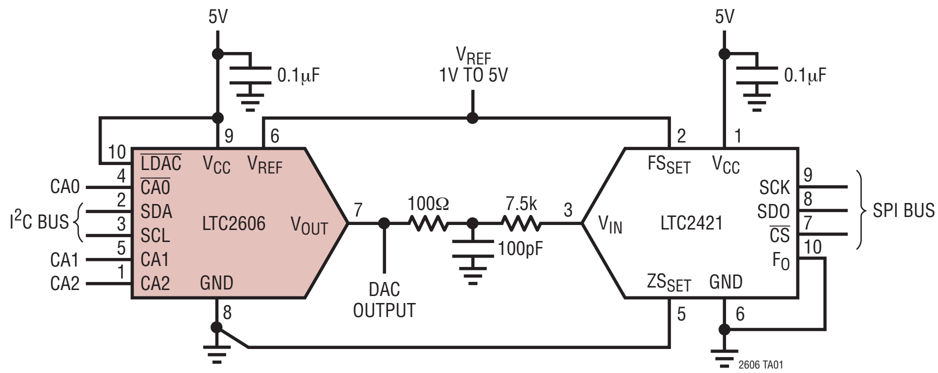
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	11/09	Insert Text in Serial Digital Interface Section	13

TYPICAL APPLICATION

Demo Circuit Schematic. Onboard 20-Bit ADC Measures Key Performance Parameters



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.096V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1654	Dual 14-Bit Rail-to-Rail V_{OUT} DAC	Programmable Speed/Power, 3.5µs/750µA, 8µs/450µA
LTC1655/LTC1655L	Single 16-Bit V_{OUT} DACs with Serial Interface in SO-8	V_{CC} = 5V(3V), Low Power, Deglitched
LTC1657/LTC1657L	Parallel 5V/3V 16-Bit V_{OUT} DACs	Low Power, Deglitched, Rail-to-Rail V_{OUT}
LTC1660/LTC1665	Octal 10/8-Bit V_{OUT} DACs in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1821	Parallel 16-Bit Voltage Output DAC	Precision 16-Bit Settling in 2µs for 10V Step
LTC2600/LTC2610 LTC2620	Octal 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2601/LTC2611 LTC2621	Single 16-/14-/12-Bit V_{OUT} DACs in 10-Lead DFN	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2602/LTC2612 LTC2622	Dual 16-/14-/12-Bit V_{OUT} DACs in 8-Lead MSOP	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2604/LTC2614 LTC2624	Quad 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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