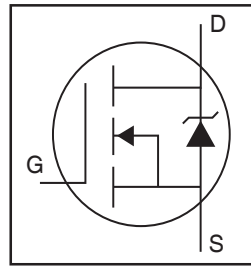


# AUIRFS4310Z

HEXFET® Power MOSFET

## Features

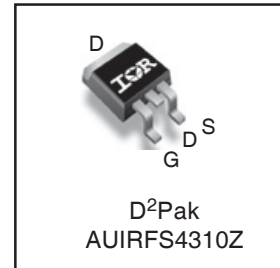
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



$V_{DSS}$	<b>100V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>4.8mΩ</b>
<b>max.</b>	<b>6.0mΩ</b>
$I_D$ (Silicon Limited)	<b>127A</b> ①
$I_D$ (Package Limited)	<b>120A</b>

## Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited)	127①	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited)	90①	
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Wire Bond Limited)	120	
$I_{DM}$	Pulsed Drain Current ②	560	
$P_D$ @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	250	W
	Linear Derating Factor	1.7	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ③	130	mJ
$I_{AR}$	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
$E_{AR}$	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode Recovery ④	18	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.6	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤	—	40	

HEXFET® is a registered trademark of International Rectifier.

\*Qualification standards can be found at <http://www.irf.com/>

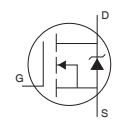
### Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to $25^\circ\text{C}, I_D = 5mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.8	6.0	m $\Omega$	$V_{GS} = 10V, I_D = 75A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$g_{fs}$	Forward Transconductance	150	—	—	S	$V_{DS} = 50V, I_D = 75A$
$R_G$	Internal Gate Resistance	—	0.7	—	$\Omega$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

### Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge	—	120	170	nC	$I_D = 75A$ $V_{DS} = 50V$ $V_{GS} = 10V$ ⑤ $I_D = 75A, V_{DS} = 0V, V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source Charge	—	29	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	35	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	85	—		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	$V_{DD} = 65V$ $I_D = 75A$ $R_G = 2.7\Omega$ $V_{GS} = 10V$ ⑤
$t_r$	Rise Time	—	60	—		
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		
$t_f$	Fall Time	—	57	—		
$C_{iss}$	Input Capacitance	—	6860	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0MHz$ , See Fig. 5 $V_{GS} = 0V, V_{DS} = 0V$ to $80V$ ⑦, See Fig. 11 $V_{GS} = 0V, V_{DS} = 0V$ to $80V$ ⑧
$C_{oss}$	Output Capacitance	—	490	—		
$C_{riss}$	Reverse Transfer Capacitance	—	220	—		
$C_{oss}$ eff. (ER)	Effective Output Capacitance (Energy Related)	—	570	—		
$C_{oss}$ eff. (TR)	Effective Output Capacitance (Time Related)	—	920	—		

### Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	127	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ②	—	—	560	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ⑤
$t_{rr}$	Reverse Recovery Time	—	40	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 85V,$
		—	49	—		$T_J = 125^\circ\text{C}$ $I_F = 75A$
$Q_{rr}$	Reverse Recovery Charge	—	58	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	89	—		$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	2.5	—	A	$T_J = 25^\circ\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

#### Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.047mH$   
 $R_G = 25\Omega, I_{AS} = 75A, V_{GS} = 10V$ . Part not recommended for use above the  $E_{as}$  value and test conditions.
- ④  $I_{SD} \leq 75A, di/dt \leq 600A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to  $80\% V_{DSS}$ .
- ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to  $80\% V_{DSS}$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Automotive (per AEC-Q101) <sup>††</sup>	
	Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>	D <sup>2</sup> Pak	MSL1
<b>ESD</b>	Machine Model	Class M4 (+/- 800V) <sup>†††</sup> AEC-Q101-002
	Human Body Model	Class H2 (+/- 4000V) <sup>†††</sup> AEC-Q101-001
	Charged Device Model	Class C5 (+/- 2000V) <sup>†††</sup> AEC-Q101-005
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

†† Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

††† Highest passing voltage.

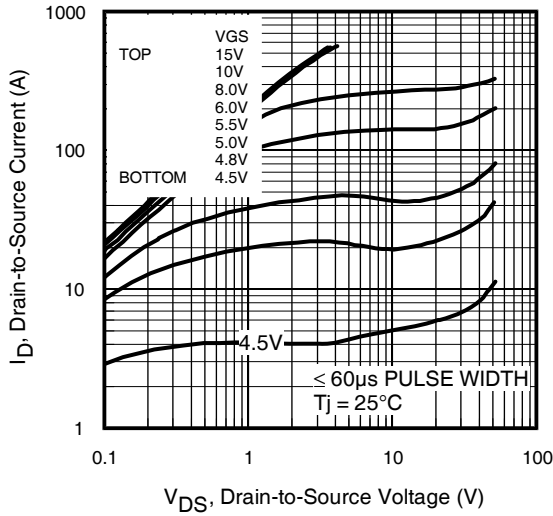


Fig 1. Typical Output Characteristics

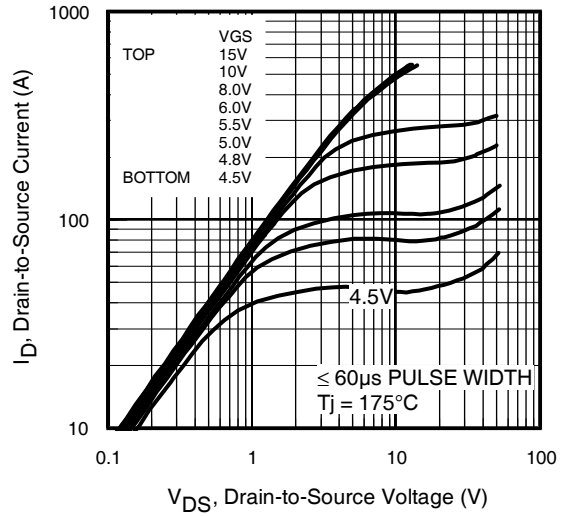


Fig 2. Typical Output Characteristics

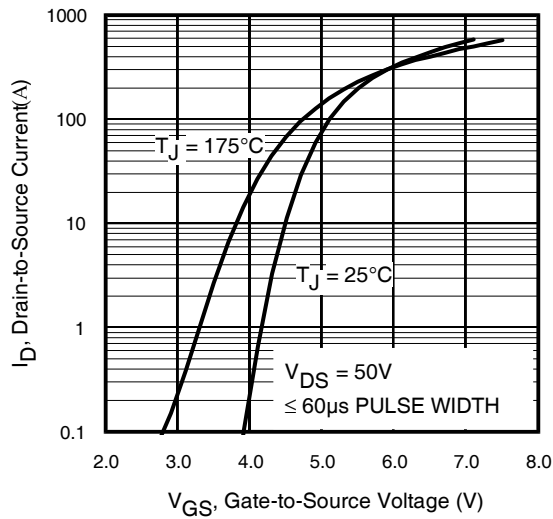


Fig 3. Typical Transfer Characteristics

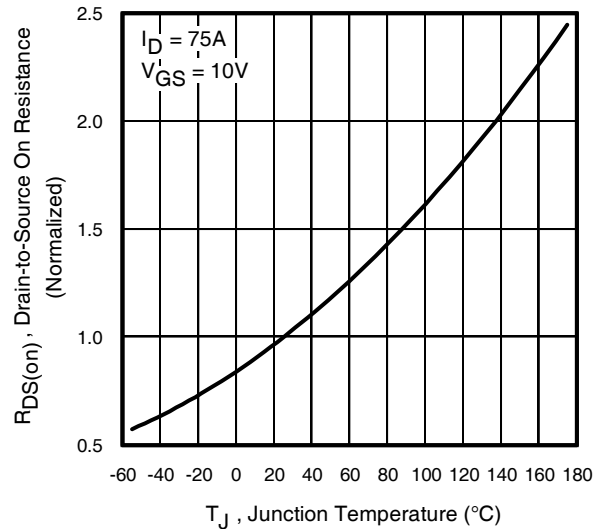


Fig 4. Normalized On-Resistance vs. Temperature

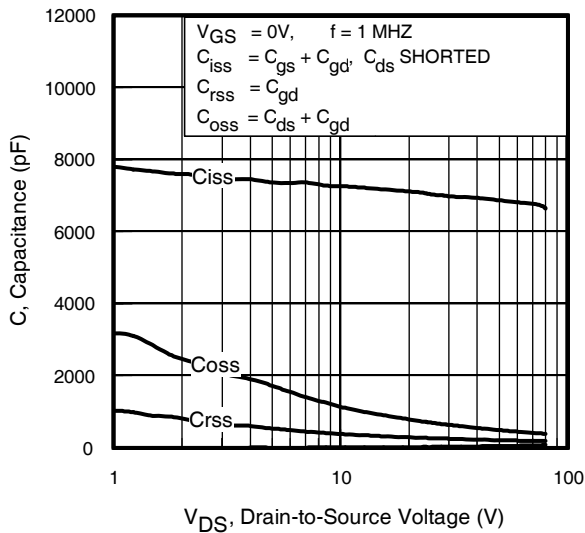


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

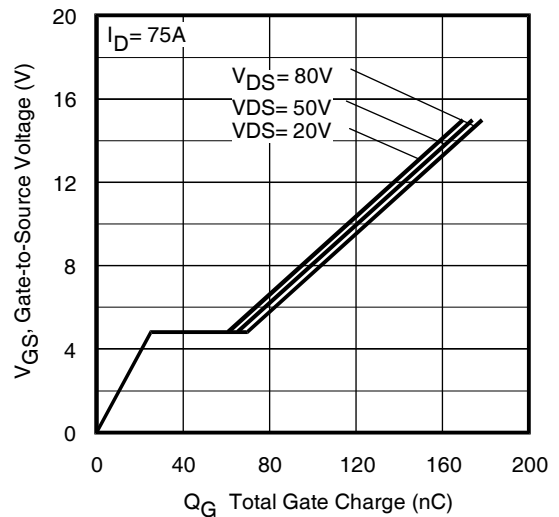
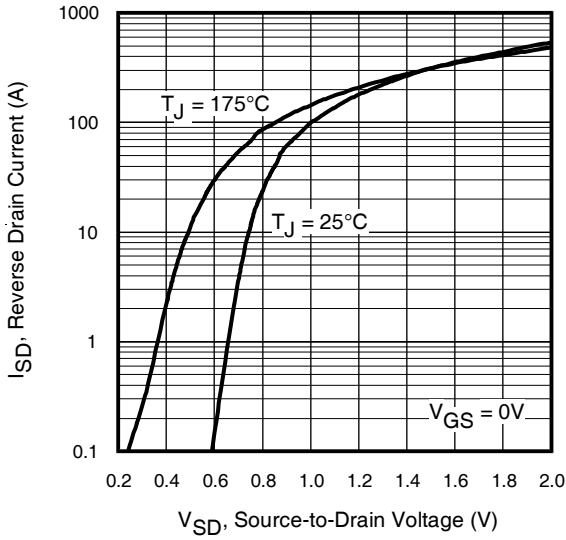
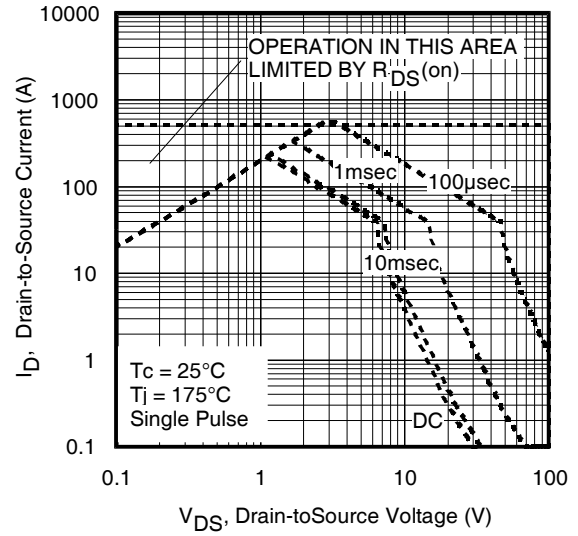


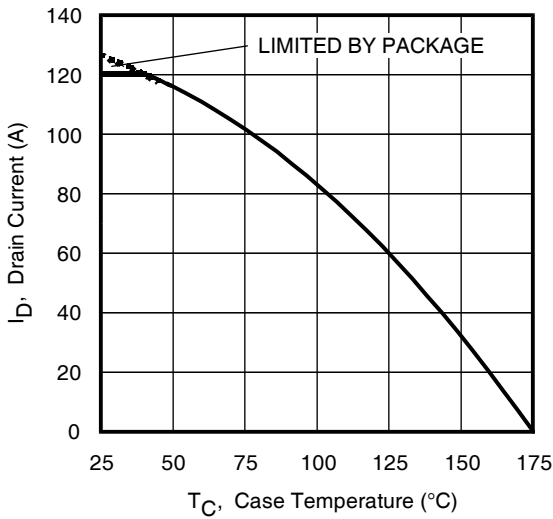
Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



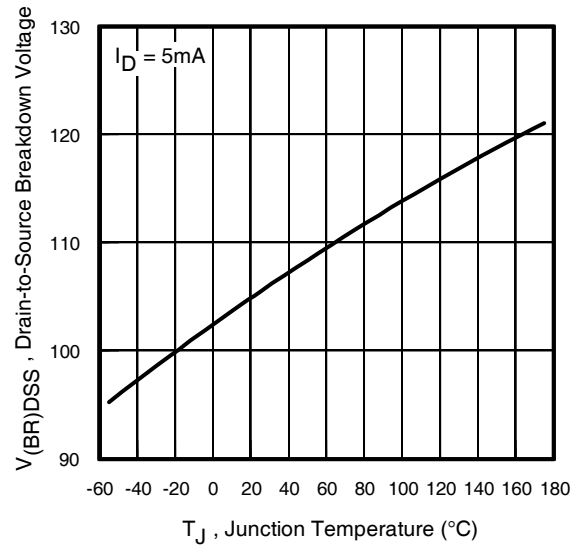
**Fig 7.** Typical Source-Drain Diode Forward Voltage



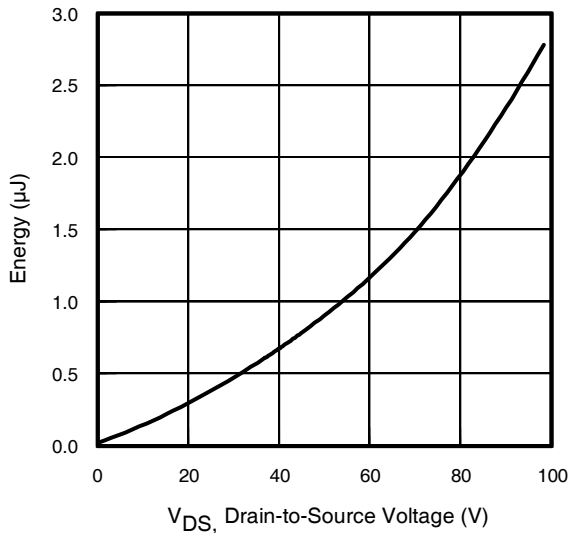
**Fig 8.** Maximum Safe Operating Area



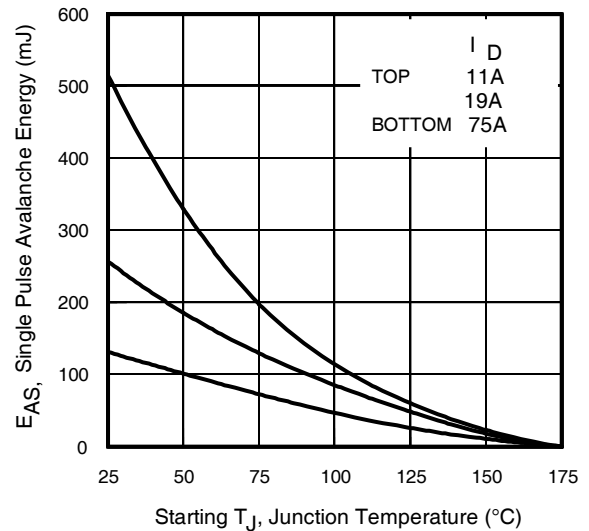
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy Vs. Drain Current

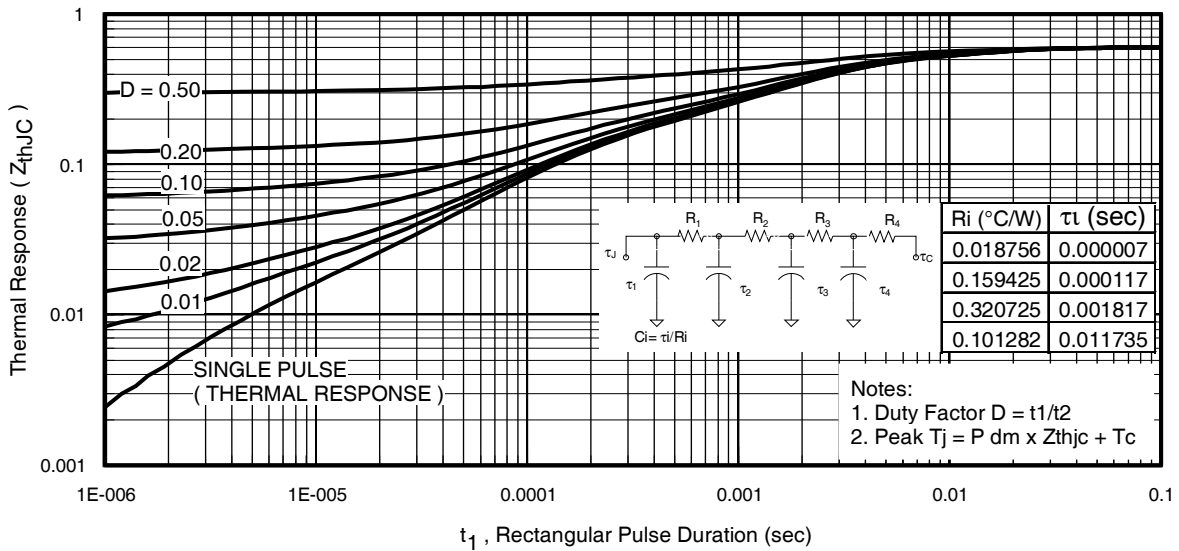


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

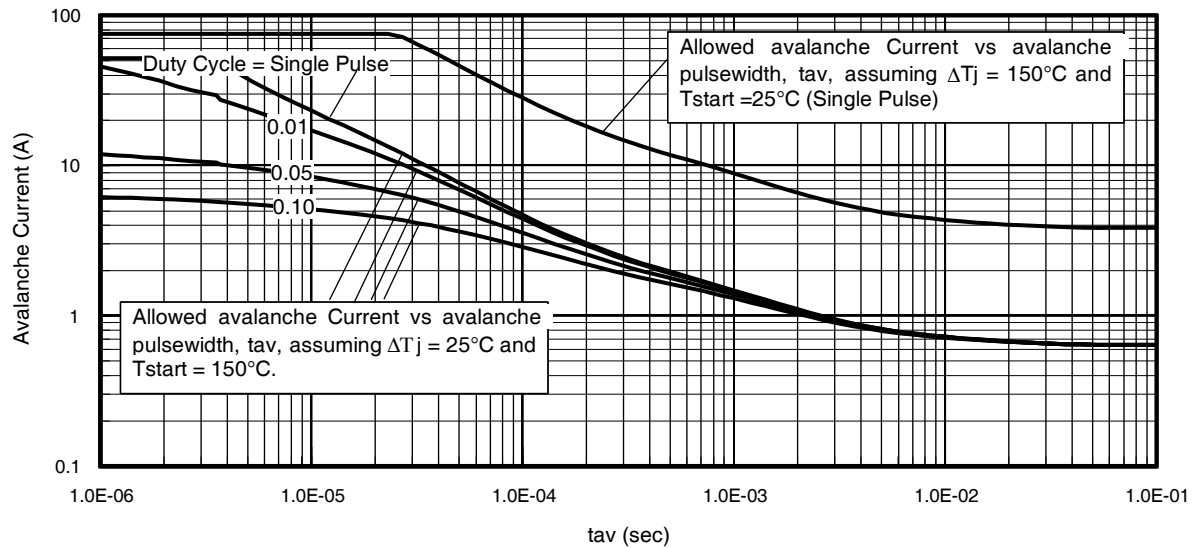
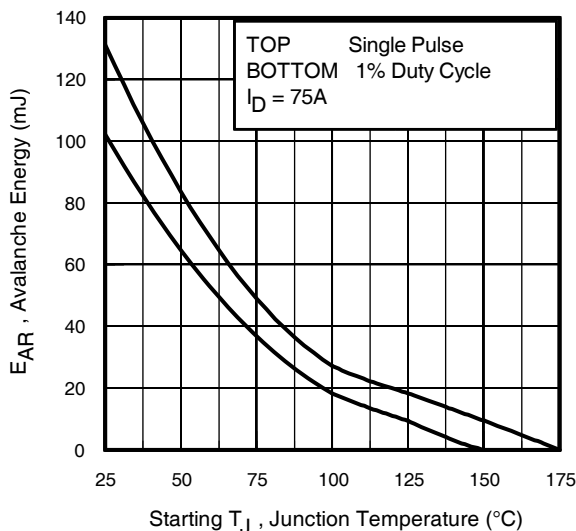


Fig 14. Typical Avalanche Current vs. Pulsewidth



**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2 \Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

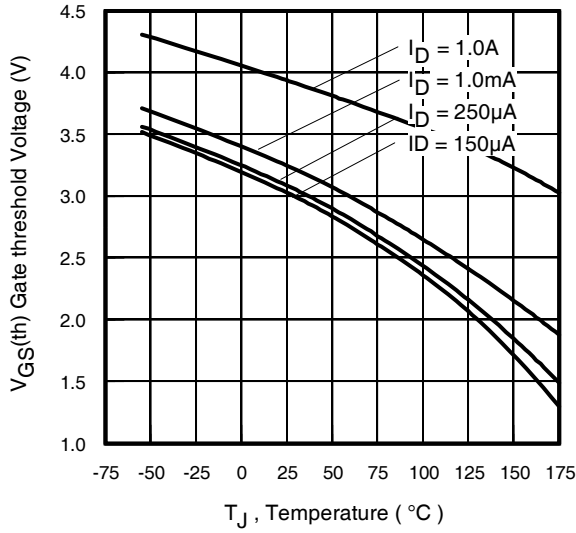


Fig 16. Threshold Voltage Vs. Temperature

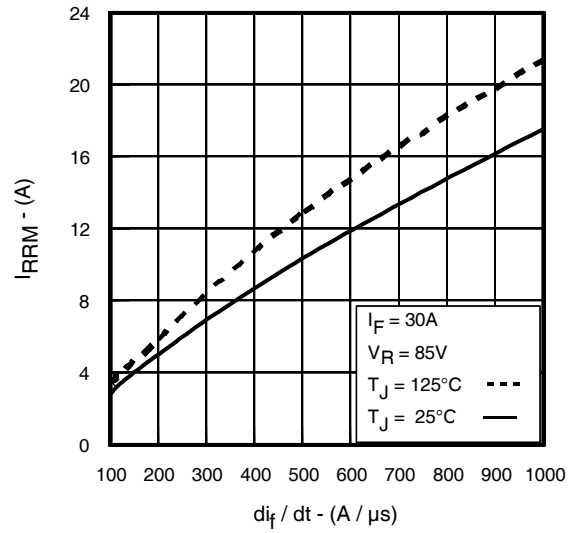


Fig. 17 - Typical Recovery Current vs.  $di_T/dt$

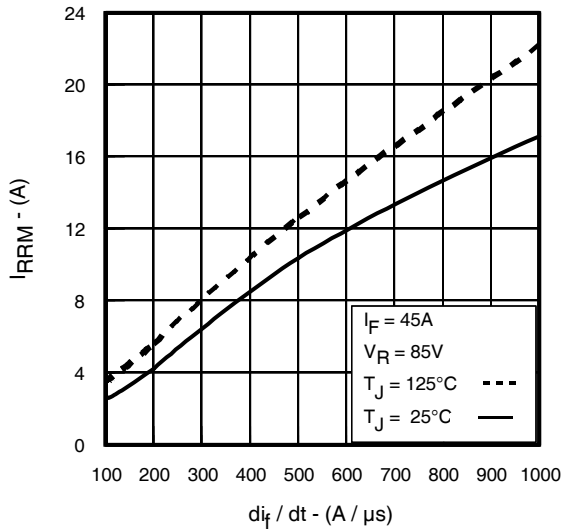


Fig. 18 - Typical Recovery Current vs.  $di_T/dt$

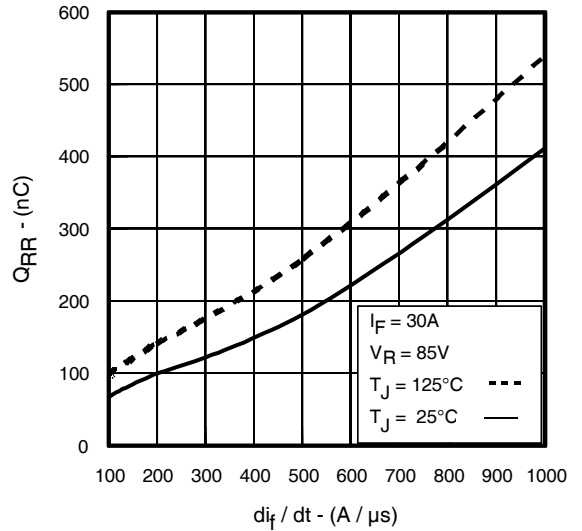


Fig. 19 - Typical Stored Charge vs.  $di_T/dt$

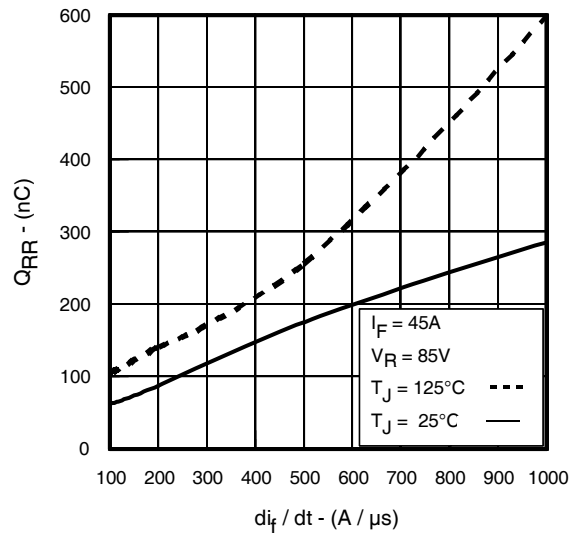


Fig. 20 - Typical Stored Charge vs.  $di_T/dt$

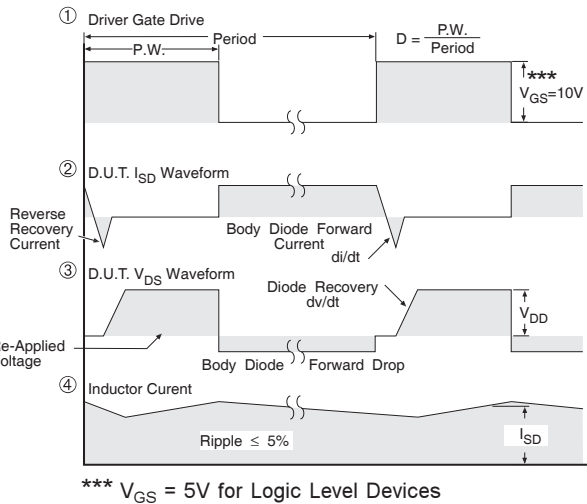
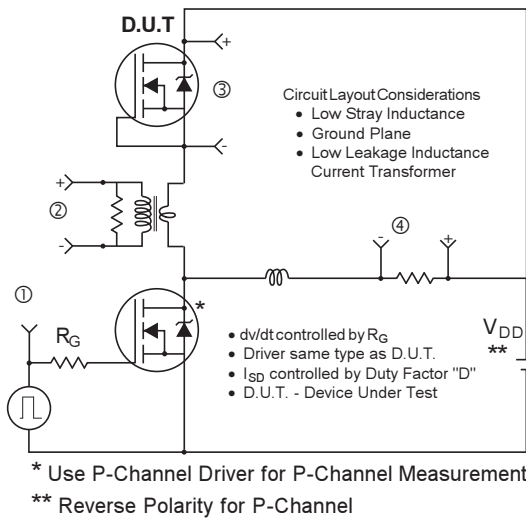


Fig 21. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

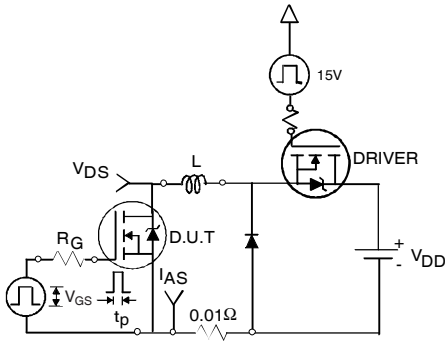


Fig 22a. Unclamped Inductive Test Circuit

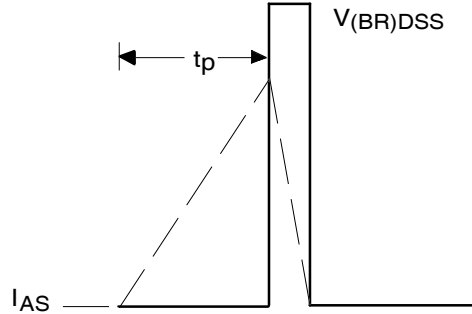


Fig 22b. Unclamped Inductive Waveforms

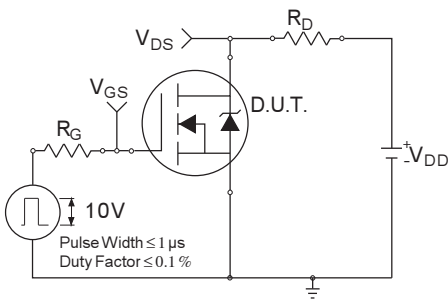


Fig 23a. Switching Time Test Circuit

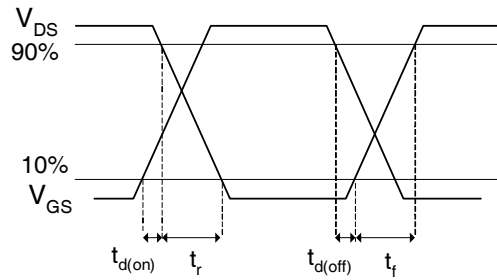


Fig 23b. Switching Time Waveforms

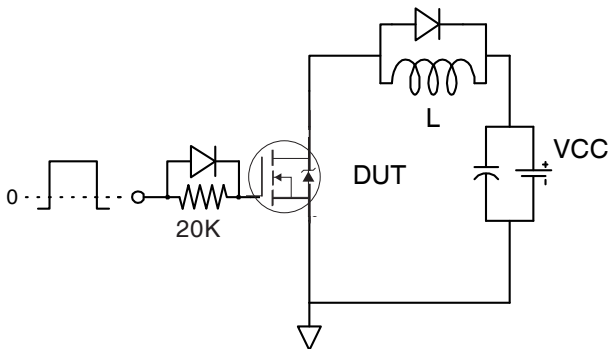


Fig 24a. Gate Charge Test Circuit

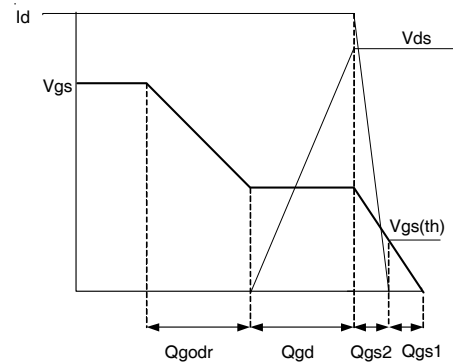
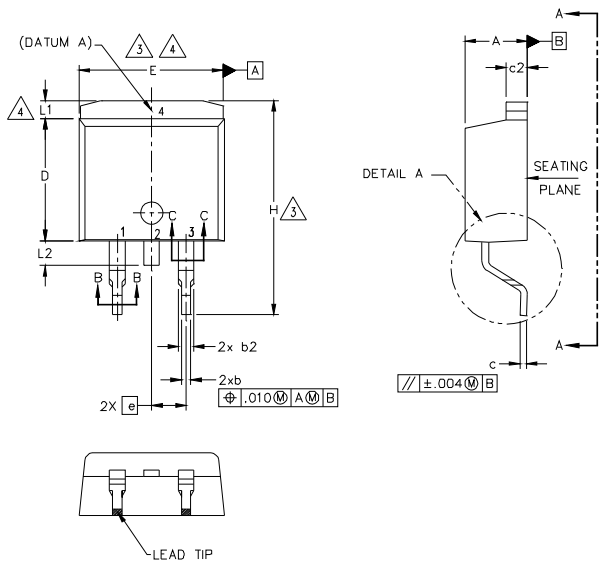
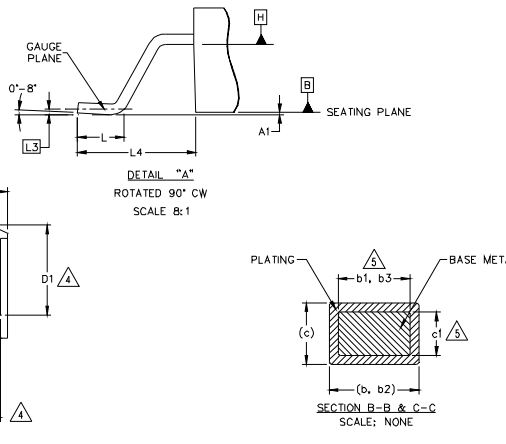


Fig 24b. Gate Charge Waveform

**D<sup>2</sup>Pak Package Outline (Dimensions are shown in millimeters (inches))**

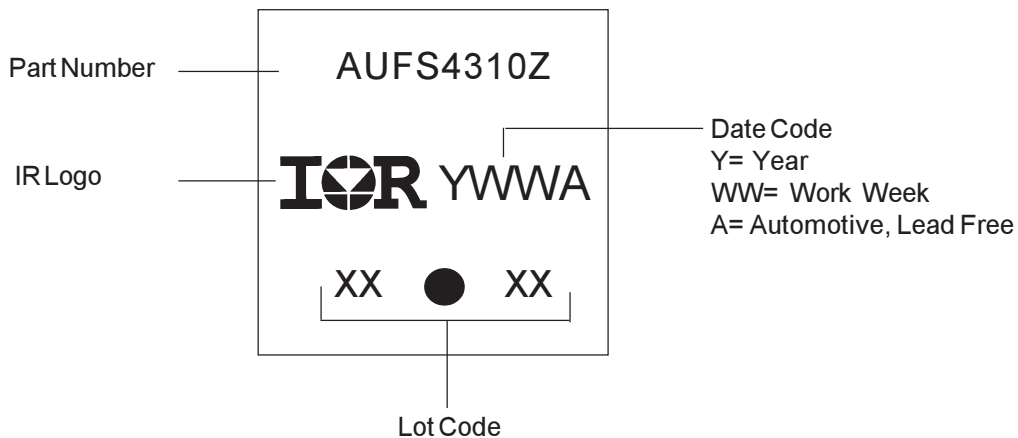


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	<b>LEAD ASSIGNMENTS</b>  <b>DIODES</b> 1.- ANODE (TWO DIE) / OPEN (ONE DIE) 2, 4.- CATHODE 3.- ANODE  <b>HEXFET</b> <b>IGBTs, CoPACK</b> 1.- GATE                              1.- GATE 2, 4.- DRAIN                          2, 4.- COLLECTOR 3.- SOURCE                            3.- EMITTER
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	
E	9.65	10.67	.380	.420	
E1	6.22	-	.245	-	
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	
L2	1.27	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

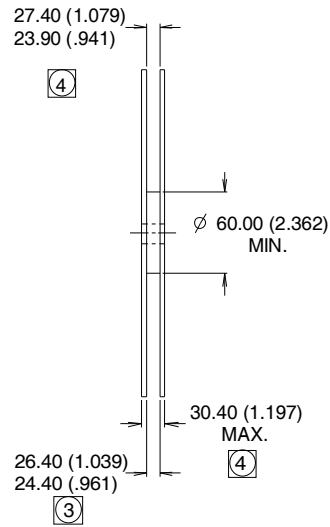
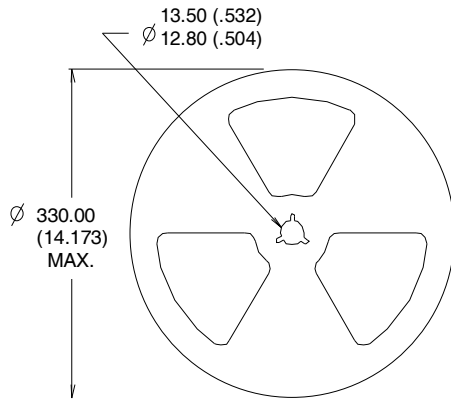
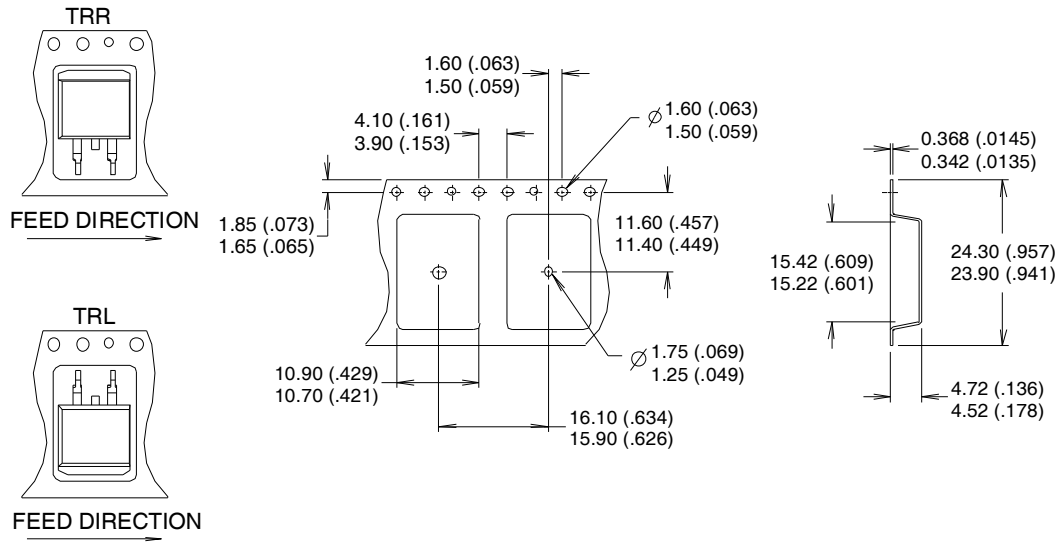


- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  - DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [".005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  - THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  - DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  - DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  - CONTROLLING DIMENSION: INCH.
  - OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

**D<sup>2</sup>Pak Part Marking Information**



D<sup>2</sup>Pak Tape & Reel Information



- NOTES :
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Ordering Information**

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRFS4310Z	D2Pak	Tube	50	AUIRFS4310Z
		Tape and Reel Left	800	AUIRFS4310ZTRL
		Tape and Reel Right	800	AUIRFS4310ZTRR

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