



Hi-Fi Voice Synthesis LSI

BU6929FV

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< revision history >

Date	Rev No	remarks
Jan/07/2008	1.00	Initial Version
Jan/23/2009	1.05	P19(add notice about command Timing) P22(correct about using 16kHz ampling data) Correct Index. New LOGO

1. Function overview and Features

BU6929FV is a voice synthesis IC which can playback highly compressed voice/audio data stored in external SPI-interface ROM by commands from serial interface or from the pins. One channel of voice/audio data can be decoded and playback. The main functions are described below.

- 1) High compression algorithm ("ROHM-HiFi") is adopted. Available bit-rate is 16kbps ~ 192kbps.
- 2) Voice/audio data is stored in serial Flash ROM which is connected to BU6929FV through SPI-serial Interface (See chapter13.9. for available SPI serial ROM). Duration for playback is 32seconds/Mbits(standard) or max 64s/Mbits(Maximum).
- 3) The package is SSOP-B28, which is one of the smallest size for voice synthesis LSI. Also, BU6929FV is completely pin-compatible architecture with BU6954FV/BU6952FV. For this feature, BU6929FV is also used for pre-production system before mass-production using BU6954FV.
- 4) Input system clock: 16.384MHz/8.192MHz/4.096MHz/2.048MHz (see Chapter 11).
- 5) Audio sampling rate is 32KHz or 16kHz and Built-in 16bits DAC.
- 6) Operation by single power supply. Available voltage:2.7 to 3.6V
- 7) Max numbers of tunes : 480
- 8)HOST-I/F is selectable from serial interface with status or direct pin.
- 9) Enable to access(read/write) data stored in serial ROM connected directly to BU6929FV.(Available Serial ROM is described at chapter 13.9. Access unit is 512kbit.)
- 10) Various play modes are available.

【play modes from serial Interface】

- decodable 1 channel.
- adjustable volume.
- enable to playback tunes which are registered in the sequencer list. Order of tunes can be randomly selected. Max 16 tunes can be registered.
- enable to playback a selected tune or to playback tunes in the sequencer list with/without loop.
- fade-in and fade-out functions are supported.

【Play modes from direct pin control】

- decodable only 1channel.
- maximum 8 tunes are registered to play.
- sequencer is not supported. Normal play mode only.

2. Applicable products

electronics/electric products, home appliance, factory appliance, etc.

3. Absolute maximum rating

($T_a=25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Power dissipation ^{*)}	P_d	640	mW
Applied voltage	V_{DD}	-0.2 ~ 7.0	V
Input voltage	V_{IN}	-0.2 ~ $V_{DD}+0.3$	V
Operating temperature range	T_{OPR}	-40 ~ +85	$^\circ\text{C}$
Storage temperature range	TSTG	-50 ~ 125	$^\circ\text{C}$

*) Over $T_a = 25^\circ\text{C}$ or more, reducing 6.4mW per $^\circ\text{C}$.

4. Operating conditions

($T_a=-40 \sim +85^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Specified value			Unit	Condition
		Min	Typ	Max		
Operation power-supply voltage	V_{DD5_IN}	2.7	-	3.6	V	-

5. Electric characteristic (DC characteristic)

5.1.DC Characteristics

■VDD5_IN=3V (Ta=25℃)

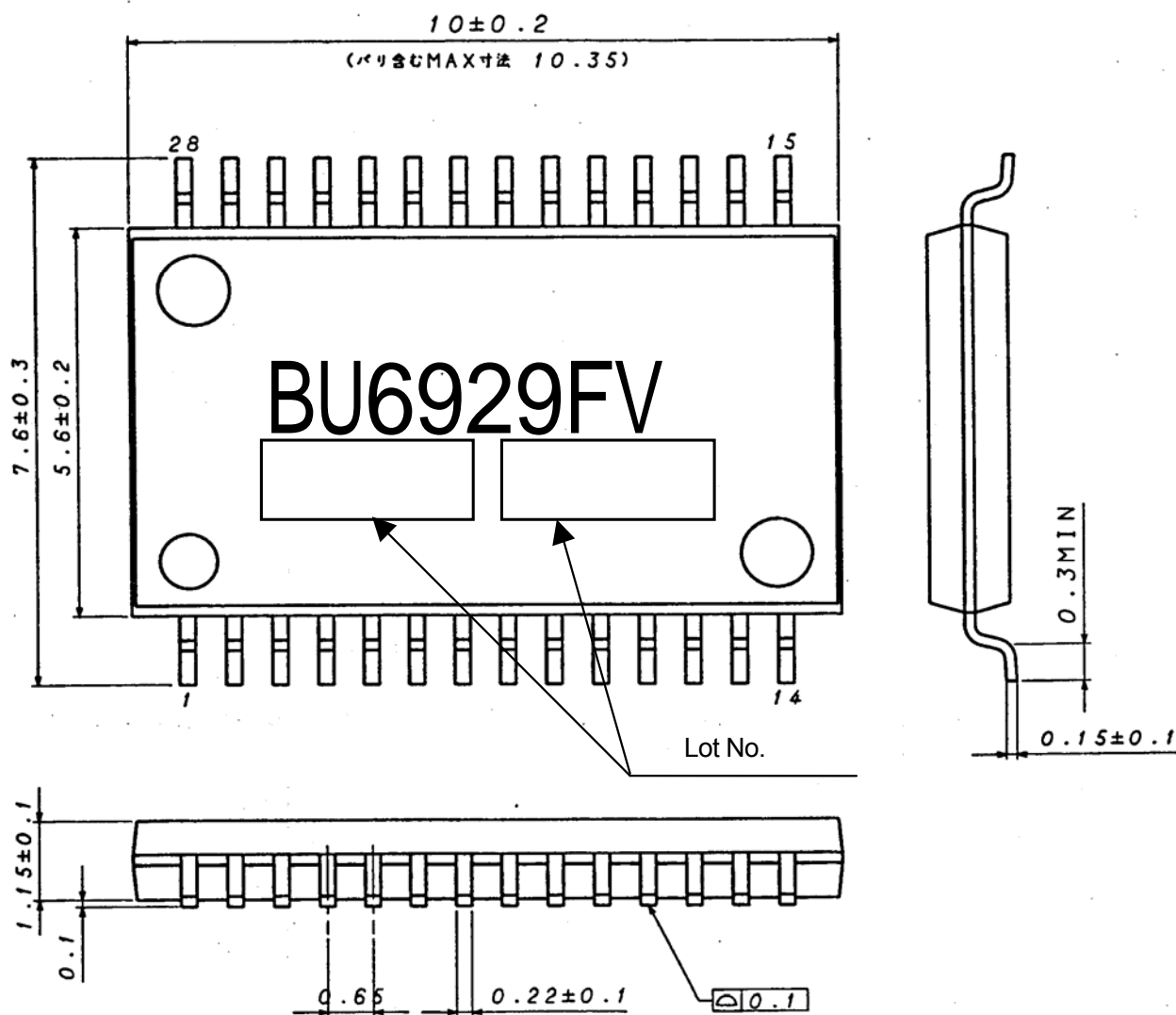
Item	Symbol	Specified value			Unit	Condition	Circuit form
		Min	Typ	Max			
"H" Input Voltage	V _{IH}	0.7VDD	-	-	V		□
"L" Input Voltage	V _{IL}	-	-	0.3VDD	V		□
"H" Output Voltage	V _{OH}	VDD-0.4	-	-	V	IO=2.0mA	□
"L" Output Voltage	V _{OL}	-	-	0.4	V	IO=2.0mA	□
"H" Input current	I _{IH}	-	-	10	μA	V _{IH} =VDD	I
"L" Input current	I _{IL}	-	-	-10	μA	V _{IL} =GND	I
Static consumption current	I _{ST}	-	-	10	μA	V _I =V _{DD} orGND	-

5.2. DAC Characteristics

■VDD5_IN=3V時 (Ta=25℃)

Item	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
DACOUT Output Load Resistance	R _{AOUT}	10	-	-	KΩ	No Load
DACOUT Output Voltage	V _{AOUT}	GND	-	VDD	V	No Signal

6. Outline dimensions



(UNIT : mm)

SSOP-B28

7. Block Diagram

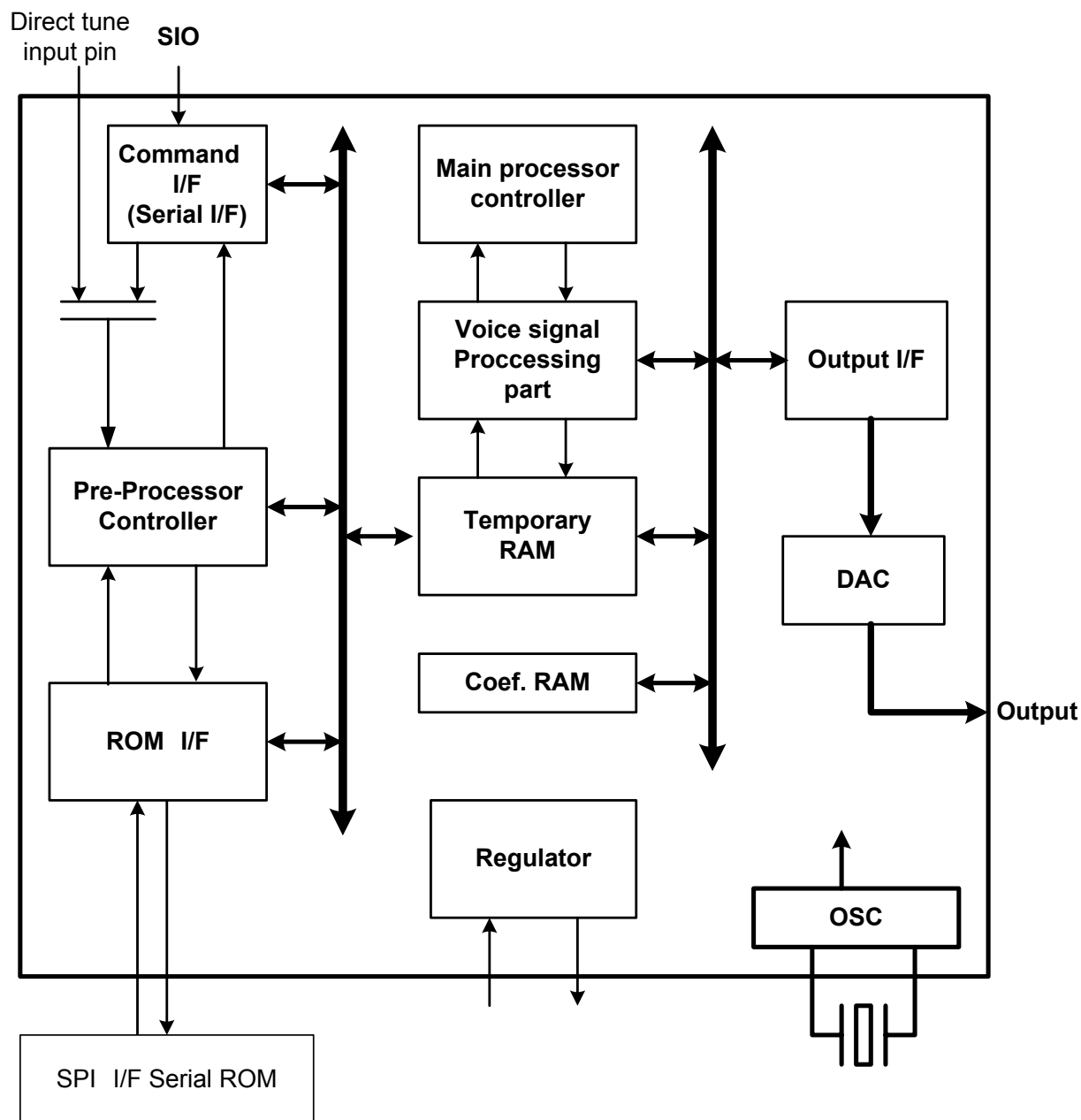


Figure7-1. Block Diagram

8. Pin No. and Pin Name

8.1. Pin name Detailed table

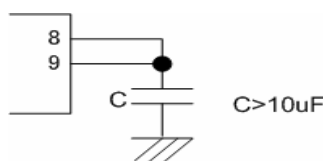
Table 8-1.Pin name Detailed table

PIN NO.	Pin name	I/O	I/O Circuit form	Function
1	GND	-	-	GND
2	VSEL2/TXD	IO		tune number pin#2 ^{*1)} / Serial Interface output data
3	VSEL1/RXD	I	- A	tune number pin#1 ^{*1)} / Serial Interface input data
4	VSEL0/RXCB	I	- A	tune number pin#0 ^{*1)} / Serial Interface clock
5	TSEVENT/BUSY	O	- A	Playing / ending flag("H":playing "L":stop) Access to Flash ROM ("H" : access "L" : not access)
6	VPLAY/SYNCREQ	IO		tune number pin Trigger signal ^{*1)} / Synchronous character request ("H" synchronization error)
7	GND	-	-	GND
8	VDD1.8_IN	I	- C	Core power supply input ^{*3)}
9	REG18	O	- B	Core power supply output ^{*3)}
10	STBY	I	- A	Standby ("H" oscillation stop) normally "L"
11	TESTEN	I	- A	Test Input("L" fixation)
12	VDD5_IN	-	-	Power supply input
13	SPISCK	O	- A	clock for serial SPI-ROM
14	SPISO	O	- A	serial output data to serial SPI-ROM
15	SPISI	I	- A	serial input data from serial SPI-ROM
16	SPICEB	O	- A	CEB for serial SPI-ROM
17	GND	-	-	GND
18	VVOLH/BFULLB	O	- A	PIN volume H/L selection/command buffer Full signal
19	APOFF	I	- A	DAC Circuit Power off
20	CLK16SEL	I	- A	Clock selection "H":16.384Mhz mode "L":4.096MHzmode
21	REFOUT	O	- B	LSI TEST Pin (attach capacitance(>10uF))
22	DACOUT	O	- B	DAC out
23	GND	-	-	GND
24	VDD5_IN	-	-	Power supply input
25	RESETB	I	I - B	Reset pin (low active)
26	SIO_ENBL	I	I - A	Selection of host interface(SIO or direction pin input ^{*1)}
27	XIN	I		Oscillation cell input ^{*2)}
28	XOUT	O		Oscillation cell Output ^{*2)}

*1) At SIO_ENBL="L", VSEL2, VSEL1, VSEL0 and VVOLH is valid, and SIO is invalid.

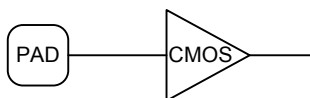
*2) At no setting CLK setting Register, Clock is 16.384MHz at CLK16SEL="H", 4.096MHz at CLK16SEL="L".

*3) pin#8 and pin#9 should be connected in a shortest pass, and attach capacitance(>10uF) as following figure.

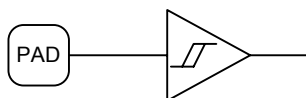


8.2. Circuit form

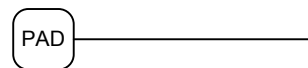
.Input Cell



(A) CMOS Input

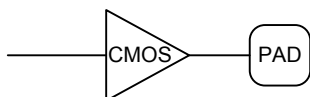


(B) SCHMITT Input

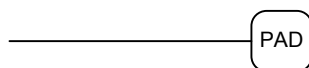


(C) Direct Input

.Output Cell

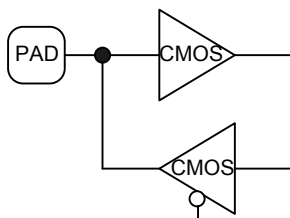


(A) CMOS Output



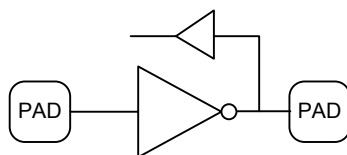
(B) Direct Output

.Bidir Cell

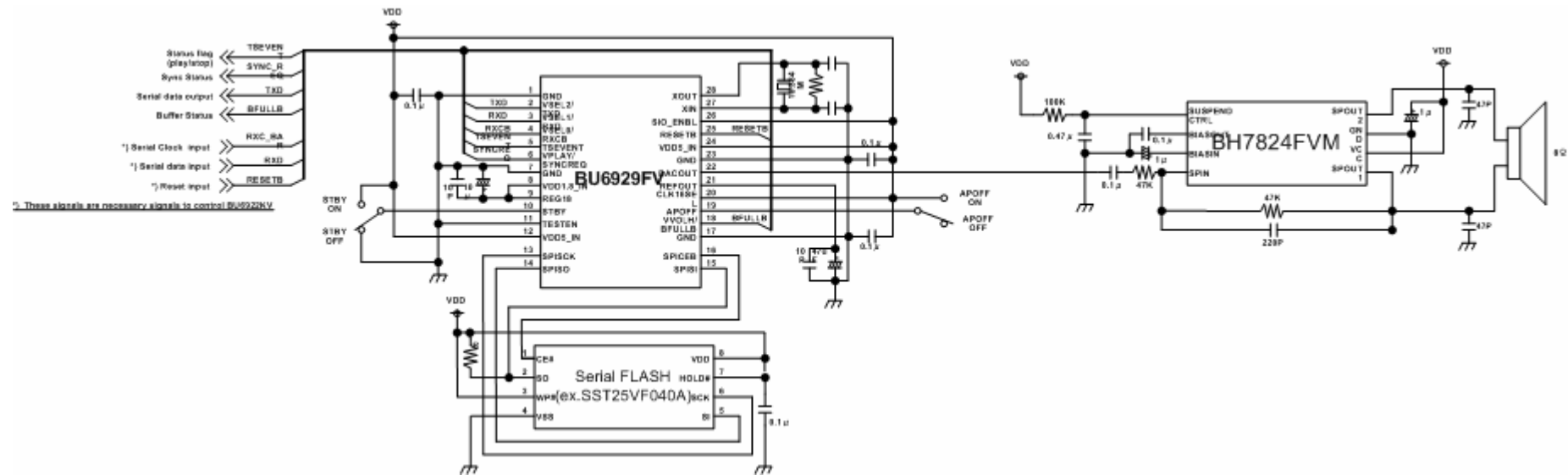


CMOS InOut

.OSC. Cell



9 . Application examples



10. Interface Timing

10.1. XIN

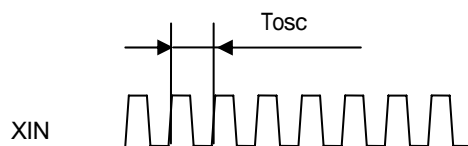


Figure 10-1. XIN Timing

Items	Name	Min	Typ	Max	Unit
Clock Frequency	fosc	-	16.384	-	MHz
		-	8.192	-	
		-	4.096	-	
		-	2.048	-	
Clock Duty	Wosc	45	-	55	%

*) Available CLK Frequency due to CLK setting Register and CLK16SEL pin.

10.2. RESETB

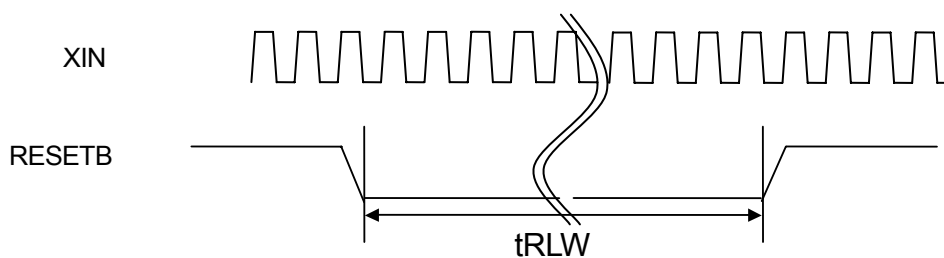


Figure 10-2. Reset timing

Item	Symbol	Min	Typ	Max	Unit
Reset "L" pulse width	t _{RLW}	16	-	-	CLK

SIO commands which is invoked within 1ms after reset is discarded because of the chip initialization stage.

10.3. Serial interface (RXCB, RXD, TXD)

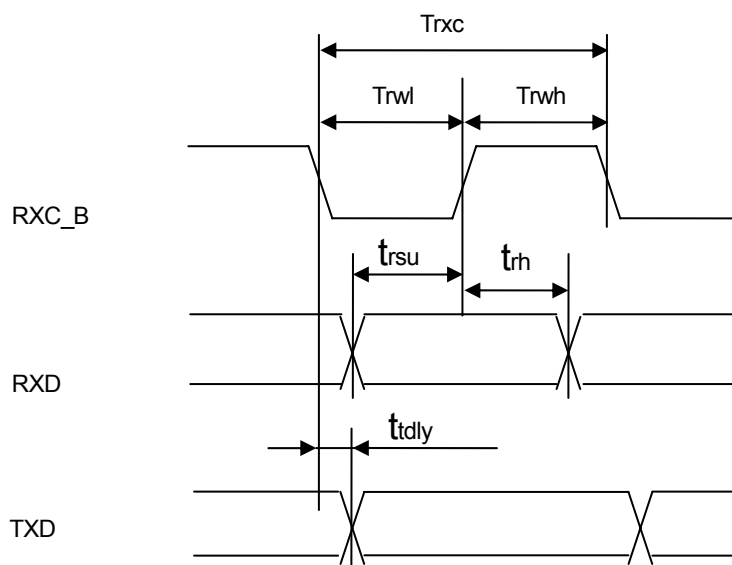


Figure 10-3. Serial interface timing

Item	Symbol	Min	Typ	Max	Condition	Unit
RXCB Cycle	T_{rxc}	$10 \cdot T_{osc}$	-	-	Normal play	ns
RXCB Lo Cycle	T_{rwl}	$4 \cdot T_{osc}$	-	-		ns
RXCB Hi Cycle	T_{rwh}	$4 \cdot T_{osc}$	-	-		ns
RXCB Cycle	T_{rxc}	$16 \cdot T_{osc}$	-	-	Flash R/W	ns
RXCB Lo Cycle	T_{rwl}	$7 \cdot T_{osc}$	-	-		ns
RXCB Hi Cycle	T_{rwh}	$7 \cdot T_{osc}$	-	-		ns
RXD Setup Time	t_{rsu}	$2 \cdot T_{osc}$	-	-		ns
RXD Hold Time	t_{rh}	$2 \cdot T_{osc}$	-	-		ns
TXD Output delay	t_{tdly}	-	-	$4 \cdot T_{osc}$		ns

10.4. Serial Flash ROM Interface

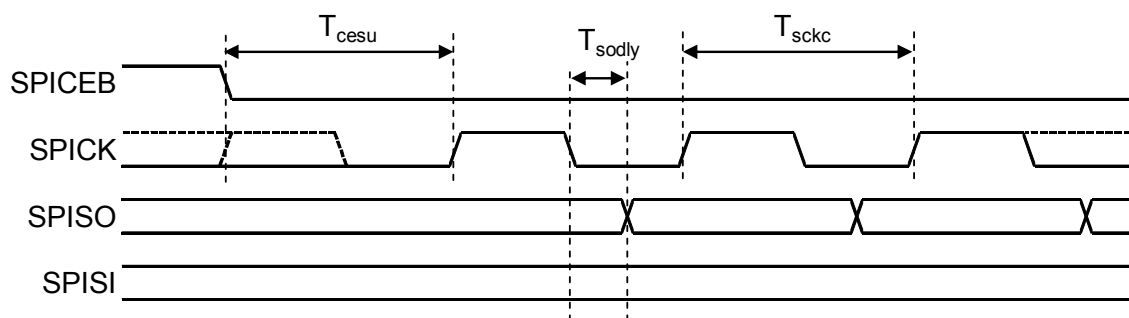


Figure 10-4-1. Serial Flash ROM Output

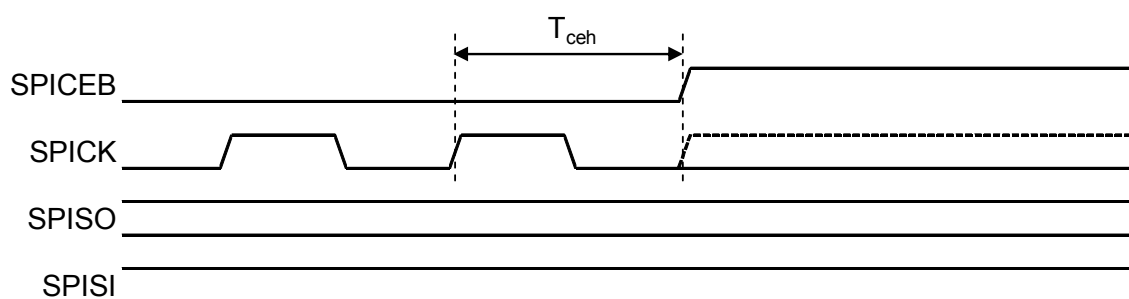


Figure 10-4-2. Serial Flash ROM Output

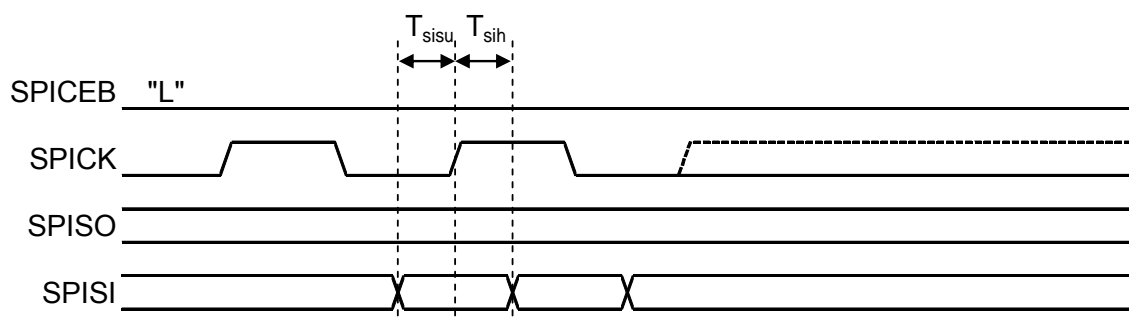


Figure 10-4-3. Serial Flash ROM Input Timing

Item	Symbol	Min	Typ	Max	Unit
SPISCK Cycle	T_{sckc}	-	T_{osc}	-	ns
SPICEB Setup Time	T_{cesu}	T_{osc}	-	-	ns
SPICEB Hold Time	T_{ceh}	T_{osc}	-	-	ns
SPISI Setup Time	T_{sisu}	10	-	-	ns
SPISI Hold Time	T_{sih}	3	-	-	ns
SPISO Output delay	T_{sodly}	-	-	10	ns

11 . System Clock

For System Input Clock, 16.384MHz/8.192MHz/4.096MHz/2.048MHz is available. *)

Followings are the table of parameters and performance.

System Clock	Value of CLK16SEL Pin	Setting from SIO	Numbers of channels	Available Performance
16.384MHz	"H"	-	1	16 ~ 128
8.192MHz	"H"	SCLK=001b	1	16 ~ 64
4.096MHz	"L"	—	1	16 ~ 64
2.048MHz	"L"	SCLK=001b	1	16 ~ 32

*) When SIO is not used, available system clock is 16.384MHz or 4.096MHz only.

12. Command Interface

Command interface is a serial interface receiving 8 or 16 bits command data synchronized with input clock, non parity, and sync-code (BFh). Sync-code is a fixed value, BF (h). The order of received data is LSB FAST.

12.1. Command communication

The command is communicated with clocks and the data as follows;

- (1) Serial data transfer clock input (RXC_BAR); retrieves data by rising edge. Frequency shall be equal to or less than 1MHz.
- (2) Serial data input (RXD); 8 bits or 16 bits serial data (LSB FAST).
- (3) Sync-code request output (SYNC_REQ); when this signal is "H", sync-code should be sent followed by the commands.

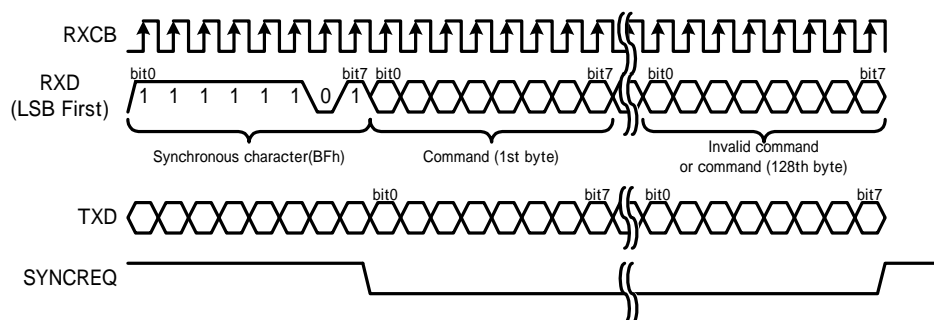


Figure 12-1. Serial interface time chart

At Figure.8-1, sync-code (more than 1 byte) is input before sending command. The maximum chunk of consecutive commands is 128 bytes after sync-code. If more than 129 bytes of command are consecutively input, 129th byte or later is ignored. Noted that, if 128th byte is the first byte of 2 byte command, 129th byte (2nd byte of 2 byte command) can be accepted.

If 128th byte is sync-code, it is ignored. In this case, SYNCREQ becomes "H" and its status becomes "waiting" for sync-code.

After command transfer is completed, interface shall be one of the following states until next command transfer.

1. continue to input sync-code.
2. stop clock (RXC_BAR)

12.2. Command Buffer Full Signal

There are 16 command stack buffer (“play command” and “tune command”) for each channel. BFULLB terminal becomes “L” when stack buffer of any channel becomes FULL. During “Sequence Play”, BFULLB does not become “L” even when Sequence buffer is overflown. Other commands not stated the above is activated just after being invoked without being qued.

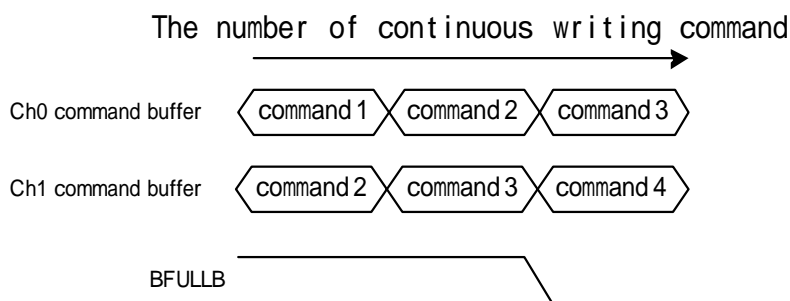


Figure 12-2. Command buffer FULL signal

12.3. Status signal

BU6929FV outputs the following status signals.

12.3.1. SYNCREQ

SYNCREQ is a sync-code request signal. "L" shows the state of synchronization, and "H" shows the state of “waiting for sync-code”, or synchronization error.

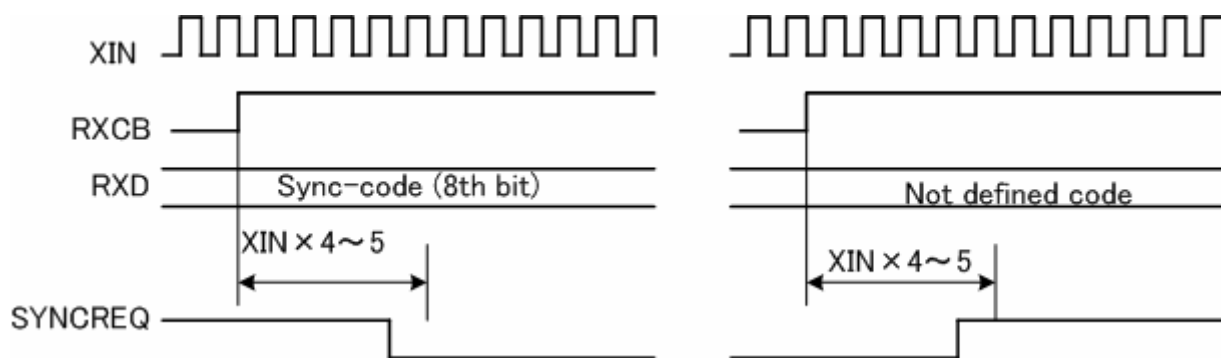


Figure 12-3-1. SYNCREQ timing

12.3.2. TSEVENT

TSEVENT signal becomes "H" when any of the track receives play command.

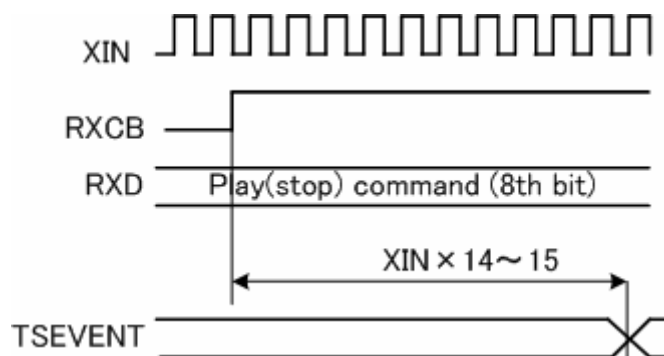


Figure 12-3-2a. TSEVENT timing

Noted that outputting sound has several ms delay after BU6929FV accepts play command. When stop commands are issued and accepted to all tracks, TSEVENT signal becomes "L". Noted also that there is several ms delay until the sound stops after stop command is issued.

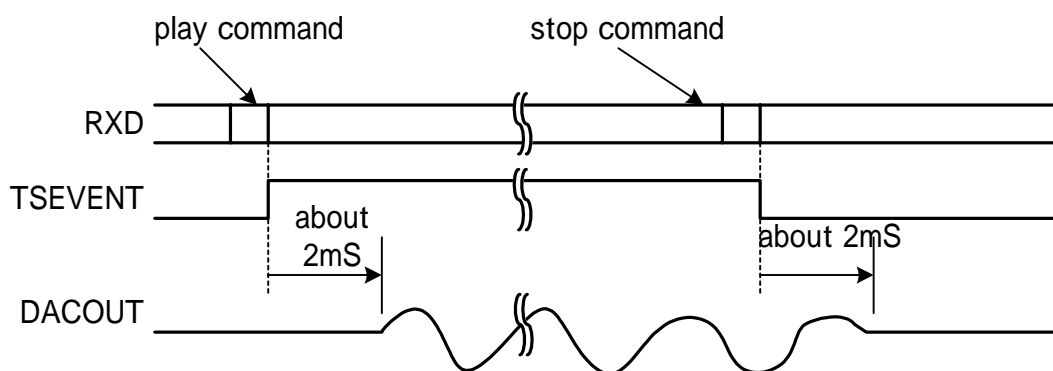


Figure 12-3-2b. TSEVENT and DACOUT timing

12.3.3. TXD

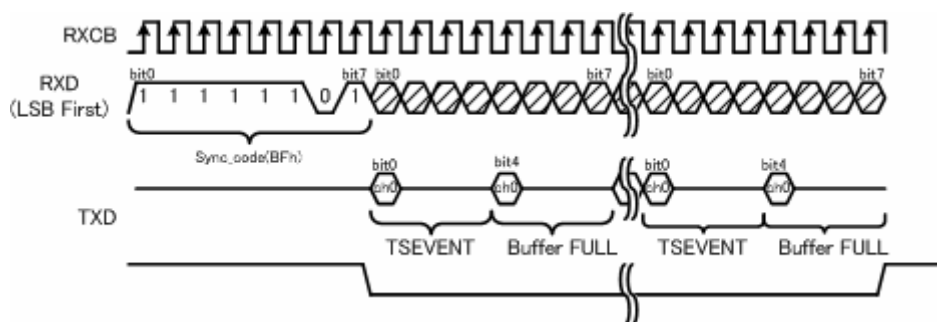


Figure 12-3-3. TXD output timing chart

bit	Item	Description
0	TSEVENT	Ch0 TSEVENT flag (H: playing)
4	Command buffer FULL	Ch0 BFULL flag (H: Buffer FULL)

*)After send STOP Command, please don't send any Command during 2 ~ 3mS(end of playback)
Operation is not guaranteed

12.4. Command details

12.4.1. Command list

All commands are 1 byte or 2 bytes command.

Table 12-4-1 shows the command list. Also, details of each command are described from the later page.

Table 12-4-1 command list

Content of command	Bit allocation(CMD[7:0])								
	7	6	5	4	3	2	1	0	
System setting	0	0	0	0	0	1	0	MODE	
System CLK setting*	0	0	0	0	1	SCLK			
Software reset**	0	0	0	1	1	1	1	1	
LOOP setting	0	1	0	0	1	Loop	0		
Pause	0	1	0	0	0	1	0		
Play	0	0	1	0	Mode	Loop	0		
Stop	0	1	0	0	0	0	0		
Sequence clear	0	1	0	1	1	0	0		
Buffer Clear*	0	1	0	1	1	1	0		
Tune selection	1	1	0	1	0	Mode	0		
	Tune(00h ~ DFh, F0 ~ FFh)								
Tune selection*	1	1	0	1	1	Mode	0		
	(Tune-256) (00h ~ DFh, F0 ~ FFh)								
Volume	1	0	0	1	Fade	Maste r	0		
	0	0	0	Vol					
Fade volume initial value	1	0	1	0	0	0	0		
	0	0	0	Vol					
Fade interval time	1	0	1	0	0	1	0		
	0	Time							
Flash control**	1	1	1	0	FlsCmd				
	(12-4-2 See the Detail of each command(14).)								
Synchronization	1	0	1	1	1	1	1	1	

*) new commands from BU6954FV/BU6952FV and BU6930/BU6929FV

***) new commands from BU6930/BU6929FV

Noted) When the command which is not specified is transmitted, operation is not guaranteed.

Commands of "Tune selection" and "play" is in buffered (max 16 commands). Other commands are executed just after a command is received.

12.4.2. Detail of each command

12.4.2.1. System setting command (1byte command)

Set "channel mode" when active

Content of command	Bit allocation(CMD[7:0])							
	7	6	5	4	3	2	1	0
System setting	0	0	0	0	0	1	0	Mode

Item	Number of bits	Initial value	Description	
Mode	1	0b	The system mode is set.	
			Set value	Function
			0b	NOP mode
			1b	active mode

12.4.2.2. System Clock Setting (1byte command)

Set system clock frequency (2.048~16.384MHz).

This command is also used for selecting sampling rate(16kHz or 32kHz).

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
System Clock setting	0	0	0	0	1	SCLK		

CLK16SEL=1, settings of clock are follows;

Item	Number of bits	Initial value	Description	
SCLK	3	000b	Setting of System Clock Frequency	
			Set value	Function
			000b	16.384MHz
			001b	8.192MHz
			010b	4.096MHz
			011b	2.048MHz
			100b	reserved
			101b	reserved
110b	(use for 16kHz sampling data.)			

CLK16SEL=0, settings of clock are follows;

Item	Number of bits	Initial value	Description	
SCLK	3	000b	Setting of System Clock Frequency	
			Set value	Function
			000b	4.096MHz
			001b	2.048MHz
			010b	reserved
			011b	reserved
			100b	reserved
			101b	reserved

***) When use 16kHz sampling**

16kHz sampling data and 32kHz sampling audio data are available.

When 16kHz sampling data is to be used, following settings are necessary.

System Clock	Audio Data Sampling	CLK16SEL	SCLK
16.384MHz	32kHz	1	000b
16.384MHz	16kHz	1	110b
8.192MHz	32kHz	1	001b
8.192MHz	16kHz	1	000b
4.096MHz	32kHz	1	010b
4.096MHz	16kHz	1	001b
2.048MHz	32kHz	1	011b
2.048MHz	16kHz	1	010b
4.096MHz	32kHz	0	000b
2.048MHz	32kHz	0	001b
2.048MHz	16kHz	0	000b

***When Not use SIO, System CLK is 16.384MHz or 4.096MHz only.**

12.4.2.3. Software reset (1byte command)

This command is for MCU to reset a chip by software.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Software reset	0	0	0	1	1	1	1	1

12.4.2.4. Play command (1byte command)

Play a tune.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Play	0	0	1	0	Mode	Loop	0	

Item	Number of bits	Initial value	Description	
Mode	1	0b	Play mode is set.	
			Set value	Function
			0b	Normal play
			1b	Sequencer is executed
Loop	1	0b	Loop control of Channel is set.	
			Set value	Function
			0b	Loop disable
			1b	Loop enable

12.4.2.5. Stop command (1byte command)

Stop a tune.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Stop	0	1	0	0	0	0	0	

*)During Playback phrase, when you send STOP Comaand and next play command,
Need more than 10mS between STOP command and next play command.

12.4.2.6. Pause command (1byte command)

Pause or resume at a tune.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Pause / resume	0	1	0	0	0	1	0	

12.4.2.7. LOOP setting command (1byte command)

Set looping.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
LOOP setting	0	1	0	0	1	Loop	0	

Item	Number of bits	Initial value	Description	
Loop	1	0b	Set loop control.	
			Set value	Function
			0b	Loop disable
			1b	Loop enable

The usage of this command is to disable loop mode during playing with loop mode. The command is also valid for sequencer mode. When disabling loop during playing tunes at sequencer mode, sequencer stops at the end of the tune in the sequencer list. For example, when five tunes are set for looping, it stops playback at the end of 5th tune after “disable loop” command is issued.

12.4.2.8. Sequence clear command (1 byte command)

Sequence set by selection command is cleared.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Sequence clear	0	1	0	1	1	0	0	

12.4.2.9. Buffer clear command (1 byte command)

Clear the buffer for tune-buffer and play-buffer (normal play buffer).

Use sequence buffer clear when sequence buffer needs to be cleared.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Buffer clear	0	1	0	1	1	1	0	

12.4.2.10. Tune selection command (2 Bytes command)

Set tune number to be played.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Selection (#0 ~ #223) (#240 ~ #255)	1	1	0	1	0	Mode	0	
Tune ^{*)}								

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Selection (#256 ~ #479) (#496 ~ #511)	1	1	0	1	1	Mode	0	
Tune ^{**)*)}								

^{*)} e0 h-efh (#224-#239) and 1e0h-1efh (#480-#495) are prohibition of use because of a System Reserve domain. The operation is not guaranteed when set up accidentally at the above area.

^{**)} Selection of 100h-1dfh (#256-#479) and 1f0h-1ffh (#496-#511) sets up (the selection number -256).

Item	Number of bits	Initial value	Description		
Mode	1	0b	Set tune-selection mode.		
			Set value	Function	Number of command bytes
			0b	Specify normal tune	2 bytes
			1b	Add to sequence	2 bytes
Tune	8	00h	Select a tune number.		

12.4.2.11. Volume command (2bytes command)

Control volume.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Volume	1	0	0	1	Fade	Master	0	
	0	0	0	Vol				

Item	Number of bits	Initial value	Description	
Fade	1	0b	Set Fade in/out. It fades from the initial value to volume value specified by this command.	
			Set value	Function
			0b	Disable
1b	Enable			
Master	1	0b	Set validity of volume value. When fade-in/fade-out mode, Set "0" at each Channel.	
			Set value	Function
			0b	Disable
1b	Enable			
Vol	5	1Fh	Set the volume value. 0 = mute, 31 = maximum volume.	

12.4.2.12. Fade volume initial value set command (2bytes command)

Set initial value for executing fade in/out.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Fade volume initial value	1	0	1	0	0	0	0	
	0	0	0	Vol				

Item	Number of bits	Initial value	Description
Vol	5	1Fh	Set Volume value. 0 = mute, 31 = maximum volume.

12.4.2.13. Fade interval time set command (2bytes command)

Set interval time value for fade in/out.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Fade interval of time	1	0	1	0	0	1	0	
	0	Time						

Item	Number of bits	Initial value	Description
Time	7	00h	Interval time at fading is set. The unit is 1ms. ^{*)}

^{*)} Interval time of fade-in/fade-out is $16/T$ ms (T: system CLK frequency) . For example, when system SCLK=16/T (MHz), the interval is 1ms.

12.4.2.14. Serial Flash ROM control command

By the command from SIO, BU6929FV access external ROM via SPI interface. 13 commands are provided (2bytes command).

Command setting value		Symbol	Description
The 1st byte	The 2nd byte		
E0h	Data to be written	WRSR	Write status register
E1h	Sector address	BP	Byte program
E2h	Sector address	PP	Page program
E3h	Sector address	READ	Lead data byte
E4h	BFh	WRDI	Write disable
E5h	-	RDSR	Read status register
E6h	BFh	WREN	Write enable
E7h	-	RDID	Read ID
E8h	BFh	RES	Return from deep power down
E9h	BFh	DP	Deep power down
EAh	BFh	CE	Chip erase
EBh	Sector address	SE	selector erase
EFh	BFh	AC2B	ROM address control (2 bytes)

The access unit for Flash ROM from SIO is 1 sector, which is set to 64kByte(65,536Byte). Details for access is described at Chapter 13.

12.4.2.15. Synchronization command(1byte command)

This is a command for establishing synchronization.

Content of command	Bit allocation (CMD[7:0])							
	7	6	5	4	3	2	1	0
Synchronization	1	0	1	1	1	1	1	1

The maximum chunk of consecutive commands is 128 bytes. Noted that, if sync-code is input after command transfer, sync-code are accepted.

If more than 129 bytes of command are consecutively input, 129th byte or later is ignored. Noted that, if 128th byte is the first byte of 2 byte command, 129th byte (2nd byte of 2 byte command) can be accepted.

If 128th byte is sync-code, it is ignored. In this case, SYNCREQ becomes "H" and its status becomes "waiting" for sync-code.

13. command sequence to access Serial Flash ROM

This chapter (13.1~13.9) describes details of the commands for accessing SPI Flash ROM.

Following description is assuming that Flash ROM is controlled by 3-byte address).

13.1. Writing to SPI-interface FLASH ROM

The followings are description for writing SPI Flash ROM from SIO

- (1) Sending Sync Req command(BFh).
- (2) Sending Write-enable command(E6h, BFh).
- (3) Sending Program command. Program commands are different along with Flash ROM type.
At chunk of bytes are 256bytes for writing(SPANSION, ST-Micro), a command of "page program" is set. At writing 1 byte(SST), a command of "Byte Program" is set.
- (4) At page program mode, sending 65,536bytes(64kbytes) consequently checking if 256 bytes are done to be written by "BUSY" pin. At byte program mode, sending 1byte by checking if 1byte is done to be written by "BUSY" pin.
- (5) Sending software reset command(1Fh).

*) Before writing data, need to unprotect a block-protect register in Status registers at Flash ROM. See Chapt9-4 for the method of writing status registers. Erase command for a sector(or sectors) shall be invoked before writing data into a sector or sectors.

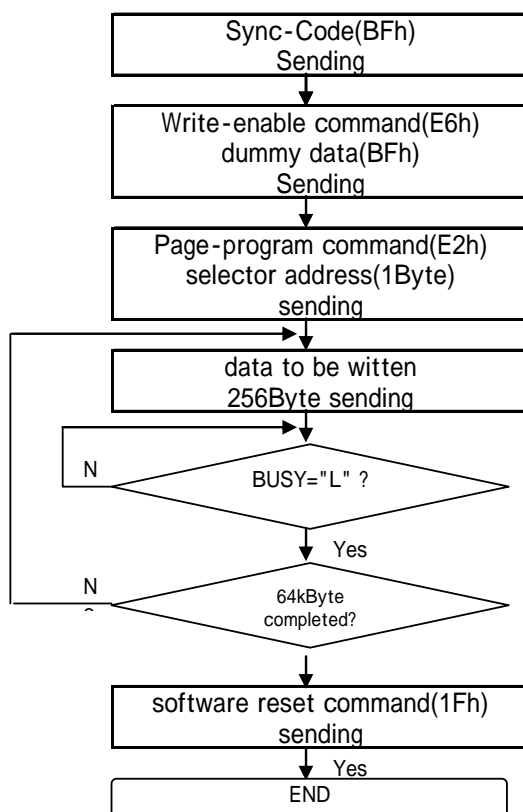


Figure13-1a. Sequence for writing data into Flash ROM(PP)

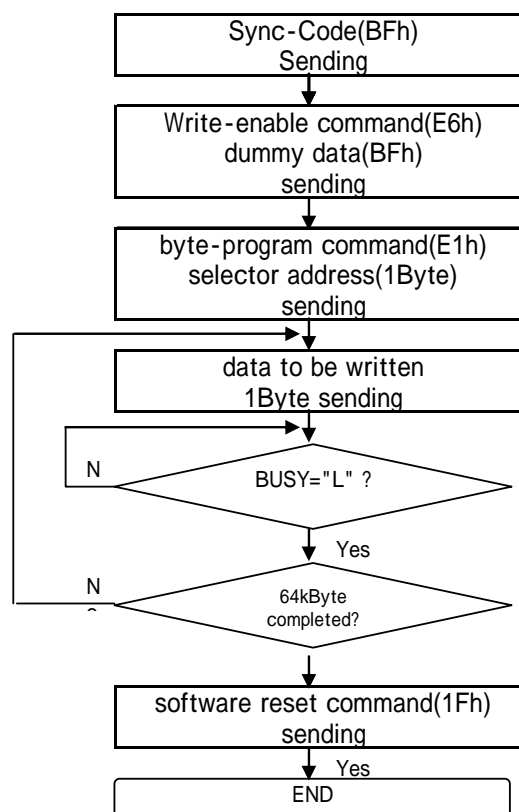


Figure913-1b. Sequence for writing data into FlashROM(BP)

13.2. Reading data from external FLASH ROM

This command is to read data from external Flash ROM. For example, this command is used for verifying data in Flash ROM. Unit for reading data is 64kBytes. When reading data, send "BF" on RXD.

Followings are procedure for reading.

- (1) sending Sync-code (BFh).
- (2) sending "read data byte" command(E3h).
- (3) After checking that BUSY pin is "L", read 64kByte data consecutively. During reading data, send "BF" on RXD.
- (4) After reading 64kByte data, send Software reset command(1Fh).

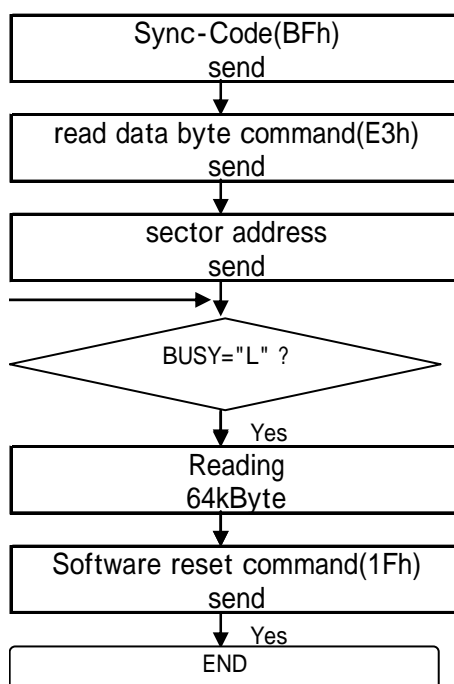


Figure 13-2. read data sequence

13.3. Reading JEDEC-ID of external FLASH ROM

This command is for reading device info of external flash ROM.

During receiving 3bytes of JEDEC-ID, send BFh at RXD pin.

Followingings are the command sequence.

- (1) sending Sync-Req command(BFh).
- (2) Sending read-ID command(E7h).
- (3) After confirming that BUSY pin is "L", read 3bytes data from TXD. When reading 3bytes, send BFh at RXD pin.
- (4) Sending software reset command(1Fh).

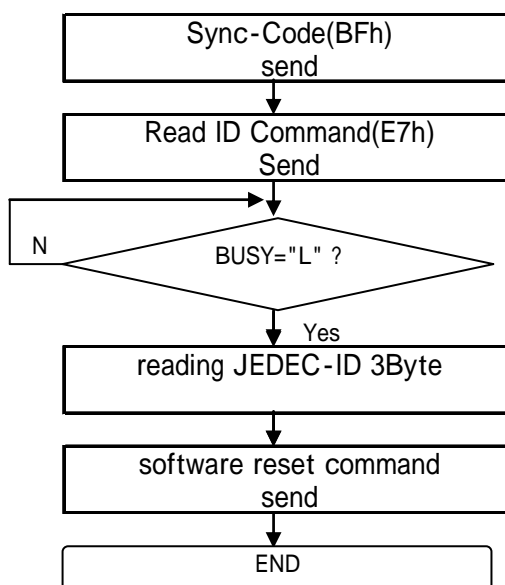


Figure 13-3. JEDEC-ID reading sequence

13.4. Setting status register in an external Flash ROM

This command is setting status register in external ROM. The access to Flash ROM is valid after this command is invoked. Block test function shall be always unlocked when writing/erasing data into Flash ROM. See flash ROM manual for details of status registers.

Followings are procedure to set value into status registers.

- (1) Sending a Sync-Code (BFh).
- (2) Sending a write-enable command(E6h, BFh).
- (3) Sending a write-status register command(E0h).
- (4) Sending value into a status register.

*) A certain time is required until the value is set after sending a command. For the exact time, see the manual of flash ROM.

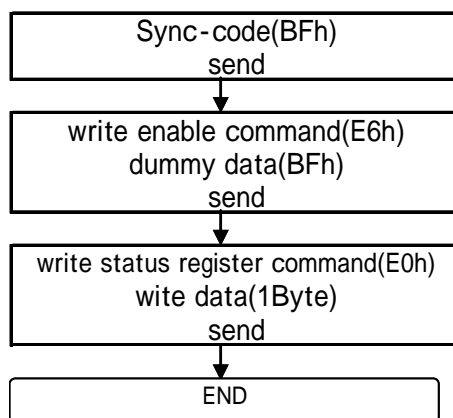


Figure13-4 writing sequence for status-register

13.5. Reading status registers in an external Flash ROM

This command is to read status register in an external flash ROM. When reading status register, send Sync-Code(BFh) command on RXD. See manuals of flash ROM device for the details of status register. Followings are the procedure for reading status registers.

- (1) Sending Sync-Code(BFh).
- (2) Sending read-status register command(E5h).
- (3) Read 1 byte data from TXD after checking that BUSY-pin is "L". BHh shall be sent on RXD.

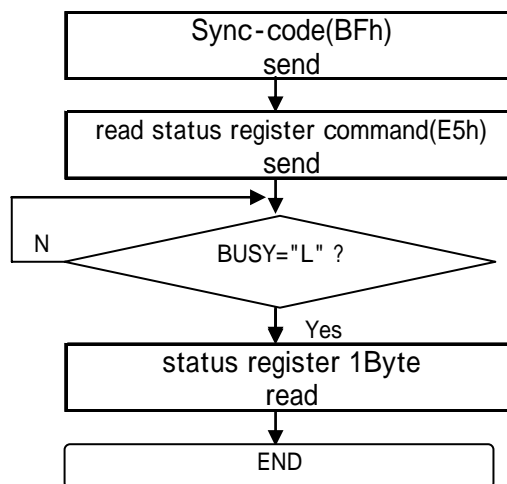


Figure 13-5 reading sequence for status-register

13.6. Erasing data in an external Flash ROM

For erase function for an external ROM, 2 commands are supported, chip-erasing and sector-erasing. Chip-erasing command erases all area in Flash ROM at once. A sector-erase command erases one sector, which has 64kbyte area.

The following the procedure for chip-erasing command.

- (1) sending Sync-code (BFh).
- (2) Sending write-enable command(E6h, BFh).
- (3) Sending Chip-erase command(Eah, BFh).
- (4) Wait for the necessary time to erase flash ROM.

See Flash ROM manual for necessary erase time.

Before chip erase, Block protect register (Flash ROM) shall be unlocked.

The procedure of status-register , see Chapt13-4.

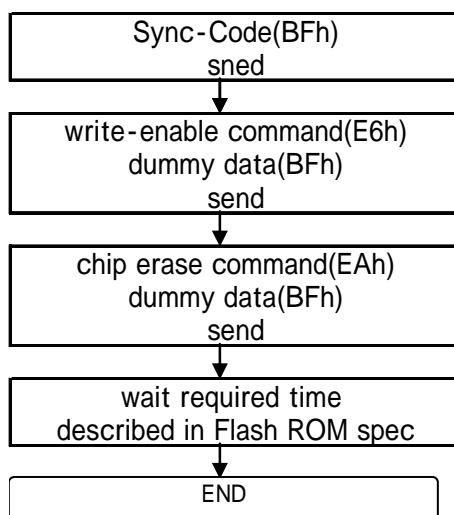


Figure 13-6a. Chip Erase Sequence

Followings are steps for sector erase.

- (1) Sending Sync-req command(BFh).
- (2) Sending write-enable command(E6h, BFh).
- (3) Sending sector-erase command(Ebh).
- (4) Sending a sector address(1byte) to be erased.
- (5) Waiting for erase time required for each Flash ROM.

See Flash ROM manual for necessary erase time.

Before chip erase, Block protect register (Flash ROM) shall be unlocked.

The procedure of status-register, see Chapt13-4.

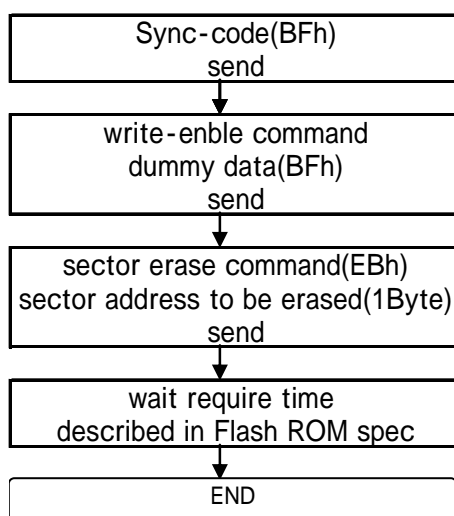


Figure13-6b. Sector-erase-sequence

13.7. Deep power down of external Flash ROM and restoring from Deep power down

This command is setting deep power down mode (and restoring deep power down mode) into external Flash ROM. See Flash ROM manual which is provided by the Flash ROM manufactures for details.

Noted that SST Flash ROM does not support Deep Power down mode.

Deep Power Down

- (1) Sending Sync-code (BFh).
- (2) Sending deep power down command(E9h, BFh).

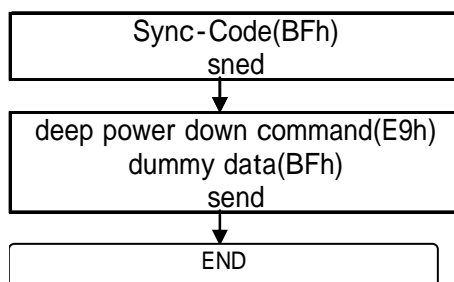


Figure 13-7a. Deep Power down sequence

Restoring Deep Power Down

- (1) Sending Sync-Code (BFh).
- (2) Sending restoration command from deep power down(E8h, BFh)

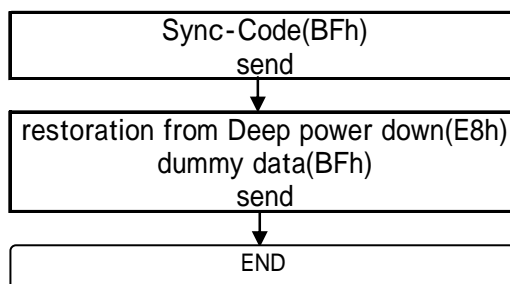


Figure13-7b. Sequence for restoring deep power down

13.8. ROM Address Control command

This command is used for SPI interface Flash/EEPROM whose address is controlled by 2 bytes, and valid only for playback. The default setting of the chip after Reset is 3 bytes address mode, so need to set 2 bytes address mode by SIO before playback tunes when ROM is 2bytes-mode.

Use hardware reset (RESETB='L') when reset address mode. Software reset command is not valid.

When 2bytes address mode, serial Flash control commands are all invalid. So when update Flash ROM/EEPROM, re-write data at off-line tools like ROM writer.

Followings are the commands;

- (1) Sending Sync-code (BFh).
- (2) Sending ROM address control command(EFh, BFh).

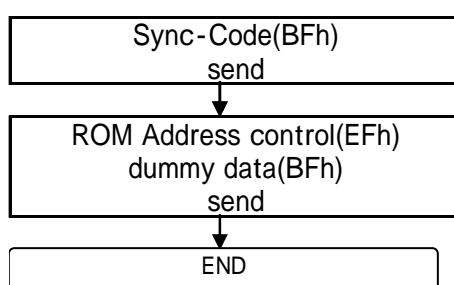


Figure 13-8. ROM Address control sequence

13.9. Available Serial Flash ROM

Following Serial Flash ROM is available Serial Flash ROM. Others are not guaranteed.

SST

- SST25VF512B(512kbit)
- SST25VF040B (4Mbit)
- SST25VF080B (8Mbit)
- SST25VF016B (16Mbit)
- SST25VF032B^{*)} (32Mbit)

SPANSHION

- S25FL004A (4Mbit)
- S25FL008A (8Mbit)
- S25FL016A (16Mbit)
- S25FL032A^{*)} (32Mbit)

ST Micro

- M25P40 (4Mbit)
- M25P80 (8Mbit)
- M25P16 (16Mbit)
- M25P32^{*)} (32Mbit)

*) These Flash ROMs have not been tested, but some of the family products are tested. Therefore, these flash ROMs should be working correctly.

14. Sequencer

Control of sequencer and addition/clear of tune in a sequencer mode are done by play command and tune-selection command respectively. Each track has a sequencer independently. The maximum numbers of tunes registered to sequencer are 16. The example of sequencer is shown below;

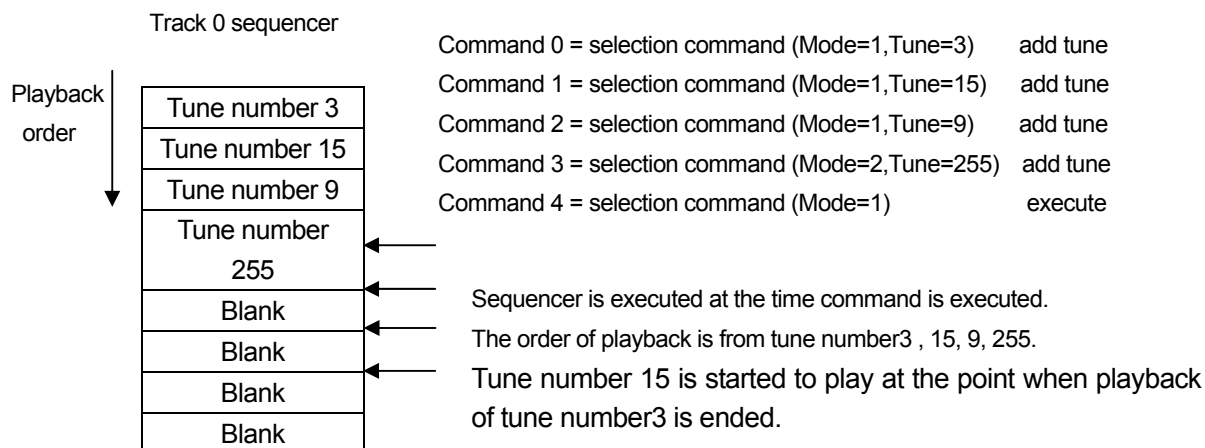


Figure14-1. Example of sequencer

- Addition of a tune to sequencer

It is done by selection command (Mode=1).

When sequencer is stopped by stop command while sequencer is running, or when additional command is issued after execution of sequencer is finished, a tune is added at the end of sequencer list.

- Sequencer clear

Clear of sequencer is done by tune-selection command (Mode=2). When sequencer clear is issued, all tunes in the list are cleared shown in figure 10-1. For changing the order of tunes, it is necessary to clear sequencer once, and add tune by tune-selection command. Clear command during sequencer is running is ignored.

-tune add command after 16 tunes are already registered in a sequencer

Tune add command is discarded when 16 tunes are already registered in a sequencer. Noted that BFULLB is not active in a sequencer mode

15. Loop playback

The order of playback when sequencer is running with LOOP mode is from tune number 3→15→9→255→3→15→9→..... as described in Figure 15-1.

Also, when disabling LOOP command is issued while LOOP is on, sequencer is stopped at the end of next tune of the tune currently running.

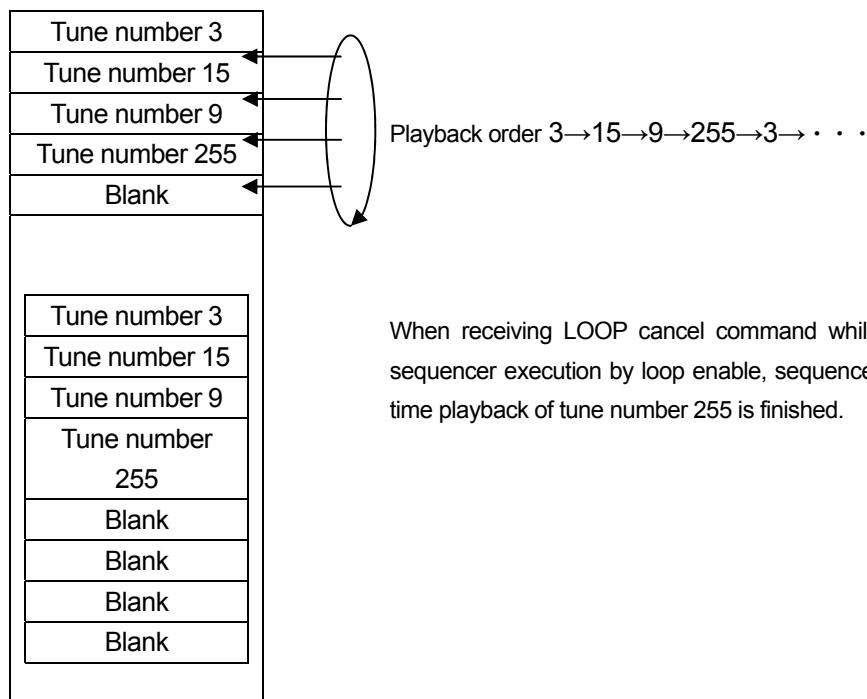


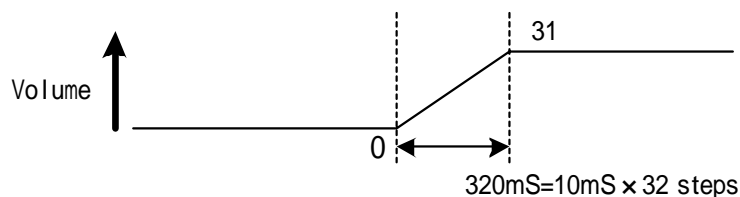
Figure15-1. Loop processing by the sequencer

16. Fade

BU6929FV supports the function of fade in/out.

The example of fade in is described below.

1. Fade volume initial value command (Vol=0)
2. Fade interval time command (Time=10)
3. Volume command (Fade=1, Master=0, Vol=31) ---Fade in is executed when this command is issued.



In this example, volume is increased from 0 to 31 in the period of 320 ms.

In the case that volume value of initial value command is bigger than the volume set by volume command, fade out is executed.

17. Direct Pin Input mode

When SIO_ENABLE="L", command input is not from SIO, but from PIN direct.

At PIN direct mode, just set tunes from #0 to #7 and volume (High or Low) by "VSEL" pin for tune playback.

17-1. timing chart at direct pin input

At up edge timing of VPLAY pin, tune number is selected by VSEL [2:0]. After VPLAY up-edge, wait minimum 30 clocks for next command input. Selected tune is played only once (Fig.17-1a).

(1) In the case that #7 tune is selected to be played

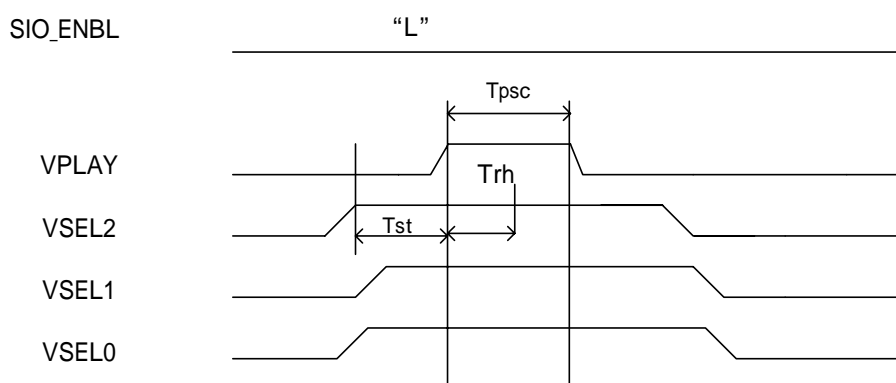


Figure 17-1a. Direct Pin input timing chart

Table 17-1 Direct pin input timing chart

Item	Symbol	Min	Typ	Max	Unit
VPLAY Enable period	Tpsc	16	-	-	CLK
VSEL Setup time	Tst	1	-	-	CLK
VSEL Hold time	Trh	0	-	-	CLK

(2) In the case that #7 and #6 of tune are selected to play in sequentially

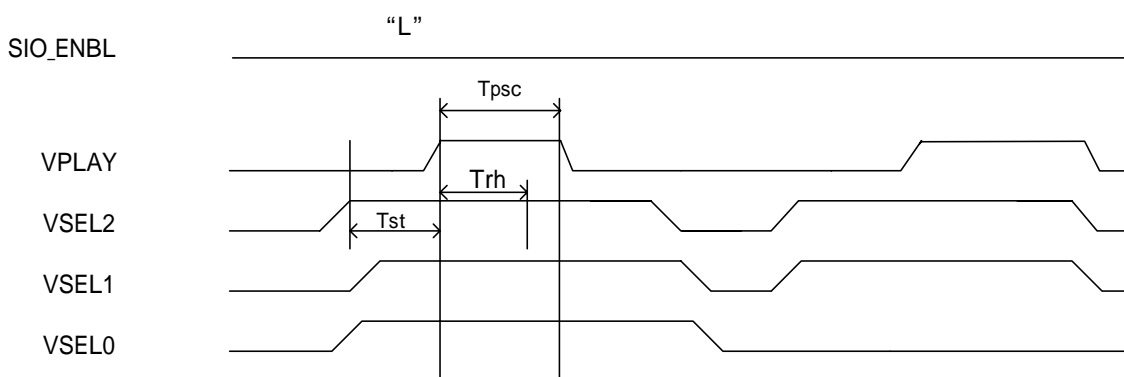


Figure.17-1b. 2 tunes sequential play timing chart

Maximum 16 tunes are enable to buffering, and playback sequentially.

17.2. Volume control from Pin Direct

When SIO_ENABLE = "L", command input mode is direct pin mode, and volume is also from pin direct.

VOLH pin is "L", volume is set small, and "H" is set large. Noted that this command is valid just after command is invoked.

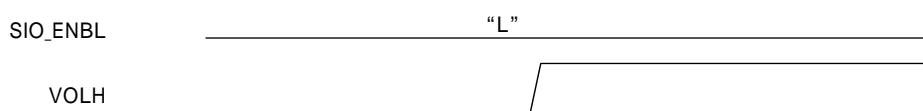


Figure 17-2. Volume setting from Pin di

18. RESET sequence and AP OFF pin and STBY pin

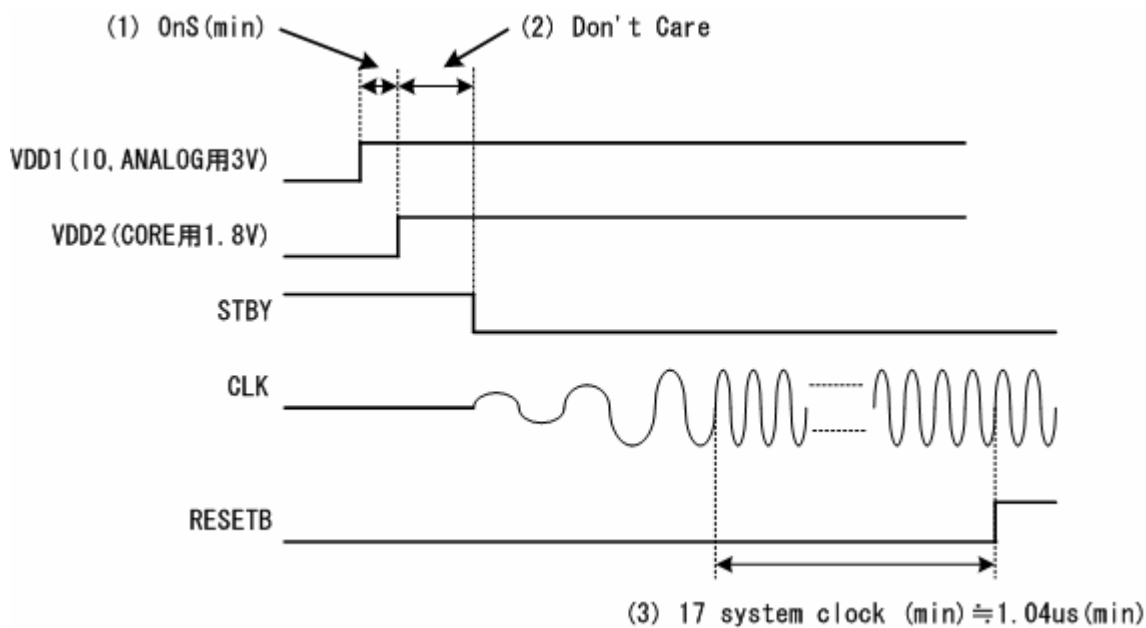
Please follow the below steps at initial sequence.

Internal regulator and DAC start working by setting APOFF to "L".

Clock is oscillated by STBY signal setting to "L". Reset is not invoked automatically.

When initial, Reset procedure shall be done as follows;

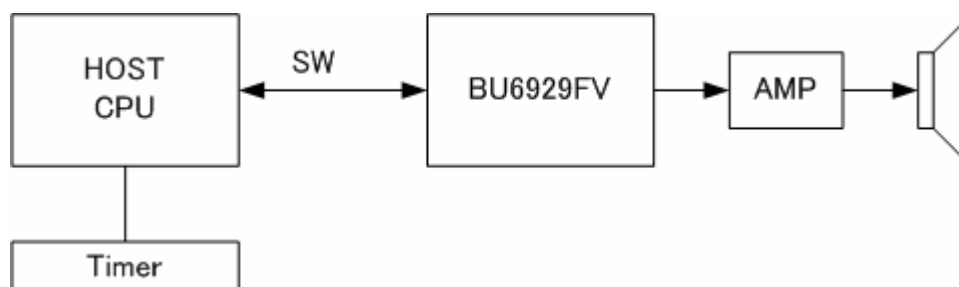
1. Set APOFF pin to "L".
2. Set STBY signal to "L" (Clock is oscillated).
3. input 17 clock or more after RESETB is "L"
4. Set RESETB signal to "H".



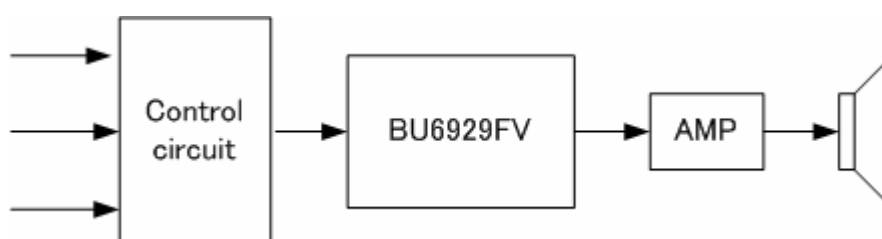
When invoke APOFF (setting to "H"), STBY shall be "H" first.

19. Example of system block diagram using BU6929FV and example of command setting

Examples of system block diagram using BU6929FV is shown in Figure 19-1, and also example of command setting is listed below



Example of HOST-BU6929FV connection



Example of CPU-less connection

Figure 19-1. System Example

Example of command setting

The example shows the case when playing tunes and executing fade out at the end of the sequence. For the tune number to play, channel 0 loop from 0th to 5th tune, and channel 1 repeats 10th tune.

Table 19-1 Command setting example

Procedure	Operation	Command setting value		Content
		1st byte	2nd byte	
1	Synchronization command issue	BFh	—	Synchronization command is established.
2	System setting command issue	05h	—	changes from NOP to play mode
3	Selection command issue	D4h	00h	adding tune #0 into sequence buffer
		D4h	05h	adding tune #5 into sequence
4	Volume setting command	90h	0Fh	The volume is set to 15.
5	Fade volume initial setting	A0h	0Fh	Initial value is set to 15.
6	Fade time setting	A4h	70h	set at 127ms intervals.
7	Play	2Ch	—	played with sequencer and loop. (0→5→0→5-----)
8	Volume command setting	98h	00h	Volume is set to "0". Start fade out.
9	Stop command	40h	—	stop

20. Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Others

In case of use this LSI, please peruse some other detail documents(Technical note, Application note and so on).