

MM74HCT04 Hex Inverter

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH} , t_{PHL} = 12 ns (typ)
- Low power: 10 μ W at DC, 3.7 mW at 5 MHz
- High fanout: ≥ 10 LS loads
- Inverting, triple buffered

General Description

The MM74HCT04 is a logic function fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. This device is input and output characteristic as well as pin-out compatible with standard 74LS logic families. The MM74HCT04, triple buffered, hex inverters, features low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Ordering Information

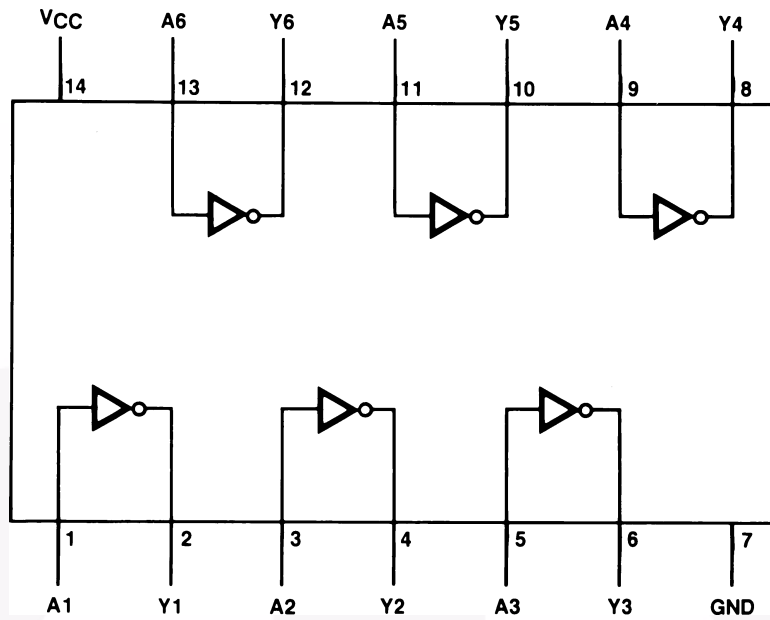
Order Number	Package Number	Package Description
MM74HCT04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HCT04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5 to +7.0V
V_{IN}	DC Input Voltage	−1.5 to $V_{CC}+1.5V$
V_{OUT}	DC Output Voltage	−0.5 to $V_{CC}+0.5V$
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	−65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: −12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	°C
t_r, t_f	Input Rise or Fall Times		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		T _A = −40°C to 85°C	T _A = −55°C to 125°C	Units
			Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V _{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 20μA	V _{CC}	V _{CC} − 0.1	V _{CC} − 0.1	V _{CC} − 0.1	V
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4.0mA, V _{CC} = 4.5V	4.2	3.98	3.84	3.7	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4.8mA, V _{CC} = 5.5V	5.2	4.98	4.84	4.7	
V _{OL}	Maximum LOW Level Voltage	V _{IN} = V _{IH} , I _{OUT} = 20μA	0	0.1	0.1	0.1	V
		V _{IN} = V _{IH} , I _{OUT} = 4.0mA, V _{CC} = 4.5V	0.2	0.26	0.33	0.4	
		V _{IN} = V _{IH} , I _{OUT} = 4.8mA, V _{CC} = 5.5V	0.2	0.26	0.33	0.4	
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0μA		2.0	20	40	μA
		V _{IN} = 2.4V or 0.5V ⁽³⁾		0.3	0.4	0.5	mA

Note:3. This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics

$V_{CC} = 5.0V$, $t_r = t_f = 6ns$, $C_L = 15pF$, $T_A = 25^\circ C$ (unless otherwise noted)

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
t_{PLH} , t_{PHL}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

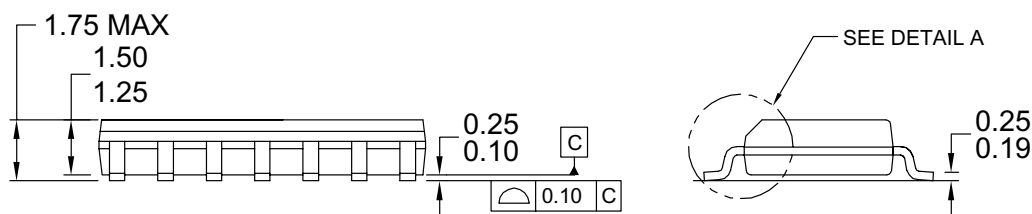
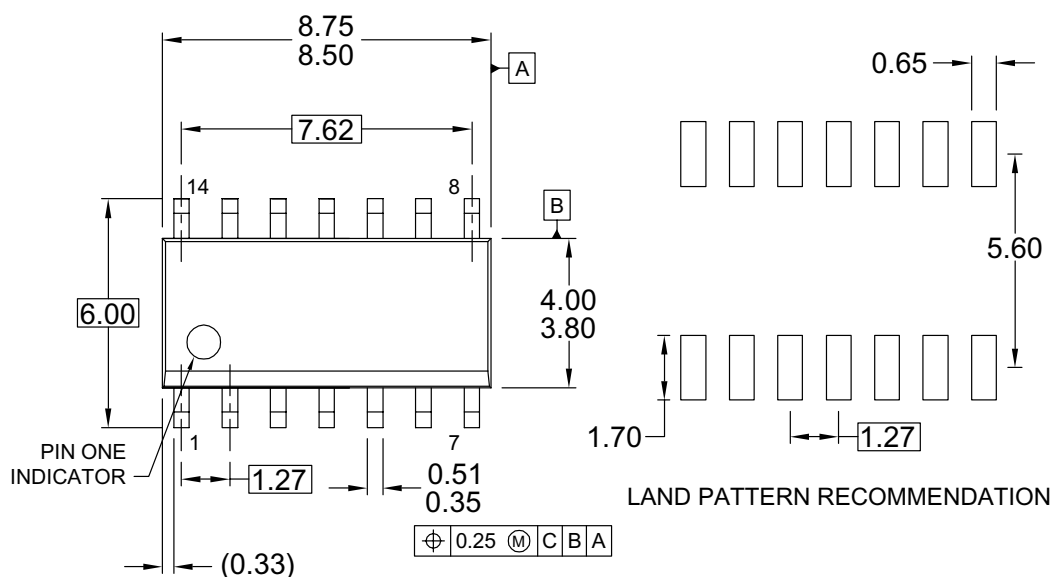
$V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6ns$, $C_L = 50pF$ (unless otherwise noted)

Symbol	Parameter	Conditions	T _A = 25°C		T _A = −40°C to 85°C	T _A = −55°C to 125°C	Units
			Typ.	Guaranteed Limits			
t _{PLH} , t _{PHL}	Maximum Propagation Delay		14	20	25	30	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C _{PD}	Power Dissipation Capacitance	(4)	20				pF
C _{IN}	Input Capacitance		5	10	10	10	pF

Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD:
SOIC127P600X145-14M
E) DRAWING CONFORMS TO ASME Y14.5M-1994
F) DRAWING FILE NAME: M14AREV13

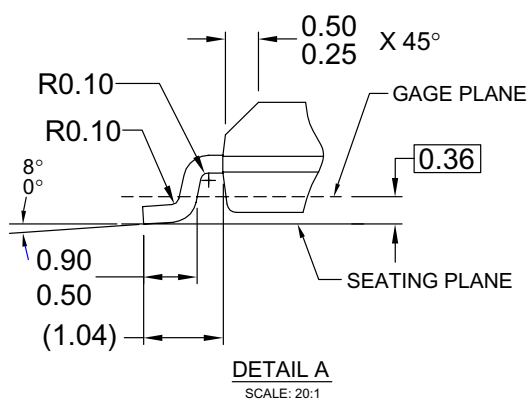


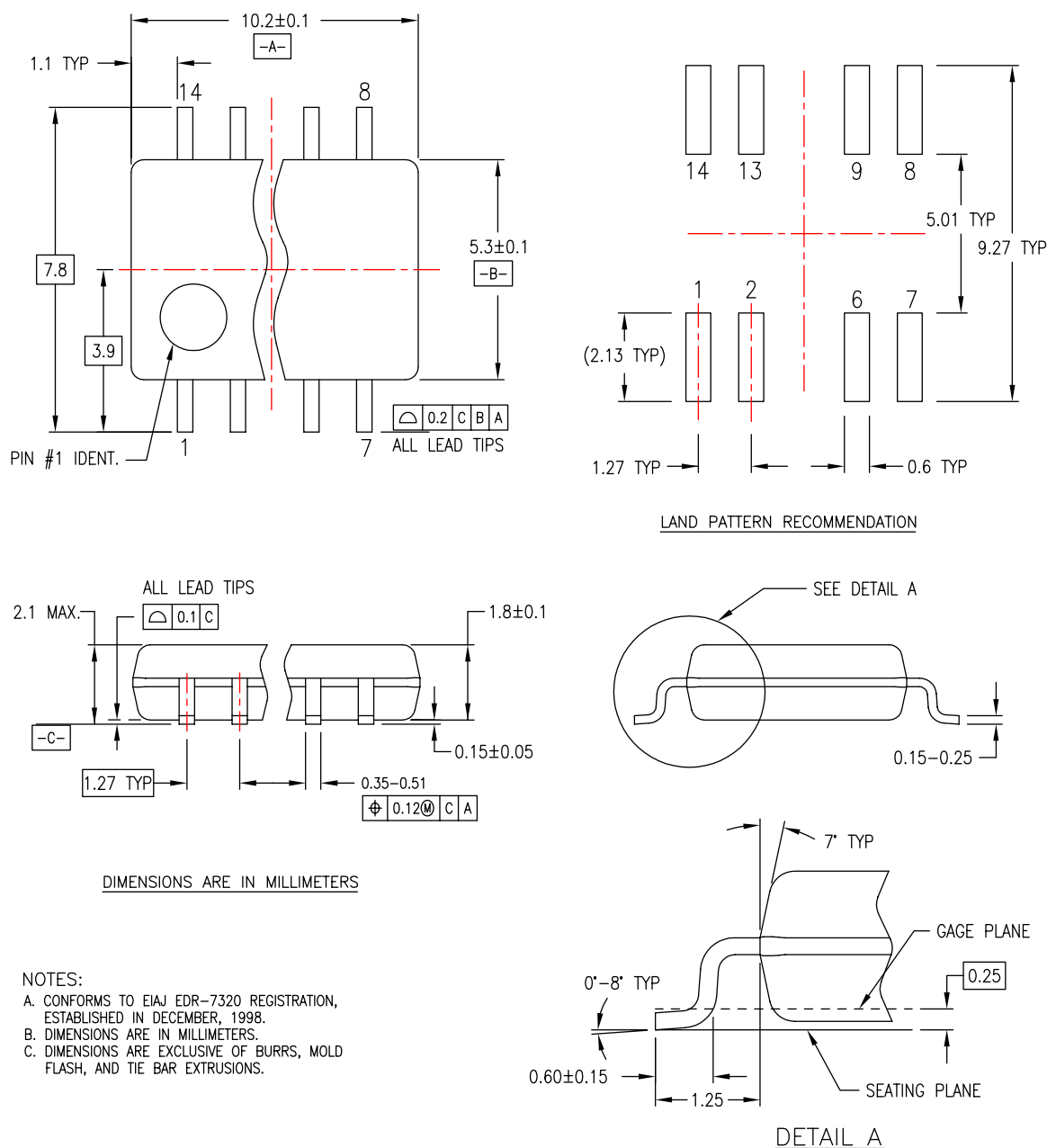
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)**NOTES: UNLESS OTHERWISE SPECIFIED**

THIS PACKAGE CONFORMS TO

A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSIONS.D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx [®]	FPS [™]	PDP-SPM [™]	SupreMOS [™]
Build it Now [™]	FRFET [®]	Power220 [®]	SyncFET [™]
CorePLUS [™]	Global Power Resource SM	POWEREDGE [®]	SYSTEM [®]
CROSSVOLT [™]	Green FPS [™]	Power-SPM [™]	GENERAL [®]
CTL [™]	Green FPS [™] e-Series [™]	PowerTrench [®]	The Power Franchise [®]
Current Transfer Logic [™]	GTO [™]	Programmable Active Droop [™]	the power [®]
EcoSPARK [®]	i-Lo [™]	QFET [®]	franchise
EZSWITCH [™] *	IntelliMAX [™]	QS [™]	TinyBoost [™]
	ISOPLANAR [™]	QT Optoelectronics [™]	TinyBuck [™]
	MegaBuck [™]	Quiet Series [™]	TinyLogic [®]
Fairchild [®]	MICROCOUPLER [™]	RapidConfigure [™]	TINYOPTO [™]
Fairchild Semiconductor [®]	MicroFET [™]	SMART START [™]	TinyPower [™]
FACT Quiet Series [™]	MicroPak [™]	SPM [®]	TinyPWM [™]
FACT [®]	MillerDrive [™]	STEALTH [™]	TinyWire [™]
FAST [®]	Motion-SPM [™]	SuperFET [™]	μSerDes [™]
FastvCore [™]	OPTOLOGIC [®]	SuperSOT [™] 3	UHC [®]
FlashWriter [®] *	OPTOPLANAR [®]	SuperSOT [™] 6	Ultra FRFET [™]
		SuperSOT [™] 8	UniFET [™]
			VCX [™]

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I33