



STW62NM60N

N-channel 600 V, 0.04 Ω typ., 65 A, MDmesh™ II
Power MOSFET in a TO-247 package

Datasheet — production data

Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STW62NM60N	600 V	0.049 Ω	65 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

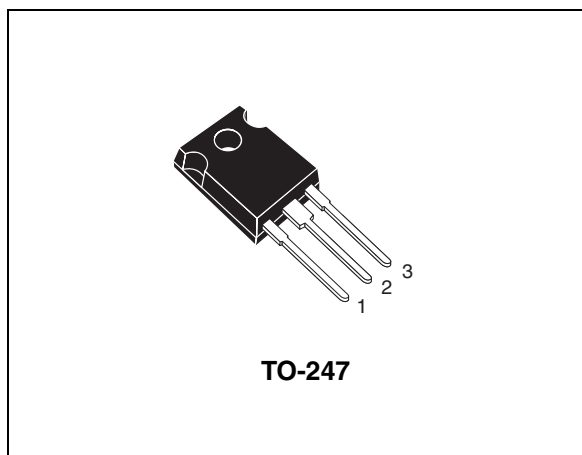


Figure 1. Internal schematic diagram

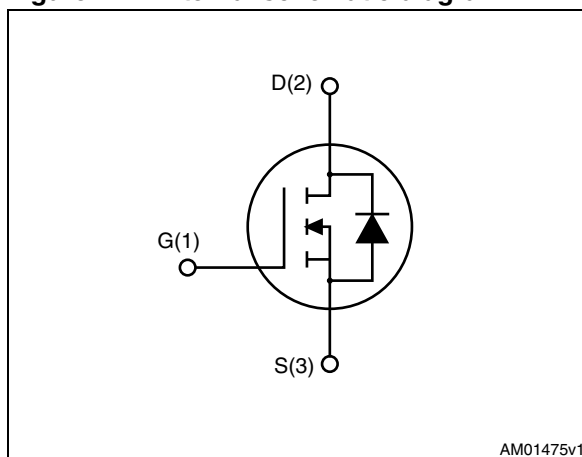


Table 1. Device summary

Order code	Marking	Package	Packaging
STW62NM60N	62NM60N	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	65	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	41	A
$I_{DM}^{(1)}$	Drain current (pulsed)	260	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	450	W
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{J\text{ max}}$)	10	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^{\circ}\text{C}$, $I_D=I_{AS}$, $V_{DD}=50\text{ V}$)	480	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_J	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 65\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.28	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$, $T_j = 125\text{ °C}$			10 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 0.1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 32.5\text{ A}$		0.04	0.049	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	5800	-	pF
C_{oss}	Output capacitance			250		pF
C_{rss}	Reverse transfer capacitance			12		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }480\text{ V}$	-	1000	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain		2		Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 65\text{ A}$, $V_{GS} = 10\text{ V}$, (see Figure 14)	-	174	-	nC
Q_{gs}	Gate-source charge			28		nC
Q_{gd}	Gate-drain charge			92		nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 32.5\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13)	-	30	-	ns
t_r	Rise time			35		ns
$t_{d(off)}$	Turn-off delay time			65		ns
t_f	Fall time			210		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		65	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		260	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 65\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 65\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	470		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$	-	10		μC
I_{RRM}	Reverse recovery current	(see Figure 15)	-	45		A
t_{rr}	Reverse recovery time	$I_{SD} = 65\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	570		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	15		μC
I_{RRM}	Reverse recovery current	(see Figure 15)	-	50		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

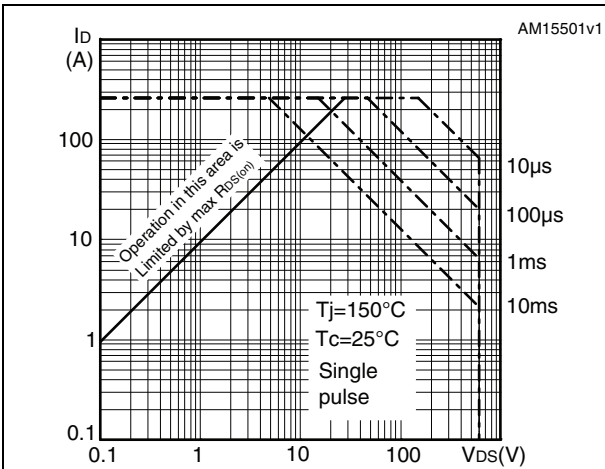


Figure 3. Thermal impedance

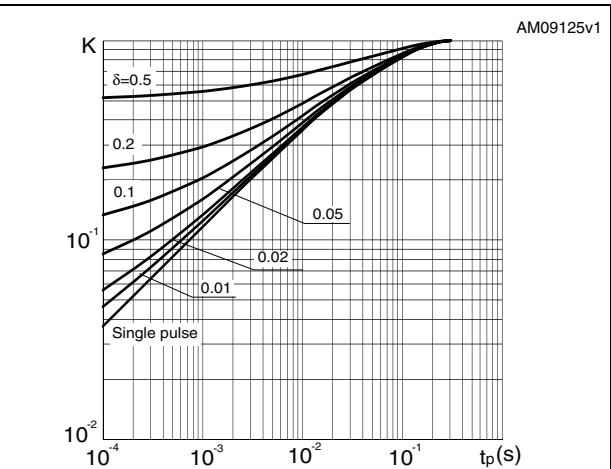


Figure 4. Output characteristics

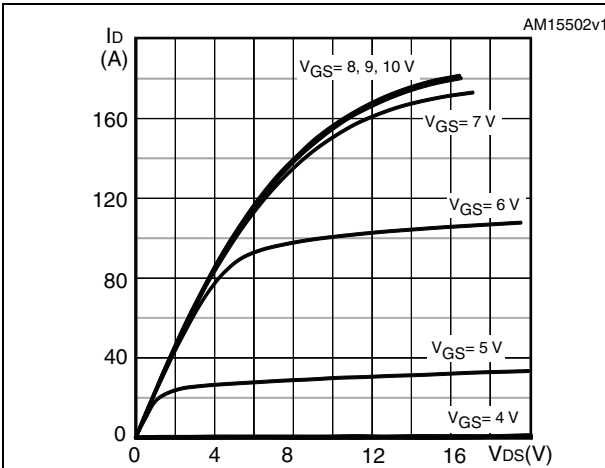


Figure 5. Transfer characteristics

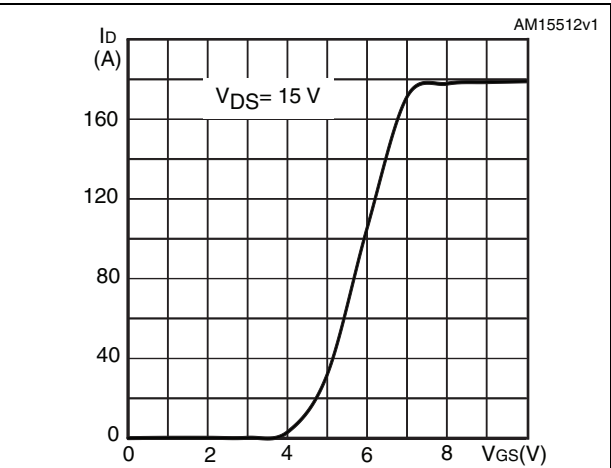


Figure 6. Gate charge vs gate-source voltage

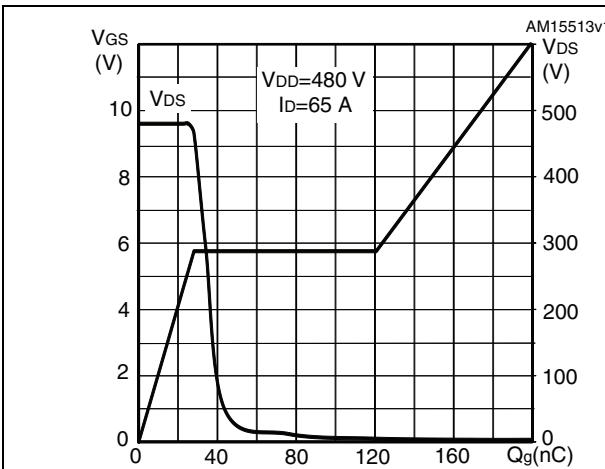


Figure 7. Static drain-source on-resistance

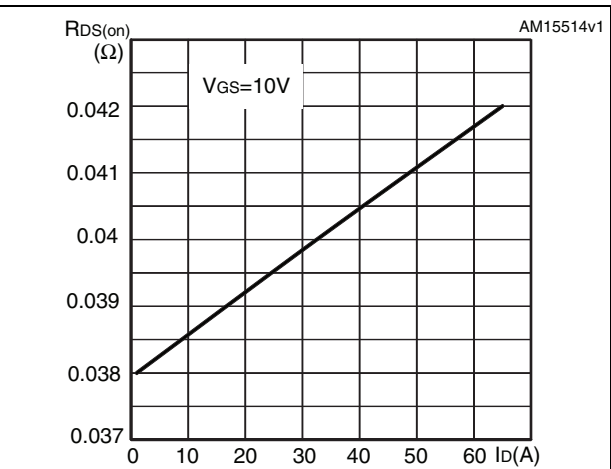


Figure 8. Capacitance variations

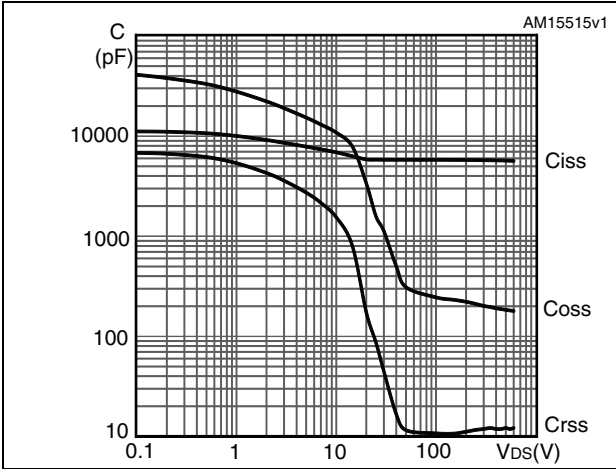


Figure 9. Source-drain diode forward characteristics

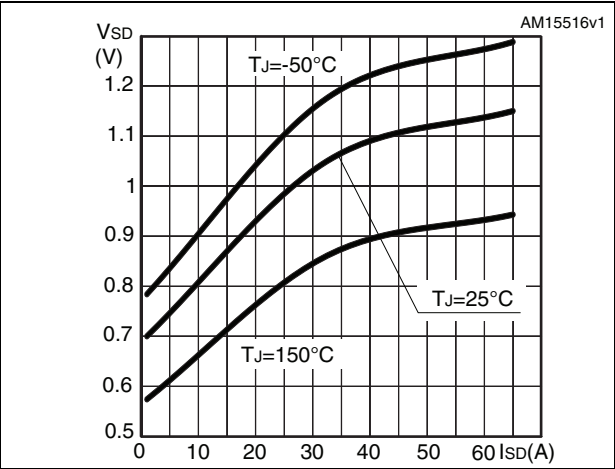


Figure 10. Normalized gate threshold voltage vs temperature

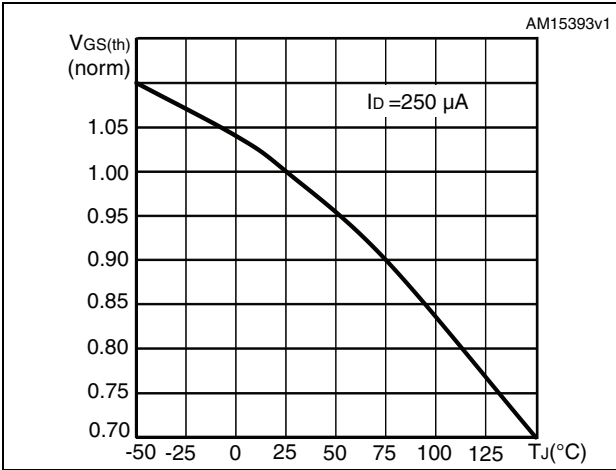


Figure 11. Normalized on-resistance vs temperature

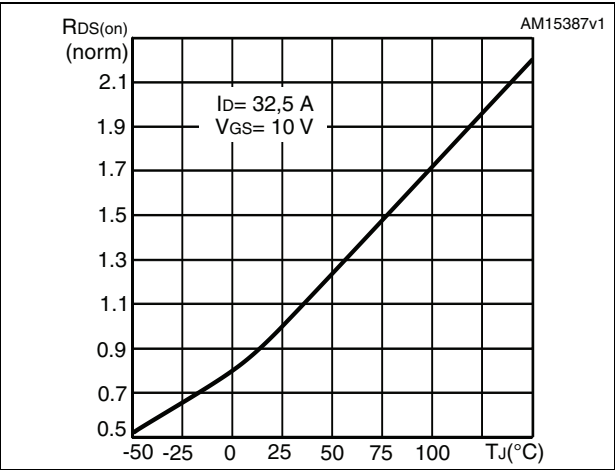
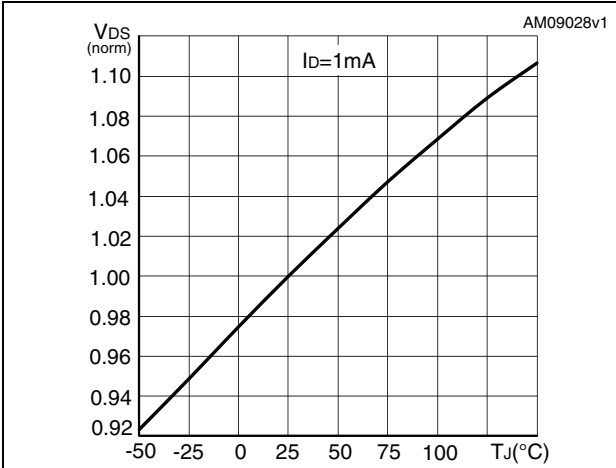


Figure 12. Normalized $B_{V_{DS}}$ vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

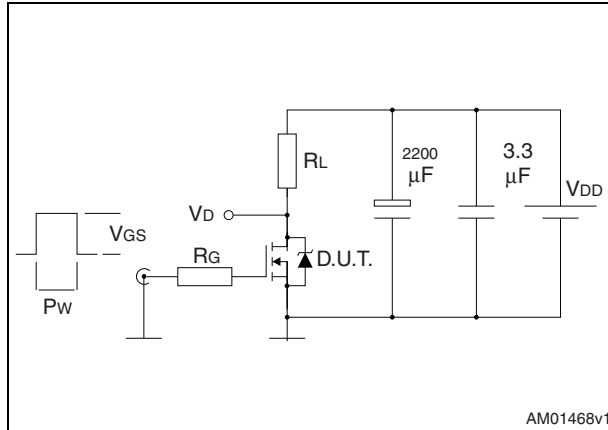


Figure 14. Gate charge test circuit

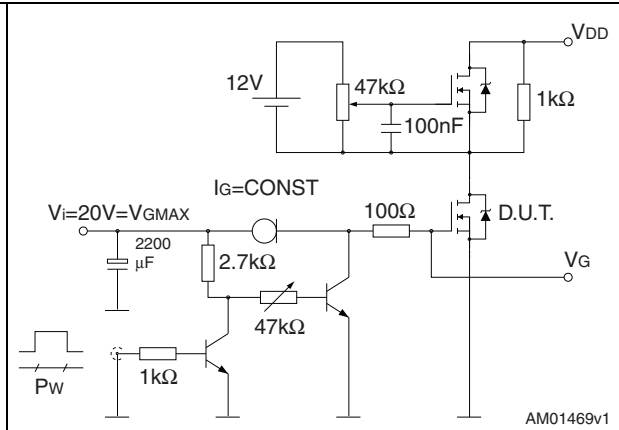


Figure 15. Test circuit for inductive load switching and diode recovery times

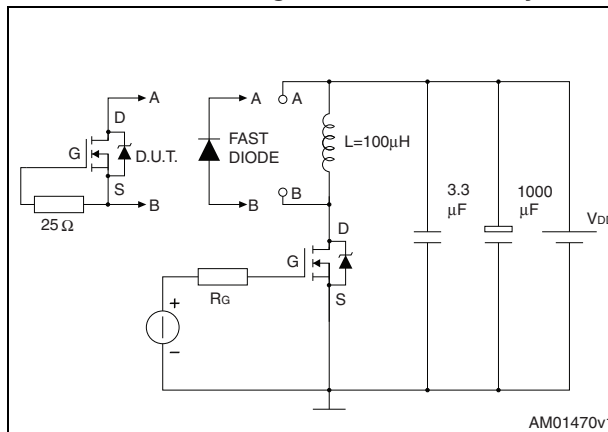


Figure 16. Unclamped inductive load test circuit

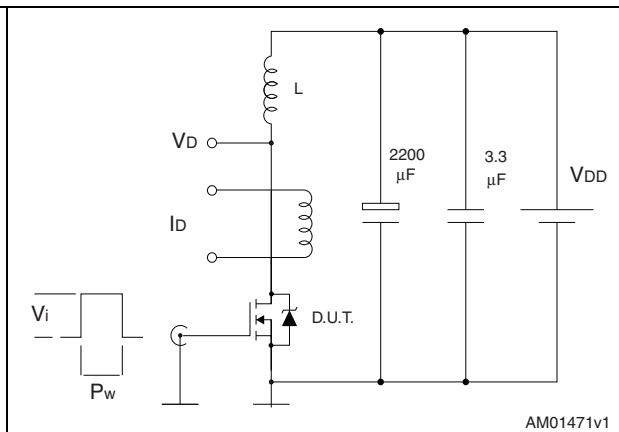


Figure 17. Unclamped inductive waveform

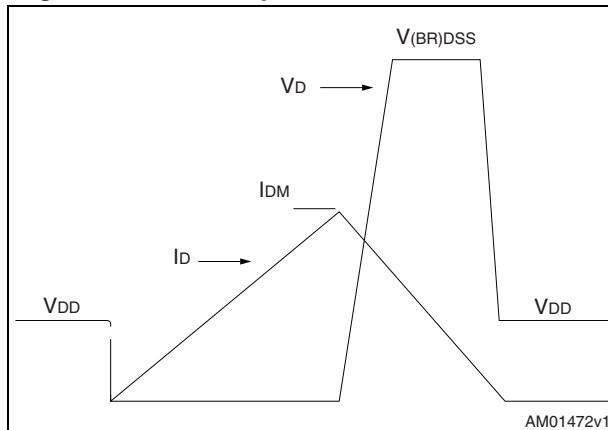
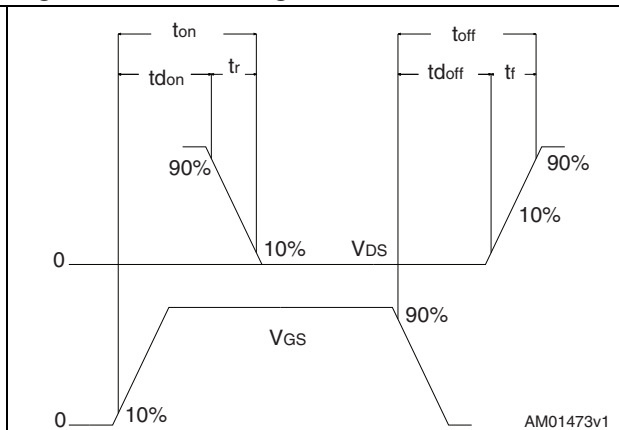


Figure 18. Switching time waveform



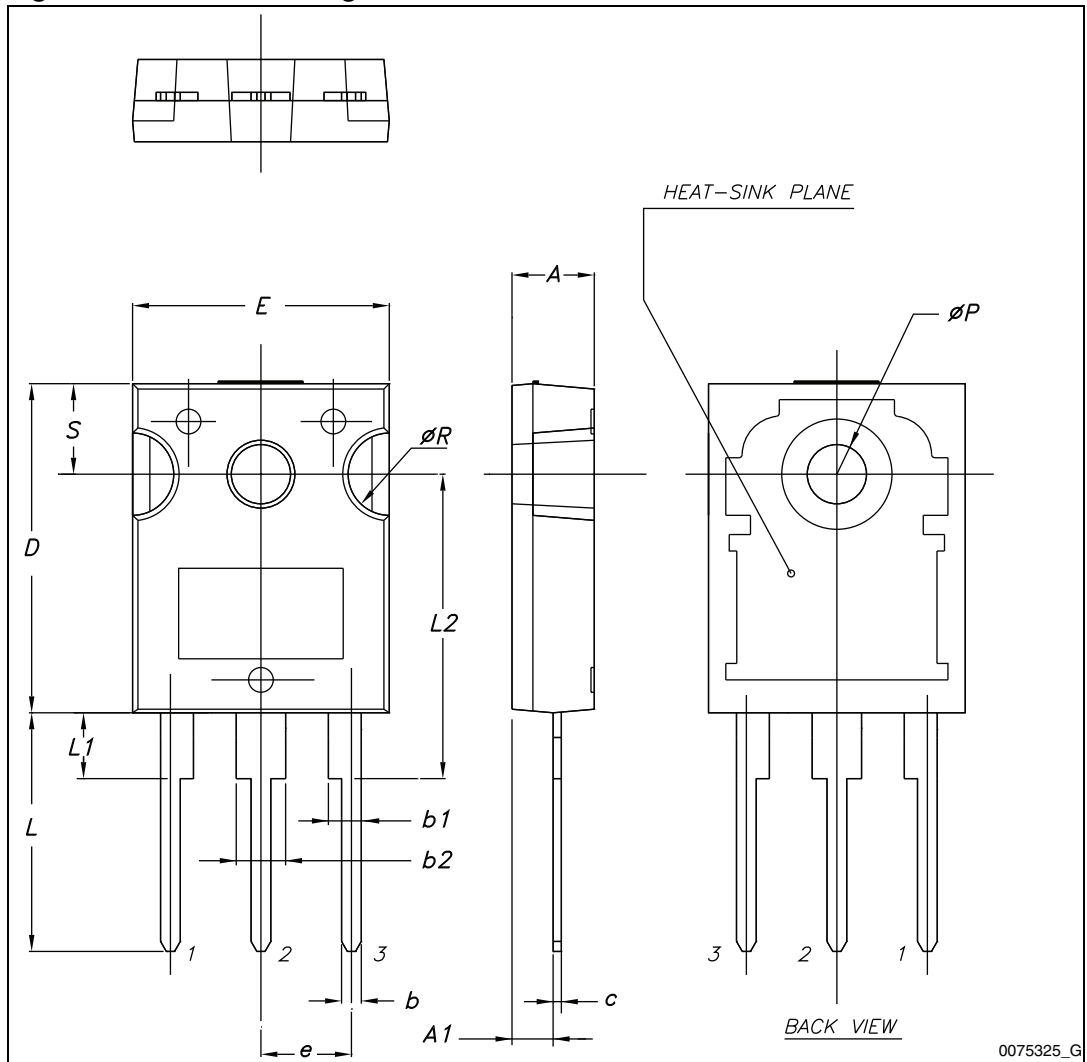
4 Package mechanical data

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Table 8. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 19. TO-247 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
27-Jun-2011	1	First release.
14-Jul-2011	2	$R_{DS(on)}$ value has been corrected.
19-Dec-2012	3	– Minor text changes – Document status promoted from preliminary to production data – Modified: $R_{DS(on)max}$ and I_D values – Modified: I_D, I_{DM}, P_{TOT}, I_{AS} values and note 2 on Table 2 – Modified: $R_{\theta jcase}$ on Table 3, I_{GSS} max value, V_{GS} typical value on Table 4 – Modified: max and typical values on Table 7 – Inserted: Section 2.1: Electrical characteristics (curves)

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