EDP System And Baseboard Manual

This document contains information on the structure
and features of the basic EDP system.
It also contains the user manual for the two slots & four slots base boards

Version v4.0, 10/06/2010

Contents

1. Introduction

The EDP baseboard is designed to be used and reused with new CPU and application modules being introduced on a regular basis. Its robust design has been rigorously tested, and every effort has been made at the design stage to protect the EDP from the most common human errors: the motherboard will have a significantly longer life than the average development board and is suitable for use in specialist one-off and low-volume products. Typical applications might be industrial controllers, scientific instrument controllers, data logging and remote monitoring. For these reasons the EDP will prove attractive to all design engineers looking for a cost effective solution which allows them to significantly improve their development process and thus deliver products in reduced time. Design engineers, consultants, educators and trainers will quickly realise the benefits and recognise the potential of the development platform modules system as an effective solution.

1.1 Bread-Boarding Platform

With the difficulty in applying traditional “bread-boarding” techniques to today’s tiny SMT components, evaluating new active devices has become major problem. There is usually no alternative to creating a special “try-out” PCB using rapid PCB production houses just to get a new device up and running. The EDP has been designed to host such experimental and trial designs, providing “clean” 5 and 3V3 supplies and instant access to a range of standard microcontrollers and IO blocks and devices. The design information necessary to allow you to create your own module for experimenting with new devices is available free of charge but in many cases, RS will already have such a module available to save you the effort.

The EDP represents the start of a continuous launch process which will see the introduction of new processor and application modules on a monthly basis.

1.2 EDP Modules Available Now

Processor Modules
EDP-CM-STR9: ST Microelectronics 32bit ARM9 Based STR912
EDP-CM-XC167: Infineon 16bit XC167
EDP-CM-LPC1768: NXP Cortex M3 based LPC1768
EDP-CM-LPC1343: NXP Cortex M3 based LPC1343
EDP-CM-LPC1113: NXP Cortex M0 based LPC1113
EDP-CM-LPC2368: NXP ARM7 based LPC2368
EDP-CM-MBED: ARM MBED – LPC1768 Web Based Development
EDP-CM-PIC-PIM: Microchip PIC PIM – Provides access to all Microchip 100 pin PIM module based device. This includes PIC16Cxx, PIC18Cxx, dsPIC33, PIC32 etc.

Application Modules
EDP-AM-AN16: Analogue Input
EDP-AM-DIO54: Digital Input / Output
EDP-AM-CO1: Basic Communications Module
EDP-AM-MC1: Brushed DC Motor Control MC1
EDP-AM-MC2: Twin Brushless DC Motor Drive Module MC2

Base Boards
EDP-BB-2A: 2 slot
EDP-BB-4A: 4 slot

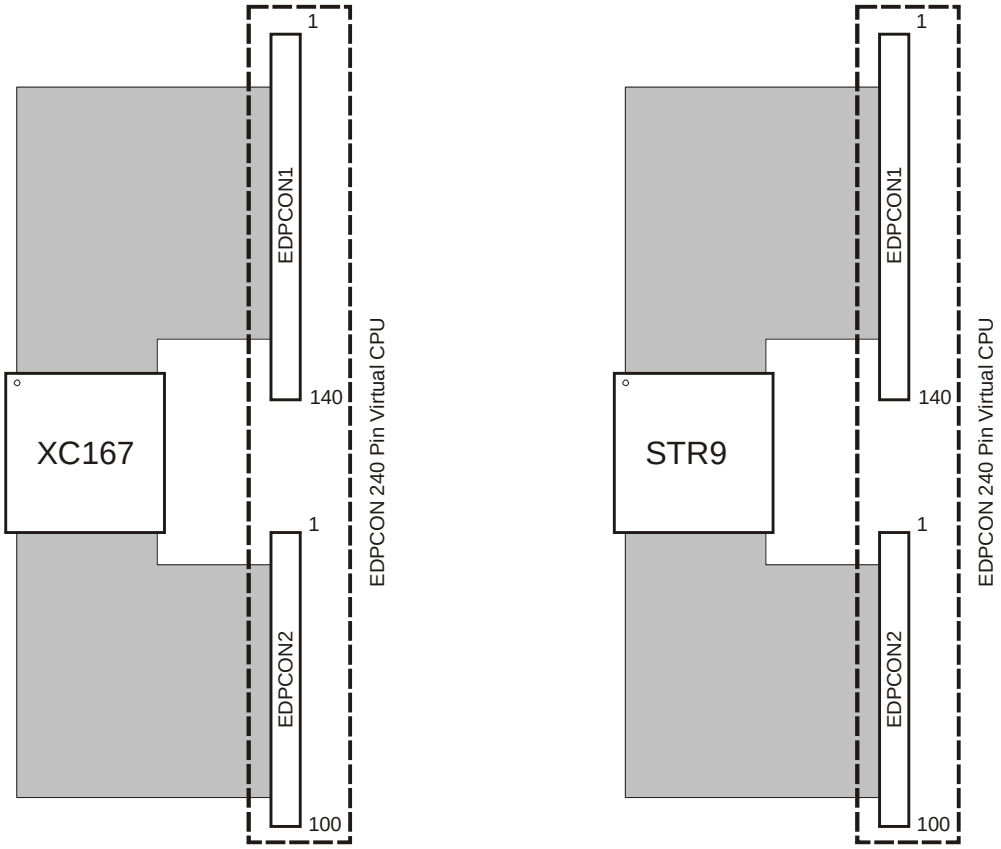
Under development
Application Module: Prototyping Module
Application Module: RFID Module
Application Module: Bluetooth Module

1.3 The EDP Virtual CPU Concept

A microcontroller that has its IO pins mapped appropriately onto the EDPCON1 and EDPCON2 connectors appears to be a virtual CPU to other IO devices fitted on the bus. Thus for example, a 14-bit ADC device Application Module on the EDPCON baseboard will see a CPU module also on the bus, as a virtual CPU whose pin out is defined by the EDP bus. There are many processors that have had their IO pins mapped onto the EDPCON system. These include STR9, XC167, LPC1768, mbed, and dsPIC. Thus the pin mapping to the EDPCON is not 100% in that on the XC167 version for example, the USB device pins are unused. Each MCU has its own set of peripherals and not all of the CPU Modules can make use of all of the features of the EDP platform for example.

Hence for example, a brushless DC motor control module with half-bridges can be designed to interface to the motor control region of the EDPCON bus without any regard for the CPU type to be ultimately used. The net result is that subject some limitations, a range of modules bearing different CPUs can be freely connected to a range of IO modules.

The EDPCON has been designed to accommodate all the common peripherals found on current microcontrollers, including advanced interfaces like SD/MMC and I2S. Thus it is possible to map almost any microcontroller to this format.



1.4 Basic EDP Concepts

The EDP allows microcontrollers and IO devices to communicate through a standardised interface which is effectively implemented as a backplane on the baseboard. To some extent this interface is analogous to PC104 or STE busses where a connectors pin out is defined that allows the interconnection of address and data-bus connected devices. Such busses tend to include only power line, data and address busses plus control signals such as chip selects and interrupt request lines.

For microcontroller systems, such a collection of signals is of very limited use, especially for single-chip CPUs that use no external bus. It also takes no account of the specialist pin functions available on microcontrollers such as CAN, I2C, SPI, signal measurement and signal generation peripherals.

2. EDP Baseboards

2.1 EDP-BB-4A - Four Slot.

The EDP Baseboard (or “motherboard”) consists of four ‘stations’ with the minimum configuration of the motherboard with a single plug-in processor module. All 4 stations are identical, and there are many permutations of CPU modules and Application modules possible. Even with just the minimum configuration of Motherboard and CPU module for example, you can easily run a web-server through the standard onboard Ethernet connection. There are various application modules; we have introduced an initial starter range consisting of basic digital and analogue I/O, a motor control module and a communications module. The more advanced user will discover that it is possible to run more than one processor module on the motherboard in a Master and Slave configuration.

The motherboard is an Extended Euro card size (220 x 100 mm) fitted with rubber feet to lay flat on the bench, but able to be used in a standard rack system. Add a 64-way DIN (RS 381-8696) connector and you can plug the EDP into a backplane. Connectors for four module stations are supplied, arranged to ensure correct module fitting. There are also fitted +3.3V and +5V switching voltage regulators, a back-up battery, an RJ45 Ethernet connector, a mini-USB connector, +12 volt power-supply jack, I/O breakout header and eight DIP switches ported onto the system I2C bus. The base board is also fitted with an I2C serial EEPROM for storing of configuration data. The default fitted item is an 24LC32 32k bit device.

The DIP switches allow the user software running on a processor module to read a configuration setting, enabling I/O ports to be set up correctly, for example, or for CAN or TCP/IP addresses to be set. Depending on the capability of the particular processor module in use, up to three I2C buses and two CAN networks are available. Many of the application modules use an I2C bus for primary communication with the processor providing maximum flexibility. Some processor chips will require +5 volts, others +3.3 volts. A factory link on the CPU module selects the correct supply for the CPU Module and this voltage is output back on to the base board on the Vcc_CM signal line. This signal is used for multiple purposes. These include referencing the power on reset circuit and the pull up voltage required by the I2C pull up resistors. For 5V and 3.3V systems these of course need to be different.

The four slot base board also has a power input terminal block and a power input jack, giving the user the option to power from a wall cube type power supply or a bench power supply. The input circuit is protected by a vertically mounted fuse (in a fuse holder). A common mode input power line filter is included providing some protection from unwanted external transients. The four slot base board has switching regulator for both the 3.3V and the 5.0V power supplies which allow the unit to deliver higher current loads with getting too hot.

The Ethernet connector populated on the base board includes the required magnetics to make a standard Ethernet interface. The CPU Modules with Ethernet capability provide the PHY devices and the magnetics are provided on the base board.

A mini USB connection is also present on the base board which is used for debug and programming purposes. This debug connector is not used by all of the CPU modules as each development tool set and debug arrangement is different for each of the CPU Modules. The Infineon XC167 for example makes much use of this but the PIC PIM module for example does not. For MCU's which have a USB capability the USB connector that should be used in the one provided on the Communications Module. This is effectively the user USB connection.

In summary we have

- 4 slots for CPU Modules or Application Modules
- Power Input Terminal block for 12V/GND power input from bench power supply
- Input power jack for use with a wall cube
- Fuse holder
- Common mode input supply choke
- Switching 5V and switching 3.3V voltage regulator
- Reset switch
- 8 way DIP switch input
- Serial I2C EEPROM 24LC32
- Pull Up resistors for I2C_CNTRL lines
- Pull Up Resistor for GEN0_I2C and GEN1_I2C
- Ethernet socket with built in magnetic
- miniUSB debug connector for debugging only.
- Screw holes for PCB mounting (rubber feet also fitted)
- Eurocard connector for backplane systems
- Battery backup option VBAT capability

2.2 EDP-BB-2A - Two Slot.

The two slot base board has been designed as a cut down version of the four board unit. In order to save some cost and provide a lower cost entry in to the RS-EDP platform many of the components have been replaced or not populated. The basic capability of the 2 slot unit is as follows:

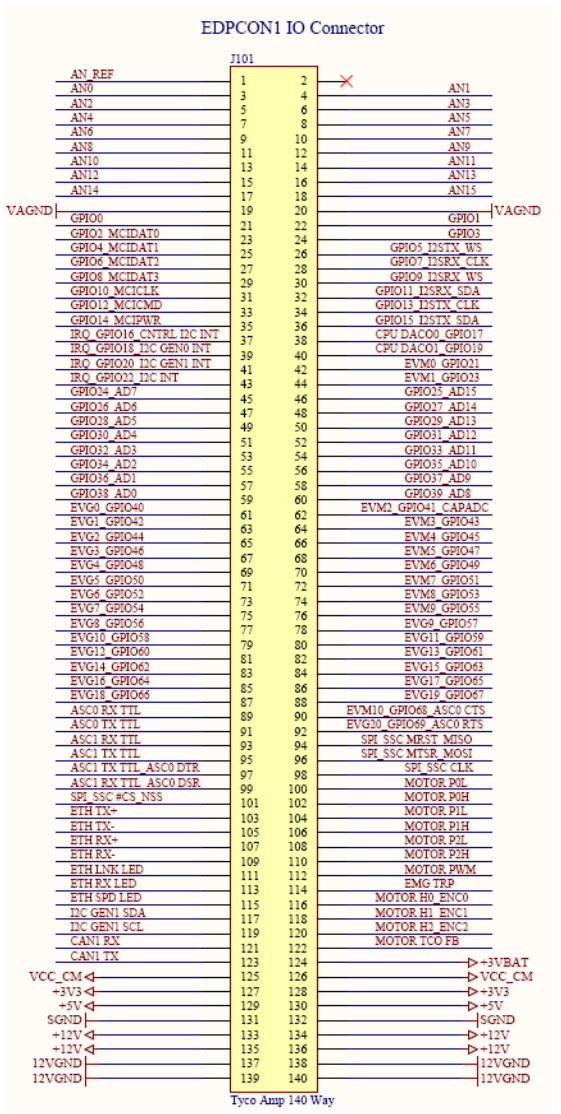
- 2 slots for CPU Modules or Application Modules
- Power Input Terminal block for 12V/GND power input from bench power supply
- Input power jack for use with a wall cube
- Fuse holder (not populated and replaced by a shorting link)
- Linear 5V and linear 3.3V voltage regulator
- Reset switch
- 8 way DIP switch input (Not populated)
- Serial I2C EEPROM (Not populated – user can fit 24LC32 for example)
- Pull Up resistors for I2C_CNTRL lines
- Pull Up Resistor for GEN0_I2C and GEN1_I2C (not populated)
- Ethernet socket with built in magnetic
- miniUSB debug connector for debugging only.
- Screw holes for PCB mounting (no rubber feet fitted)

3. Standardised Signal Set For Embedded Microcontrollers

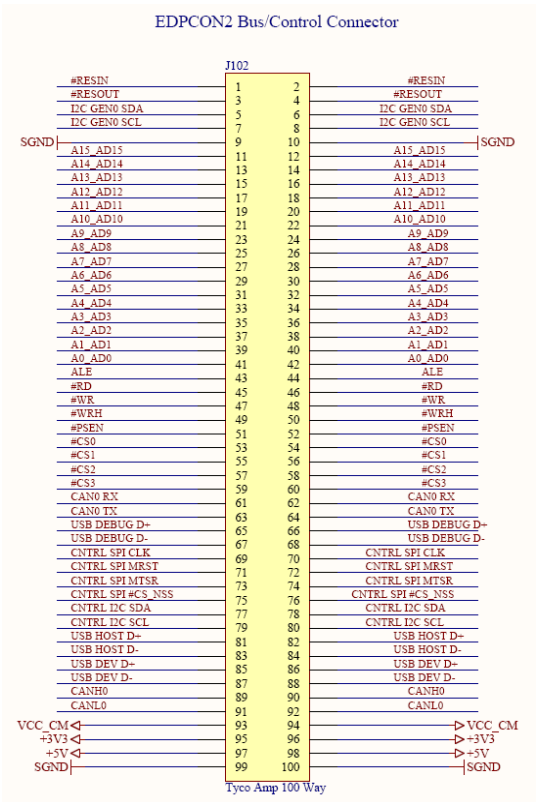
The base board connectors EDPCON1 and 2 connectors defines a set of signals on a standardised format that are relevant to typical 8, 16 and 32-bit microcontrollers. In addition to address bus, data

bus and chip select signals, they include 3 I2C channels, 2 CAN channels, groups of pins able to create interrupts in response to external events, groups of pins able to create pulse trains, others dedicated to motor control, I2S, memory cards and many other common microcontroller IO types.

The EDP bus contained in the EDP baseboard is accessed through two Tyco-AMP .8mm pitch connectors. The signal names are intended to convey something of the capabilities of that signal. For example signal EVG0_GPIO40 is a pin that can generate timed events (i.e. pulses and pulse trains) as well as performing simple on/off pin control.



EDPCON1 Connector



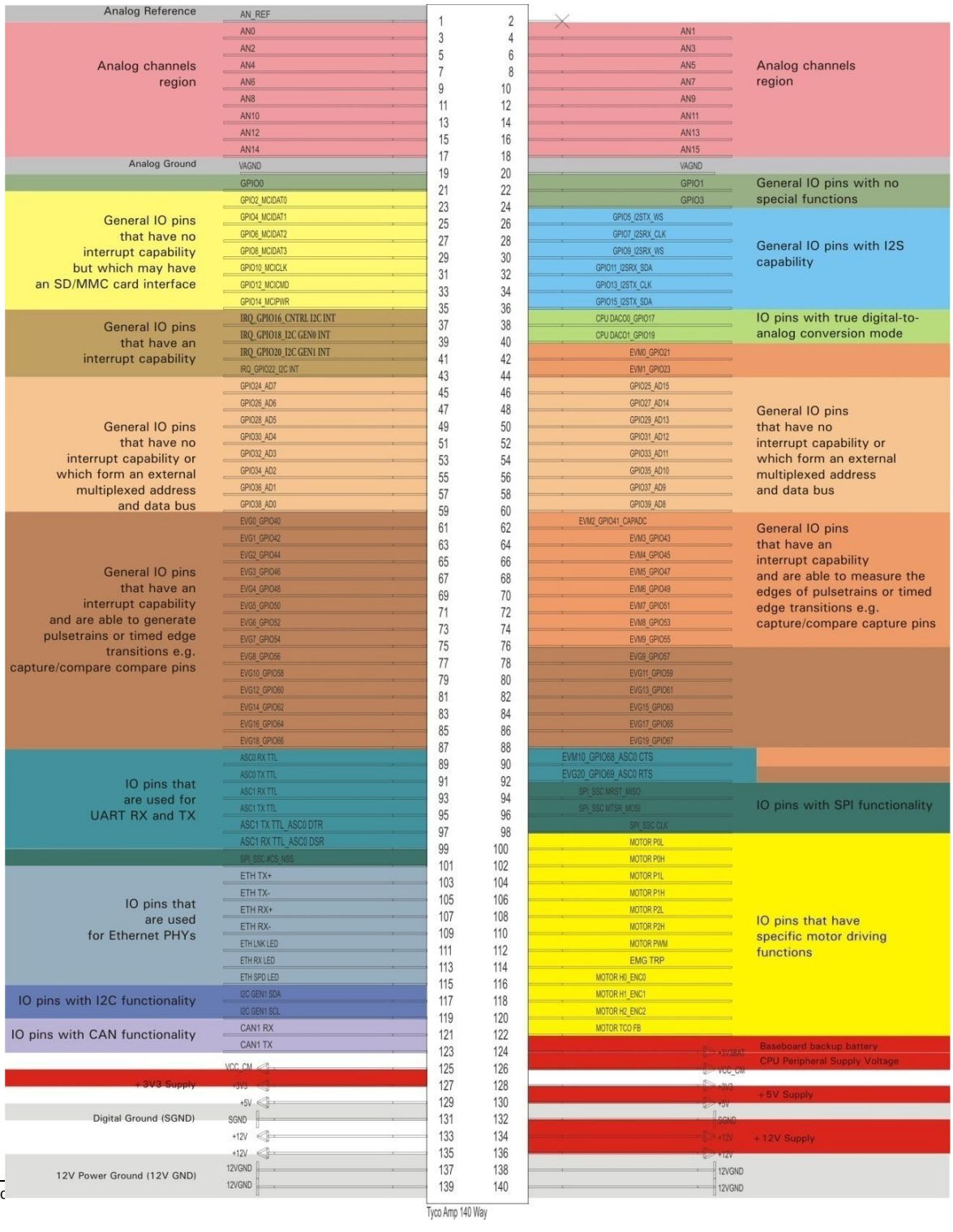
EDPCON2 Connector

3.1 Grouping Of Signals On The EDP Connectors

The EDPCON1 and 2 connector specification divide the total available 240 pins into groups or regions of similar characteristics, as shown below:

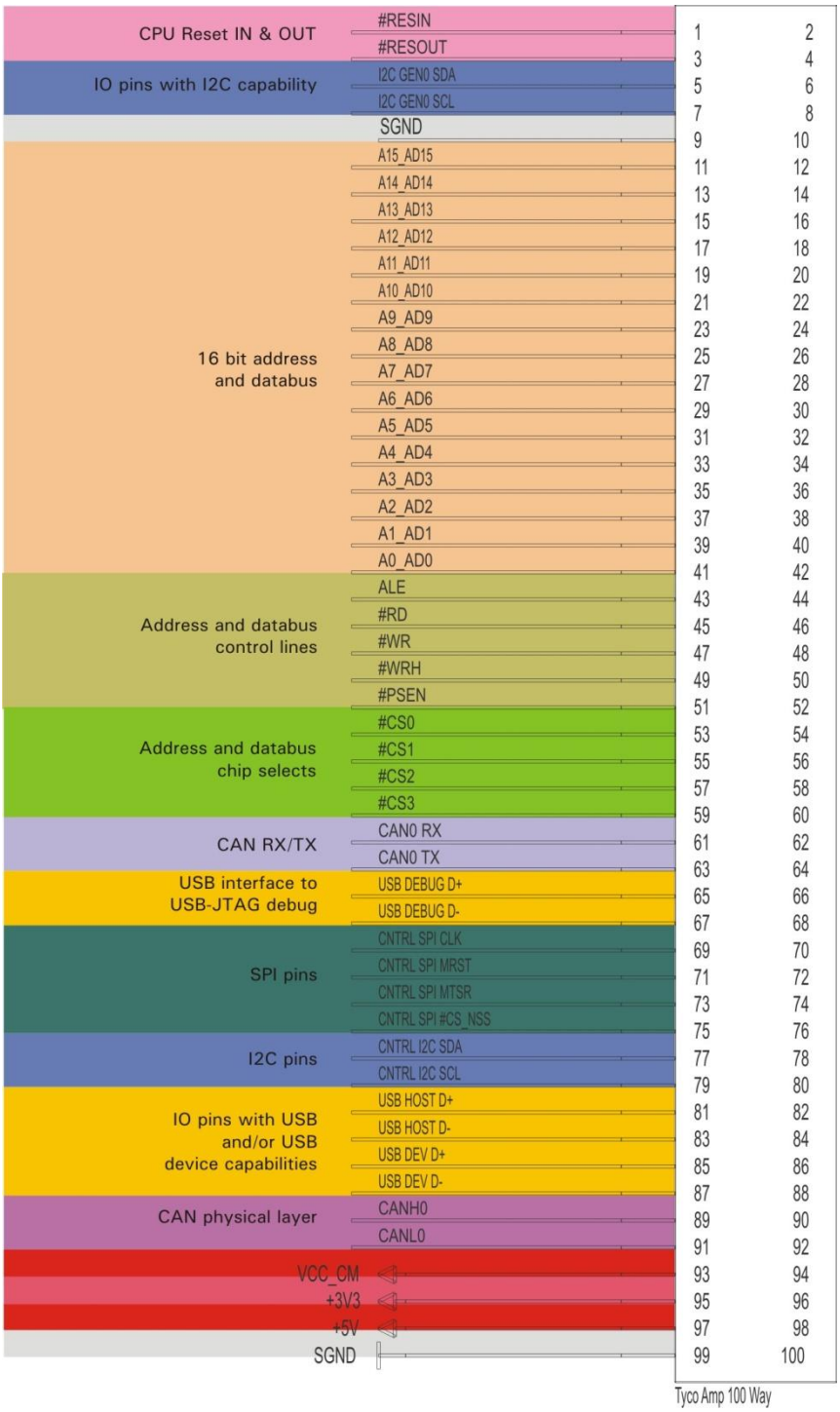
3.1.1 EDPCON1 Connector IO Regions

EDPCON1 carries both analog and digital signals. The analog signals are grouped together in a "quiet zone".



3.1.2 EDPCON2 Connector Regions

EDPCON2 carries mainly bus signals such as I2C, SPI, CAN and the multiplexed 16-bit external bus from the CPU module. The pins are connected together horizontally on the EDPCON2 connector so pin1 and pin2 are the same for example. For clarity here, only the signals are shown on the left.



3.2 EDP Signal Names

The generic signals present on the connectors have names which indicate their primary and secondary functions.

3.2.1 EDPCON1 Signal Description

ANx:	Analog signals
VAGND:	Analog ground, referenced to CPU and Analog application analog signal grounds
GPIOx:	Pins that can only be set to 1 or 0 by a CPU instruction. It has no special or alternate function.
GPIOx_MCIxxx:	Pins that have basic IO function like “GPIOx” but which also form an SM/MMC card interface
GPIOx_I2S_XXX:	Pins that have basic IO function like “GPIOx” but which also form an I2S interface.
IRQx_GPIOx_X_I2C_INT:	Pins that are used by the three I2C busses to request a CPU interrupt. **Note:** IRQ_GPIO16_CNTRL_I2C_INT should always be reserved for use by the I2C CNTRL I2C bus.
CPU_DACx_GPIOx:	Pins where CPUs with true digital to analog converter outputs are always connected. Alternatively, PWM will be available if there is no DAC.
EVMx_GPIOx:	Pins which have basic IO function but which also can measure timed events, pulse times and durations e.g. CAPCOM input.
GPIOx_ADx:	Pins with basic IO function but which also can form a multiplexed address and data bus.
EVGx_GPIOx:	Pins which have basic IO function but which also can generate events like timed pulses and transitions e.g. CAPCOM output.
EVM2_GPIO41_CAPADC:	Pins which have basic IO function but which also can measure pulse times and durations e.g. CAPCOM input. If the CPU supports the triggering of ADC readings on an edge, the function will be on this pin.
ASC0_RX_TTL:	Logic level connection to CPU module’s serial port 0 receive pin.
ASC0_TX_TTL:	Logic level connection to CPU module’s serial port 0 transmit pin.
ASC1_RX_TTL:	Logic level connection to CPU module’s serial port 1 receive pin.
ASC1_TX_TTL:	Logic level connection to CPU module’s serial port 1 transmit pin.
ASC1_TX_TTL_ASC0_DTR:	If CPU supports DTR function on ASC0, the function is available here.
ASC1_RX_TTL_ASC0_DSR:	If CPU supports DSR function on ASC0, the function is available here.
EVM_GPIOx_ASC0_xTS:	Event measurement, general IO and ASC0 RTS and CTS functions, where available.
SPI_XXXX:	Pins associated with SPI function, where supported by CPU module.
ETH_xxx:	Pins connected to an Ethernet PHY on CPU module, where available.
I2C_GEN1_SDA/SCL:	Pins connected to CPU’s I2c channel 1
MOTOR_XXXX:	Pins required for driving three-phase AC and DC brushless motors, including inputs for Hall sensors and tachometers or other speed-related signals.
EMRG_TRP:	Emergency stop/trip function for motor control.
CAN1_RX/TX:	Logic level connection to CPU module’s second CAN module (where fitted).
VCC_CM:	Peripheral operating voltage of CPU module currently fitted.
+3V3:	+3V3 supply from baseboard voltage regulator
+5V:	+5V supply from baseboard voltage regulator
+12V:	Raw 12V from power input to baseboard
12VGND:	Ground connection to power supply.
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard
3V3 Vbatt:	Permanent 3V3 supply from Lithium cell on baseboard (where fitted)

3.2.2 EDPCON2 Signal Description

#RESIN:	Reset input to CPU module
#RESEOUT:	Reset out signal from CPU module (where available)
I2C_GEN0_SDA/SCL:	Secondary I2C bus data and clock (where available)
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard
Axx_ADxx:	16 bit multiplexed address/data bus when enabled by jumpers on CPU module.
ALE:	CPU module's address latch enable signal
#RD:	CPU module's READ signal
#WR:	CPU module's WRITE (or WRITELOW) signal
#WRH:	CPU module's WRITE (or WRITEHIGH) signal
#PSEN_A16:	CPU module's PSEN signal (8051) or A16, where available
#CS0:	CPU module's first chip select signal
#CS1:	CPU module's second chip select signal
#CS2:	CPU module's third chip select signal
#CS3:	CPU module's fourth chip select signal
CAN0_RX/TX:	Logic level connection to CPU module's first CAN module (where fitted).
USB-DEBUG+/-	USB signals connected to FTDI USB-JTAG device on CPU module
CNTRL_SPI_XX:	Signals connected to CPU module's first SPI peripheral
CNTRL_I2C_SDA/SCL:	Signals connected to CPU module's first or primary I2C channel. (This is the I2C control backbone for the EDP baseboard).
CANH0/CANL0:	CPU module's first CAN module via physical layer drivers.
VCC_CM:	Peripheral operating voltage of CPU module currently fitted.
+3V3:	+3V3 supply from baseboard voltage regulator
+5V:	+5V supply from baseboard voltage regulator
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard

4. Inter-Module Communication

With up to 4 modules on the EDPCON bus, some form of communication is required. With a limited number of CPU pins available, it is necessary to use a serial communications protocol to for example, take readings from a high-precision ADC that might be present on an IO module at the same time as read a serial EEPROM on another module. The I2C protocol is used as the main communication channel for such actions, although provision is made for SPI or even a CAN physical layer.

Module	I2C Device	Possible Range	Actual 7-bit Address Module 1	I2C channel	Actual 7-bit Address Module 2	I2C channel	Comment
Analog Module	MAX1138 address	0x35	0x35	CNTRL	0x35	Gen0	MAX1138 has no address pin so only one can be present per I2C channel
	MAX1038 address	0x65	0x65	CNTRL	0x65	Gen0	
	AD5263 BRU50 address	0x2C-0x2F	0x2C	CNTRL	0x2C	Gen0	
	PCA8575 address	0x20-0x27	0x21	CNTRL	0x21	Gen0	
Baseboard	PCF9675	0x20-0x21	0x20	CNTRL	XXXXX	XXXXX	
	24C32 (Rev B Only)	0x50-0x57	0x51	CNTRL	0x52	CNTRL	0x50 is occupied by PCA8583
Comms AM	RTC PCA8583	0x50-0x51	0x50	CNTRL	XXXXX	XXXXX	
Digital AM	PCA9555 IN address	0x20-0x27	0x22	CNTRL	0x24	CNTRL	
	PCA9555 OUT address	0x20-0x27	0x23	CNTRL	0x25	CNTRL	
Brushless DC Motor Drive MC2	dsPIC33 slave x 2	0x40 – 0x47		CNTR			The dsPIC slave I2C address can be changed in software to suite.

Default I2C Addresses Used In The EDP System

There are three possible I2C channels available although in most cases the default one (I2C_CTRL) will be sufficient. EDP modules that carry I2C device do, where possible, allow the user to configure the I2C addresses. This allows for example, up to three digital IO modules to be fitted, with the GPIO devices on each module given an unique address. Where the address space of a particular I2C channel becomes full, devices can be connected to an alternative channel to get access to a completely new address space.

4.1 Inter-EDP System Communications

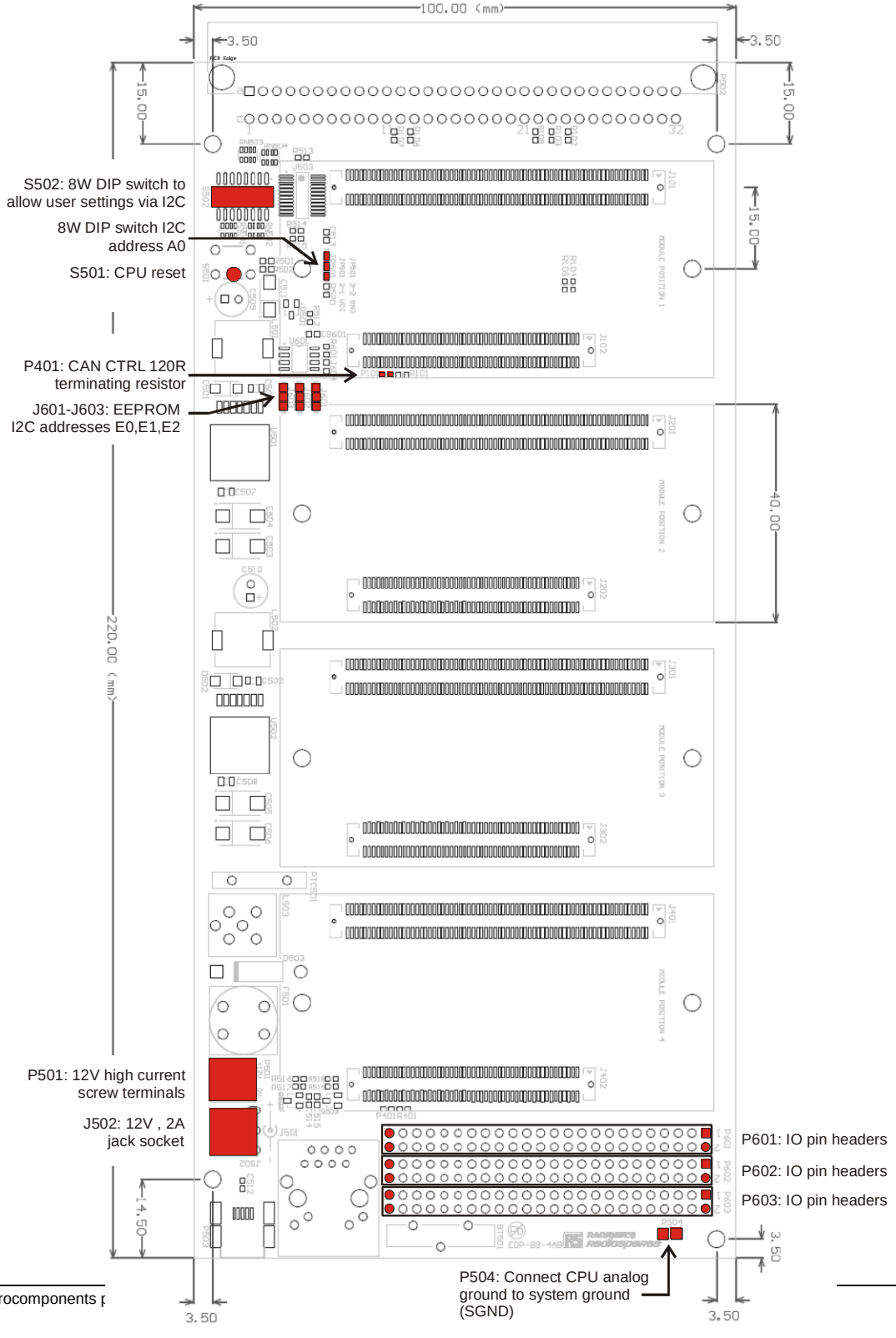
In a situation where there are multiple EDP baseboards, each with their own CPU modules in a complete system, I2C can still be used to allow the CPUs to communicate but it is strongly recommended to use CAN. EDP IO signals that are intended to be taken off-board are brought out on a standard DIN414162 64-way connector.

5. Using The EDP Baseboard

This section gives information on the features of the EDP baseboards, its connectors and the overall structure of the EDP system.

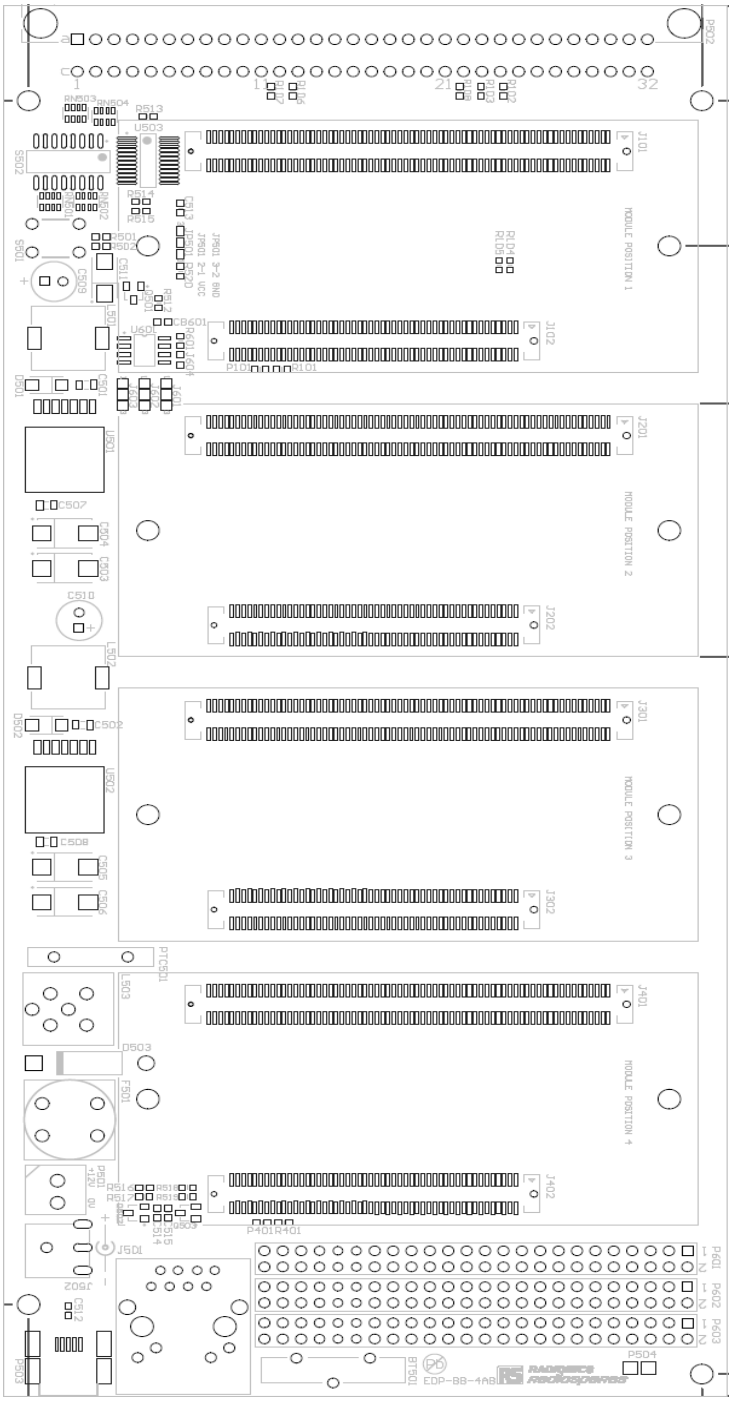
5.1 EDP 4 Slot Baseboard User Options Placement

There are a number of user-selectable functions on the baseboard, as shown below:



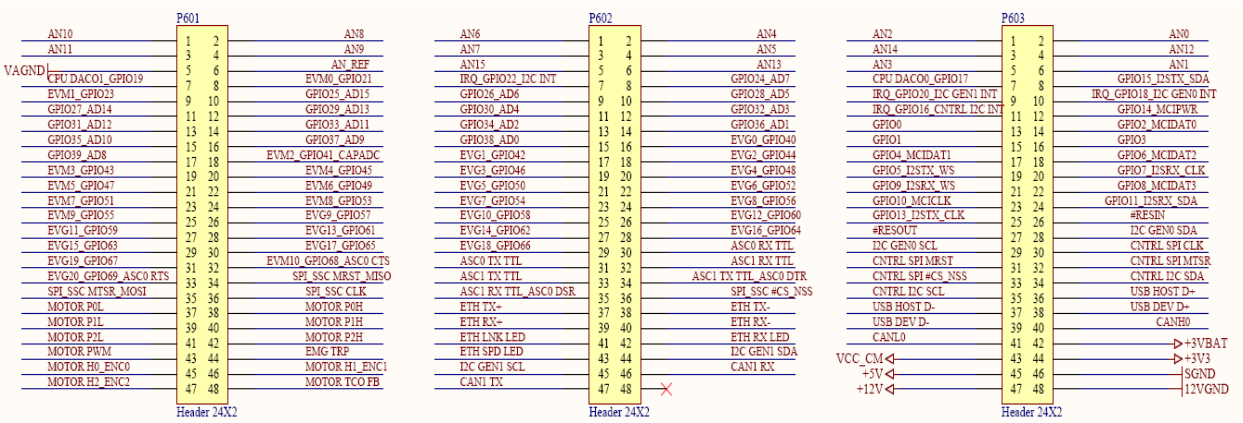
5.2 EDP Baseboard Component Placement

The location of the major items on the EDP baseboard is shown below.



5.3 EDP IO Pin Headers

All the signals in the EDP backplane are available here on 0.1” pin headers for sampling by ‘scopes etc. This connector is easiest way to access the backplane signals in the EDP system.

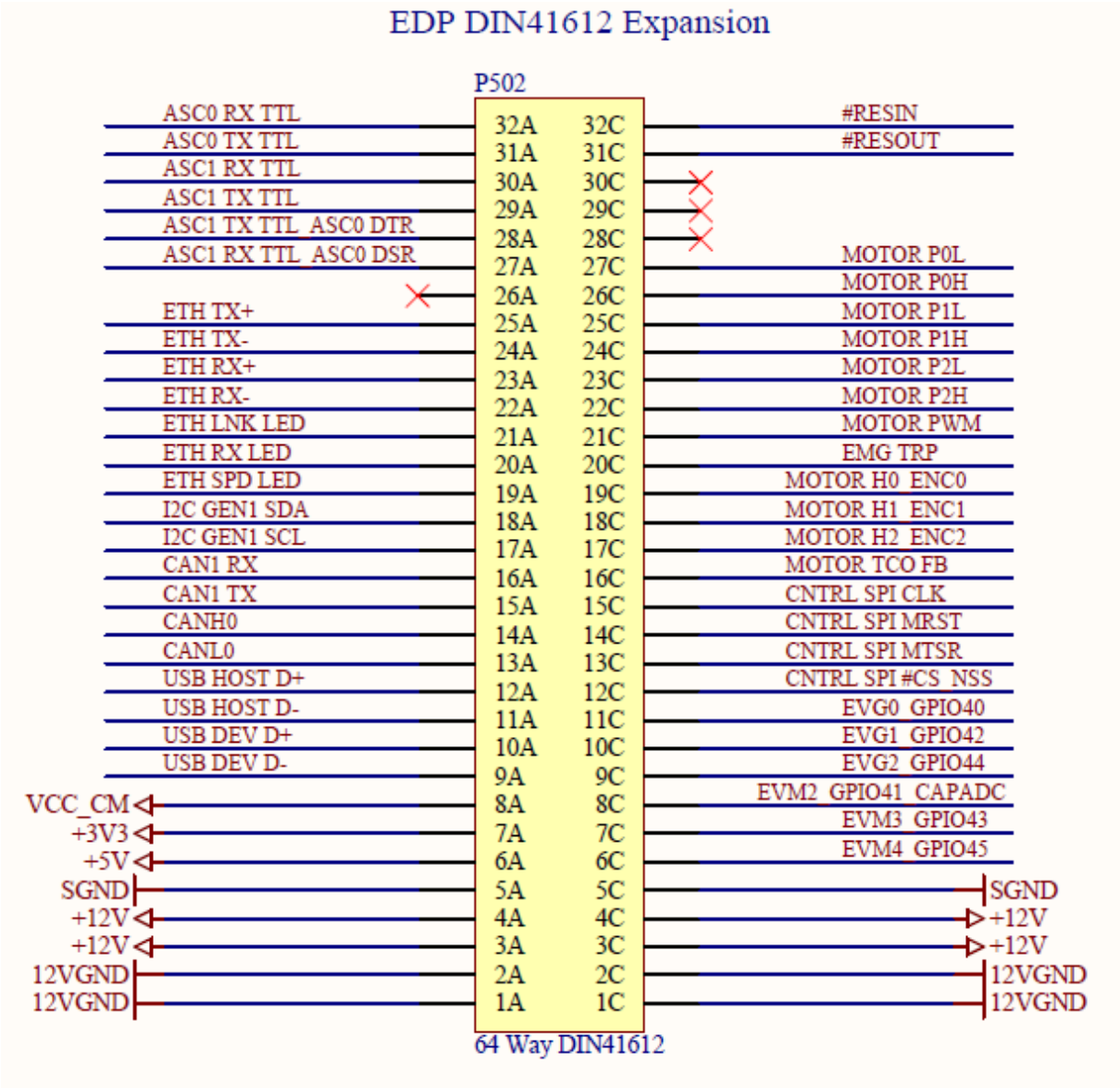


Each of the MCU pins is effectively allocated to an RS-EDP back plan function. To help with the mapping of the MCU pins to the back plane signals a spreadsheet of pin numbers, names and functions has been produced. This is called the Pin Allocation Spreadsheet and one exists for each of the CPU Modules. This Pin Allocation spreadsheet should be available to down load off the Hitex or RS Web Sites. This pin allocation information may also be present in the respective user manual for the CPU Module.

As the mapping process is quite complicated it is often difficult to see what how the CPU Module can communicate with the Application Modules as there may well be several different link options. For this reason a Mapping Aid document exists which is basically a Power Point presentation detailing all of the link options on it. This mapping aid can at a glance give some indication as to which resources the CPU Modules has and how it can interface with the Application Modules. For example you can determine whether a CPU module has a CAN capability and if it is possible to connect to the Communications Module.

5.4 Eurocard Connector

For those users wishing to use the Eurocard expansion, the pin out is as follows...

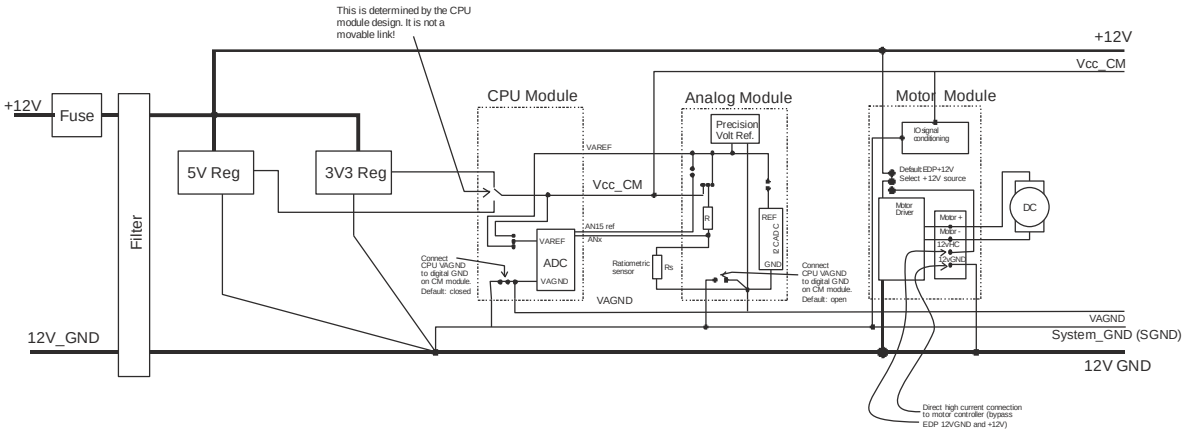


6. Grounding Arrangements

The system ground (SGND) and 12V GND are connected together at a star point on the baseboard. The 12V GND is used for high current devices like the motor controller and the ULN2003 output drivers on the digital IO AM. System ground is used for all returns on logic devices on all modules. It can be used for analog returns but there is a risk of noise (ground bounce).

Analog ground (VAGND) by default is an offshoot of the system ground which occurs only on the CM. It is routed to the VAGND pins of the CPU and also acts as a return for filter circuits used for analog inputs. The analog ground (AGND) and the system ground (SGND) need to be connected together at some point in the circuit.
The preferred way to do this is on the CPU module especially if the CPU module is reading ADC values with its on board ADC peripheral. Alternatively the two grounds can be connected on the

analogue module. A third option also exists as the base board provides a mechanism for connecting the two grounds also. The user starting a new design should decide early on, it grounding arrangement. Not all of the MCU modules (STR9 for example) do not have the ability to connect the two grounds together in which case the two grounds need to be connected on the base board or the Analog module if fitted.
Having all of the grounds connected could introduce a ground loop, so be careful you connect this at only one point.



7. Positive Supplies

The +12V line comes via the screw terminals on the baseboard or the mini-jack. It is fused and filtered (4 slot board only) before entering the EDP backplane. The 3V3 and 5V voltage regulators are driven from the +12V.

The power rating for the EDPCON1 and EDPCON2 connectors is 2A. This means higher currents required for the MC1 Motor Drive Module (>2A) for example need to be bought directly in to this AM module. The user manual for this module will describe in more details how this should be done.

The four slot base board has two switching regulator for the 3.3V and 5.0V lines. This means they are able to take a lot of current without getting hot. The two slot base board however has only linear regulator and are designed to work with much lower currents. Be careful not to take too much current from these as they may start to get too hot. No characterisation data is currently available for the 2 slot base board regulators so it's up to the user to determine a safe level of current for these. If 12V is not been used in the system the user can lower the input voltage to reduce the power dissipation in this device.

7.1 Logic Supplies

Both 3V3 and 5V are available on the EDPCON to support both 5V and 3V3 processors and devices. To allow the interfacing of IO devices at the required voltage, the positive supply to the CPU IO domain is routed into the EDPCON through Vcc_CM. It is intended to be used for pull-ups on IO pins and powering small active components that connect directly to the CPU such as discrete logic, op-amps etc.. Vcc_CM is limited to 500mA total current draw from other modules and the baseboard.

Vcc_CM is connected inside the CM to the voltage used by the CPU's IO domain.

7.2 Analog Supply

The Analog supply to the CPU ADC may be derived from the local Vcc or from a precision reference located on the Analog AM. Ideally the Analog AM and CM should be in adjacent positions on the baseboard to keep the signal length to a minimum if the latter is chosen.
The I2C ADC on the analog module can use the Vcc_CM or the local precision voltage references, either 3V3 or 5V. The 5V reference is driven from the 12V to guarantee no drop-out problems.

As the anti-aliasing filters are run at 5V, the local ADC is not tied to the same voltage range as the CPU's ADC. It is the user's responsibility to make sure that the input does not exceed the permissible input voltage range of the CPU ADC. Protection resistors are provided to prevent damage.

8. Limits And Restrictions

For the 4 slot base board we have

Vcc CM max current	500mA
3V3 max current	2000mA
5V max current	2000mA
Sum of 3V3 current + 5V current + Vcc_CM =	2000mA
SGND max current	2000mA
12VGND max current	2000mA

For the 2 slot base board, no characterisation data exists, but the maximum current rating for the EDPCON1 and EDPCON2 connectors is 2A. The limiting factor is likely to be the power dissipation in the 5.0V linear voltage regulator on the base board.

Warning: do not attempt to fit two CPU modules to the baseboard at the same time. If they have different peripheral supply voltages then damage is likely to occur.

9. EDP Control Busses

9.1 I2C Busses

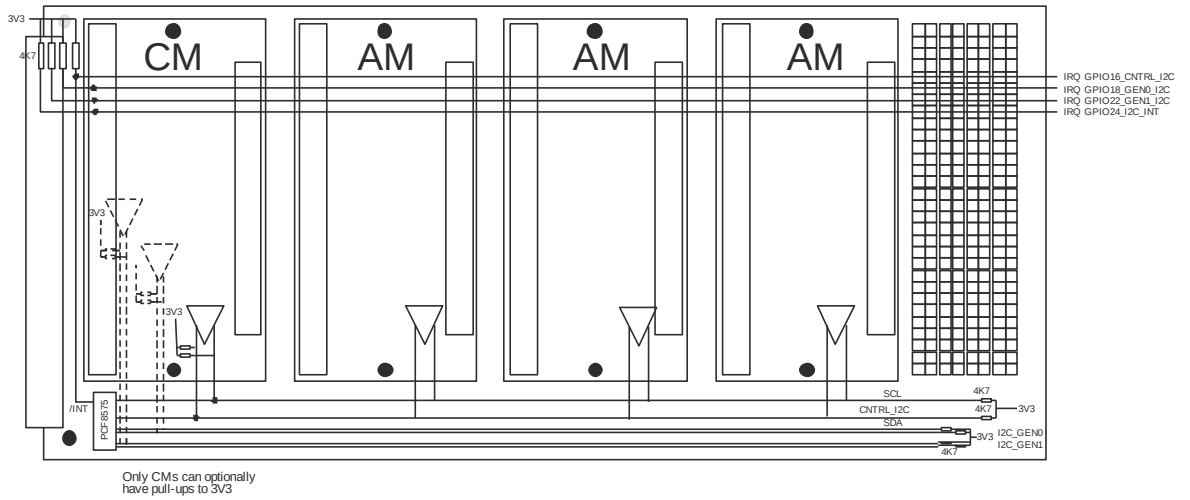
The EDP uses I2C as the data and control backbone. Depending on the capabilities of the CM fitted, up to three independent I2C busses are available. I2C channel “CNTRL_I2C” is the primary I2C device bus and is used by default to communicate with I2C devices on the baseboard and application modules.

The I2C address space is based on the 7-bit addressing scheme. I2C devices that are able to generate an interrupt request by default use the IRQ_GPIO16_CNTRL_I2C_INT line, with the option of using up to another three interrupt-capable lines. A pull-up resistor is provided on IRQ_GPIO16_CNTRL_I2C_INT so that the open collector /INT outputs on I2C devices can signal an interrupt by pulling this line down.

The I2C bus runs at 3V3 so any 5V devices must be connected via a level shifting mechanism.

The I2C bus devices require pull-up resistors on the SDA and SCL lines and these are incorporated on the baseboard.

There are three possible I2C channels available although in most cases the default one (I2C_CTRL) will be sufficient. EDP modules that carry I2C device do, where possible, allow the user to configure the I2C addresses. This allows for example, up to three digital IO modules to be fitted, with the GPIO devices on each module given an unique address. Where the address space of a particular I2C channel becomes full, devices can be connected to an alternative channel to get access to a completely new address space.



9.1.1 Default I2C Addresses

At the time of writing, the default addresses for the I2C devices on the existing modules are:

Module	I2C Device	Possible Range	Actual 7-bit Address Module 1	I2C channel	Actual 7-bit Address Module 2	I2C channel
Analog Module	MAX1138 address	0x35	0x35	CNTRL	0x35	Gen0
	MAX1038 address	0x65	0x65	CNTRL	0x65	Gen0
	AD5263 BRU50 address	0x2C-0x2F	0x2C	CNTRL	0x2C	Gen0
	PCA8575 address	0x20-0x27	0x21	CNTRL	0x21	Gen0
Baseboard	PCF9675	0x20-0x21	0x20	CNTRL	XXXXX	XXXXXX
	24LC32	0x50-0x57	0x51	CNTRL	xxxxx	xxxxx
Comms AM	RTC PCA8583	0x50-0x51	0x50	CNTRL	XXXXX	XXXXXX
Digital AM	PCF8575 IN address Or PCA9555	0x20-0x27	0x22	CNTRL	0x24	CNTRL
	PCF8575 OUT address Or PCA9555	0x20-0x27	0x23	CNTRL	0x25	CNTRL
Brushless DC Motor Drive MC2	dsPIC33 slave x 2	0x40 – 0x47	0x40 & 0x41	CNTR		

9.1.2 Available I2C Interrupt Request Lines

Each of the three potential I2C channels has a dedicated interrupt request line into the CM. A spare interrupt line is provided that can be allocated to any channel, as defined by the user. However it is up to user to make sure that the software is able to determine the I2C device that requested the interrupt.

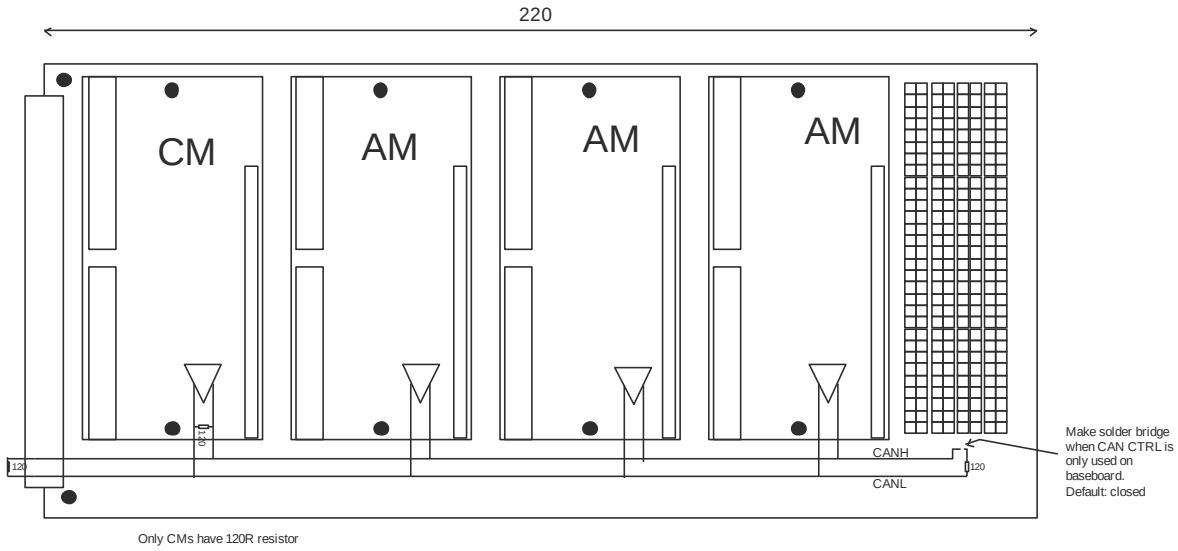
I2C_CTRL	IRQ GPIO16_CNTRL_I2C	(integral pull-ups)
I2C_GEN0	IRQ GPIO18_GEN0_I2C	(integral pull-ups)
I2C_GEN1	IRQ GPIO22_GEN1_I2C	(integral pull-ups)
Uncommitted	IRQ GPIO24_I2C_INT	(integral pull-ups)

9.2 CAN

The on-board CAN network comprises of both TTL level CAN signals, referred to as CAN0_TX/RX and CAN1_Rx/TX plus a physical layer CAN signals referred to as CANH0 and CANL0. Whilst the backplane supports two channels of TTL level CAN traffic the backplane only support one physical layer CAN channel.

The physical layer CAN is normally what is used to connect CAN devices together.
The CAN physical layer (i.e. after the CAN transceivers) and can run at up 1MB/s.
The 120R termination resistors at the ends of the network are located on the CPU Modules and also on the base board.
There are two 120ohm terminating resistor at two different points on the base board.
If the CANH0/L0 is taken off-board via the DIN14162 expansion connector then one of the 120R resistors on the baseboard must be disconnected via the P101/P401 links.

The CAN CNTRL bus is available through a 9D connector on the optional EDP-AM-CO1-A communications module. This Application Module also supports TTL level CAN traffic as well and can generate the physical layer CAN as an isolated output.



10. EDP Baseboard Jumper Settings

There are a number of user-definable jumpers on the baseboard. Their significance is given below. For the two slot base board most of the circuitry has not been populated during manufacturer but the user has the option to populate the missing circuitry. Should the user wish to do this he will have the functionality as indicated below.

Jumper	Type	Purpose	Default
P401	Solder	Apply 120R terminating resistor to on-board CAN	Closed
P101	Solder	Apply 120R terminating resistor to on-board CAN	Closed
JP501	Solder	Set address pin A0 for I2C GPIO	2-3
P504	Solder	VAGND and SGND shorting link option	Open
J601	Solder	Set address pin A0 for I2C EEPROM	1-2
J602	Solder	Set address pin A1 for I2C EEPROM	2-3
J603	Solder	Set address pin A2 for I2C EEPROM	2-3
J604	Solder	Enable write control /WC for EEPROM	Open

10.1 P401 - Terminating CAN Resistor

Most physical layer CAN networks require a 120 ohm terminating resistor at both ends of the network. The base boards provide a mechanism for this by having a 120 ohm terminating resistor selectable via a zero ohm resistor. P401 is located close to slot 4. The user should also note that a 120ohm terminating resistor is also provided also close to slot 1, selectable via P101. The user should ensure that the correct number of terminating resistors are selected.

P401 - Shorted	A 120 ohm terminating resistor in included between CAN0H and CAN0L close to slot 4
P401 - Open	No terminating resistor in included between CAN0H and CAN0L

10.2 P101 - Terminating CAN Resistor

Most physical layer CAN networks require a 120 ohm terminating resistor at both ends of the network. The base boards provide a mechanism for this by having a 120 ohm terminating resistor selectable via a zero ohm resistor. P101 is located close to slot 1. The user should also note that a 120ohm terminating resistor is also provided also close to slot 4, selectable via P401. The user should ensure that the correct number of terminating resistors are selected.

P101 - Shorted	A 120 ohm terminating resistor in included between CAN0H and CAN0L close to slot 1
P101 - Open	No terminating resistor in included between CAN0H and CAN0L

10.3 JP504 – VAGND and SGND shorting link

The VAGND and SGND signals can be shorted together with this link. See the section on grounding arrangements for more details of this option.

JP504 - Closed	The VAGND and the SGND grounds are shorted together
JP504 - Open	The VAGND and the SGND grounds are not shorted together

10.4 JP501 – DIP Switch A0 Slave Address selector

This jumper allows you to change the slave I2C address for the latch and DIP switch present on the base board.

JP501 – position 2-3	A0 is set to 0 7 bit I2C Slave address is 0x20

JP501 – position 1-2	A0 is set to 1 7 bit I2C Slave address is 0x21

10.5 J604 – Serial EEPROM write Protect Jumper

It is possible to protect the serial EEPROM from overwriting by inserting a zero ohm link in here or solder bridge. In normal operation the link is left open so the EEPROM can be read and written to.

J604 - Open	The EEPROM can be both written to and read from.
J605 - Closed	The EEPROM can only be read. The EEPROM is protected from both write and erase cycles.

10.6 J601, J602, J603 – I2C Slave Address Selector Serial EEPROM

These jumpers allow the user to change the slave I2C address of the base board serial EEPROM.

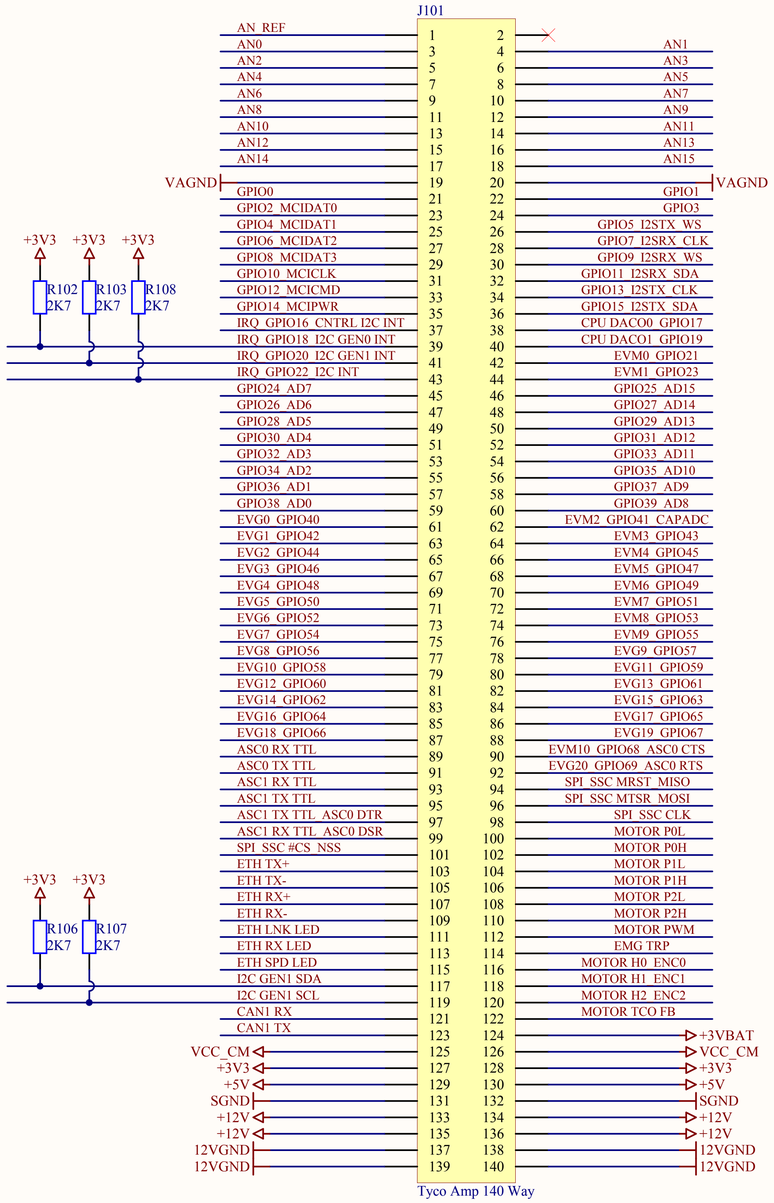
Jumper J603	Jumper J602	Jumper J601	Slave I2C Address
Position 2-3	Position 2-3	Position 2-3	0x50
Position 2-3	Position 2-3	Position 1-2	0x51 (default)
Position 2-3	Position 1-2	Position 2-3	0x52
Position 2-3	Position 1-2	Position 1-2	0x53
Position 1-2	Position 2-3	Position 2-3	0x54
Position 1-2	Position 2-3	Position 1-2	0x55
Position 1-2	Position 1-2	Position 2-3	0x56
Position 1-2	Position 1-2	Position 1-2	0x57

11. 3V Battery Backup

The four slot base board has provision for a 3V coin cell which provides a voltage to the VBATT signal on the back plane. This VBATT signal is used to support the Real Time Clock on the Communications Module during power down. Some of the CPU Modules also make use of the VBATT signal. The VBATT signal is not available on the two slot base board and hence the RS-EDP system has some reduced functionality. The user can link across the VBATT signal with the 3.3V signal if required on the break out connector. Most of the CPU modules also have the ability to select between VBATT and 3.3V in many cases via link options on the CPU Module.

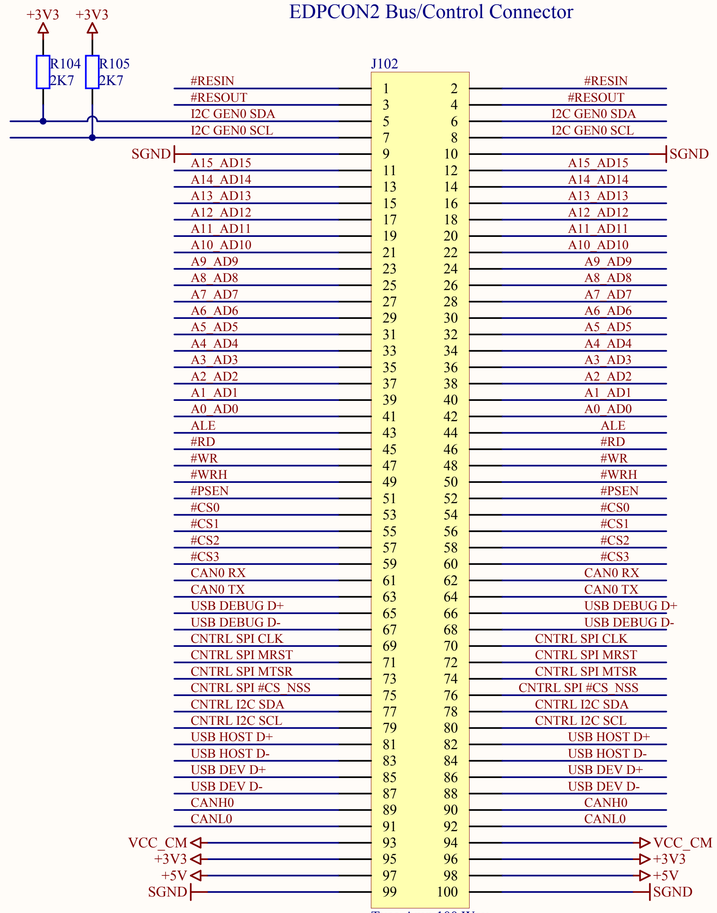
Module Position 1

EDPCON1 IO Connector

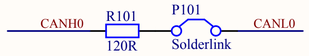


Tyco Amp 140 Way

EDPCON2 Bus/Control Connector



Tyco Amp 100 Way



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Module Position 2

EDPCON1 IO Connector

J201

AN_REF	1	2	
AN0	3	4	AN1
AN2	5	6	AN3
AN4	7	8	AN5
AN6	9	10	AN7
AN8	11	12	AN9
AN10	13	14	AN11
AN12	15	16	AN13
AN14	17	18	AN15
VAGND	19	20	VAGND
GPIO0	21	22	GPIO1
GPIO2_MCIDAT0	23	24	GPIO3
GPIO4_MCIDAT1	25	26	GPIO5_I2STX_WS
GPIO6_MCIDAT2	27	28	GPIO7_I2SRX_CLK
GPIO8_MCIDAT3	29	30	GPIO9_I2SRX_WS
GPIO10_MCICLK	31	32	GPIO11_I2SRX_SDA
GPIO12_MCICMD	33	34	GPIO13_I2STX_CLK
GPIO14_MCIPWR	35	36	GPIO15_I2STX_SDA
IRQ_GPIO16_CNTRL I2C INT	37	38	CPU DACO0_GPIO17
IRQ_GPIO18_I2C GEN0 INT	39	40	CPU DACO1_GPIO19
IRQ_GPIO20_I2C GEN1 INT	41	42	EVM0_GPIO21
IRQ_GPIO22_I2C INT	43	44	EVM1_GPIO23
GPIO24_AD7	45	46	GPIO25_AD15
GPIO26_AD6	47	48	GPIO27_AD14
GPIO28_AD5	49	50	GPIO29_AD13
GPIO30_AD4	51	52	GPIO31_AD12
GPIO32_AD3	53	54	GPIO33_AD11
GPIO34_AD2	55	56	GPIO35_AD10
GPIO36_AD1	57	58	GPIO37_AD9
GPIO38_AD0	59	60	GPIO39_AD8
EVG0_GPIO40	61	62	EVM2_GPIO41_CAPADC
EVG1_GPIO42	63	64	EVM3_GPIO43
EVG2_GPIO44	65	66	EVM4_GPIO45
EVG3_GPIO46	67	68	EVM5_GPIO47
EVG4_GPIO48	69	70	EVM6_GPIO49
EVG5_GPIO50	71	72	EVM7_GPIO51
EVG6_GPIO52	73	74	EVM8_GPIO53
EVG7_GPIO54	75	76	EVM9_GPIO55
EVG8_GPIO56	77	78	EVG9_GPIO57
EVG10_GPIO58	79	80	EVG11_GPIO59
EVG12_GPIO60	81	82	EVG13_GPIO61
EVG14_GPIO62	83	84	EVG15_GPIO63
EVG16_GPIO64	85	86	EVG17_GPIO65
EVG18_GPIO66	87	88	EVG19_GPIO67
ASC0 RX TTL	89	90	EVM10_GPIO68_ASC0 CTS
ASC0 TX TTL	91	92	EVG20_GPIO69_ASC0 RTS
ASC1 RX TTL	93	94	SPI_SSC MRST_MISO
ASC1 TX TTL	95	96	SPI_SSC MTSR_MOSI
ASC1 TX TTL_ASC0 DTR	97	98	SPI_SSC CLK
ASC1 RX TTL_ASC0 DSR	99	100	MOTOR P0L
SPI_SSC #CS_NSS	101	102	MOTOR P0H
ETH TX+	103	104	MOTOR P1L
ETH TX-	105	106	MOTOR P1H
ETH RX+	107	108	MOTOR P2L
ETH RX-	109	110	MOTOR P2H
ETH LNK LED	111	112	MOTOR PWM
ETH RX LED	113	114	EMG TRP
ETH SPD LED	115	116	MOTOR H0_ENC0
I2C GEN1 SDA	117	118	MOTOR H1_ENC1
I2C GEN1 SCL	119	120	MOTOR H2_ENC2
CAN1 RX	121	122	MOTOR TCO FB
CAN1 TX	123	124	+3VBAT
VCC_CM	125	126	VCC_CM
+3V3	127	128	+3V3
+5V	129	130	+5V
SGND	131	132	SGND
+12V	133	134	+12V
+12V	135	136	+12V
12VGND	137	138	12VGND
12VGND	139	140	12VGND

Tyco Amp 140 Way

EDPCON2 Bus/Control Connector

J202

#RESIN	1	2	#RESIN
#RESOUT	3	4	#RESOUT
I2C GEN0 SDA	5	6	I2C GEN0 SDA
I2C GEN0 SCL	7	8	I2C GEN0 SCL
SGND	9	10	SGND
A15_AD15	11	12	A15_AD15
A14_AD14	13	14	A14_AD14
A13_AD13	15	16	A13_AD13
A12_AD12	17	18	A12_AD12
A11_AD11	19	20	A11_AD11
A10_AD10	21	22	A10_AD10
A9_AD9	23	24	A9_AD9
A8_AD8	25	26	A8_AD8
A7_AD7	27	28	A7_AD7
A6_AD6	29	30	A6_AD6
A5_AD5	31	32	A5_AD5
A4_AD4	33	34	A4_AD4
A3_AD3	35	36	A3_AD3
A2_AD2	37	38	A2_AD2
A1_AD1	39	40	A1_AD1
A0_AD0	41	42	A0_AD0
ALE	43	44	ALE
#RD	45	46	#RD
#WR	47	48	#WR
#WRH	49	50	#WRH
#PSEN	51	52	#PSEN
#CS0	53	54	#CS0
#CS1	55	56	#CS1
#CS2	57	58	#CS2
#CS3	59	60	#CS3
CAN0 RX	61	62	CAN0 RX
CAN0 TX	63	64	CAN0 TX
USB DEBUG D+	65	66	USB DEBUG D+
USB DEBUG D-	67	68	USB DEBUG D-
CNTRL SPI CLK	69	70	CNTRL SPI CLK
CNTRL SPI MRST	71	72	CNTRL SPI MRST
CNTRL SPI MTSR	73	74	CNTRL SPI MTSR
CNTRL SPI #CS_NSS	75	76	CNTRL SPI #CS_NSS
CNTRL I2C SDA	77	78	CNTRL I2C SDA
CNTRL I2C SCL	79	80	CNTRL I2C SCL
USB HOST D+	81	82	USB HOST D+
USB HOST D-	83	84	USB HOST D-
USB DEV D+	85	86	USB DEV D+
USB DEV D-	87	88	USB DEV D-
CANH0	89	90	CANH0
CANL0	91	92	CANL0
VCC_CM	93	94	VCC_CM
+3V3	95	96	+3V3
+5V	97	98	+5V
SGND	99	100	SGND

Tyco Amp 100 Way

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Approved By:	Size: A3	Number: EDP-BB-4AB	Revision: B	*Sir William Lyons Road*
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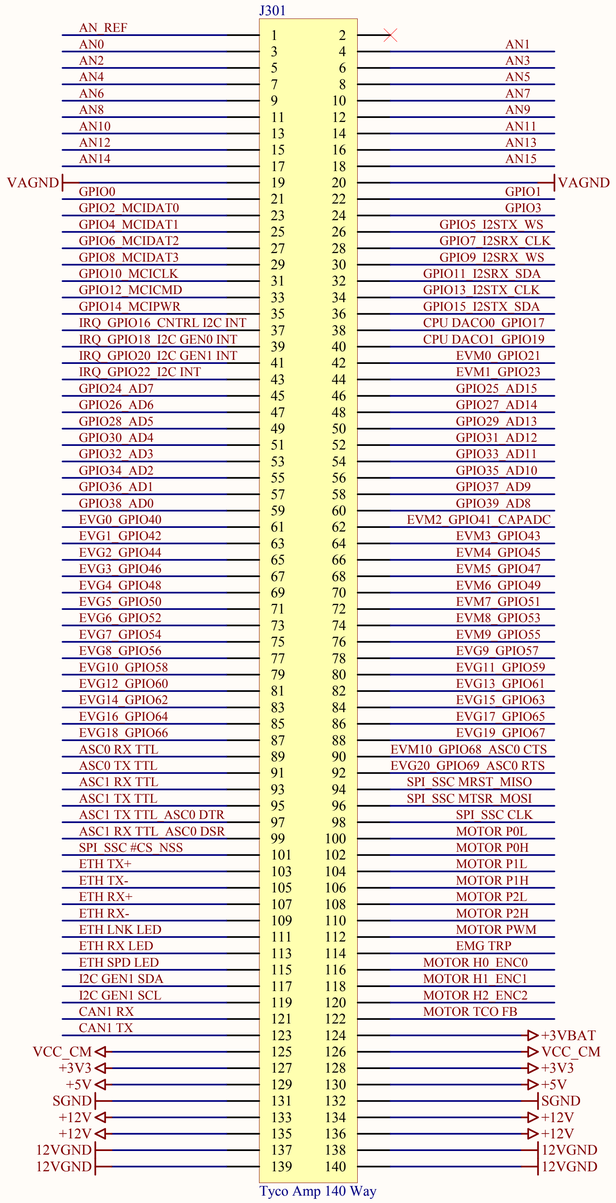
	File: E:\PCB Designs\DXP\EDP-BB-4\EDP-BB-4A\EDP-BB-4A B\Module Connectors 2.SchDoc		Author: A.Davison	*Coventry*

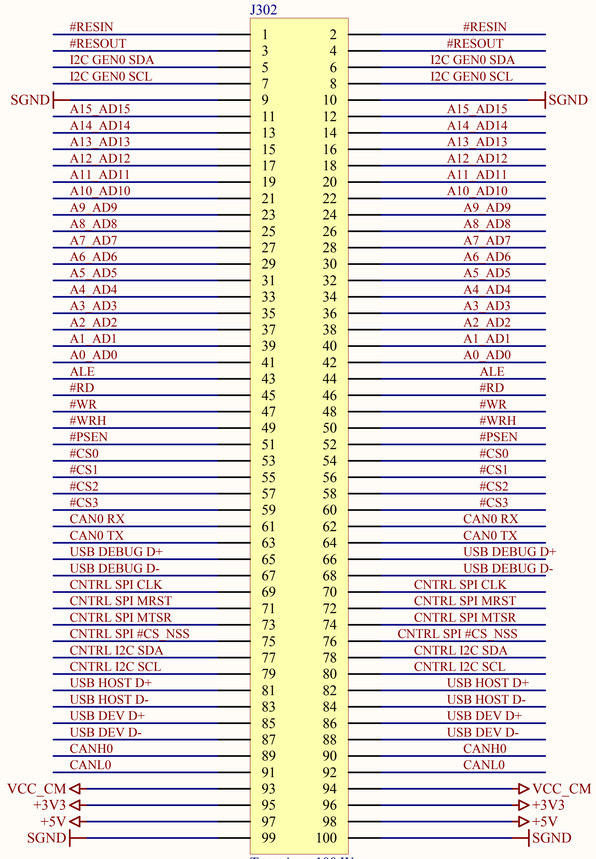
Module Position 3

EDPCON1 IO Connector



Tyco Amp 140 Way

EDPCON2 Bus/Control Connector



Tyco Amp 100 Way

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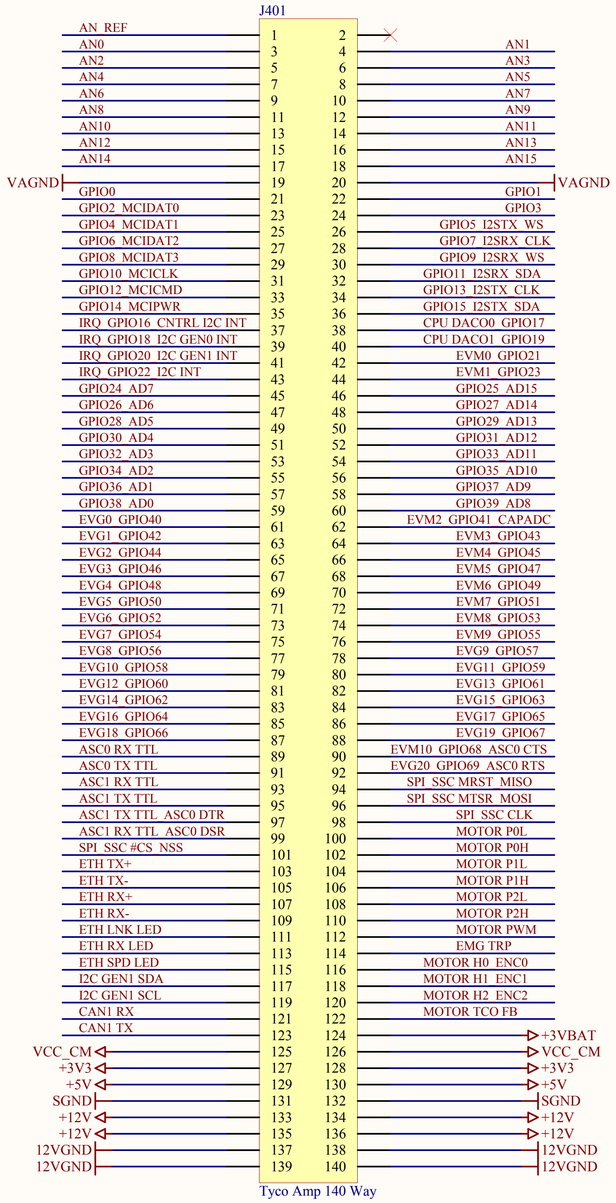
Module Position 4

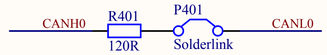
EDPCON1 IO Connector



Tyco Amp 140 Way

EDPCON2 Bus/Control Connector

Tyco Amp 100 Way



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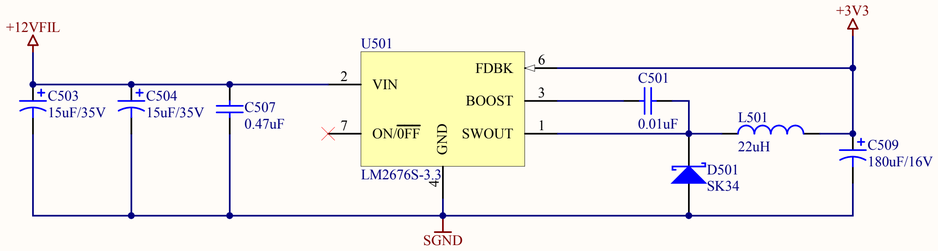
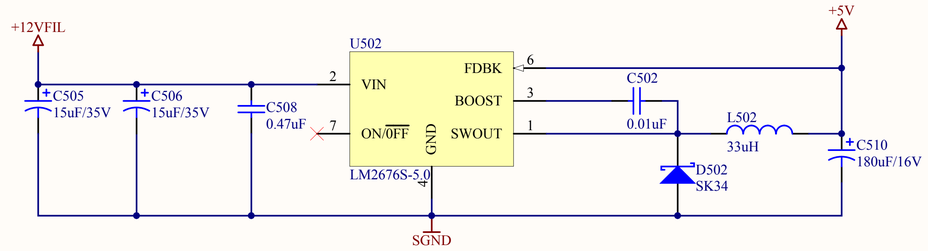
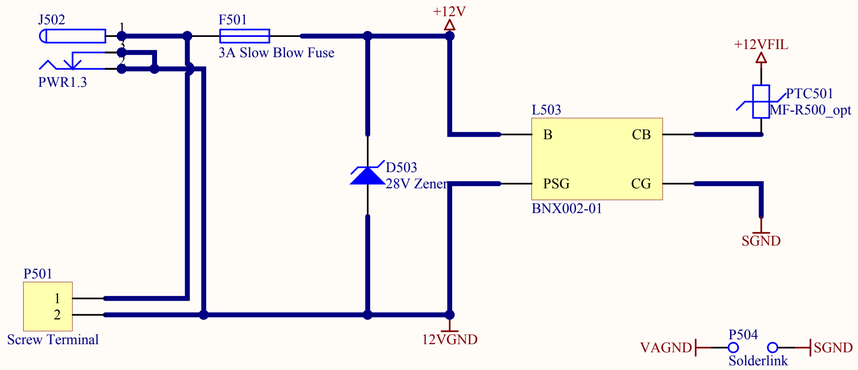
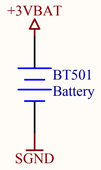
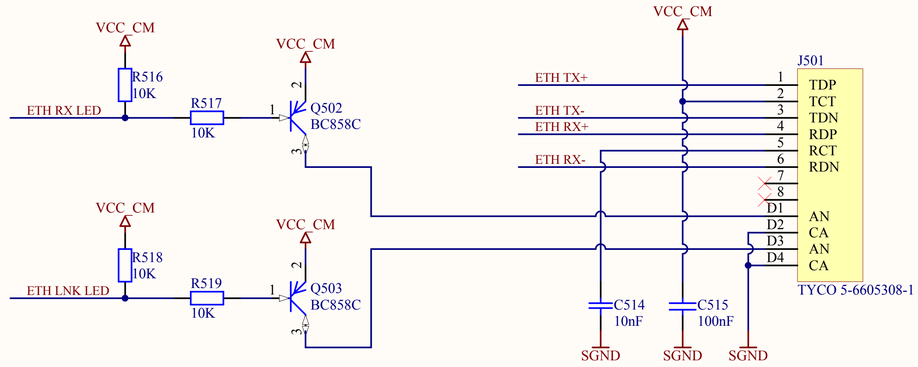


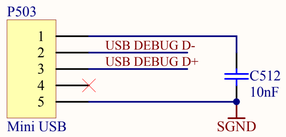




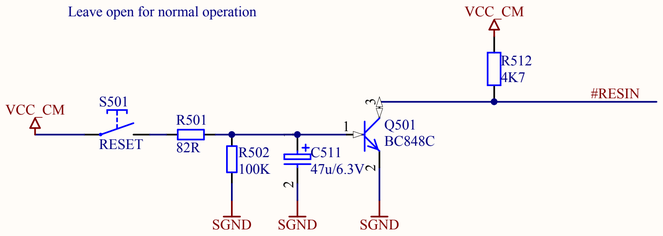


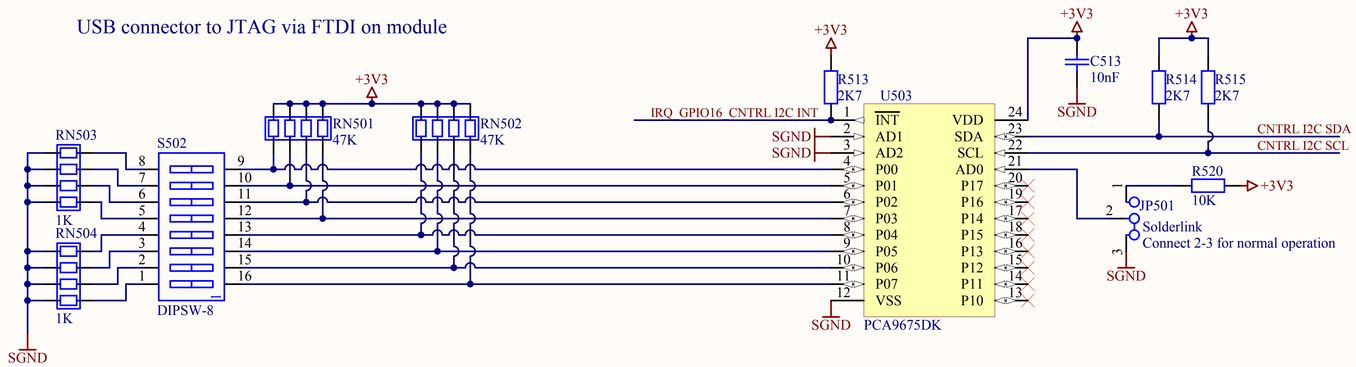


EDP DIN41612 Expansion

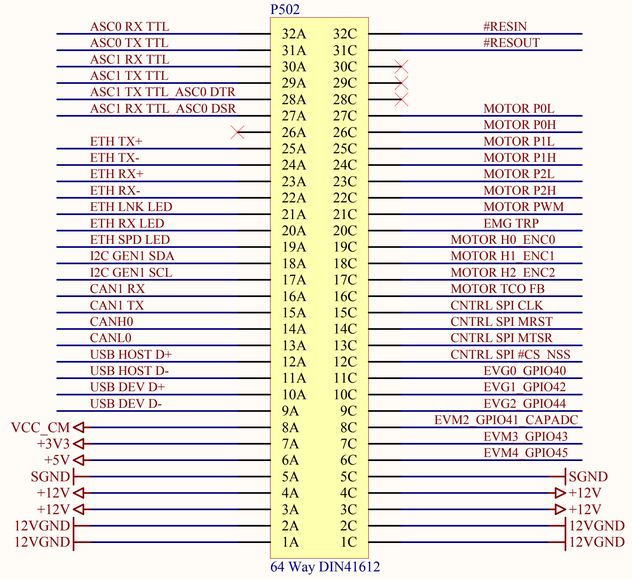


USB connector to JTAG via FTDI on module





General IO, switches off when not required



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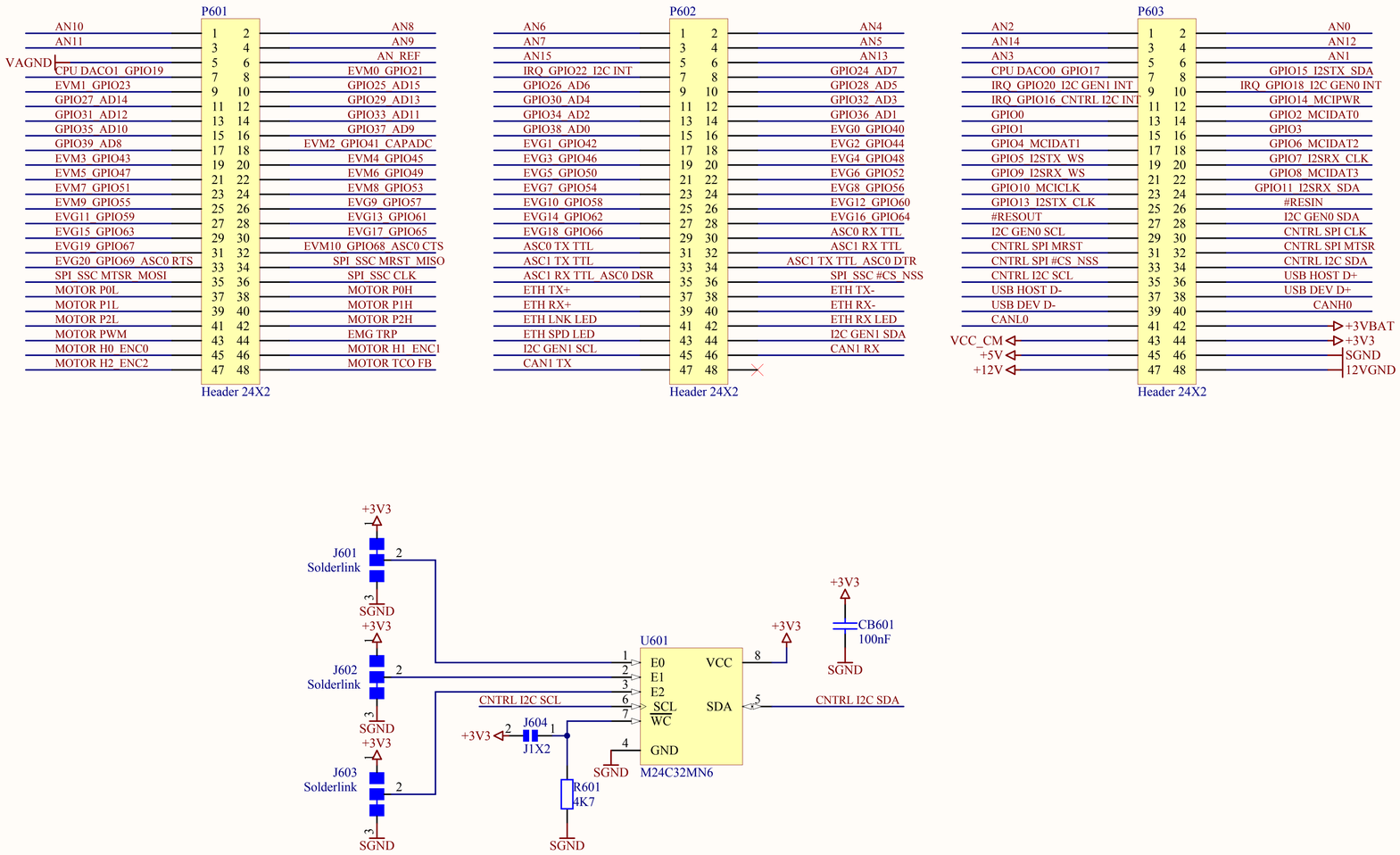

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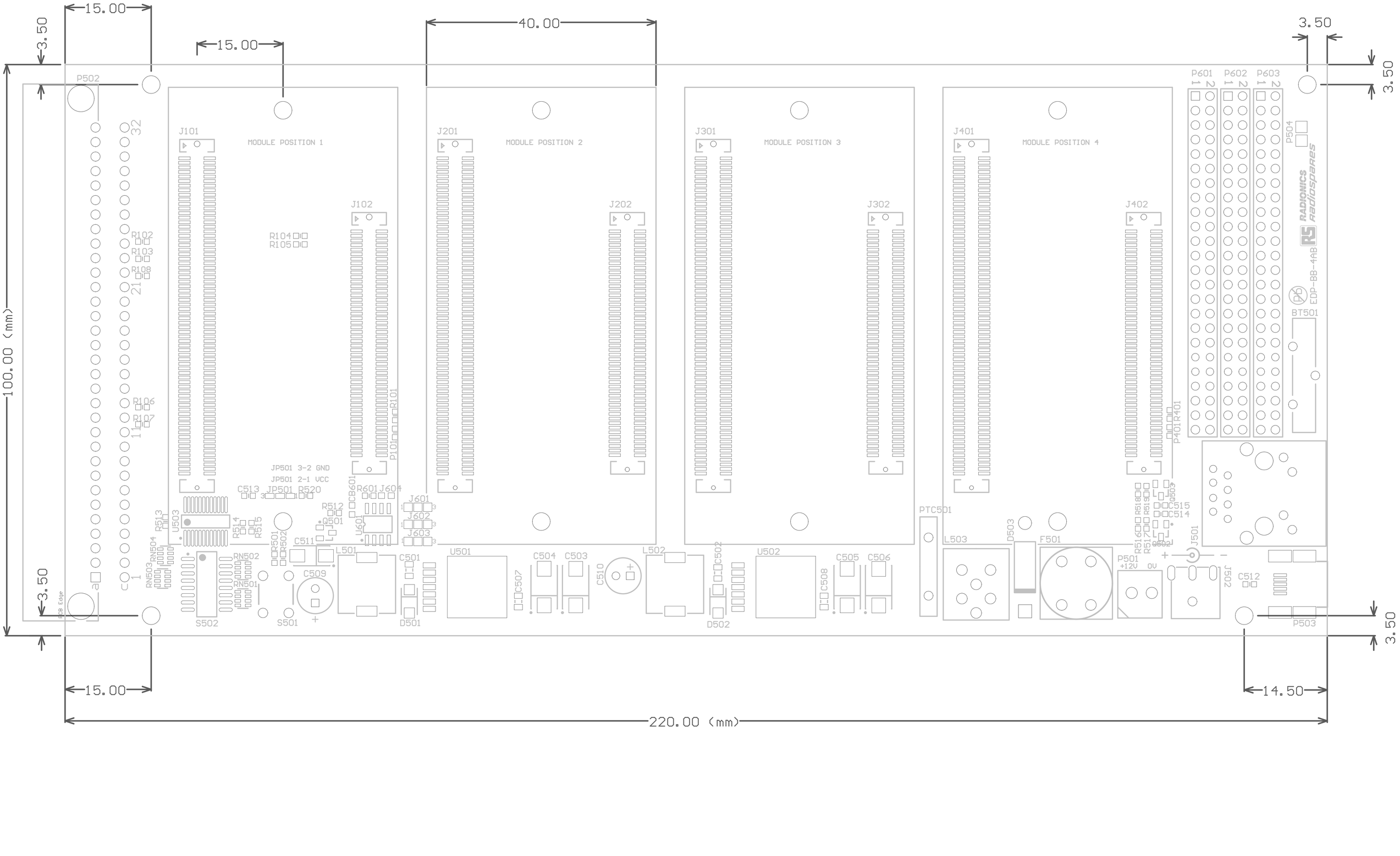
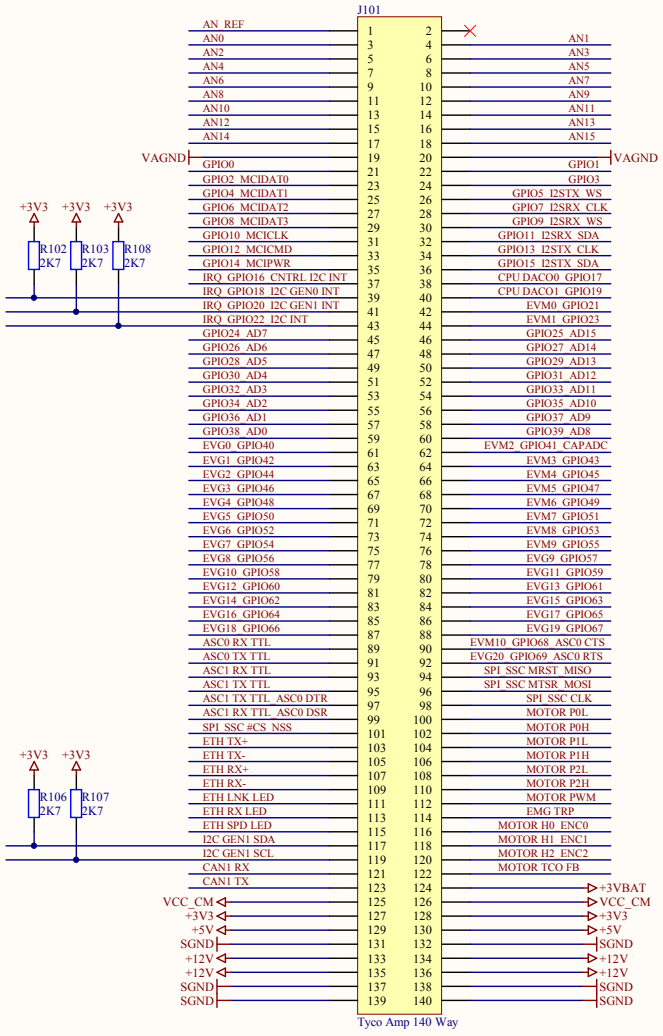
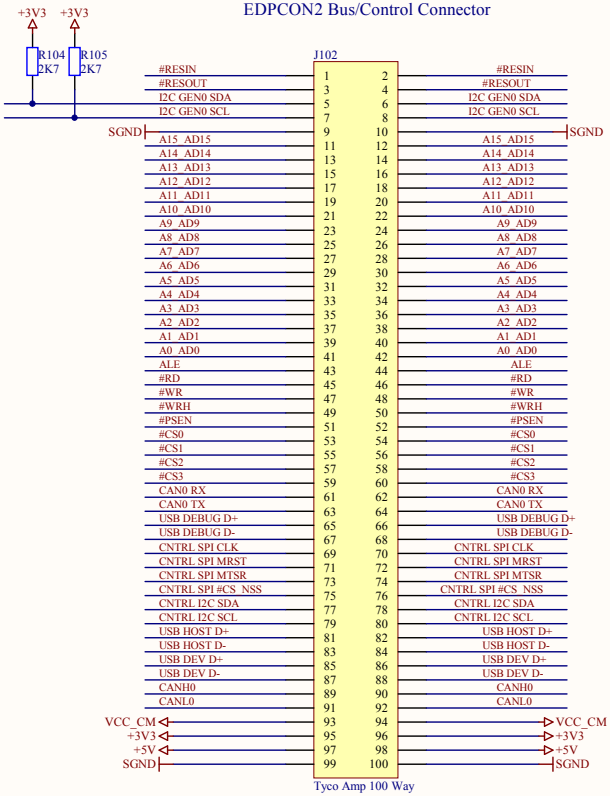

15.00
15.00
40.00
3.50
3.50
3.50
100.00 (mm)
3.50
15.00
14.50
220.00 (mm)
P502
J101
MODULE POSITION 1
J102
J201
MODULE POSITION 2
J202
J301
MODULE POSITION 3
J302
J401
MODULE POSITION 4
J402
P601
P602
P603
P504
BT501
EDP-BB-4AB
RADIONICS
radiospares
JP501 3-2 GND
JP501 2-1 VCC
PTC501
L503
D503
F501
P501
+12V
0V
J501
J502
P503
C512
C513
C514
C515
U503
U501
U502
L501
L502
D501
D502
S501
S502
C501
C502
C503
C504
C505
C506
C507
C508
C509
C510
C511
R102
R103
R104
R105
R106
R107
R108
R512
R513
R514
R515
R520
R601
RN501
RN502
RN503
RN504
Q501
Q502
Q503
J601
J602
J603
J604
CB601
PCB Edge

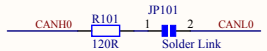
Module Position 1

EDPCON1 IO Connector



EDPCON2 Bus/Control Connector





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Approved By:	Size: A3	Number: EDP-BB-2A	Revision: A1
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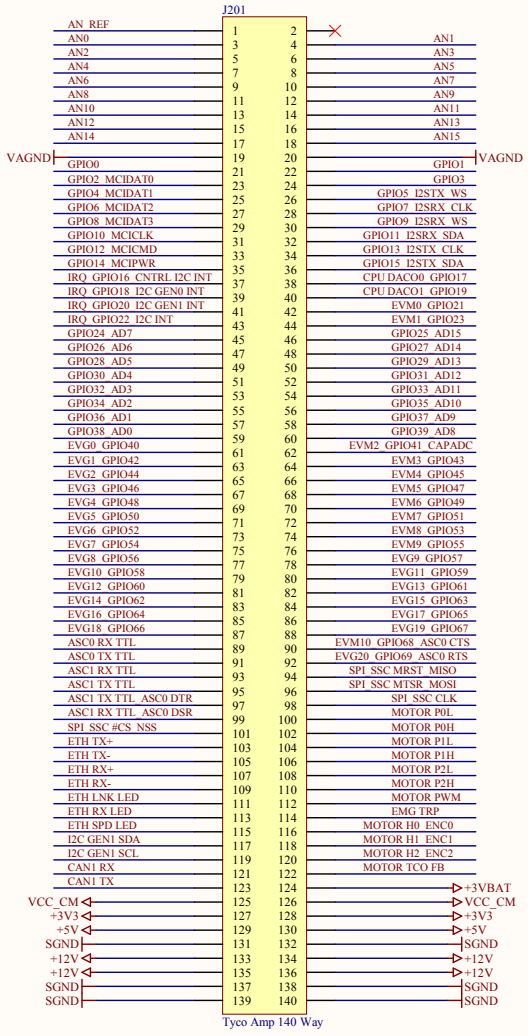
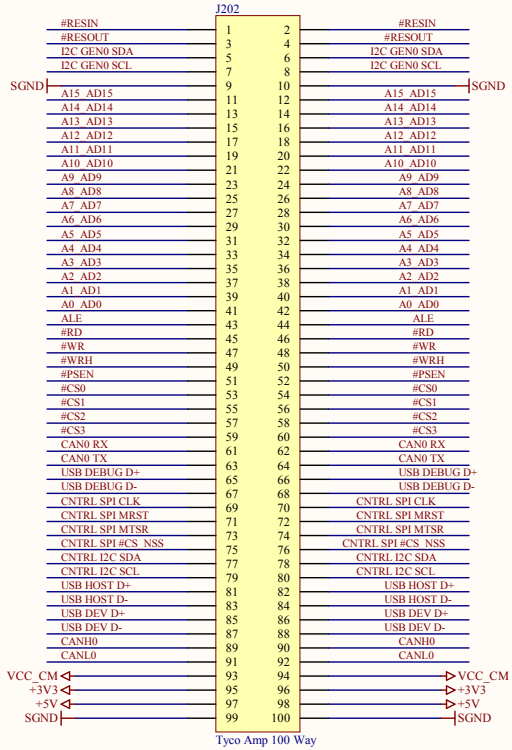
Module Position 4

EDPCON1 IO Connector



EDPCON2 Bus/Control Connector



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Approved By:	Size: A3	Number: EDP-BB-2A	Revision: A1
	Date: 21/04/2010 (c) Hitex (UK) Ltd.	Sheet2 of 4	
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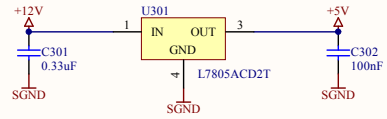
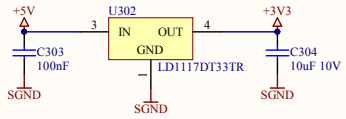
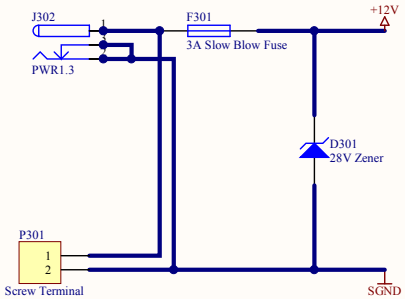
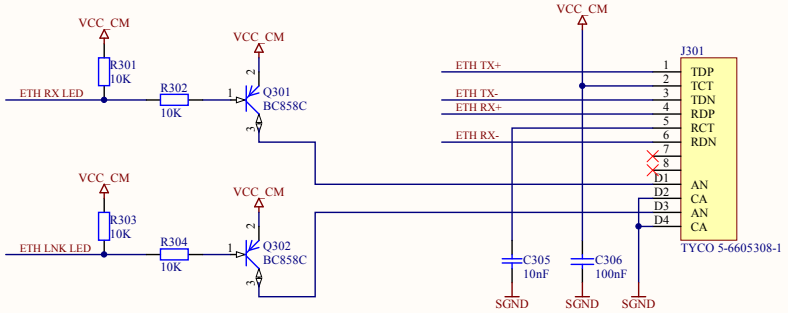
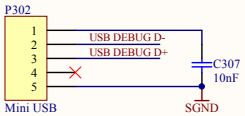
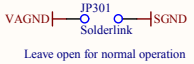


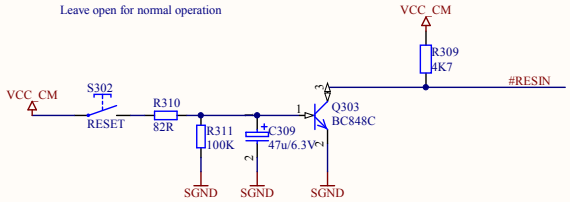






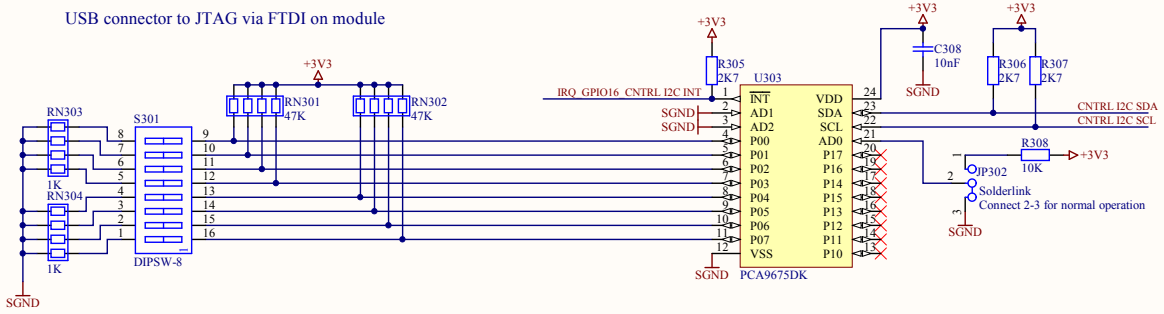






NOT POPULATED OPTION

USB connector to JTAG via FTDI on module



General IO, switches off when not required

Checked By:	Title: *Supply, EDP Expansion, Misc*		*Hitex (UK) Ltd.*
Approved By:	Size: A3	Number: EDP-BB-2A	Revision: A1	*Sir William Lyons Road*
	Date: 21/04/2010	(c) Hitex (UK) Ltd.	Sheet3 of 4	*University of Warwick Science Park*
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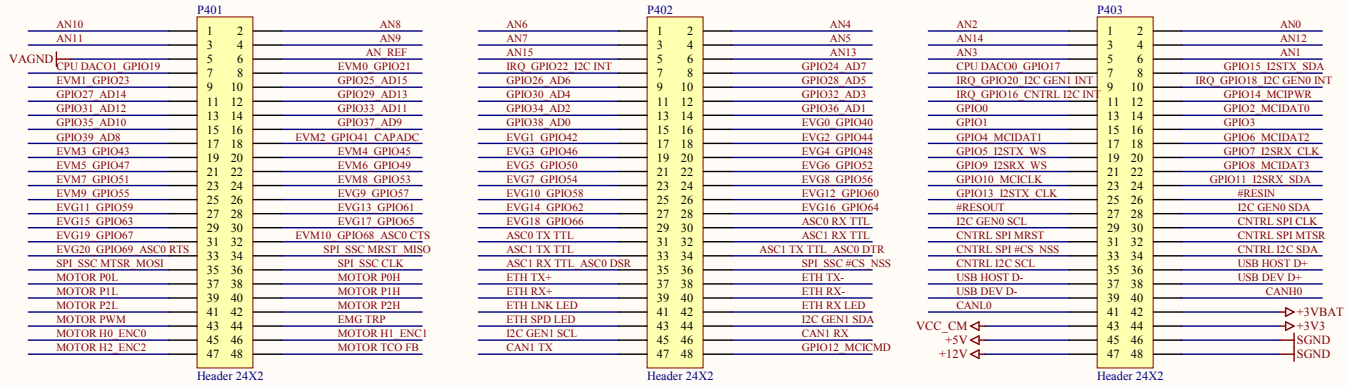
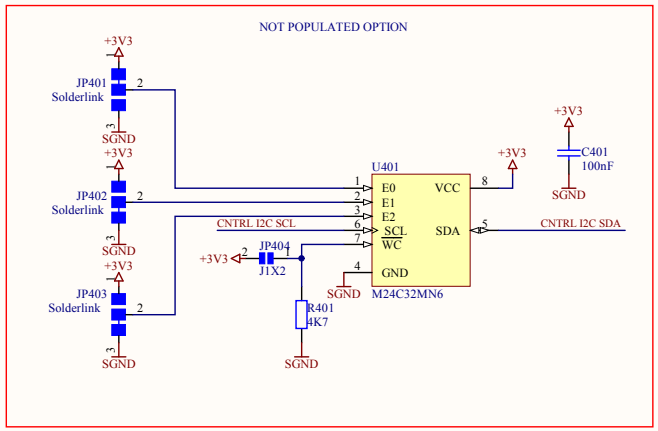
hitex DEVELOPMENT TOOLS

Author: A.Davison





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Approved By:	Size: A3	Number: EDP-BB-2A	Revision: A1
	Date: 21/04/2010	(c) Hitex (UK) Ltd.	Sheet4 of 4
	File: D:\PCB Designs\DXP\EDP-BB-2\EDP-BB-2A\IO Patch Connectors.SchDoc		Author: A.Davison

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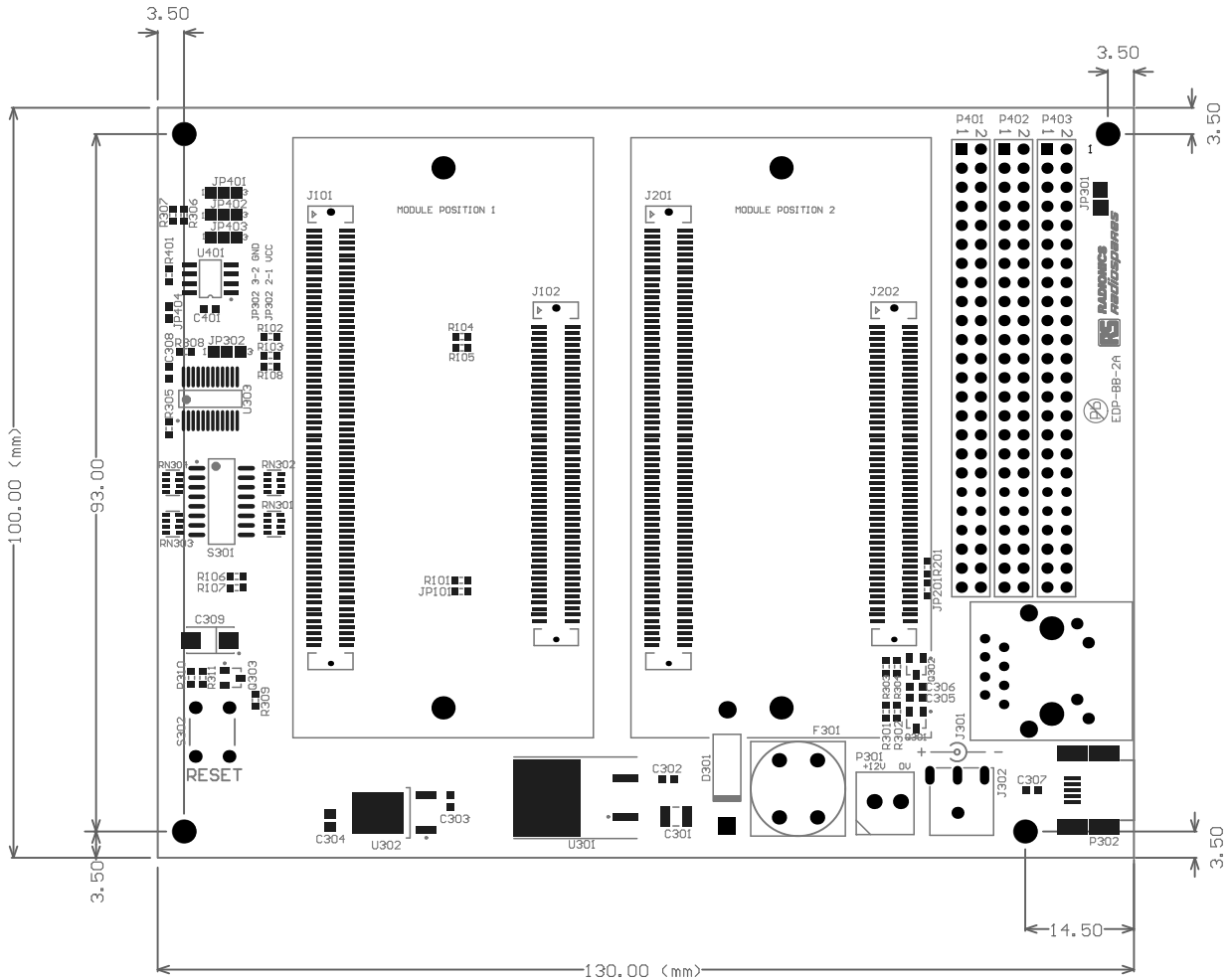
hitex DEVELOPMENT TOOLS



MATERIALS REQUIREMENTS

MATERIAL:	☐	FR4							
THICKNESS:	☐ 0.8mm	☐ 1.2mm	☒ 1.6mm	☐ 2.4mm	☐ 3.2mm				
TOLERANCE:	☒ IN A/W IPC-D-300G	CLASS	2	☐ OTHER +/-					
BOW & TWIST:	☒ IN A/W IPC-D-300G	CLASS	2	☐ AS SHOWN					

COPPER THICKNESS (FINISHED)

OUTER:	☐ 18um	☒ 35um	☐ 70um
INNER SIGNAL:	☐ 18um	☒ 35um	☐ 70um
INNER PLANE:	☐ 18um	☒ 35um	☐ 70um

COPPER LAYER STRUCTURE

LAYER NUMBER	DESCRIPTION	GERBER EXT.
1	COMPONENT SIDE	GTL
2	GROUND PLANE	GP1
3	INNER SIGNAL	G1
4	INNER SIGNAL	G2
5	POWER PLANE	GP2
6	SOLDER SIDE	GBL

SPECIAL CONSIDERATIONS

SEE .REP FILE FOR FULL GERBER INFO.

DRILLING AND FINISH REQUIREMENTS

VIEWED FROM:	☒ COMPONENT SIDE	☐ SOLDER SIDE	
REFERENCE:	☐ AS SHOWN	☐ PATTERN MASTER LIST	☒ NC DRILL FILES
PTH MINIMUM COPPER THICKNESS	☒ 20um	☐ OTHER	
NPTH	☐ TENTED	☐ PADS REMOVED	☐ REMOVE PADS
	☐ 2ND DRILL	☐ BOTH	☒ AS SHOWN ☐ NONE
VIAS	☒ TENTED	☒ COMPONENT SIDE	☐ SOLDER SIDE
LEGEND & SCREEN PRINT:	☐ NONE	☒ COMPONENT	☐ SOLDER
COLOR:	☐ YELLOW	☒ WHITE	☐ OTHER
SOLDER RESIST:	☒ LIQUID PHOTOIMAGEABLE	☐ SCREEN PRINT	
FINISH:	☐ MATTE	☐ GLOSS	☒ EITHER
COLOUR:	☒ RED	☐ GREEN	☐ YELLOW ☐ BLUE ☐ OTHER
TRACK FINISH:	☒ SELECTIVE SOLDER (HASL)	☐ REFLOW SOLDER	
	☐ 0.1um - 0.2um ELECTROLESS GOLD OVER 3um NICKEL		
	☐ IMMERSION GOLD	☐ OTHER	

ADDITIONAL NOTES:

VIAS IN PAD TENTED ON COMPONENT SIDE. OTHER VIAS NOT TENTED.

HITEX (UK) LTD.
Sir William Lyons Road
Coventry
CV4 7EZ
ENGLAND

ENGINEER: A.Davison, D.Giles	TITLE: EDP-BB-2A		
PCB DESIGNER: A.Davison			
DATE: 19/04/2010	PART NO.: EDP-BB-2A	REV: A1	
FILE NAME: EDP-BB-2A_A1.PcbDoc	DWG NO:	SCALE: 1:1	