

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CE

500V CoolMOS™ CE Power Transistor
IPD50R280CE

Data Sheet

Rev. 2.1
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE series combines the experience of the leading SJ MOSFET supplier with high class innovation while representing a cost appealing alternative compared to standard MOSFETs in target applications. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

Features ¹⁾

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Pb-free plating, available with halogen free and non-halogen free mold compound¹⁾

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, LCD & PDP TV and Lighting.

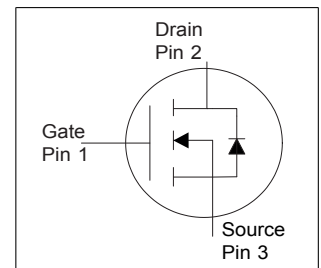
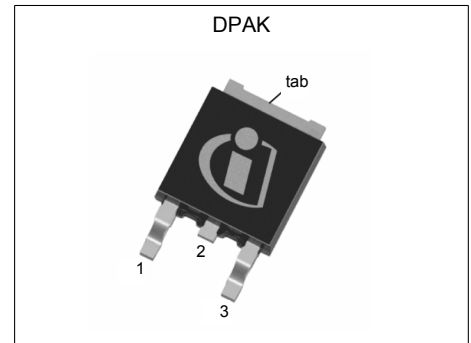


Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|----------------------|-------|------------|
| $V_{DS} @ T_{j,max}$ | 550 | V |
| $R_{DS(on),max}$ | 0.28 | Ω |
| $Q_{g,typ}$ | 32.6 | nC |
| $I_{D,pulse}$ | 42.9 | A |
| $E_{oss@400V}$ | 3.2 | μ J |
| Body diode di/dt | 500 | A/ μ s |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|-----------|---------|----------------|
| IPD50R280CE | PG-TO 252 | 5R280CE | see Appendix A |

¹⁾ Halogen free version is available with OPN: IPD50R280CEAT

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|----------------|------------|------|-----------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 13 8.2 | A | $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 42.9 | A | $T_C = 25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 231 | mJ | $I_D = 5.2\text{A}$; $V_{DD} = 50\text{V}$ |
| Avalanche energy, repetitive | E_{AR} | - | - | 0.35 | mJ | $I_D = 5.2\text{A}$; $V_{DD} = 50\text{V}$ |
| Avalanche current, repetitive | I_{AR} | - | - | 5.2 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 50 | V/ns | $V_{DS} = 0 \dots 400\text{V}$ |
| Gate source voltage | V_{GS} | -20 -30 | - | 20 30 | V | static; AC ($f > 1\text{ Hz}$) |
| Power dissipation (non FullPAK) TO-252 | P_{tot} | - | - | 92 | W | $T_C = 25^\circ\text{C}$ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 150 | $^\circ\text{C}$ | - |
| Continuous diode forward current | I_S | - | - | 11.3 | A | $T_C = 25^\circ\text{C}$ |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | - | - | 42.9 | A | $T_C = 25^\circ\text{C}$ |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 15 | V/ns | $V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$ |
| Maximum diode commutation speed ³⁾ | di/dt | - | - | 500 | A/ μs | $V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$ |

3 Thermal characteristics

Table 3 Thermal characteristics DPAK

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|---------|---------|--------------------|--|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 1.36 | $^\circ\text{C/W}$ | - |
| Thermal resistance, junction - ambient ⁴⁾ | R_{thJA} | - | - 35 | 62 - | $^\circ\text{C/W}$ | SMD version, device on PCB, minimal footprint SMD version, device on PCB, 6cm ² cooling area ⁴⁾ |
| Soldering temperature, wave- & reflowsoldering allowed | T_{sold} | - | - | 260 | $^\circ\text{C}$ | reflow MSL 1 |

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DClmk}=400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

⁴⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70 μm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|------|------|----------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 500 | - | - | V | $V_{GS}=0V, I_D=1mA$ |
| Gate threshold voltage | $V_{(GS)th}$ | 2.50 | 3 | 3.50 | V | $V_{DS}=V_{GS}, I_D=0.35mA$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 1 | μA | $V_{DS}=500V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=500V, V_{GS}=0V, T_j=150^\circ C$ |
| Gate-source leakage current | I_{GSS} | - | - | 100 | nA | $V_{GS}=20V, V_{DS}=0V$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.25 | 0.28 | Ω | $V_{GS}=13V, I_D=4.2A, T_j=25^\circ C$ $V_{GS}=13V, I_D=4.2A, T_j=150^\circ C$ |
| Gate resistance | R_G | - | 3 | - | Ω | $f=1\text{ MHz, open drain}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 773 | - | pF | $V_{GS}=0V, V_{DS}=100V, f=1MHz$ |
| Output capacitance | C_{oss} | - | 49 | - | pF | $V_{GS}=0V, V_{DS}=100V, f=1MHz$ |
| Effective output capacitance, energy related ¹⁾ | $C_{o(er)}$ | - | 40 | - | pF | $V_{GS}=0V, V_{DS}=0\dots 400V$ |
| Effective output capacitance, time related ²⁾ | $C_{o(tr)}$ | - | 173 | - | pF | $I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots 400V$ |
| Turn-on delay time | $t_{d(on)}$ | - | 8 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=5.2A, R_G=3.4\Omega$ |
| Rise time | t_r | - | 6.4 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=5.2A, R_G=3.4\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 40 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=5.2A, R_G=3.4\Omega$ |
| Fall time | t_f | - | 7.6 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=5.2A, R_G=3.4\Omega$ |

Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 4.2 | - | nC | $V_{DD}=400V, I_D=5.2A, V_{GS}=0\text{ to }10V$ |
| Gate to drain charge | Q_{gd} | - | 17.1 | - | nC | $V_{DD}=400V, I_D=5.2A, V_{GS}=0\text{ to }10V$ |
| Gate charge total | Q_g | - | 32.6 | - | nC | $V_{DD}=400V, I_D=5.2A, V_{GS}=0\text{ to }10V$ |
| Gate plateau voltage | $V_{plateau}$ | - | 5.3 | - | V | $V_{DD}=400V, I_D=5.2A, V_{GS}=0\text{ to }10V$ |

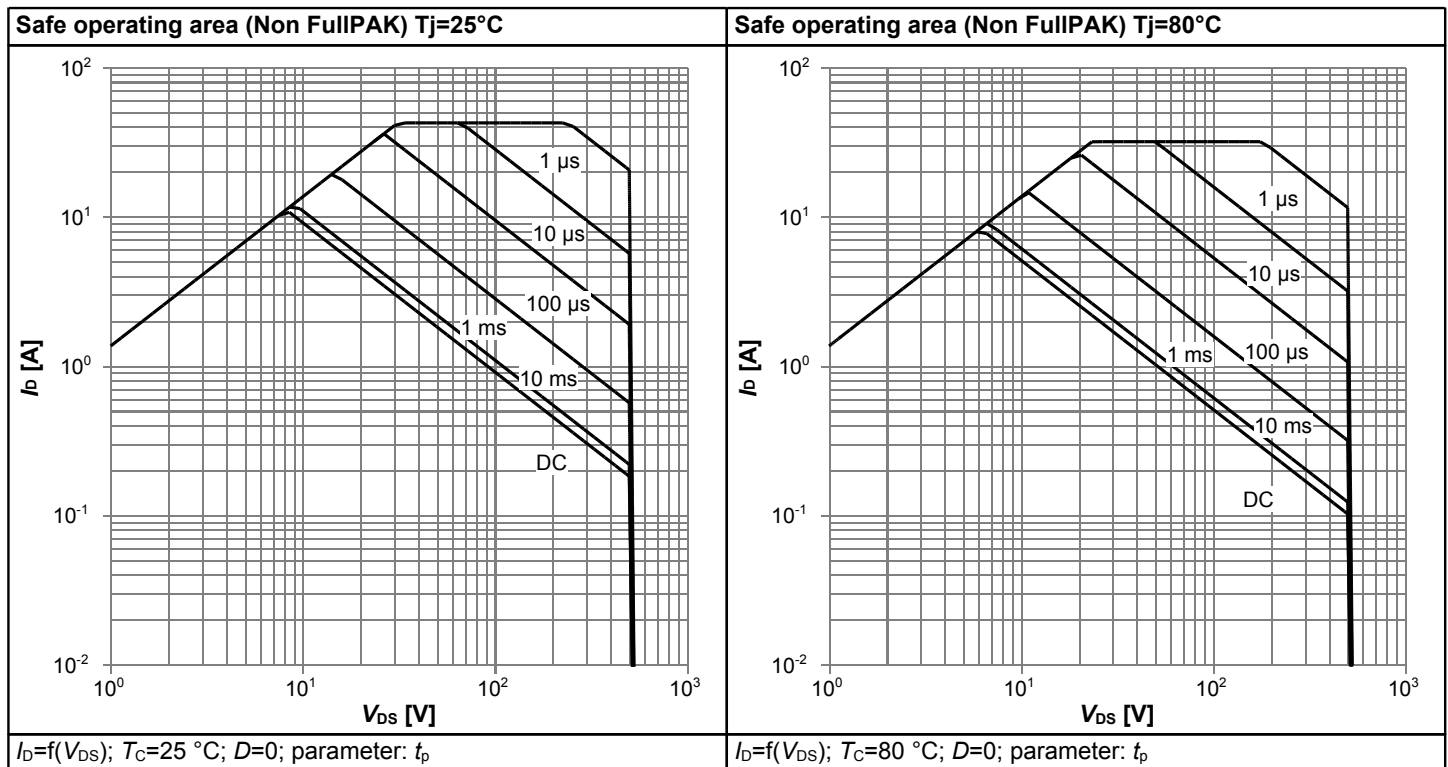
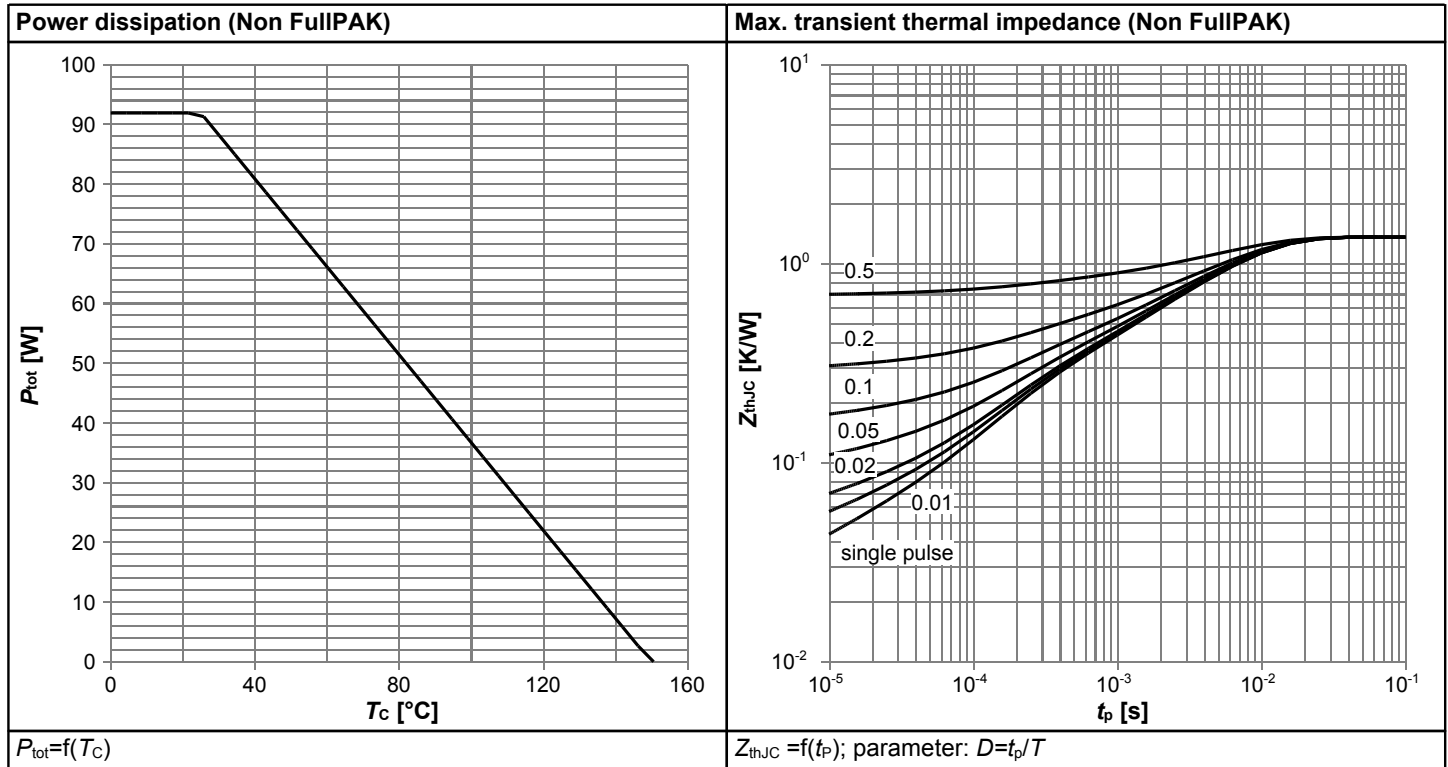
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

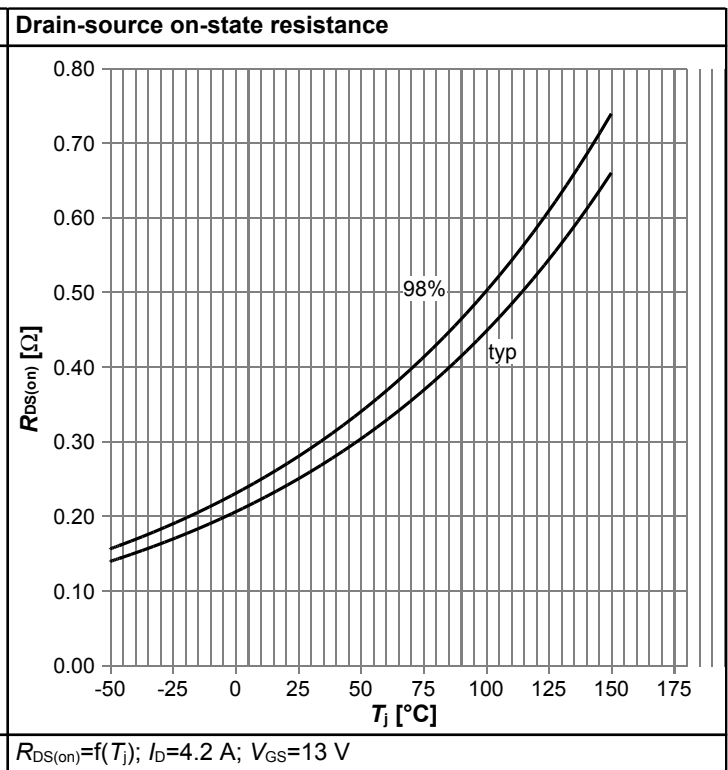
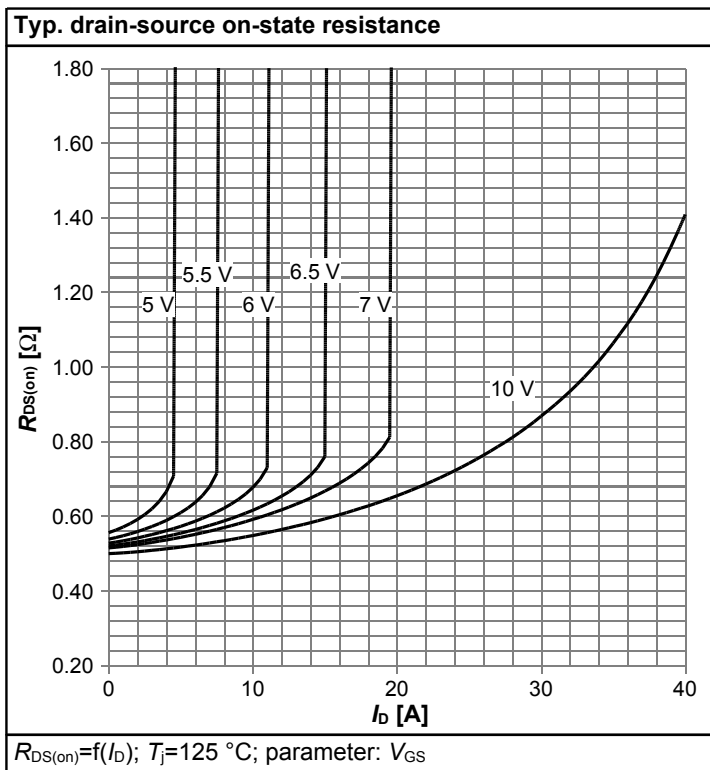
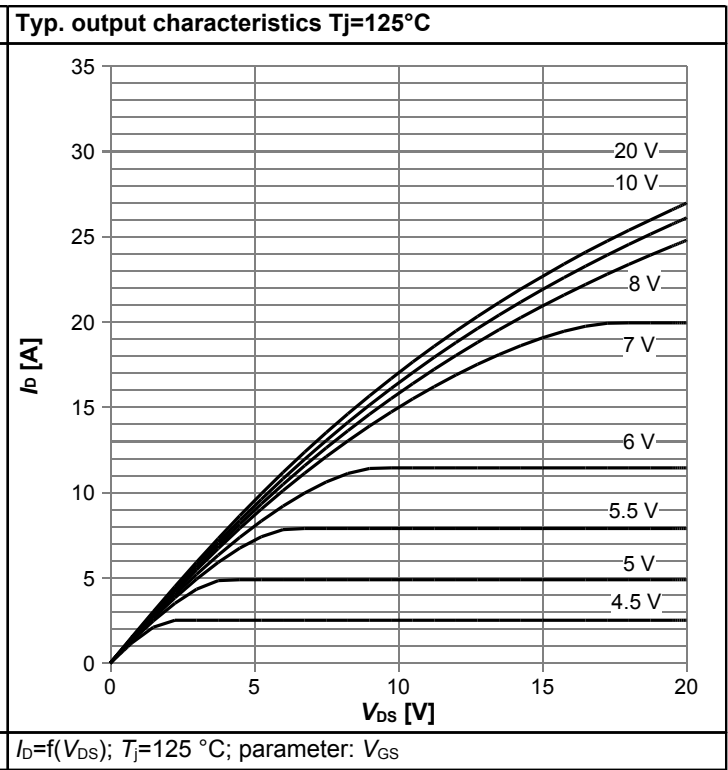
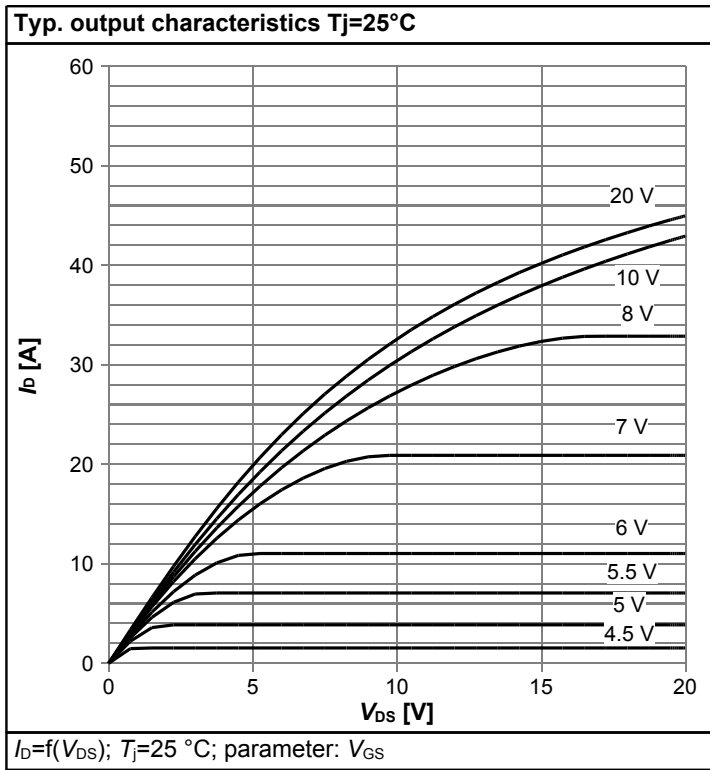
²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

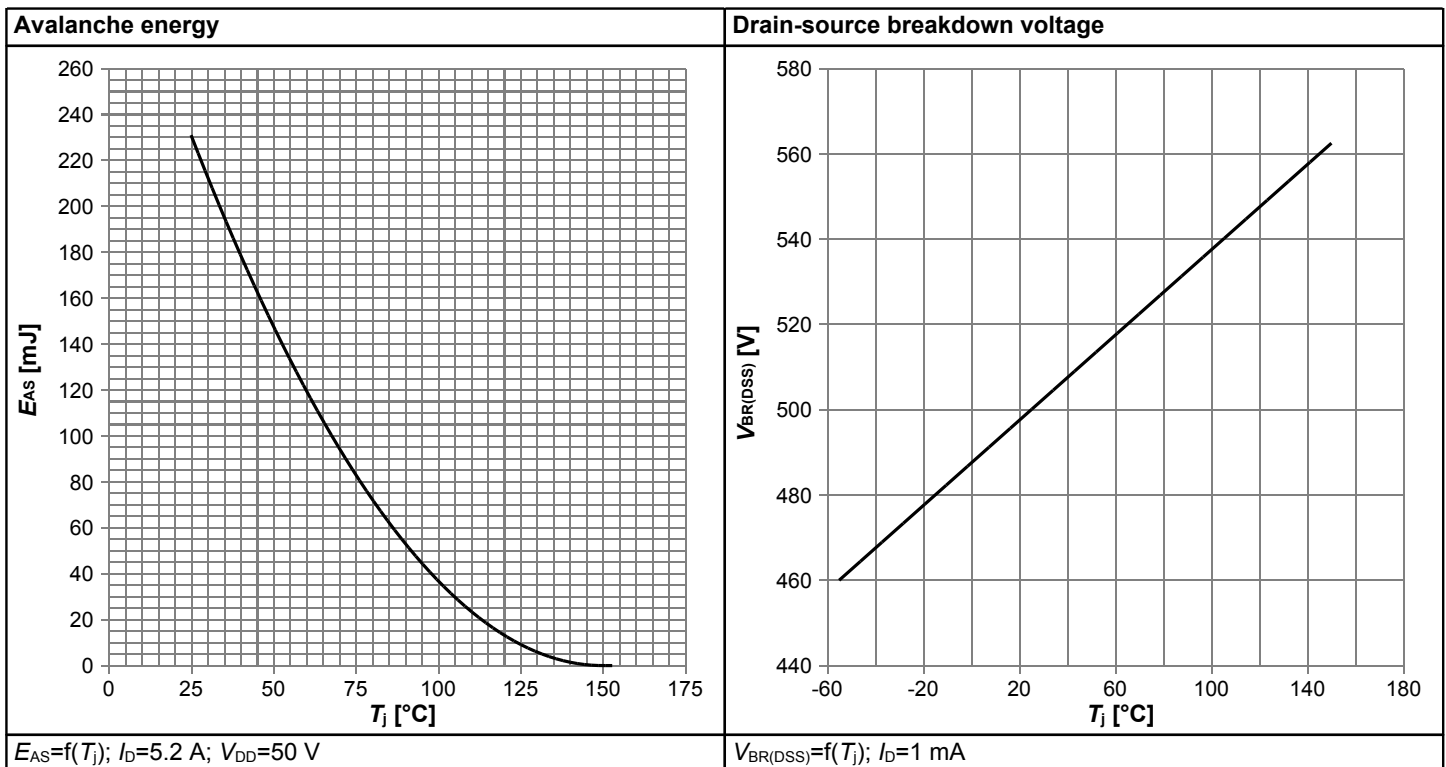
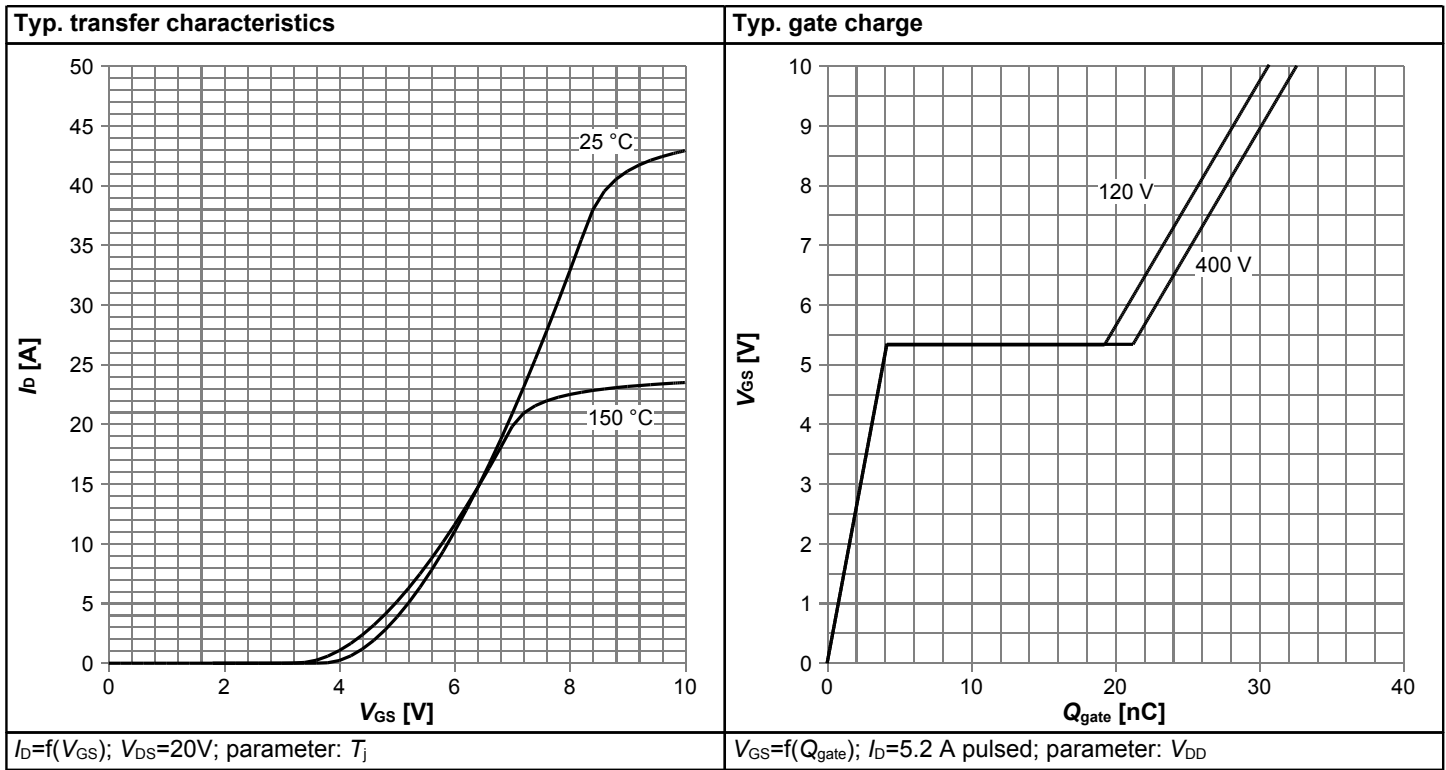
Table 7 Reverse diode characteristics

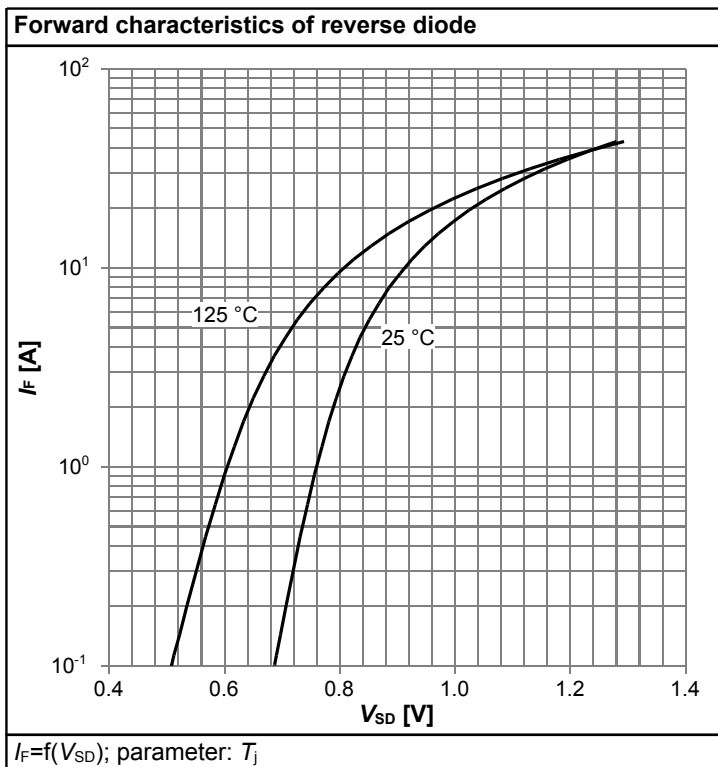
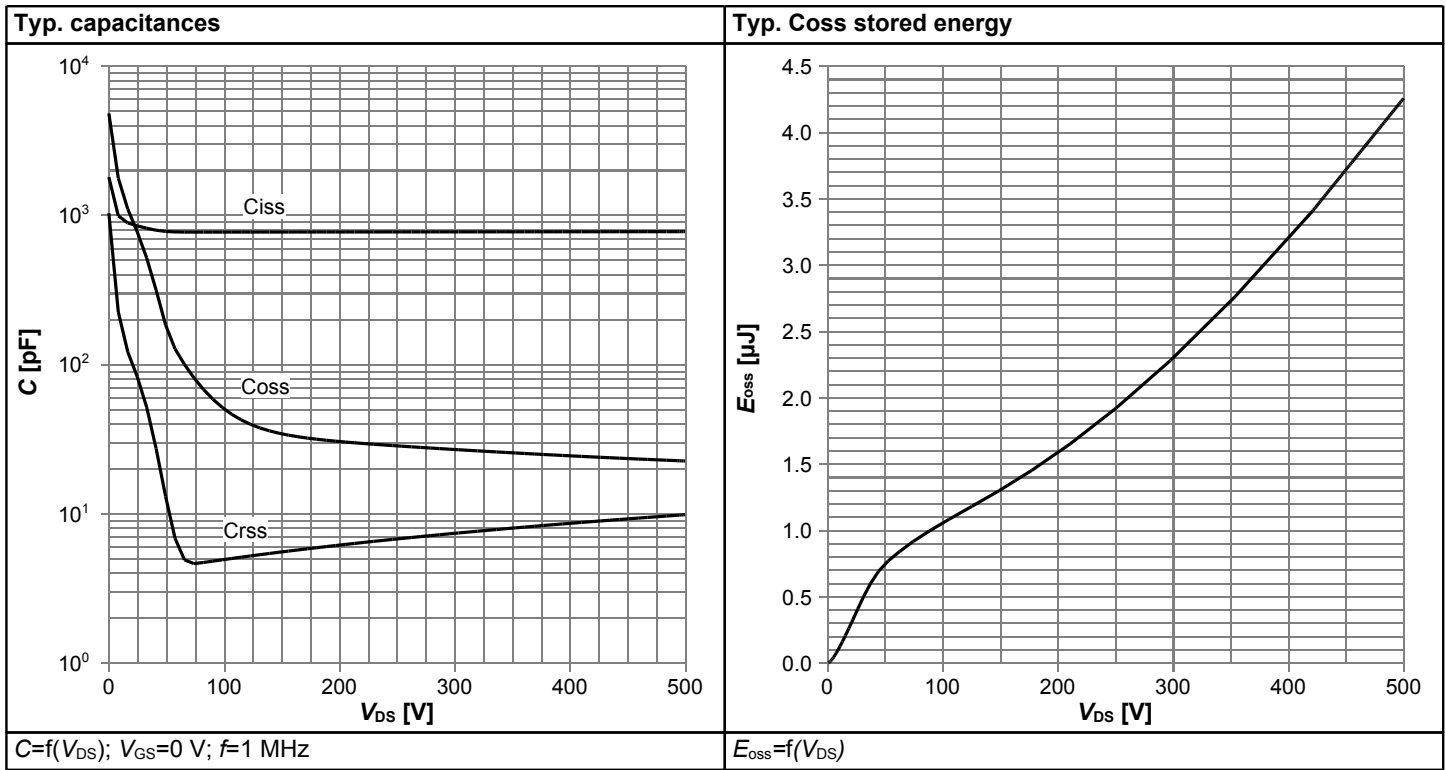
| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|-----------|--------|------|------|---------|--|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.85 | - | V | $V_{GS}=0V, I_F=5.2A, T_f=25^\circ C$ |
| Reverse recovery time | t_{rr} | - | 230 | - | ns | $V_R=400V, I_F=5.2A, di_F/dt=100A/\mu s$ |
| Reverse recovery charge | Q_{rr} | - | 2.2 | - | μC | $V_R=400V, I_F=5.2A, di_F/dt=100A/\mu s$ |
| Peak reverse recovery current | I_{rrm} | - | 17.5 | - | A | $V_R=400V, I_F=5.2A, di_F/dt=100A/\mu s$ |

5 Electrical characteristics diagrams









6 Test Circuits

Table 8 Diode characteristics

| Test circuit for diode characteristics | Diode recovery waveform |
|---|--|
| <p style="text-align: center;">$R_{g1} = R_{g2}$</p> | <p style="text-align: right;"> $t_{rr} = t_F + t_S$ $Q_{rr} = Q_F + Q_S$ </p> |

Table 9 Switching times

| Switching times test circuit for inductive load | Switching times waveform |
|---|--------------------------|
| | |

Table 10 Unclamped inductive load

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---------------------------------------|------------------------------|
| | |

7 Package Outlines

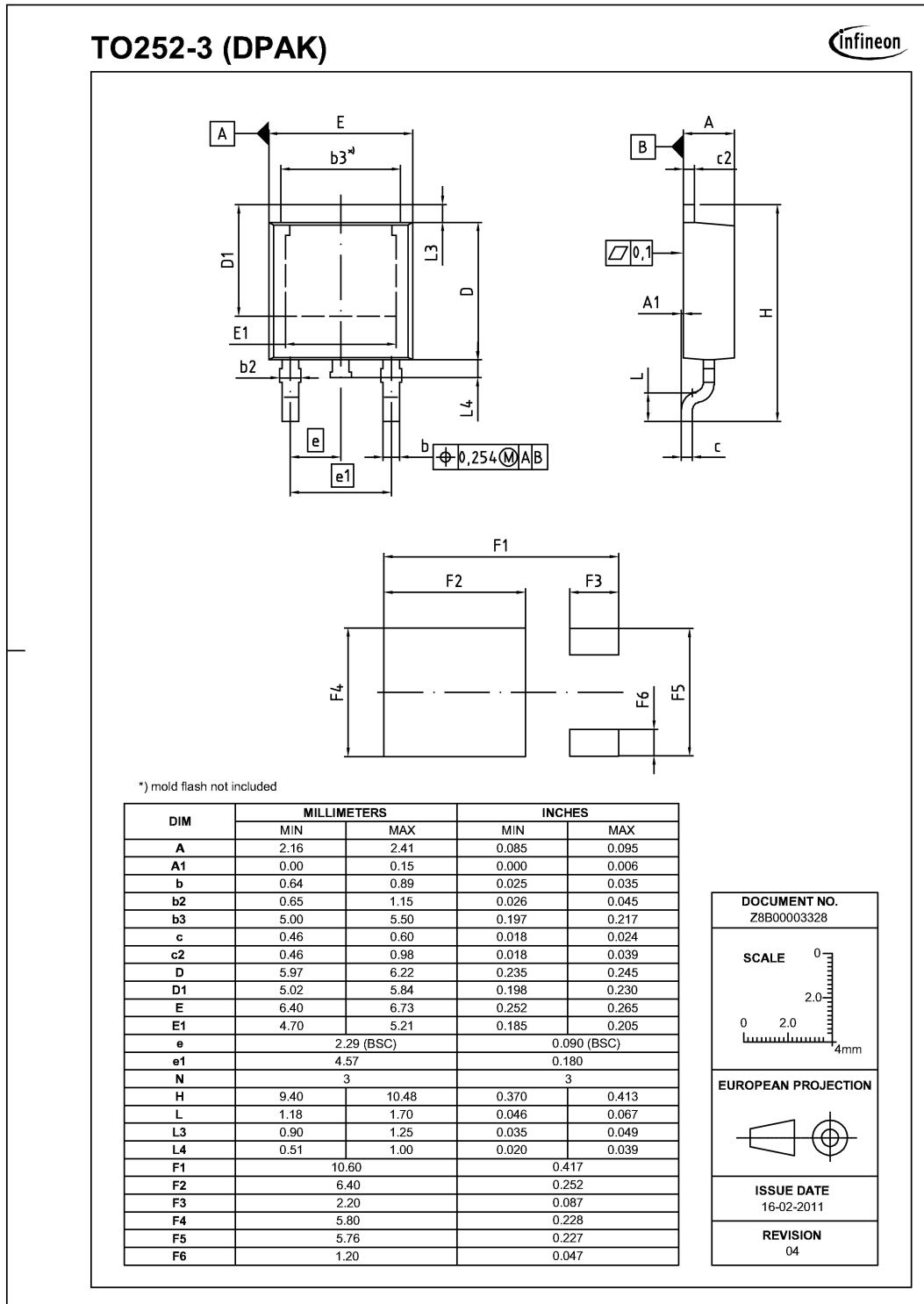


Figure 1 Outline PG-TO 252, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS Webpage: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPD50R280CE

Revision: 2013-07-15, Rev. 2.1

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2012-06-29 | Release of final version |
| 2.1 | 2013-07-15 | update to Halogen free mold compound |

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