Intel® Edison Breakout Board

Hardware Guide

September 2014

Revision 003

Document Number: 331190-003

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Contents

Figures

Tables

Revision History

Revision	Description	Date
ww32	Initial release.	August 4, 2014
ww34	Minor edits.	August 20, 2014
001	First public release.	September 9, 2014
002	Minor corrections.	September 15, 2014
003	Added handling information.	September 30, 2014

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1 Introduction

This document describes the Intel® Edison breakout board.

The Intel® Edison breakout board is designed to expose the native 1.8 V I/O of the Intel® Edison module. The board consists of power supply, battery recharger, USB OTG power switch, UART to USB bridge, USB OTG port, and I/O header.

1.1 References

Table 1 Product-specific documents

Reference	Name	Number/location
331188	Intel® Edison Board Support Package User Guide	
331189	Intel® Edison Module Hardware Guide	
331190	Intel® Edison Breakout Board Hardware Guide	(This document)
331191	Intel® Edison Kit for Arduino* Hardware Guide	
331192	Intel® Edison Native Application Guide	
331193	Intel® Edison Quick Start Guide	
[RN]	Intel® Edison Board Support Package Release Notes	
[GSG]	Intel® Edison Getting Started Guide	

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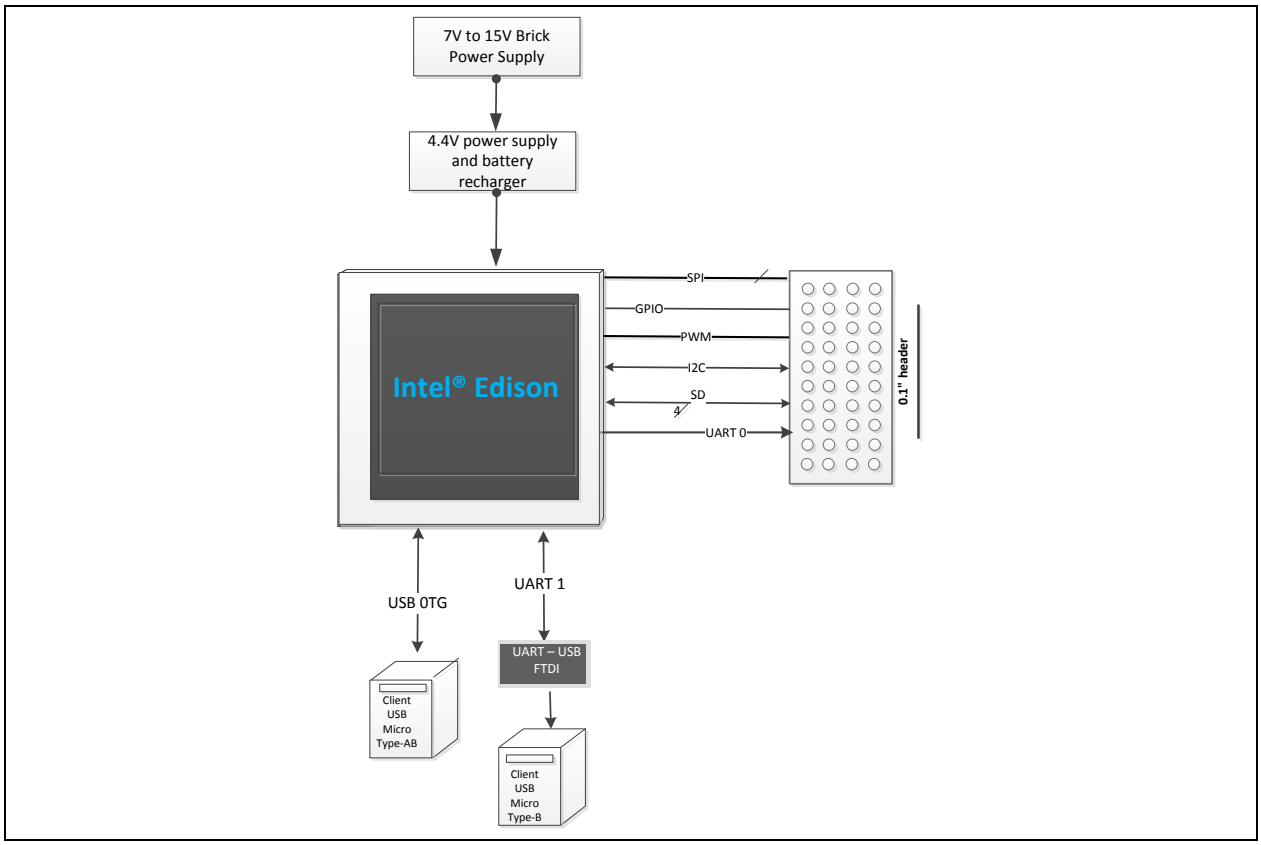
2 High-Level Functional Description

Figure 1 provides the block diagram for the Intel® Edison breakout board.

Figure 1 Intel® Edison breakout board block diagram



2.1 Intel® Edison breakout board expansion header

This section explains the expansion header.

When the pin mode is chosen as GPIO, it can be programmed as an output or input. When programmed as an input, a GPIO can serve as an interrupt or wake source. Inputs have programmable pullups or pulldowns. Pullup value can be 2, 20, or 50 kohm. I2C pins also have an additional 910 ohm value.

When in general purpose mode, input GPIO signals enter a glitch filter by default, before reaching the edge detection registers. To ensure that a pulse is detected by the edge detection register, the pulse should be five clock cycles long.

- 100 ns for a 50 MHz clock when SoC is in S0 state.
- 260 ns for 19.2 MHz clock when SoC is in S0i1 or S0i2 State.
- 155.5 µs for 32 kHz clock (RTC) when SoC is in S0i3 State.

Most GPIO capable pins are configured as GPIO inputs during the assertion of all resets and they remain inputs until configured otherwise.

As outputs, the GPIOs can be individually cleared or set. They can be pre-programmed to either state when entering standby. Output drive is ±3 mA.

Table 2 Intel® Edison breakout board expansion header signal list

Pin			Description
J17 - pin 1	GP182_PWM2		GPIO capable of PWM output.
J17 - pin 2	NC		No connect.
J17 - pin 3	NC		No connect.
J17 - pin 4	VIN		7 to 15 V.
J17 - pin 5	GP135	UART2_TX	GPIO, UART2 transmit output.
J17 - pin 6	RCVR_MODE		Firmware recovery mode.
J17 - pin 7	GP27	I2C6_SCL	GPIO,IC26 SCL output open collector.
J17 - pin 8	GP20	I2C1_SDA	GPIO, I2C1 data open collector.
J17 - pin 9	GP28	I2C6_SDA	GPIO, I2C6 data open collector.
J17 - pin 10	GP111	SSP5_FS1	GPIO, SSP2 chip select 2 output.
J17 - pin 11	GP109	SSP5_CLK	GPIO, SSP5 clock output.
J17 - pin 12	GP115	SSP5_TXD	GPIO, SSP5 transmit data output.
J17 - pin 13	OSC_CLK_OUT_0		High speed clock output.
J17 - pin 14	GP128	UART1_CTS	GPIO, UART1 clear to send input.
J18 - pin 1	GP13_PWM1		GPIO capable of PWM output.
J18 - pin 2	GP165		GPIO
J18 - pin 3	GPI_PWRBTN_N		Power button input.
J18 - pin 4	MSIC_SLP_CLK2		32 kHz sleep clock.
J18 - pin 5	V_VBAT_BKUP		RTC backup battery input.
J18 - pin 6	GP19	I2C1_SCL	GPIO,IC21 SCL output open collector.
J18 - pin 7	GP12_PWM0		GPIO capable of PWM output.
J18 - pin 8	GP183_PWM3		GPIO capable of PWM output.
J18 - pin 9	NC		No connect.
J18 - pin 10	GP110	SSP5_FS0	GPIO, SSP1 chip select 2 output.
J18 - pin 11	GP114	SSP5_RX	GPIO, SSP5 receive data input.
J18 - pin 12	GP129	UART1_RTS	GPIO, UART1 ready to send output.
J18 - pin 13	GP130	UART1_RX	GPIO, UART1 receive data input.
J18 - pin 14	FW_RCVR		Firmware recovery, active high on boot.
J20 - pin 1	V_VSYS		System input power.
J20 - pin 2	V_V3P30		System 3.3 V output.
J20 - pin 3	GP134	UART2_RX	UART2 Rx (input).
J20 - pin 4	GP45	COMPASS_DRDY	GPIO, compass data ready input.
J20 - pin 5	GP47	ACCELEROMETER_INT_2	GPIO, accelerometer interrupt input 2.
J20 - pin 6	GP49	GYRO_INT	GPIO, gyro interrupt input.
J20 - pin 7	GP15		GPIO.

Pin			Description
J20 - pin 8	GP84	SD_CLK_FB	GPIO, SD clock feedback input.
J20 - pin 9	GP42	SSP2_RXD	GPIO, SSP2 Rx data input.
J20 - pin 10	GP41	SSP2_FS	GPIO, SSP2 frame sync output.
J20 - pin 11	GP78	SD_CLK	GPIO, SD clock output.
J20 - pin 12	GP79	SD_CMD	GPIO, SD command.
J20 - pin 13	GP80	SD_DAT0	GPIO, SD data 0.
J20 - pin 14	GP81	SD_DAT1	GP81 SD data 1.
J19 - pin 1	NC		No connect.
J19 - pin 2	V_V1P80		System 1.8 V I/O output power.
J19 - pin 3	GND		Ground.
J19 - pin 4	GP44	ALS_INT_N	GPIO, ALS interrupt input.
J19 - pin 5	GP46	ACCELEROMETER_INT_1	GPIO, accelerometer interrupt input.
J19 - pin 6	GP48	GYRO_DRDY	GPIO, gyro data ready input.
J19 - pin 7	RESET_OUT#		System reset out low.
J19 - pin 8	GP131	UART1_TX	GPIO, UART 1 Tx output.
J19 - pin 9	GP14	AUDIO_CODEC_INT	GPIO, audio codec interrupt input.
J19 - pin 10	GP40	SSP2_CLK	GPIO, SSP2 clock output.
J19 - pin 11	GP43	SSP2_TXD	GPIO, SSP2 transmit data output.
J19 - pin 12	GP77	SD_CDN	GPIO, SD card detect low input.
J19 - pin 13	GP82	SD_DAT2	GPIO, SD data 2
J19 - pin 14	GP83	SD_DAT3	GPIO, SD data 3

2.2 Intel® Edison breakout board expansion USB interface

The Edison module has a single USB 2.0 interface. This interface is the primary method for downloading code. Edison is design to support OTG, using the ID signal. J16 is a microAB USB .

2.3 Intel® Edison breakout board expansion power supply

Intel® Edison is a low-power device. In general, it does not draw more than 200 mA with 600 mA short duration spikes during Wi-Fi transmit. Therefore, an Intel® Edison device may run on USB power (when configured as a device), or an external power adapter from 7 to 15 V.

Power from the external power adapter goes to a DC-DC converter and down-converted to 5 V. The 5 V rail is diode ORed with the USB VBUS rail. This power goes to a battery recharger IC, which limits the output voltage to 4.4 V. This voltage is in the safe range for the Edison module VSYS. The VSYS power range is 3.15 to 4.5 V. This allows VSYS to run off a standard lithium-ion battery. The charger IC is configured to limit the input power to 1. The charger is programmed to charge at 190 mA. This charger is designed to charge standard lithium-ion batteries with 4.2 V maximum charging voltage. You are responsible for choosing a suitable battery and following all safety precautions, to prevent overcharging or charging when the battery temperature is too high.

The drawback to this design is that the linear supply power drop places a limit on the total power through the Intel® Edison board and the 3.3 and 1.8 V supplies. The power loss through the charger will be *(4.4 to 5 V) • current*. In this

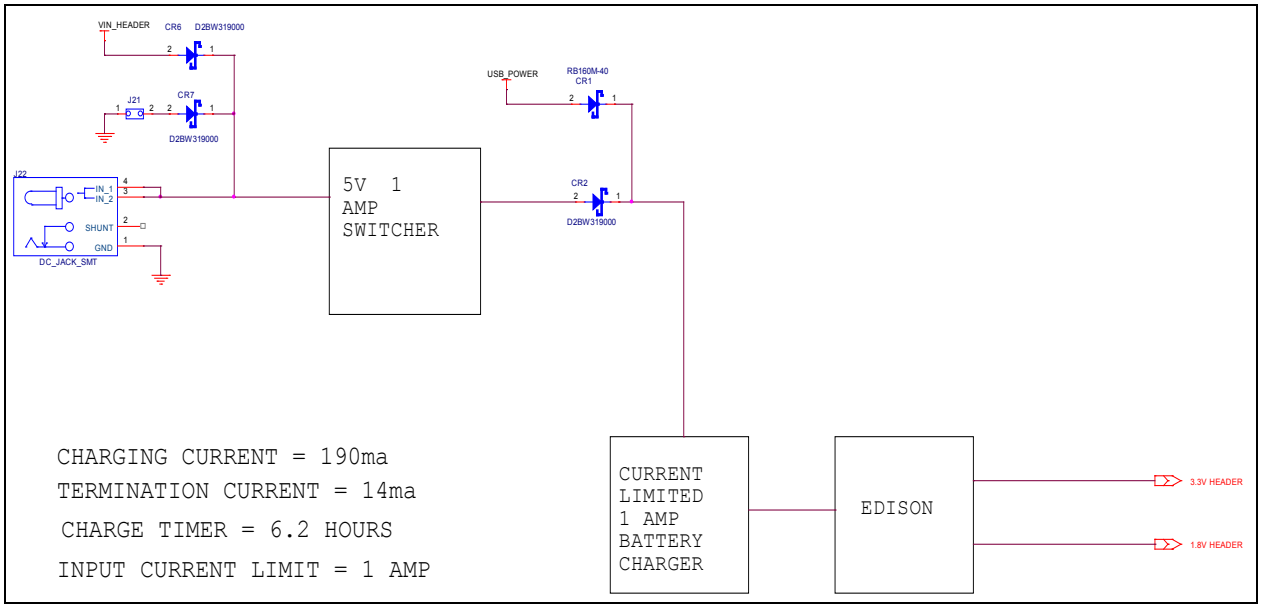
case, you should attempt to limit average current through the Intel® Edison board and its power rails to approximately 0.75 A.

The recharger IC on the Intel® Edison breakout board has input current limit and overtemperature shutdown. Assure the end design does not trip these protection mechanisms.

Some considerations of the power distribution in the Intel® Edison breakout board:

1. USB host mode always requires use of an external power adapter.
2. You are responsible for choosing a suitable battery and following all safety precautions, to prevent overcharging or charging when the battery temperature is too high. The battery should be at least 300 mAH capacity, due to the 100 mA charging current. Intel recommends battery packs with internal protection circuits.

Figure 2 Intel® Edison breakout board expansion board power distribution network



2.3.1 Boot voltage selection – DCIN signal

DCIN is a signal that indicates whether Edison is being powered from a battery or from an external power source. DCIN also sets the voltage level required on VSYS in order to boot. When DCIN is floating or tied to ground, the voltage on VSYS *must* rise from 2.5 to 3.5 V in 10 ms; otherwise the boot is aborted. When the boot is aborted, power must be cycled below 2.5 V. If DCIN is connected to VSYS, Edison will start to boot when VSYS is above 2.5 V for 100 ms.

Note: When DCIN is connected to VSYS, boot will occur whenever the voltage is above 2.8 V for 100 ms. The DCIN signal is attached to VSYS on the PCB.

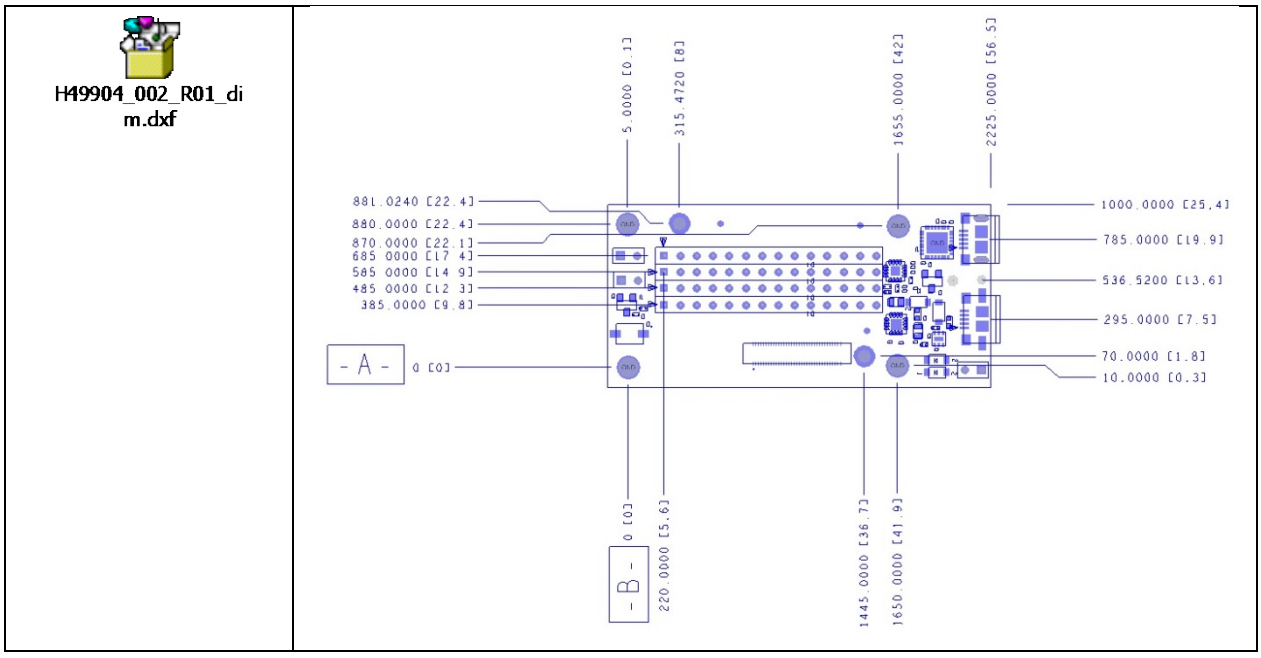
Note: The absolute minimum voltage to assure Wi-Fi and Bluetooth functionality is 3.15 V.

2.4 Intel® Edison breakout board expansion buttons

The Intel® Edison breakout board has the following buttons:

- **Power button.** SW1UI2 is the Intel® Edison power button. This button is configured by software. In general, pressing and holding this button down will cause the Intel® Edison module to power down. (It will leave the I/O configuration in the port expanders in its current state). Pressing this button momentarily when Edison is powered down (power still applied) will cause Intel® Edison module to reboot. If Edison is running, then a momentary press will cause Edison to go into low power sleep mode. Pressing the button momentarily when Edison is asleep, will bring Edison into full power mode.

Figure 3 Button schematic



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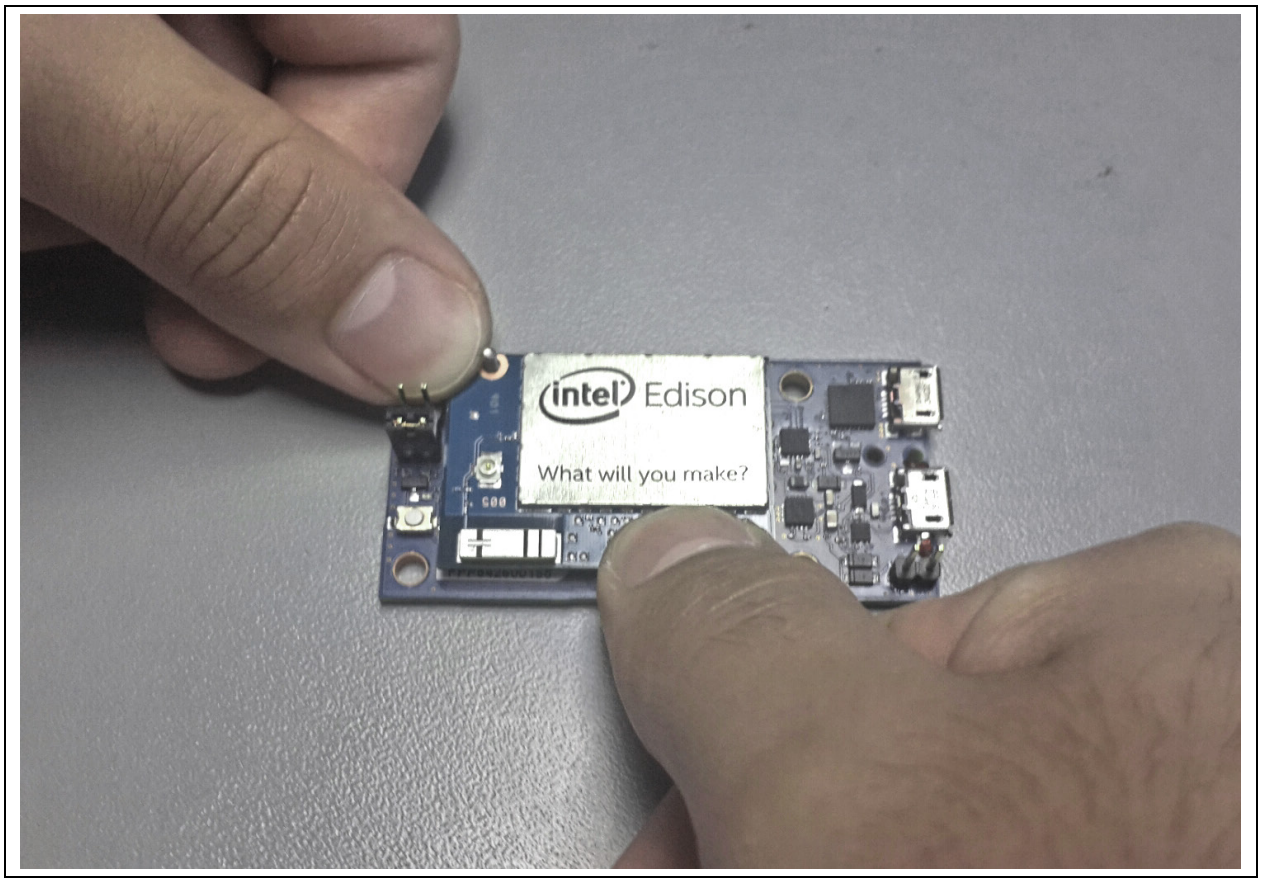
3 Handling

When attaching an Intel® Edison module to breakout board, handle the Intel® Edison module by the PCB edges. Avoid holding or exerting pressure to the shields. To mate the Intel® Edison board to the breakout board, apply pressure directly above the connector and to the left corner.

Figure 4 Inserting an Intel® Edison module to the breakout board



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4 Debug UART Errata

The Intel® Edison board has a known error on all UARTs. When Edison goes into low power sleep, the UART internal FIFO and interface is powered down. Therefore, a two-wire UART (Rx/Tx) will lose the first received character whenever Edison is in sleep mode. In order to avoid this condition, when sleep mode is enabled, a four-wire UART (Rx, Tx, CTS, and RTS) is required.

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