

- 6 A output current
- 12 V input voltage
- Wide-output voltage adjust
 - 1.2 Vdc to 5.5 Vdc for suffix 'W' and 0.8 Vdc to 1.8 Vdc for suffix 'L'
- Auto-track™ sequencing*
- Pre-bias start-up
- Efficiencies up to 93%
- Output ON/OFF inhibit
- Output voltage sense
- Point-of-Load-Alliance (POLA) compatible
- Available RoHS compliant



The PTH12050 is a next generation series of non-isolated dc-dc converters offering some of the most advanced POL features available in the industry. The primary new feature provides for sequencing between multiple modules, a function, which is becoming a necessity for powering advanced silicon including DSP's, FPGA's and ASIC's requiring controlled power-up and power-down. Other industry leading features include efficiencies up to 93%. The PTH12050 has an input voltage of 10.8 Vdc to 13.2 Vdc and offers a wide output voltage range adjustable with external trim resistor, allowing for maximum design flexibility and a pathway for future upgrades.



2 YEAR WARRANTY

All specifications are typical at nominal input, full load at 25 °C unless otherwise stated
C_{in} = 100 µF, C_{out} = 0 µF

SPECIFICATIONS

OUTPUT SPECIFICATIONS

Voltage adjustability (See Note 4)	Suffix 'W' Suffix 'L'	1.2-5.5 Vdc 0.8-1.8 Vdc
Setpoint accuracy		±2.0% V _o
Line regulation		±5 mV typ.
Load regulation		±5 mV typ.
Total regulation		±3.0% V _o
Minimum load		0 A
Ripple and noise 20 MHz bandwidth	Suffix 'W' Suffix 'L'	V _o ≤ 2.5 V 25 mV pk-pk V _o > 2.5 V 1% V _o V _o ≤ 1.0 V 20 mV pk-pk V _o > 1.0 V 30 mV pk-pk
Temperature co-efficient	-40 °C to +85 °C	±0.5% V _o
Transient response (See Note 5)		70 µs recovery time Overshoot/undershoot 100 mV
Margin adjustment		±5.0% V _o

INPUT SPECIFICATIONS

Input voltage range	(See Note 3)	10.8-13.2 Vdc
Input current	No load	10 mA typ.
Remote ON/OFF	(See Note 1)	Positive logic
Start-up time		1 V/ms
Undervoltage lockout		8.8-0.4 V typ.
Track input voltage	Pin 8 (See Note 6)	±0.3 V _{in}

EMC CHARACTERISTICS

Electrostatic discharge	EN61000-4-2, IEC801-2
Conducted immunity	EN61000-4-6
Radiated immunity	EN61000-4-3

GENERAL SPECIFICATIONS

Efficiency	See Tables on Page 2	
Insulation voltage	Non-isolated	
Switching frequency Over V _{in} and I _o ranges	Suffix 'W' Suffix 'L'	320 kHz typ. 250 kHz typ.
Approvals and standards	EN60950 UL/cUL60950	
Material flammability	UL94V-0	
Dimensions	(L x W x H)	22.10 x 12.57 x 8.50 mm 0.870 x 0.495 x 0.335 in
Weight	2.9 g (0.10 oz)	
MTBF	Telcordia SR-332	7,092,000 hours

ENVIRONMENTAL SPECIFICATIONS

Thermal performance (See Note 2)	Operating ambient, temperature Non-operating	-40 °C to +85 °C -40 °C to +125 °C
MSL ('Z' suffix only)	JEDEC J-STD-020C	Level 3

PROTECTION

Short-circuit	Auto reset	14 A typ.
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International Safety Standard Approvals



UL/cUL CAN/CSA-C22.2 No. 60950-1-03/UL 60950-1,
File No. E174104

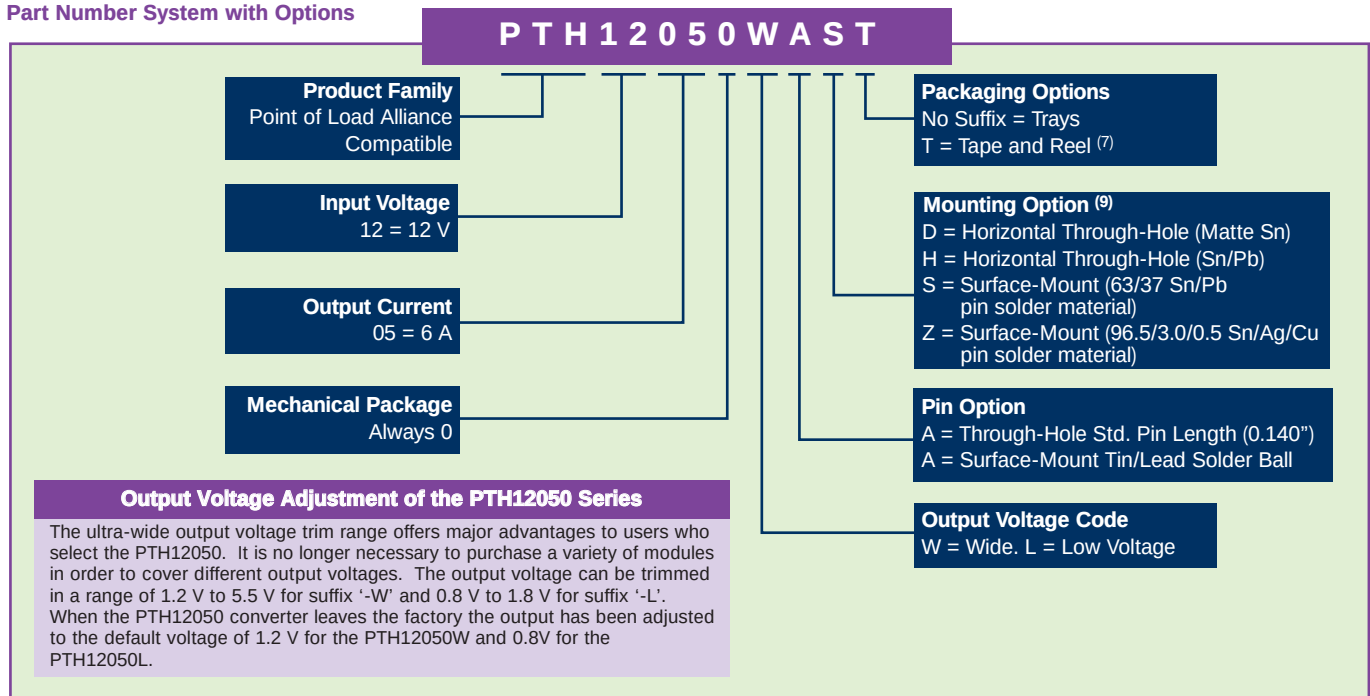


TÜV Product Service (EN60950) Certificate No. B 04 06 38572 044
CB Report and Certificate to IEC60950, Certificate No.
US/8292/UL

*Auto-track™ is a trade mark of Texas Instruments

OUTPUT POWER (MAX.)	INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT (MIN.)	OUTPUT CURRENT (MAX.)	EFFICIENCY (MAX.)	REGULATION		MODEL NUMBER ^(9,10)
						LINE	LOAD	
33 W	10.8-13.2 Vdc	0.8-1.8 Vdc	0 A	6 A	88%	±5 mV	±5 mV	PTH12050L
33 W	10.8-13.2 Vdc	1.2-5.5 Vdc	0 A	6 A	93%	±5 mV	±5 mV	PTH12050W

Part Number System with Options



Notes

- Remote ON/OFF. Positive Logic
ON: Pin 3 open; or $V > V_{in} - 0.5 V$
OFF: Pin 3 GND; or $V < 0.8 V$ (min - 0.2 V).
- See Figure 1 for safe operating curve.
- A 100 μF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimum of 750 mA rms of ripple current. C2 = 10 μF ceramic capacitor, required for output voltages of 3.3 V and higher.
- An external output capacitor is not required for basic operation. Adding 100 μF of distributed capacitance at the load will improve the transient response.
- 1 A/ μs load step, 50 to 100% I_{omax} , $C_{out} = 100 \mu F$.
If utilized V_{out} will track applied voltage by $\pm 0.3 V$ (up to V_o set point).
- Tape and reel packaging only available on the surface-mount versions.
- The pk-pk output ripple voltage is measured with an external 10 μF ceramic capacitor. See Figure 3 Standard application schematic.
- To order Pb-free (RoHS compatible) surface-mount parts replace the mounting option 'S' with 'Z', e.g. PTH12050WAZ. To order Pb-free (RoHS compatible) through-hole parts replace the mounting option 'H' with 'D', e.g. PTH12050WAD.
- NOTICE: Some models do not support all options. Please contact your local Artesyn representative or use the on-line model number search tool at <http://www.artesyn.com/powergroup/products.htm> to find a suitable alternative.

EFFICIENCY TABLE - PTH12050W ($I_o = 5 A$)

OUTPUT VOLTAGE	EFFICIENCY
$V_o = 5.0 V$	93%
$V_o = 3.3 V$	91%
$V_o = 2.5 V$	89%
$V_o = 2.0 V$	88%
$V_o = 1.8 V$	87%
$V_o = 1.5 V$	86%
$V_o = 1.2 V$	84%

EFFICIENCY TABLE - PTH12050L ($I_o = 5 A$)

OUTPUT VOLTAGE	EFFICIENCY
$V_o = 1.8 V$	88%
$V_o = 1.5 V$	87%
$V_o = 1.2 V$	85%
$V_o = 1.0 V$	83%
$V_o = 0.8 V$	81%

PTH12050W Characteristic Data

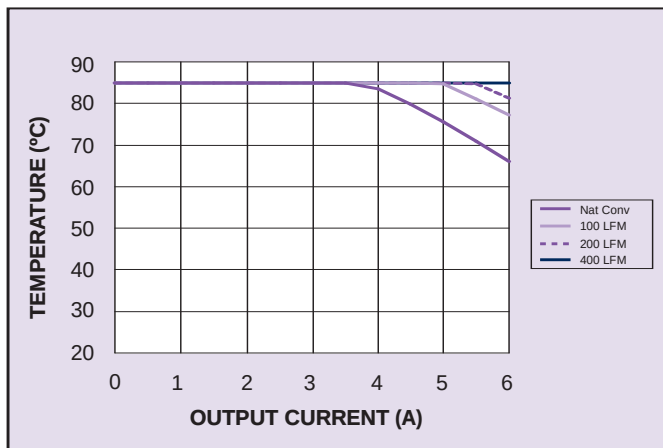


Figure 1 - Safe Operating Area for PTH12050W
Vin = 12 V, Output Voltage = 3.3 V (See Note A)

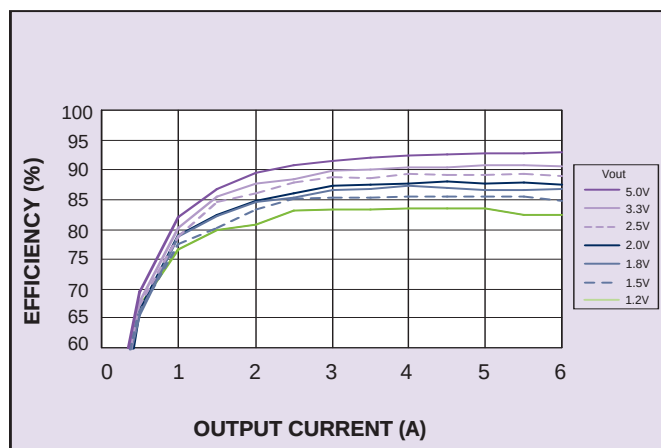


Figure 2 - Efficiency vs Load Current for PTH12050W
Vin = 12 V (See Note B)

PTH12050L Characteristic Data

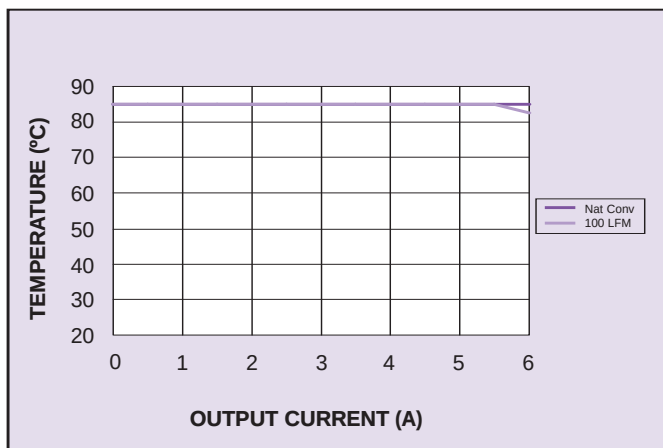


Figure 3 - Safe Operating Area for PTH12050L
Vin = 12 V, Output Voltage ≤ 1.8 V (See Note A)

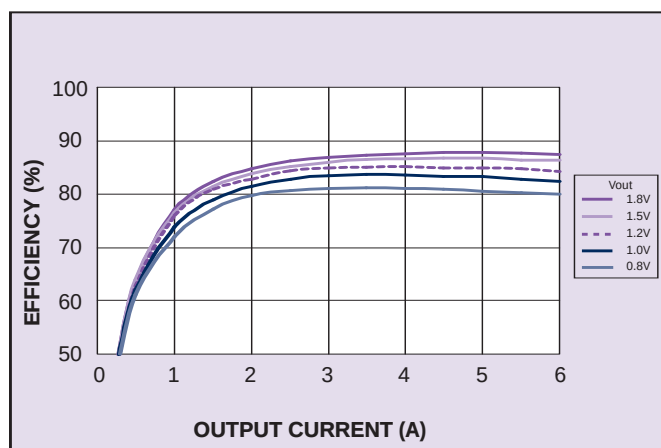


Figure 4 - Efficiency vs Load Current for PTH12050L
Vin = 12 V (See Note B)

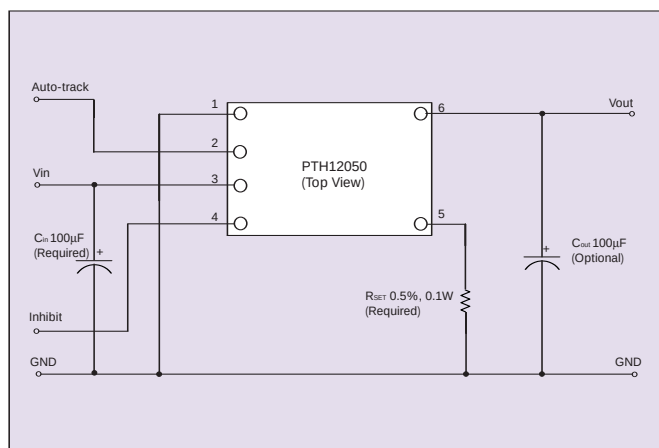


Figure 5 - Standard Application - All Models

Notes

- A SOA curves represent the conditions at which internal components are within the Artesyn derating guidelines.
- B Characteristic data has been developed from actual products tested at 25 °C. This data is considered typical data for the converter.

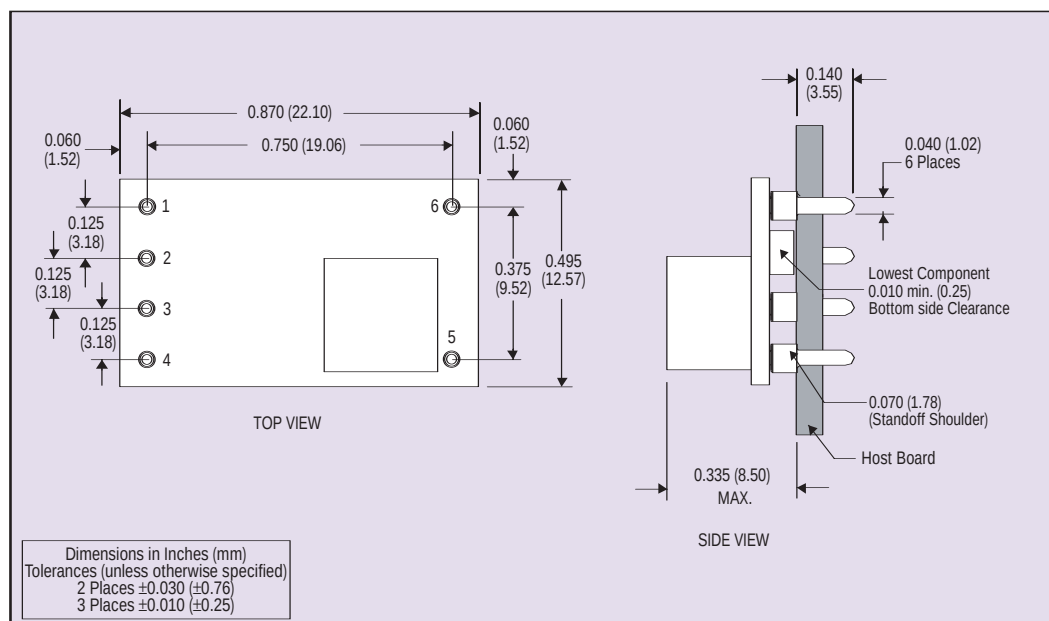


Figure 6 - Plated Through-Hole Mechanical Drawing

PIN CONNECTIONS	
PIN NO.	FUNCTION
1	Ground
2	Track
3	Vin
4	Inhibit*
5	Vo adjust
6	Vout

*Denotes negative logic:
Open = Normal operation
Ground = Function active

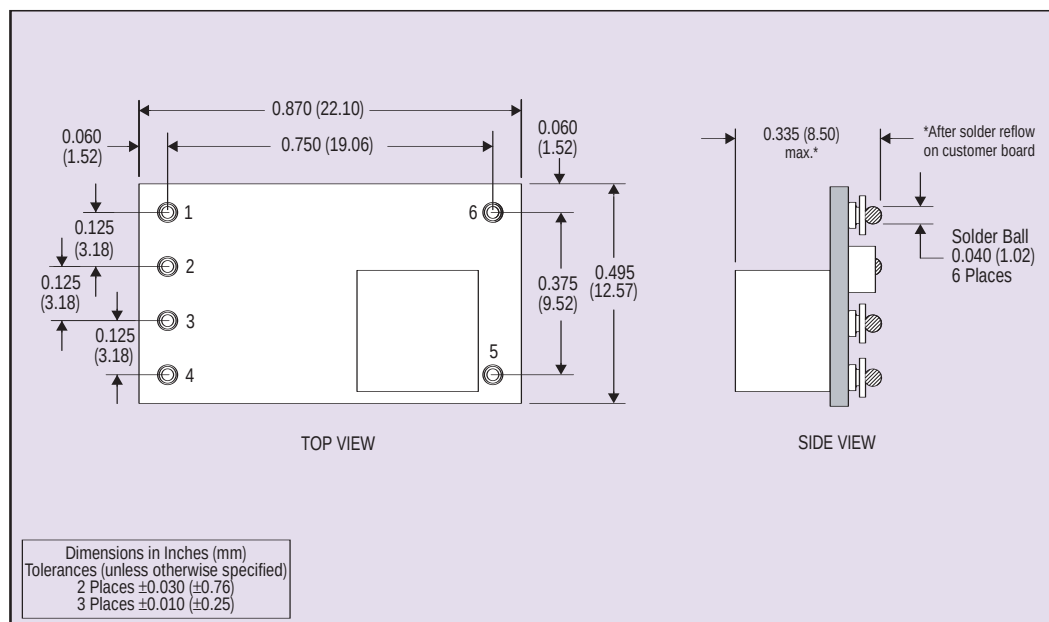


Figure 7 - Surface-Mount Mechanical Drawing