

### FEATURES

Complete Dual 12-Bit DAC  
No External Components  
+5 V Single-Supply Operation  $\pm 10\%$   
4.095 V Full Scale (1 mV/LSB)  
Buffered Voltage Outputs  
Low Power: 5 mW/DAC  
Space Saving 1.5 mm Height SO-14 Package

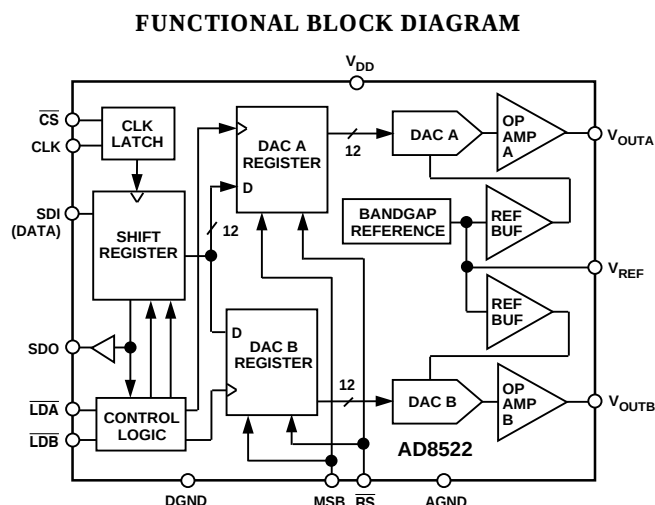
### APPLICATIONS

Digitally Controlled Calibration  
Servo Controls  
Process Control Equipment  
Computer Peripherals  
Portable Instrumentation  
Cellular Base Stations Voltage Adjustment

### GENERAL DESCRIPTION

The AD8522 is a complete dual 12-bit, single-supply, voltage output DAC in a 14-pin DIP, or SO-14 surface mount package. Fabricated in a CBCMOS process, features include a serial digital interface, onboard reference, and buffered voltage output. Ideal for +5 V-only systems, this monolithic device offers low cost and ease of use, and requires no external components to realize the full performance of the device.

The serial digital interface allows interfacing directly to numerous microcontroller ports, with a simple high speed, three-wire data, clock, and load strobe format. The 16-bit serial word contains the 12-bit data word and DAC select address, which is decoded internally or can be decoded externally using  $\overline{LDA}$ ,  $\overline{LDB}$



inputs. A serial data output allows the user to easily daisy-chain multiple devices in conjunction with a chip select input. A reset  $\overline{RS}$  input sets the outputs to zero scale or midscale, as determined by the input MSB.

The output 4.095 V full scale is laser trimmed to maintain accuracy over the operating temperature range of the device, and gives the user an easy-to-use one-millivolt-per-bit resolution. A 2.5 V reference output is also available externally for other data acquisition circuitry, and for ratiometric applications. The output buffers are capable of driving  $\pm 5$  mA.

The AD8522 is available in the 14-pin plastic DIP and low profile 1.5 mm SOIC-14 packages.

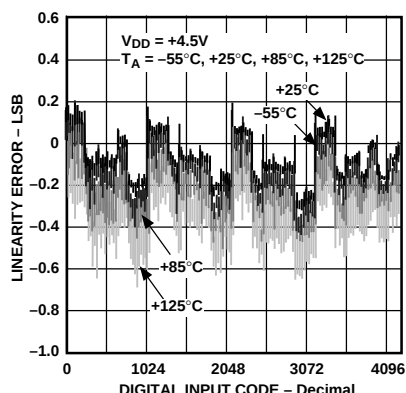
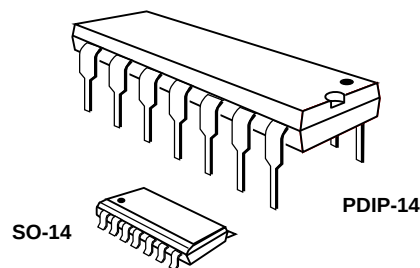


Figure 1. Linearity Error vs. Digital Code & Temperature

### PACKAGE TYPES AVAILABLE



### REV. A

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# AD8522—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_{DD} = +5.0\text{ V} \pm 10\%$ , $R_L = \text{No Load}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , both DACs tested, unless otherwise noted)

| Parameter                                   | Symbol                | Condition                                                                                                    | Min   | Typ       | Max     | Units         |
|---------------------------------------------|-----------------------|--------------------------------------------------------------------------------------------------------------|-------|-----------|---------|---------------|
| <b>STATIC PERFORMANCE</b>                   |                       |                                                                                                              |       |           |         |               |
| Resolution <sup>1</sup>                     | N                     |                                                                                                              | 12    |           |         | Bits          |
| Relative Accuracy                           | INL                   |                                                                                                              | -1.5  | $\pm 0.5$ | +1.5    | LSB           |
| Differential Nonlinearity                   | DNL                   | Monotonic                                                                                                    | -1    | $\pm 0.5$ | +1      | LSB           |
| Zero-Scale Error                            | $V_{ZSE}$             | Data = 000 <sub>H</sub>                                                                                      |       | +0.5      | +3      | mV            |
| Full-Scale Voltage <sup>2</sup>             | $V_{FS}$              | Data = FFF <sub>H</sub>                                                                                      | 4.079 | 4.095     | 4.111   | Volts         |
| Full-Scale Tempco <sup>2, 3</sup>           | $TCV_{FS}$            |                                                                                                              |       | $\pm 15$  |         | ppm/°C        |
| <b>MATCHING PERFORMANCE</b>                 |                       |                                                                                                              |       |           |         |               |
| Linearity Matching Error                    | $\Delta V_{FS}A/B$    |                                                                                                              |       | $\pm 1$   |         | LSB           |
| <b>ANALOG OUTPUT</b>                        |                       |                                                                                                              |       |           |         |               |
| Output Current                              | $I_{OUT}$             | Data = 800 <sub>H</sub> , $\Delta V_{OUT} \leq 3\text{ LSB}$                                                 |       |           | $\pm 5$ | mA            |
| Load Regulation at Half-Scale               | $LD_{REG}$            | $R_L = 402\ \Omega$ to $\infty$ , Data = 800 <sub>H</sub>                                                    |       | 1         | 3       | LSB           |
| Capacitive Load <sup>3</sup>                | $C_L$                 | No Oscillation                                                                                               |       | 500       |         | pF            |
| <b>REFERENCE OUTPUT</b>                     |                       |                                                                                                              |       |           |         |               |
| Output Voltage                              | $V_{REF}$             |                                                                                                              | 2.484 | 2.500     | 2.516   | V             |
| Output Source Current <sup>4</sup>          | $I_{REF}$             | $\Delta V_{REF} < 18\text{ mV}$                                                                              |       |           | 5       | mA            |
| Line Rejection                              | $LN_{REJ}$            |                                                                                                              |       | 0.025     | 0.08    | %/V           |
| Load Regulation                             | $LD_{REG}$            | $I_{REF} = 0\text{ to }5\text{ mA}$ , Data = 800 <sub>H</sub>                                                |       | 0.025     | 0.1     | %/mA          |
| <b>LOGIC INPUTS &amp; OUTPUTS</b>           |                       |                                                                                                              |       |           |         |               |
| Logic Input Low Voltage                     | $V_{IL}$              |                                                                                                              |       |           | 0.8     | V             |
| Logic Input High Voltage                    | $V_{IH}$              |                                                                                                              | 2.4   |           |         | V             |
| Input Leakage Current                       | $I_{IL}$              |                                                                                                              |       |           | 10      | $\mu\text{A}$ |
| Input Capacitance <sup>3</sup>              | $C_{IL}$              |                                                                                                              |       |           | 10      | pF            |
| Logic Output Voltage Low                    | $V_{OL}$              | $I_{OL} = 1.6\text{ mA}$                                                                                     |       |           | 0.4     | V             |
| Logic Output Voltage High                   | $V_{OH}$              | $I_{OH} = 400\ \mu\text{A}$                                                                                  | 3.5   |           |         | V             |
| <b>TIMING SPECIFICATIONS<sup>3, 5</sup></b> |                       |                                                                                                              |       |           |         |               |
| Clock Width High                            | $t_{CH}$              |                                                                                                              | 35    |           |         | ns            |
| Clock Width Low                             | $t_{CL}$              |                                                                                                              | 35    |           |         | ns            |
| Load Pulse Width                            | $t_{LDW}$             |                                                                                                              | 25    |           |         | ns            |
| Data Setup                                  | $t_{DS}$              |                                                                                                              | 10    |           |         | ns            |
| Data Hold                                   | $t_{DH}$              |                                                                                                              | 20    |           |         | ns            |
| Clear Pulse Width                           | $t_{CLR\overline{W}}$ |                                                                                                              | 20    |           |         | ns            |
| Load Setup                                  | $t_{LD1}$             |                                                                                                              | 10    |           |         | ns            |
| Load Hold                                   | $t_{LD2}$             |                                                                                                              | 10    |           |         | ns            |
| Select                                      | $t_{CSS}$             |                                                                                                              | 30    |           |         | ns            |
| Deselect                                    | $t_{CSH}$             |                                                                                                              | 30    |           |         | ns            |
| Clock to SDO Propagation Delay              | $t_{PD}$              |                                                                                                              | 20    | 45        | 80      | ns            |
| <b>AC CHARACTERISTICS<sup>3, 5</sup></b>    |                       |                                                                                                              |       |           |         |               |
| Voltage Output Settling Time <sup>6</sup>   | $t_S$                 | To $\pm 1\text{ LSB}$ of Final Value                                                                         |       | 16        |         | $\mu\text{s}$ |
| Crosstalk                                   | $C_T$                 | Signal Measured at $\overline{\text{DAC Output}}$ ,<br>While Changing Opposite $\overline{\text{LDA/B}}$     |       | 38        |         | dB            |
| DAC Glitch                                  | Q                     | Half-Scale Transition                                                                                        |       | 13        |         | nV s          |
| Digital Feedthrough                         | $D_{FT}$              | Signal Measured at $\overline{\text{DAC Output}}$ ,<br>While Changing Data Without $\overline{\text{LDA/B}}$ |       | 2         |         | nV s          |
| <b>SUPPLY CHARACTERISTICS</b>               |                       |                                                                                                              |       |           |         |               |
| Positive Supply Current                     | $I_{DD}$              | $V_{DD} = 5.5\text{ V}$ , $V_{IH} = 2.4\text{ V}$ or $V_{IL} = 0.8\text{ V}$                                 |       | 3         | 5       | mA            |
|                                             |                       | $V_{DD} = 5\text{ V}$ , $V_{IL} = 0\text{ V}$                                                                |       | 1         | 2       | mA            |
| Power Dissipation <sup>7</sup>              | $P_{DISS}$            | $V_{DD} = 5\text{ V}$ , $V_{IH} = 2.4\text{ V}$ or $V_{IL} = 0.8\text{ V}$                                   |       | 15        | 25      | mW            |
|                                             |                       | $V_{DD} = 5\text{ V}$ , $V_{IL} = 0\text{ V}$                                                                |       | 5         | 10      | mW            |
| Power Supply Sensitivity                    | PSS                   | $\Delta V_{DD} = \pm 5\%$                                                                                    |       | 0.002     | 0.004   | %/%           |

### NOTES

<sup>1</sup>1 LSB = 1 mV for 0 V to +4.095 V output range.

<sup>2</sup>Includes internal voltage reference error.

<sup>3</sup>These parameters are guaranteed by design and not subject to production testing.

<sup>4</sup>Very little sink current is available at the  $V_{REF}$  pin. Use external buffer if setting up a virtual ground.

<sup>5</sup>All input control signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

<sup>6</sup>The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

<sup>7</sup>Power Dissipation is calculated  $I_{DD} \times 5\text{ V}$ .

Specifications subject to change without notice.

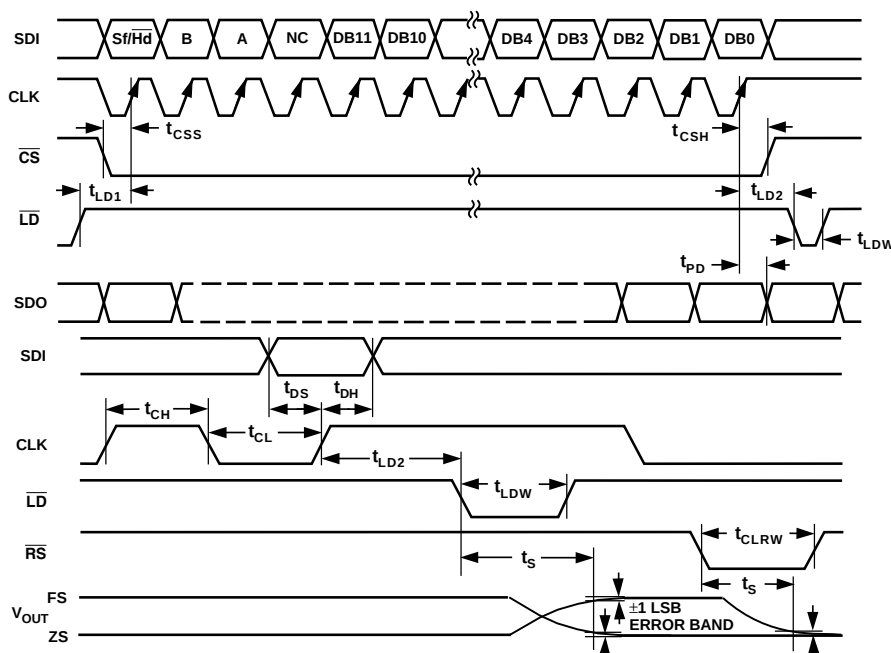


Figure 2. Timing Diagram

## SERIAL INPUT REGISTER DATA FORMAT

| Last |     |     |     |     |     |     |     |     |     |      |      |     |     | First |       |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|-----|-----|-------|-------|
| D0   | D1  | D2  | D3  | D4  | D5  | D6  | D7  | D8  | D9  | D10  | D11  | D12 | D13 | D14   | D15   |
| DB0  | DB1 | DB2 | DB3 | DB4 | DB5 | DB6 | DB7 | DB8 | DB9 | DB10 | DB11 | NC  | A   | B     | Sf/Hd |

Table I. Truth Table

| Data Word             |   |   | Ext Pins |     | DAC Register                                          |
|-----------------------|---|---|----------|-----|-------------------------------------------------------|
| Sf/Hd                 | B | A | LDA      | LDB |                                                       |
| Hardware Load:        |   |   |          |     |                                                       |
| L                     | X | X | ↓        | ↓   | Loads DACA + DACB with Data from SR                   |
| L                     | X | X | ↓        | H   | Loads DACA with Data from SR                          |
| L                     | X | X | H        | ↓   | Loads DACB with Data from SR                          |
| L                     | X | X | H        | H   | No Load                                               |
| Software Decode Load: |   |   |          |     |                                                       |
| H                     | L | L | X        | X   | No Load                                               |
| H                     | H | L | ↓        | ↓   | Loads DACB with Data from SR, See Note 1 Below        |
| H                     | H | L | H        | H   | No Load                                               |
| H                     | L | H | ↓        | ↓   | Loads DACA with Data from SR, See Note 1 Below        |
| H                     | L | H | H        | H   | No Load                                               |
| H                     | H | H | ↓        | ↓   | Loads DACA + DACB with Data from SR, See 1 Note Below |
| H                     | H | H | H        | H   | No Load                                               |

## NOTES

<sup>1</sup>In software mode  $\overline{LDA}$  and  $\overline{LDB}$  perform the same function. They can be tied together or the unused pin should be tied high.

<sup>2</sup>External Pins  $\overline{LDA}$  and  $\overline{LDB}$  should always be high when shifting Data into the shift register.

<sup>3</sup>↓ symbol denotes negative transition.

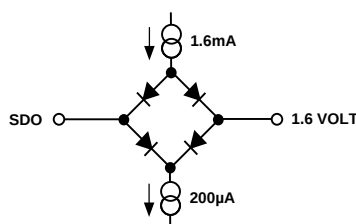


Figure 3. AC Timing SDO Pin Load Circuit

## PIN DESCRIPTION

| Pin                | Function                                                                                                                                                                                                                                                                                   |
|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDI                | Serial Data Input, input data loads directly into the shift register.                                                                                                                                                                                                                      |
| CLK                | Clock input, positive edge clocks data into shift register.                                                                                                                                                                                                                                |
| $\overline{CS}$    | Chip Select, active low input. Prevents shift register loading when high. Does not affect $\overline{LDA}$ and $\overline{LDB}$ operation.                                                                                                                                                 |
| $\overline{LDA/B}$ | Load DAC register strobes, active low. Transfers shift register data to DAC register. See truth table for operation. Software decode feature only requires one $\overline{LD}$ strobe. Tie $\overline{LDA}$ and $\overline{LDB}$ together or use one of them with the other pin tied high. |
| SDO                | Serial Data Output. Output of shift register, always active.                                                                                                                                                                                                                               |
| $\overline{RS}$    | Resets DAC registers to condition determined by MSB pin. Active low input.                                                                                                                                                                                                                 |
| MSB                | Digital input: High presets DAC registers to half scale ( $800_H$ ); Low clears all registers to zero ( $000_H$ ), when $\overline{RS}$ is strobed to active low.                                                                                                                          |
| $V_{DD}$           | Positive +5 V power supply input. Tolerance $\pm 10\%$ .                                                                                                                                                                                                                                   |
| AGND               | Analog Ground Input.                                                                                                                                                                                                                                                                       |
| DGND               | Digital Ground Input.                                                                                                                                                                                                                                                                      |
| $V_{REF}$          | Reference Voltage Output, 2.5 V nominal.                                                                                                                                                                                                                                                   |
| $V_{OUT\ A/B}$     | DAC A/B voltage outputs, 4.095 V full scale, $\pm 5$ mA output.                                                                                                                                                                                                                            |

## PIN CONFIGURATION

14-Pin Plastic DIP

14-Lead SO-14

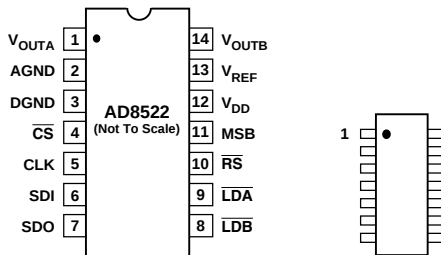


Table II. Truth Tables

| $\overline{RS}$ | MSB        | DAC Register Preset<br>Register Activity                         |
|-----------------|------------|------------------------------------------------------------------|
| 0               | 0          | Asynchronously Resets DAC Registers to Zero Scale                |
| 0               | 1          | Asynchronously Presets DAC Registers to Half Scale ( $800_H$ )   |
| 1               | X          | None                                                             |
| $\overline{CS}$ | CLK        | Shift Register<br>Shift Register                                 |
| 1               | X          | No Effect                                                        |
| 0               | $\uparrow$ | Shifts Register One Bit, SDO Outputs Data from 16 Clocks Earlier |

## ABSOLUTE MAXIMUM RATINGS\*

$V_{DD}$  to DGND & AGND ..... -0.3 V, +7 V  
 Logic Inputs and Output to DGND ..... -0.3 V,  $V_{DD} + 0.3$  V  
 $V_{OUT}$  to AGND ..... -0.3 V,  $V_{DD} + 0.3$  V  
 $V_{REF}$  to AGND ..... -0.3 V,  $V_{DD} + 0.3$  V  
 AGND to DGND ..... -0.3 V,  $V_{DD}$   
 $I_{OUT}$  Short Circuit to GND or  $V_{DD}$  ..... 50 mA  
 Package Power Dissipation .....  $(T_J \text{ max} - T_A)/\theta_{JA}$   
 Thermal Resistance,  $\theta_{JA}$

14-Pin Plastic DIP Package (N-14) ..... 83°C/W  
 14-Lead SOIC Package (SO-14) ..... 120°C/W  
 Maximum Junction Temperature ( $T_J \text{ max}$ ) ..... 150°C  
 Operating Temperature Range ..... -40°C to +85°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (Soldering, 10 sec) ..... +300°C

\*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING GUIDE

| Model    | Temperature Range | Package Description | Package Option |
|----------|-------------------|---------------------|----------------|
| AD8522AN | -40°C to +85°C    | 14-Pin P-DIP        | N-14           |
| AD8522AR | -40°C to +85°C    | 14-Lead SOIC        | SO-14          |

The AD8522 contains 1482 transistors.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8522 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## OPERATION

The AD8522 is a complete ready-to-use dual 12-bit digital-to-analog converter. Only one +5 V power supply is necessary for operation. It contains two voltage-switched, 12-bit, laser-trimmed digital-to-analog converters, a curvature-corrected bandgap reference, rail-to-rail output op amps, input registers, and DAC registers. The serial data interface consists of a serial data input (SDI), clock (CLK), and two load strobe pins (LDA, LDB) with an active low  $\overline{\text{CS}}$  strobe. In addition, an asynchronous  $\overline{\text{RS}}$  pin will set all DAC register bits to zero causing the  $V_{\text{OUT}}$  to become zero volts, or to midscale for trimming applications when the MSB pin is programmed to Logic 1. This function is useful for power on reset or system failure recovery to a known state.

## D/A CONVERTER SECTION

The internal DAC is a 12-bit voltage-mode device with an output that swings from AGND potential to the 2.5 V internal bandgap voltage. It uses a laser-trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output is internally connected to the rail-to-rail output op amp.

## AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage that provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.638 ( $= 4.095 \text{ V}/2.5 \text{ V}$ ) in order to set the 4.095 V full-scale output (1 mV/LSB). See Figure 4 for an equivalent circuit schematic of the analog section.

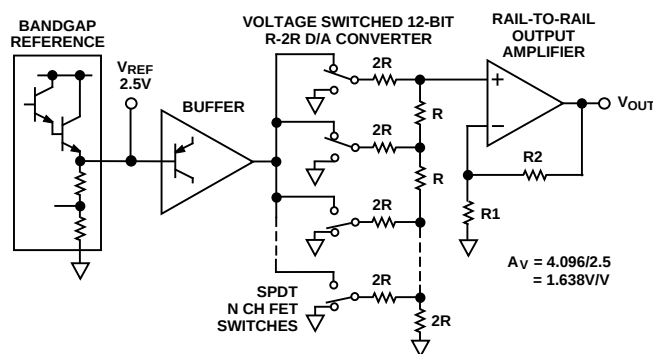


Figure 4. Equivalent AD8522 Schematic of Analog Portion

The op amp has a 16  $\mu\text{s}$  typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals versus positive. See the oscilloscope photos in the "Typical Performance Characteristics" section of this data sheet.

## OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 5 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P channel pull-up device that can supply GND terminated loads, especially important at the -10% supply tolerance value of 4.5 V.

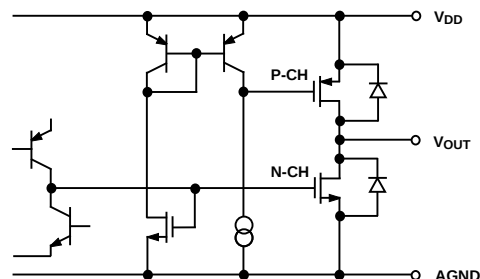


Figure 5. Equivalent Analog Output Circuit

Figures 6 and 7 in the typical performance characteristics section provide information on output swing performance near ground and full scale as a function of load. In addition to resistive load driving capability the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

## REFERENCE SECTION

The internal 2.5 V curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. The voltage generated by the reference is available at the  $V_{\text{REF}}$  pin. Since  $V_{\text{REF}}$  is not intended to drive heavy external loads, it must be buffered. The equivalent emitter follower output circuit of the  $V_{\text{REF}}$  pin is shown in Figure 4.

Bypassing the  $V_{\text{REF}}$  pin will improve noise performance; however, bypassing is not required for proper operation. Figure 10 shows broad band noise performance.

## POWER SUPPLY

The very low power consumption of the AD8522 is a direct result of a circuit design optimizing use of a CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors good analog accuracy is achieved.

For power consumption sensitive applications it is important to note that the internal power consumption of the AD8522 is strongly dependent on the actual input voltage levels present on the SDI, CLK,  $\overline{\text{CS}}$ , MSB, LDA, LDB and  $\overline{\text{RS}}$  pins. Since these inputs are standard CMOS logic structures, they contribute static power dissipation dependent on the actual driving logic  $V_{\text{OH}}$  and  $V_{\text{OL}}$  voltage levels. Consequently for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A  $V_{\text{INL}} = 0 \text{ V}$  on the logic input pins provides the lowest standby dissipation of 1 mA with a +5 V power supply.

As with any analog system, it is recommended that the AD8522 power supply be bypassed on the same PC card that contains the chip. Figure 12 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifiers used in the AD8522 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.5 V to +5.5 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the AD8522

AD8522

is possible down to +4.3 V. The minimum operating supply voltage versus load current plot, in Figure 7, provides information for operation below  $V_{DD} = +4.5$  V.

TIMING AND CONTROL

The AD8522 has a 16-bit serial input register that accepts clocked in data when the CS pin is active low. The DAC registers are updated by the Load Enable ( $\overline{LDA}$  and  $\overline{LDB}$ ) pins.

The AD8522 offers two modes of data loading. The first mode, hardware-load, directs the data currently clocked into the serial shift register into either the DAC A or the DAC B register or both depending on the external active low strobing of the  $\overline{LDA}$  or  $\overline{LDB}$  pin. Serial data register bit  $Sf/\overline{Hd}$  must be low for this mode to be in effect.

The second mode of operation is software-load which is designed to minimize the number of control lines connected to the AD8522. In this mode of operation the  $\overline{LDA}$  and  $\overline{LDB}$  pins act as one control input taking the present contents of the serial

input register and transferring the 12 bits of data into the decoded address determined by the address bits A and B in the serial input register.

Unipolar Output Operation

This is the basic mode of operation for the AD8522. The AD8522 has been designed to drive loads as low as 820  $\Omega$  in parallel with 500 pF. The code table for this operation is shown in Table III.

| Table III. Unipolar Code Table     |                                |                           |
|------------------------------------|--------------------------------|---------------------------|
| Hexadecimal Number in DAC Register | Decimal Number in DAC Register | Analog Output Voltage (V) |
| FFF                                | 4095                           | +4.095                    |
| 801                                | 2049                           | +2.049                    |
| 800                                | 2048                           | +2.048                    |
| 7FF                                | 2047                           | +2.047                    |
| 000                                | 0                              | 0                         |

Typical Performance Characteristics

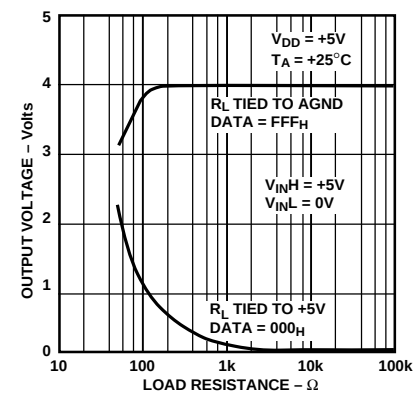


Figure 6. Output Swing vs. Load

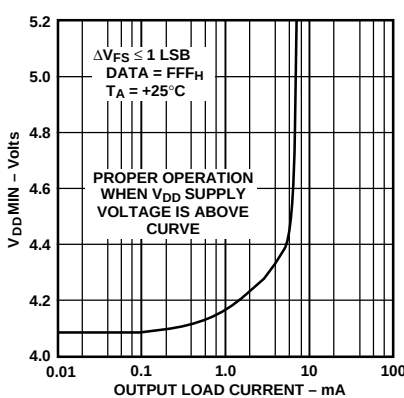


Figure 7. Minimum Supply Voltage vs. Load Current

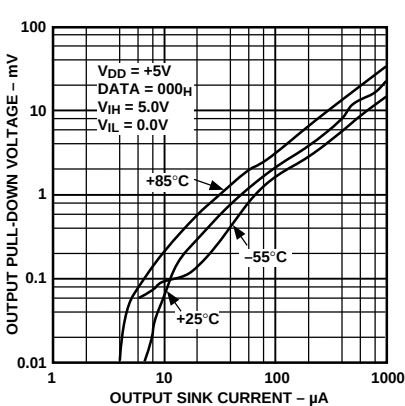


Figure 8. Pull-Down Voltage vs. Output Sink Current Capability

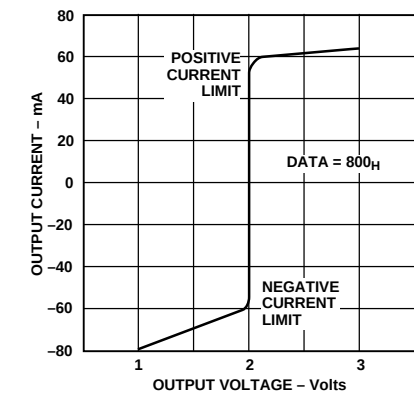


Figure 9.  $I_{OUT}$  vs.  $V_{OUT}$

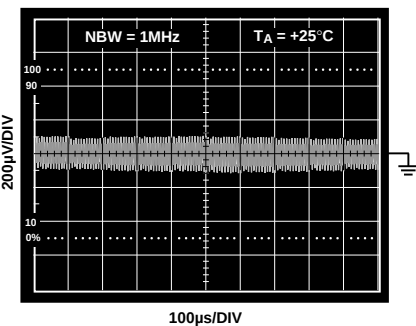


Figure 10. Broadband Noise

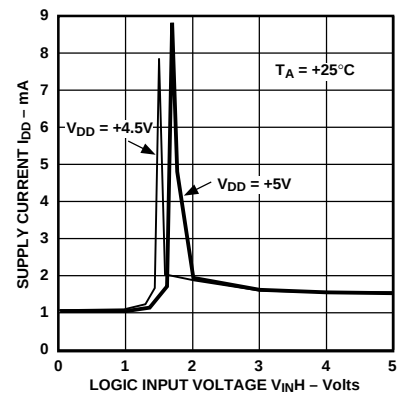


Figure 11. Supply Current vs. Logic Input Voltage

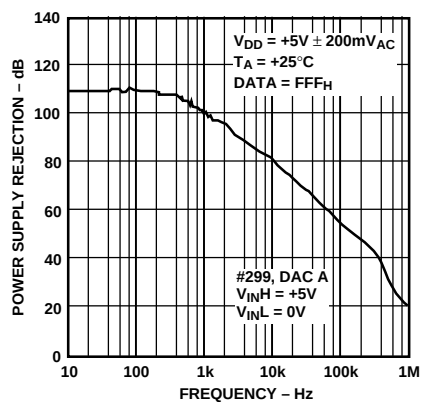


Figure 12. Power Supply Rejection vs. Frequency

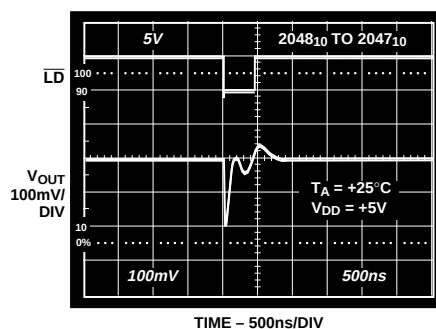


Figure 13. Midscale Transition Performance

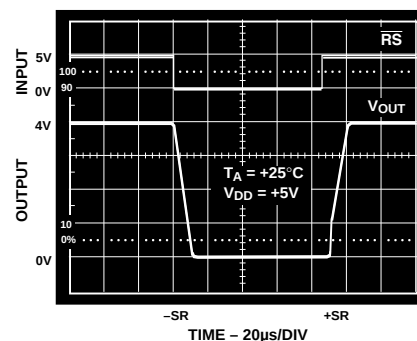


Figure 14. Large Signal Settling Time

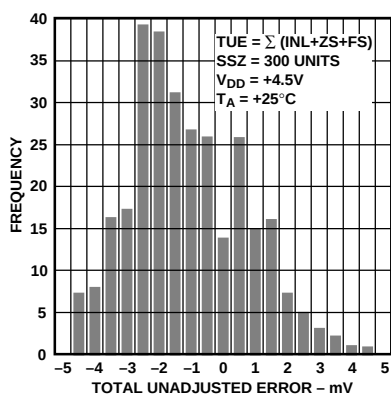


Figure 15. Total Unadjusted Error Histogram

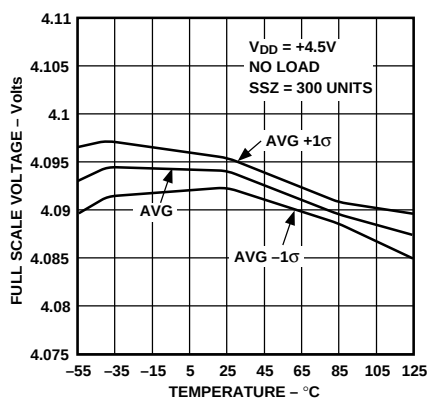


Figure 16. Full-Scale Voltage vs. Temperature

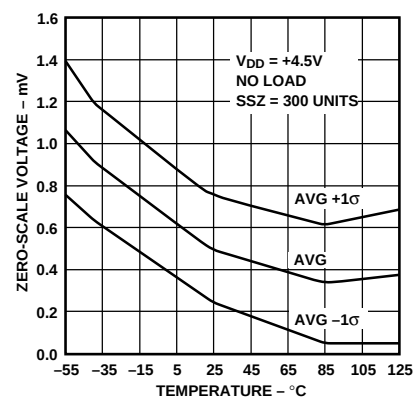


Figure 17. Zero-Scale Voltage vs. Temperature

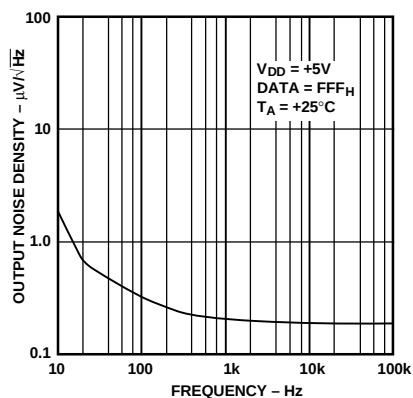


Figure 18. Output Voltage Noise Density vs. Frequency

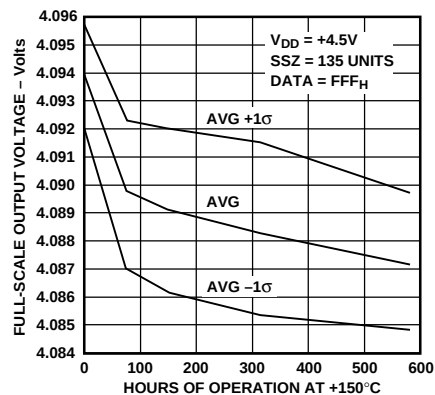


Figure 19. Long Term Drift Accelerated by Burn-In

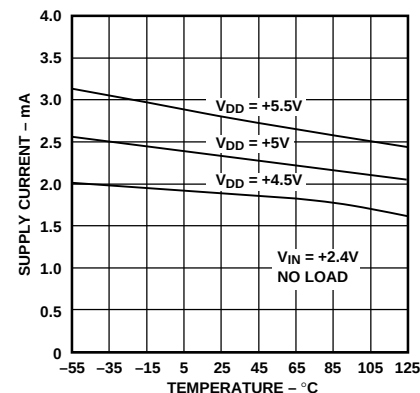


Figure 20. Supply Current vs. Temperature

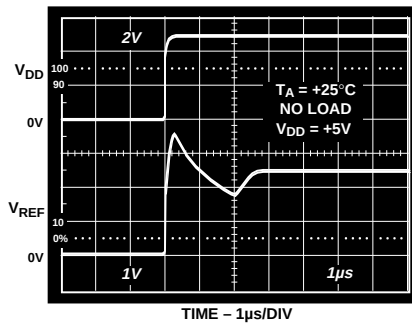


Figure 21. Reference Startup vs. Time

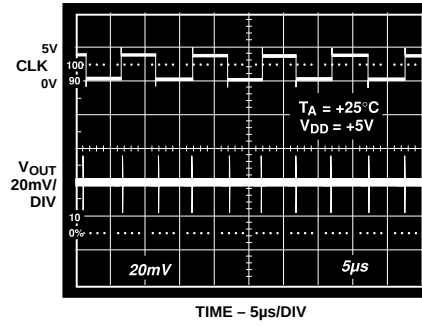


Figure 22. Digital Feedthrough vs. Time

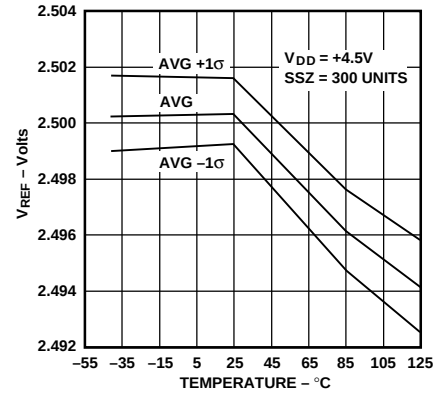


Figure 23. Reference Voltage vs. Temperature

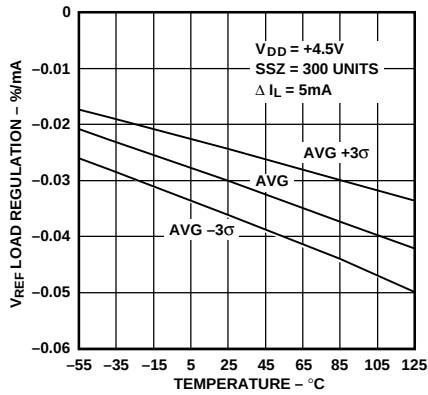


Figure 24. Reference Load Regulation vs. Temperature

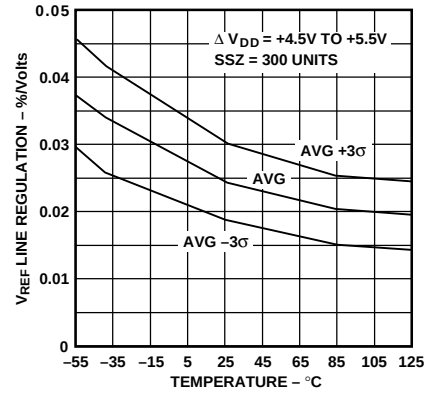
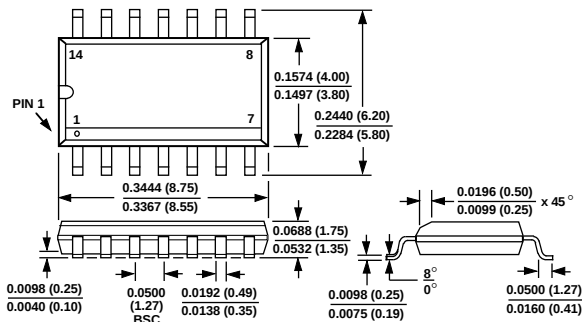


Figure 25. Reference Line Regulation vs. Temperature

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 14-Lead Narrow Body SOIC (SO-14)



### 14-Lead Epoxy DIP (N-14)

