

FAIRCHILD
SEMICONDUCTOR®

August 2006

FDFS6N754

Integrated N-Channel PowerTrench® MOSFET and Schottky Diode 30V, 4A, 56mΩ

Features

- Max $r_{DS(on)}$ = 56mΩ at $V_{GS} = 0V$, $I_D = 4A$
Max $r_{DS(on)}$ = 75mΩ at $V_{GS} = 4.5V$, $I_D = 3.5A$
- $V_F < 0.45V @ 2A$
 $V_F < 0.28V @ 100mA$
- Schottky and MOSFET incorporated into single power surface mount SO-8 package
- Electrically independent Schottky and MOSFET pinout for design flexibility
- Low Gate Charge ($Q_g = 4nC$)
- Low Miller Charge



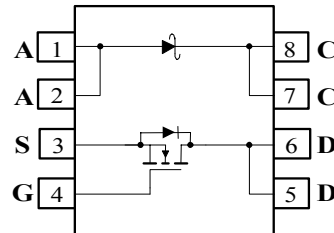
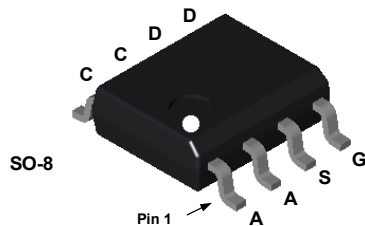
General Description

The FDFS6N754 combines the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in an SO-8 package.

This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low on-state resistance. The independently connected Schottky diode allows its use in a variety of DC/DC converter topologies.

Applications

- DC/DC converters



MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous (Note 1a)	4	A
	-Pulsed	20	
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
V_{RRM}	Schottky Repetitive Peak Reverse Voltage	20	V
I_O	Schottky Average Forward Current (Note 1a)	2	A
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ C$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDFS6N754	FDFS6N754	SO-8	330mm	12mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		24.5		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_J = 125^\circ\text{C}$			1 20	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-4.2		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 4\text{A}$		42	56	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 3.5\text{A}$		53	75	
		$V_{GS} = 10\text{V}, I_D = 4\text{A}$, $T_J = 125^\circ\text{C}$		61	81	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 4\text{A}$		10		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$		225	299	pF
C_{oss}	Output Capacitance			80	107	pF
C_{rss}	Reverse Transfer Capacitance			42	63	pF
R_G	Gate Resistance			5.1		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 1\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 6\Omega$		6	12	ns
t_r	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			20	32	ns
t_f	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{DS} = 15\text{V}$, $I_D = 4\text{A}$		4	6	nC
$Q_{g(5)}$	Total Gate Charge at 5V			2	3	nC
Q_{gs}	Gate to Source Gate Charge			0.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			1		nC

Drain-Source Diode Characteristics and Maximum Ratings

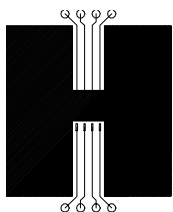
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1.3\text{A}$ (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 4\text{A}, di/dt = 100\text{A}/\mu\text{s}$		13	20	ns
Q_{rr}	Reverse Recovery Charge	$I_F = 4\text{A}, di/dt = 100\text{A}/\mu\text{s}$		4	6	nC

Schottky Diode Characteristics

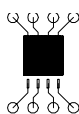
V_R	Reverse Breakdown Voltage	$I_R = -1\text{mA}$	-30			V
I_R	Reverse Leakage	$V_R = -10\text{V}$	$T_J = 25^\circ\text{C}$	39	250	μA
			$T_J = 125^\circ\text{C}$	18		mA
V_F	Forward Voltage	$I_F = 100\text{mA}$	$T_J = 25^\circ\text{C}$	225	280	mV
			$T_J = 125^\circ\text{C}$	140		
		$I_F = 2\text{A}$	$T_J = 25^\circ\text{C}$	364	450	
			$T_J = 125^\circ\text{C}$	290		

Notes:

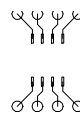
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

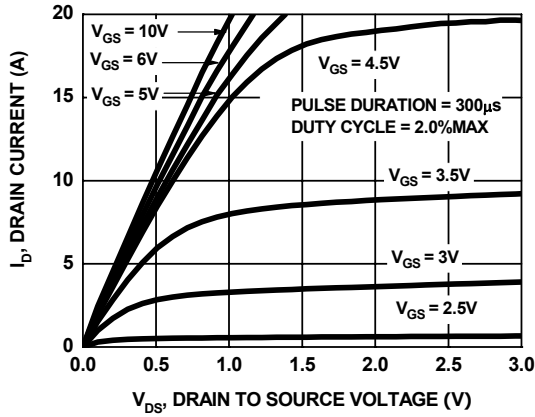


Figure 1. On Region Characteristics

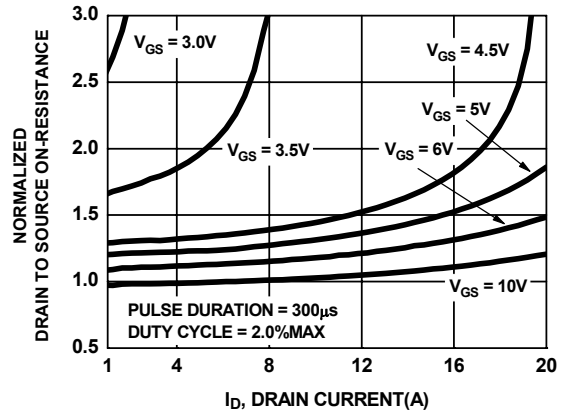


Figure 2. On-Resistance vs Drain Current and Gate Voltage

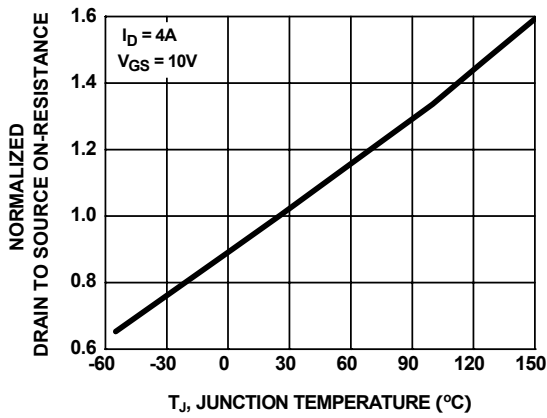


Figure 3. On Resistance vs Temperature

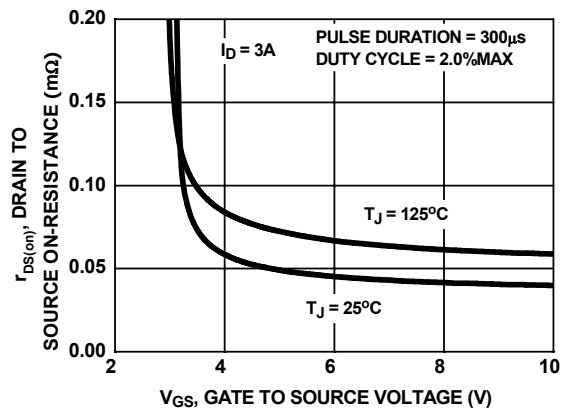


Figure 4. On-Resistance vs Gate to Source Voltage

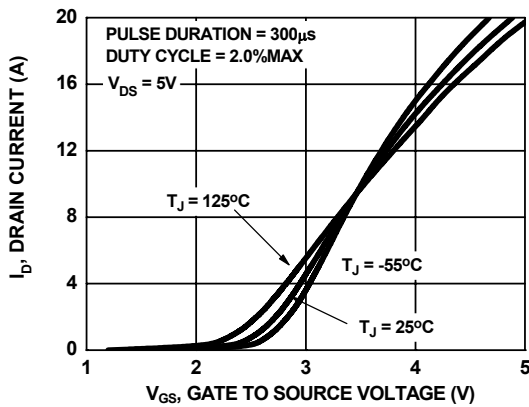


Figure 5. Transfer Characteristics

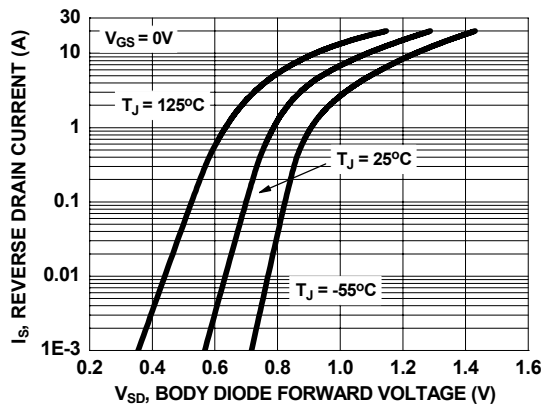


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

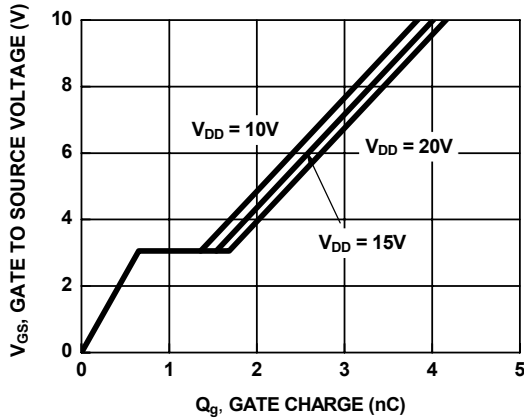


Figure 7. Gate Charge Characteristics

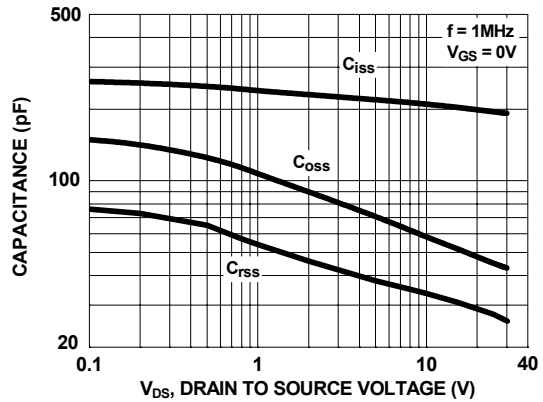


Figure 8. Capacitance vs Drain to Source Voltage

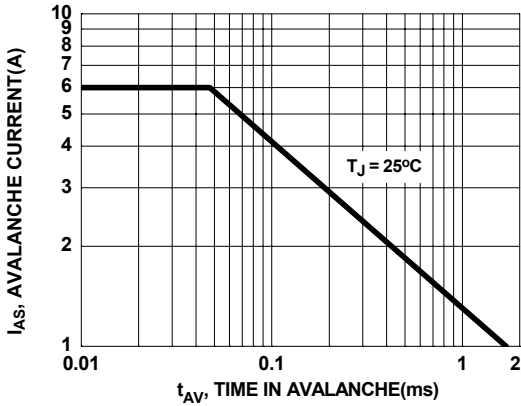


Figure 9. Unclamped Inductive Switching Capability

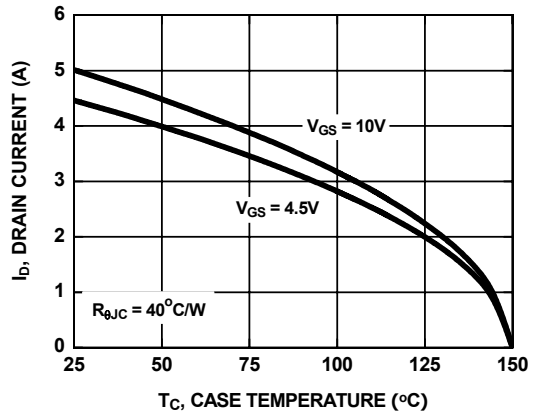


Figure 10. Maximum Continuous Drain Current vs Case Temperature

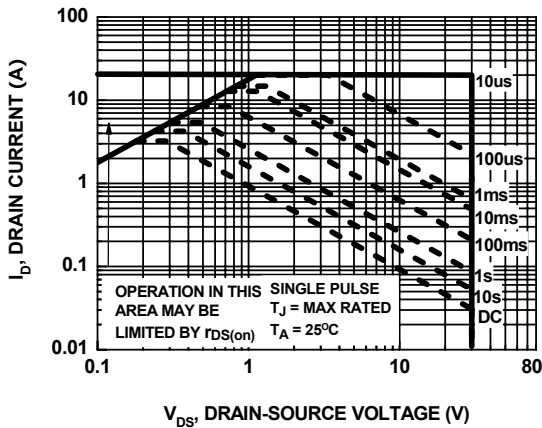


Figure 11. Forward Bias Safe Operating Area

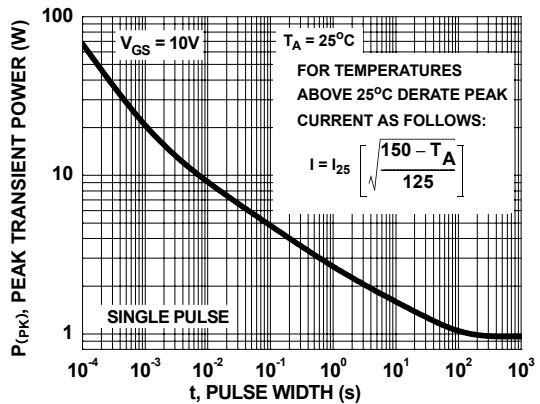


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

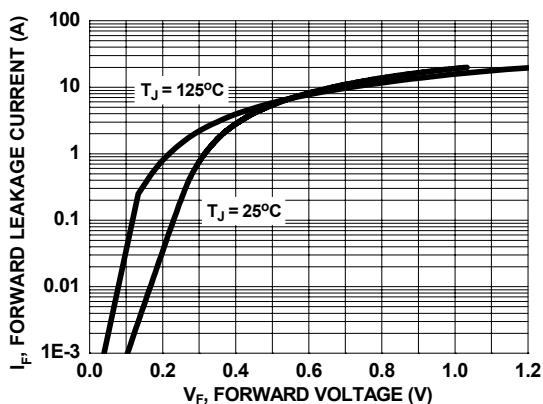


Figure 13. Schottky Diode Forward Voltage

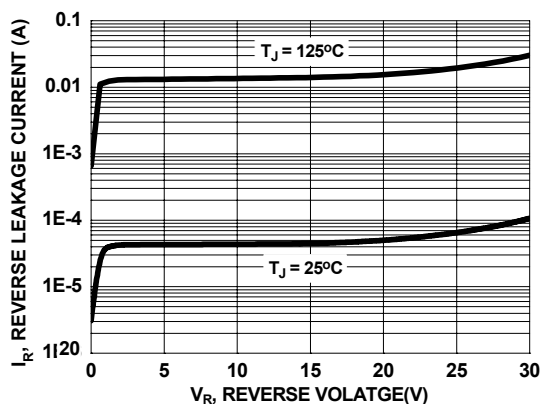


Figure 14. Schottky Diode Reverse Current

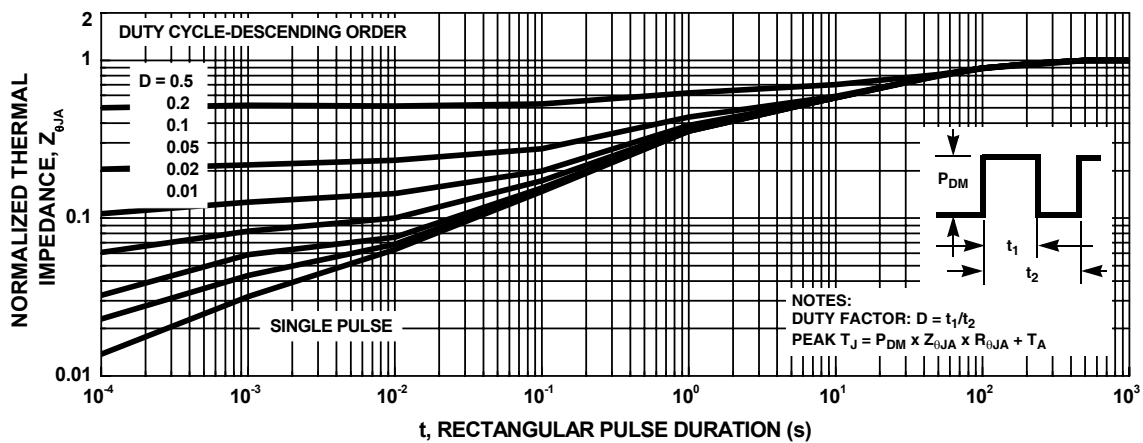


Figure 15. Transient Thermal Response Curve

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Rev. I20