

IRF7601

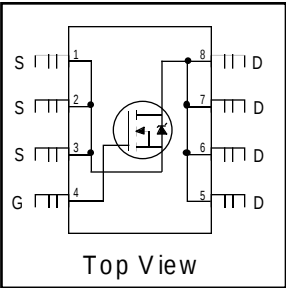
HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- N-Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel
- Fast Switching

Description

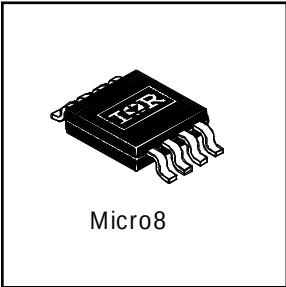
Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8 package, with half the footprint area of the standard SO-8, provides the smallest footprint available in an SOIC outline. This makes the Micro8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



$V_{DS} = 20V$

$R_{DS(on)} = 0.035\Omega$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_A = 25^{\circ}C$	Continuous Drain Current, V_{GS} @ 4.5V	5.7	A
I_D @ $T_A = 70^{\circ}C$	Continuous Drain Current, V_{GS} @ 4.5V	4.6	
I_{DM}	Pulsed Drain Current ①	30	
P_D @ $T_A = 25^{\circ}C$	Power Dissipation	1.8	W
	Linear Derating Factor	14	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④	—	70	°C/W

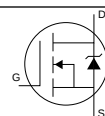
All Micro8 Data Sheets reflect improved Thermal Resistance, Power and Current -Handling Ratings- effective only for product marked with Date Code 505 or later .

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.024	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.035	Ω	$V_{GS} = 4.5V, I_D = 3.8A$ ③
		—	—	0.050		$V_{GS} = 2.7V, I_D = 1.9A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	6.1	—	—	S	$V_{DS} = 10V, I_D = 1.9A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	14	22	nC	$I_D = 3.8A$
Q_{gs}	Gate-to-Source Charge	—	2.0	3.0		$V_{DS} = 16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	6.3	9.5		$V_{GS} = 4.5V$, See Fig. 6 and 9 ③
$t_{d(on)}$	Turn-On Delay Time	—	5.1	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	47	—		$I_D = 3.8A$
$t_{d(off)}$	Turn-Off Delay Time	—	24	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	32	—		$R_D = 2.6\Omega$, See Fig. 10 ③
C_{iss}	Input Capacitance	—	650	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	300	—		$V_{DS} = 15V$
C_{rss}	Reverse Transfer Capacitance	—	150	—		$f = 1.0MHz$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	—	—	1.8	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	30		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 3.8A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	51	77	ns	$T_J = 25^\circ\text{C}, I_F = 3.8A$
Q_{rr}	Reverse Recovery Charge	—	69	100	nC	$di/dt = 100A/\mu s$ ③



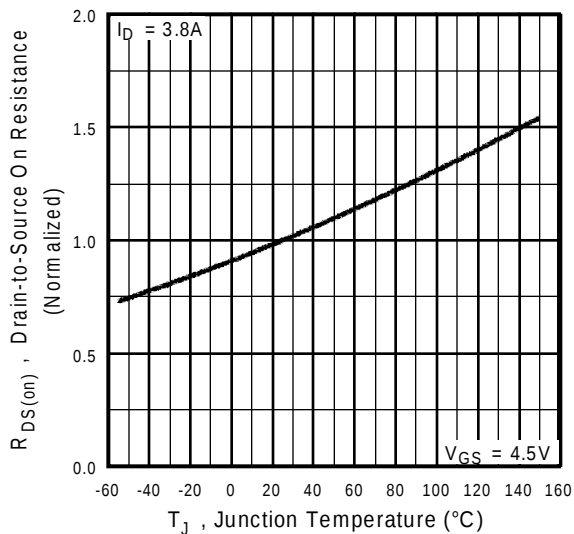
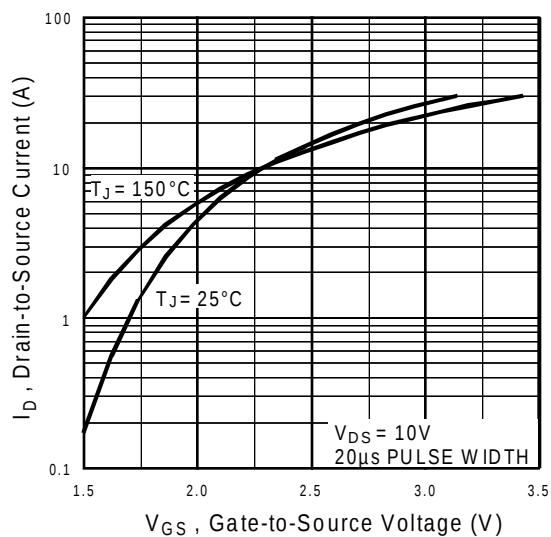
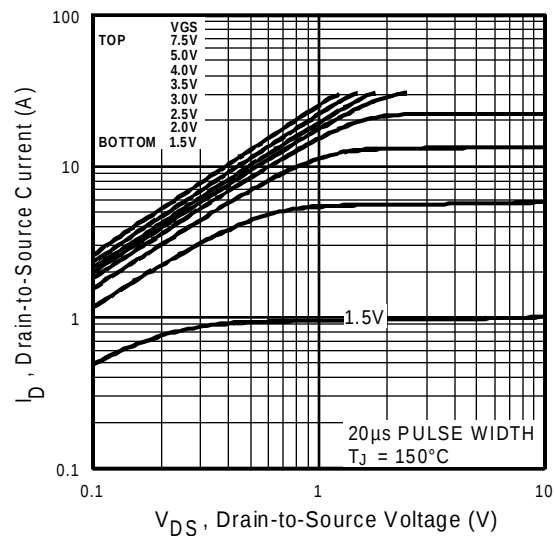
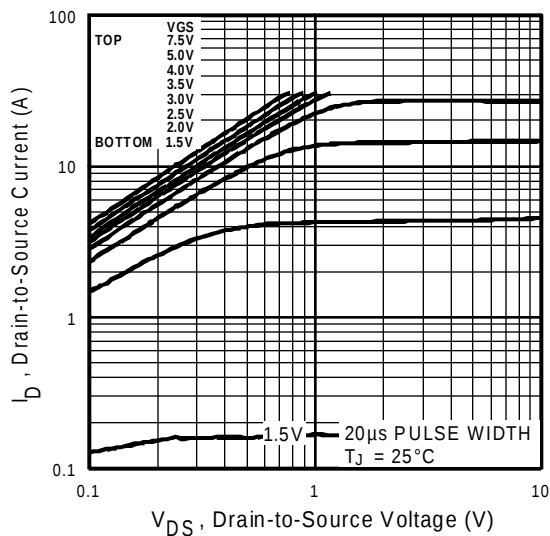
Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

② $I_{SD} \leq 3.8A, di/dt \leq 96A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

④ Surface mounted on FR-4 board, $t \leq 10sec$.



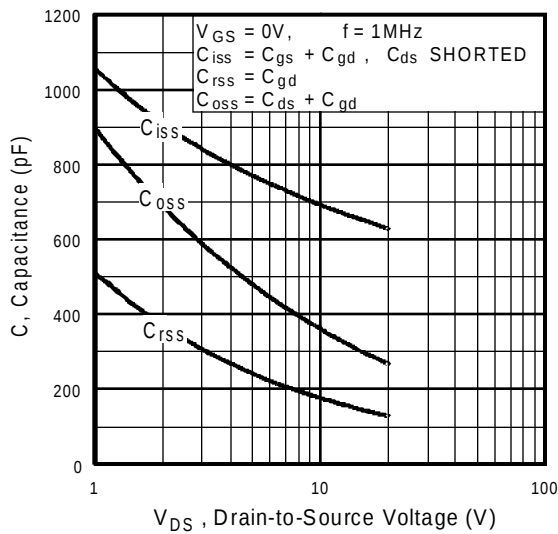


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

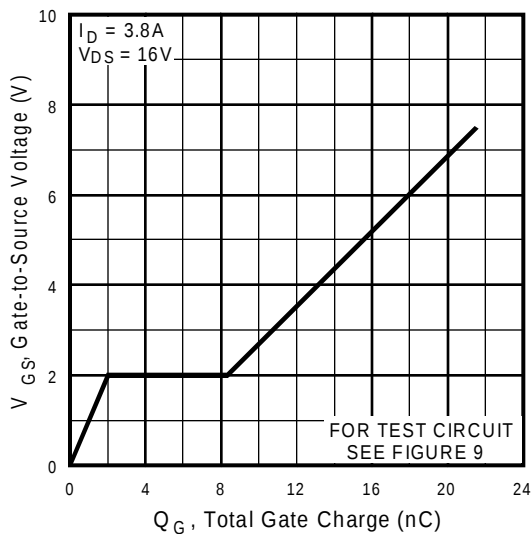


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

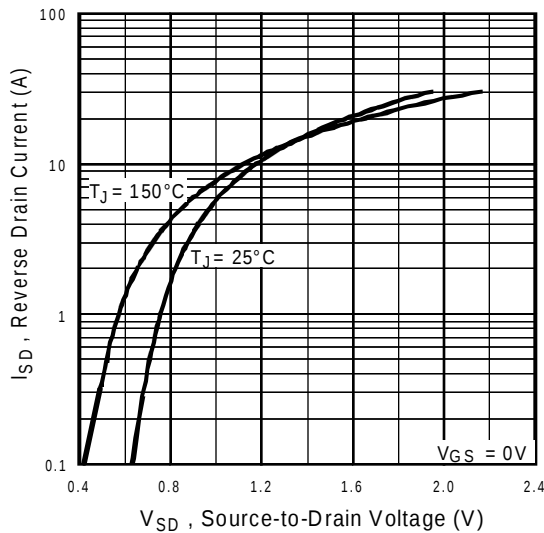


Fig 7. Typical Source-Drain Diode Forward Voltage

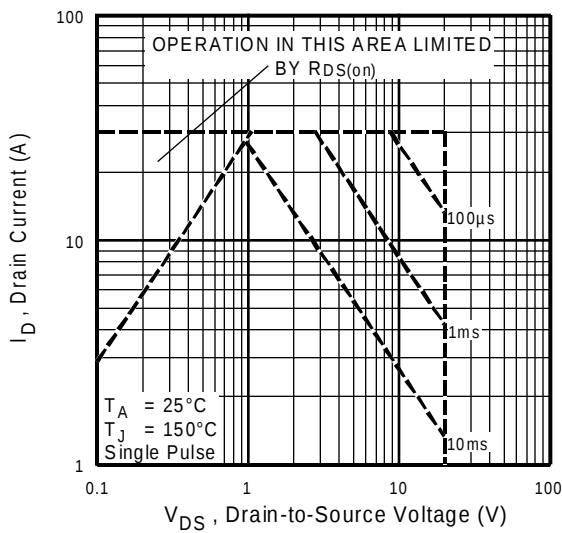


Fig 8. Maximum Safe Operating Area

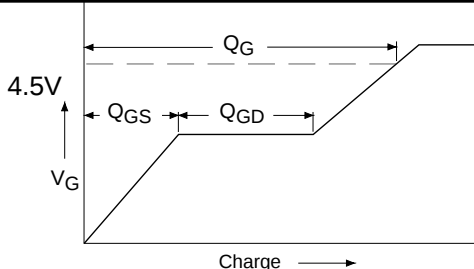


Fig 9a. Basic Gate Charge Waveform

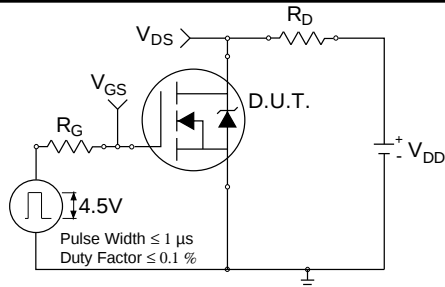


Fig 10a. Switching Time Test Circuit

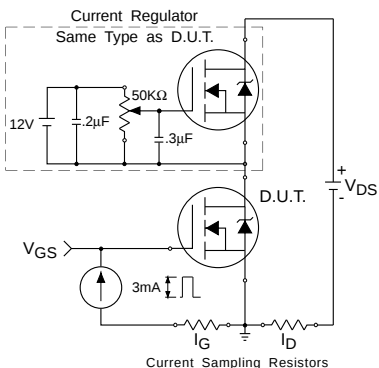


Fig 9b. Gate Charge Test Circuit

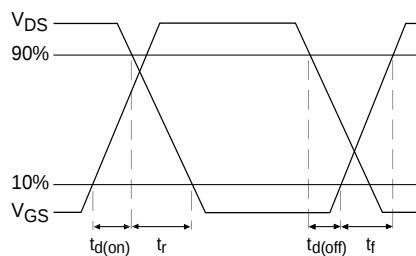


Fig 10b. Switching Time Waveforms

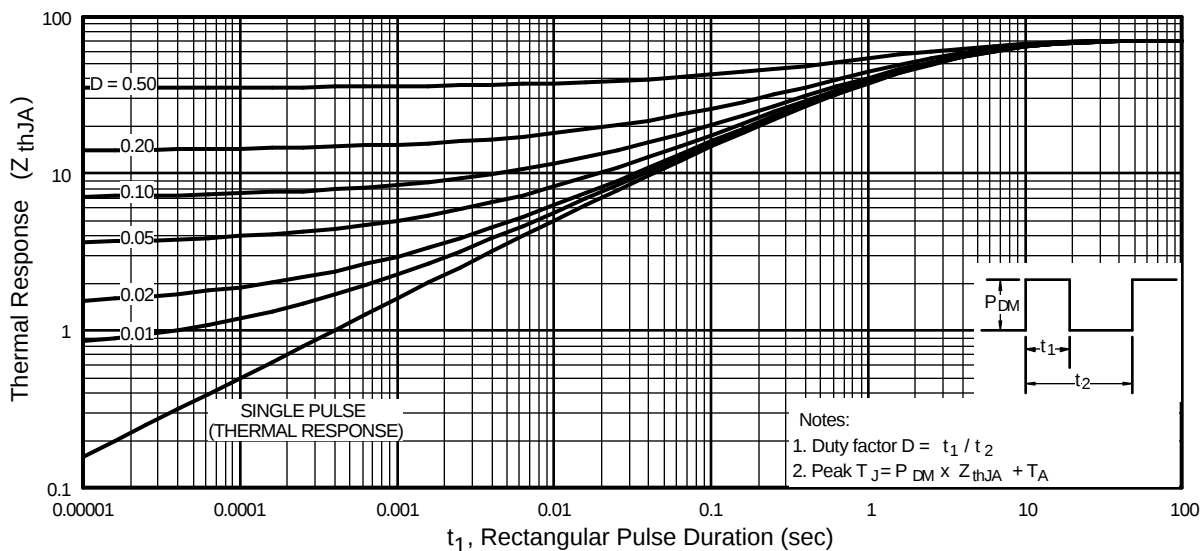
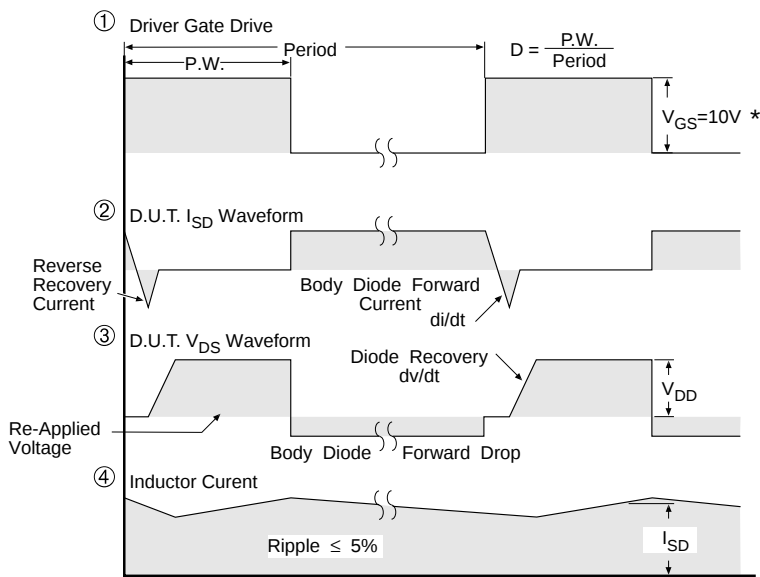
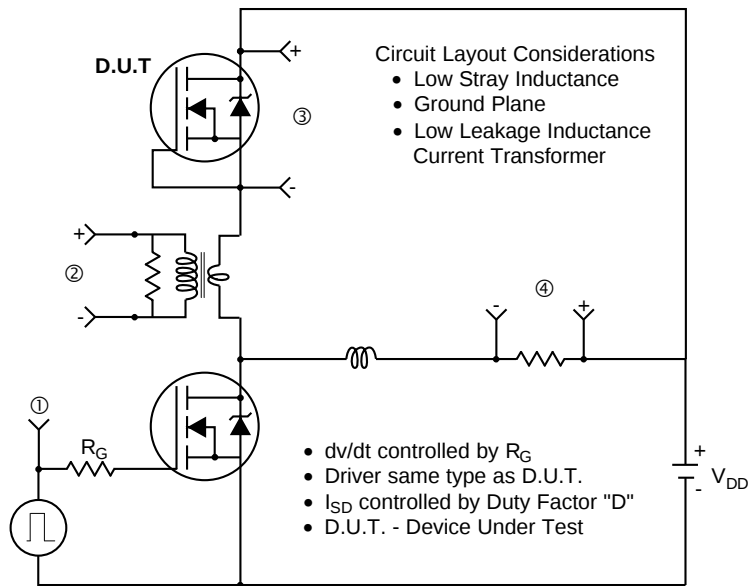


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



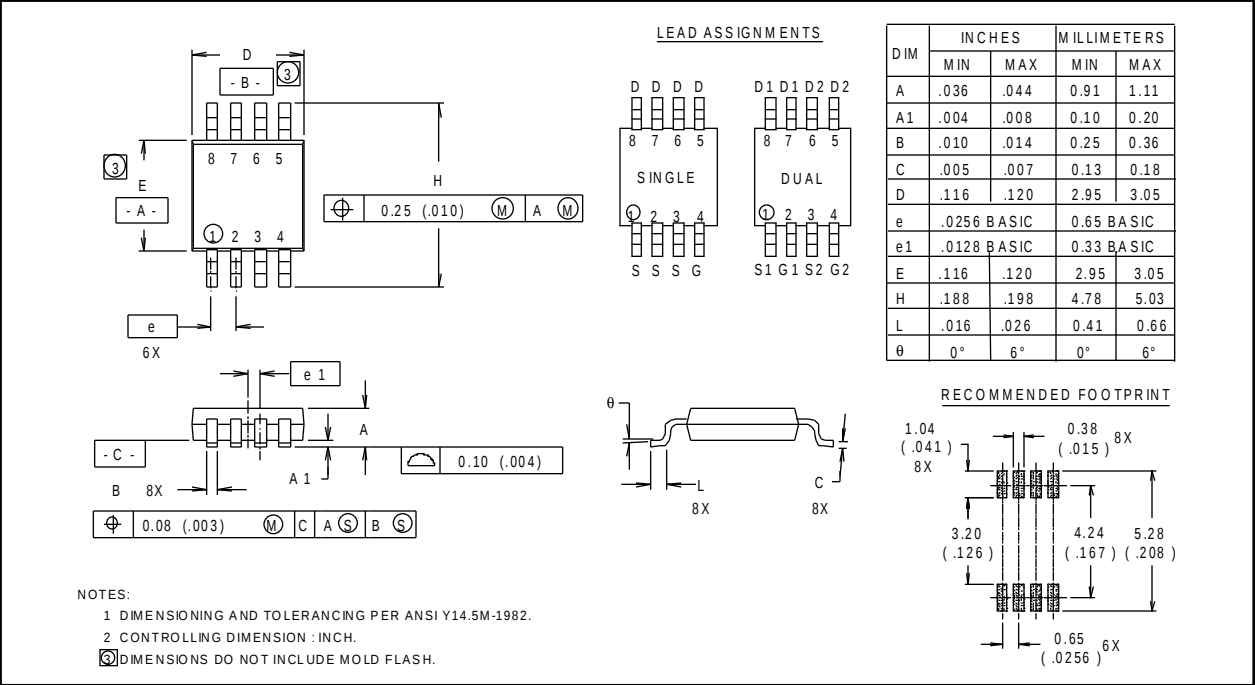
* $V_{GS} = 5V$ for Logic Level Devices

Fig 12. For N-Channel HEXFETS

Package Outline

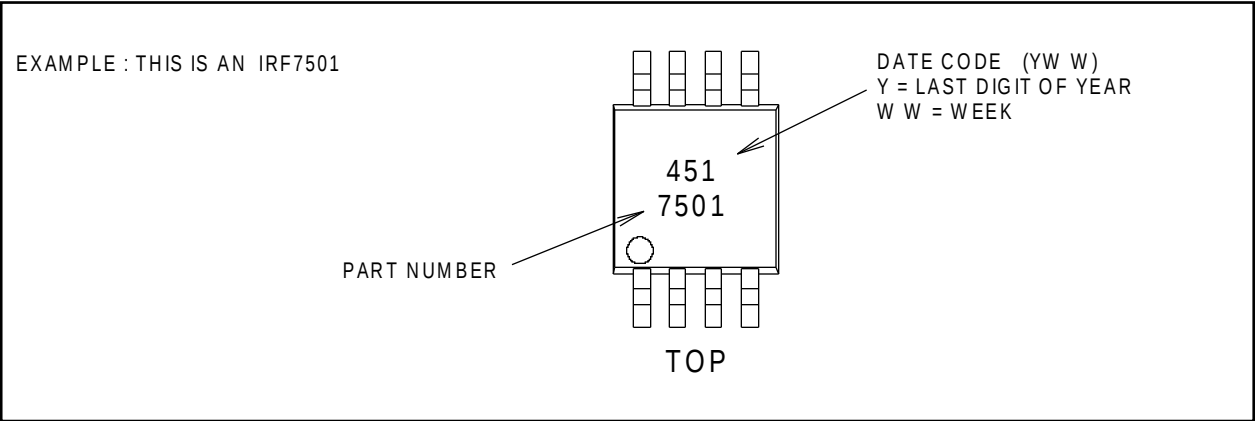
Micro8 Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

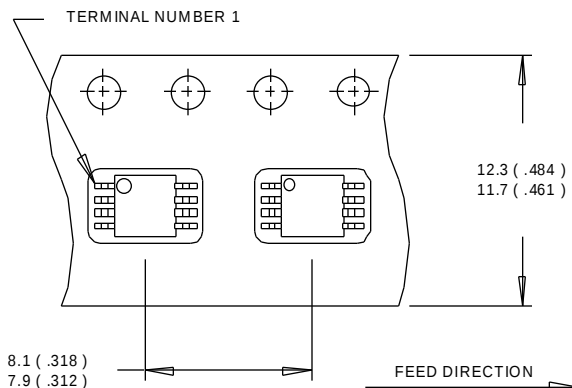
Micro8



Tape & Reel Information

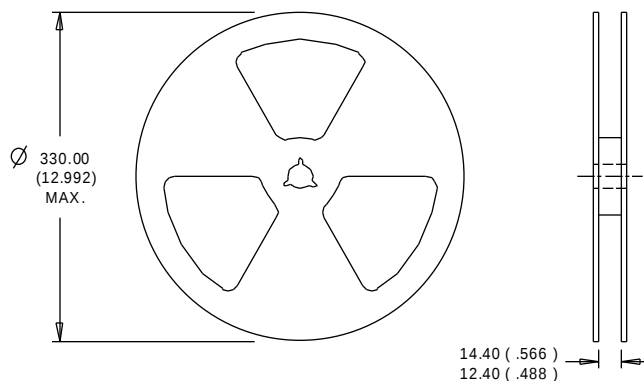
Micro8

Dimensions are shown in millimeters (inches)



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.