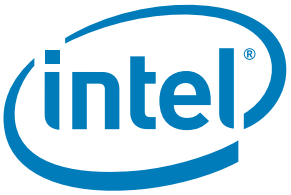
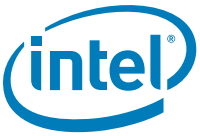


Intel® System Controller Hub (Intel® SCH)

Datasheet

March 2009

Document Number: 319537-002US



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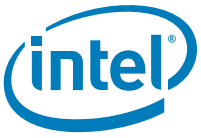

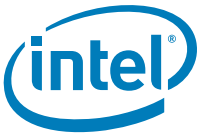

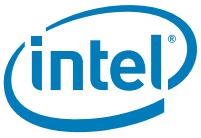

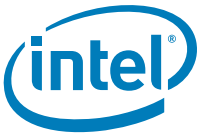

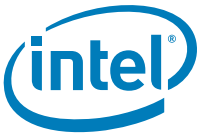

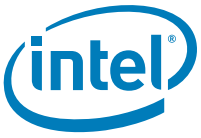

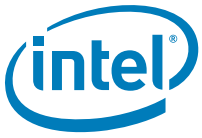

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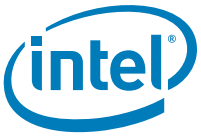


Tables

Revision History

Revision Number	Description	Revision Date
-001	• Initial Release	April 2008
-002	• Updated Reference Documents • Chapter 1.3.2 – Added support of 2GB of memory and of 2048Mb devices • Chapter 2.1 – Corrected CMOS/AGTL+ assignments • Chapter 2.5 – Added that PCIe compensation pins also act for LVDS and SDVO interfaces • Chapter 2.10 – Clarified that SMB_ALERT# does not wake the system or generate an interrupt • Chapter 2.11 – Clarified that RTCRST# does not clear CMOS • Chapter 2.14 – Clarified that the Intel® SCH will not de-assert CLKREQ# • Chapter 3.1 – Corrected reset states for CLKREQ# (VOX-known), RSMRST# (VLI), and LVDS (VOH) • Chapter 5.3 – Added support of up to 2GB of memory • Chapter 8.2 – Added 2048 Mbit device support • Chapter 9.3.2 – Removed assertion that display PLLs can be disabled • Chapter 9.4.2 – Updated Device ID Register • Chapter 11.1.4 – Added section asserting that No Snoop is not supported • Chapter 11.2.15 – Corrected default value • Chapter 12.2.16 – Corrected Bit[1:0] definitions • Chapter 15.2.8 – Removed CRID description - wrong place • Chapter 15.3.10 – Corrected Bit 10 definition • Chapter 17.1 – Clarified that the Intel® SCH does not support LPC DMA • Chapter 17.5.1 – Corrected Bit[15:12] definitions • Chapter 18.7.2 – Corrected CGIO default value • Chapter 20.2 – Added $I_{VCC33RTC}$, $I_{VCC5REF}$ and $I_{VCC5REFSUS}$ and corrected $I_{VCCPCIEBG}$ parameter description	March 2009

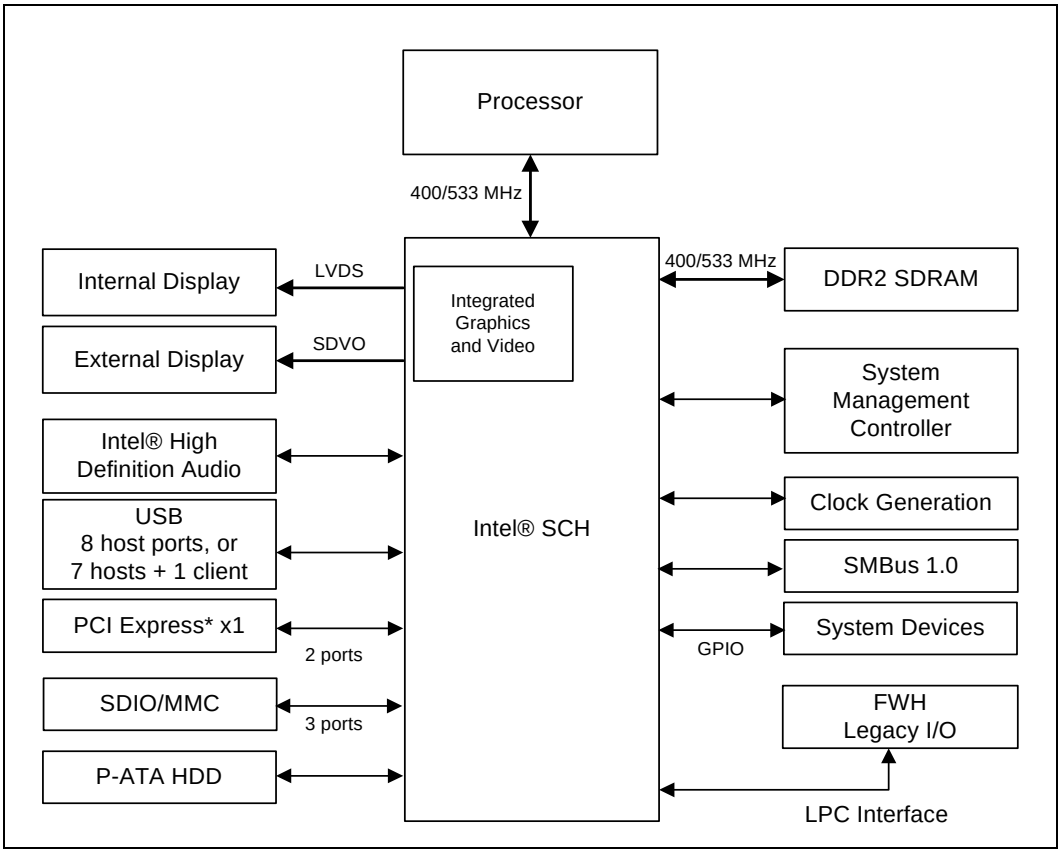
§ §

1 Introduction

The Intel® System Controller Hub (Intel® SCH) is a component of Intel® Atom™ processor technology. The Intel® SCH combines functionality normally found in separate GMCH (integrated graphics, processor interface, memory controller) and ICH (on-board and end-user I/O expansion) components into a single component consuming less than 2.3 W of thermal design power. The features of the Intel® SCH provide functionality necessary for traditional operating systems (such as Microsoft Windows Vista* or Linux*) as well as functionality normally associated with handheld devices (such as SDIO/MMC and USB client). The Intel® SCH was designed to be used with the Intel® Atom™ processor Z5xx series processor. Figure 1 shows an example system block diagram. Section 1.3 provides an overview of the major features of the Intel® SCH.

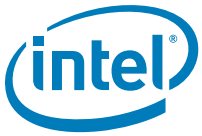
This document is the datasheet for the Intel System Controller Hub component. The document content includes signal description, system memory map, register descriptions, a description of the Intel® SCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

Figure 1. System Block Diagram Example



1.1 Terminology

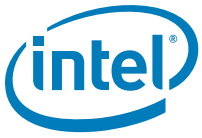
Term	Description
ACPI	Advanced Control Programmable Interface.
ADD2	Advanced Digital Display 2. An interface specification that accepts serial DVO inputs and translates them into different display outputs such as DVO, TV-OUT, and LVDS.
Core	The internal base logic in the Intel® SCH.
CRT	Cathode Ray Tube
DBI	Dynamic Bus Inversion
DDR2	A second generation Double Data Rate SDRAM memory technology.
DVI	Digital Video Interface. DVI is a specification that defines the connector and interface for digital displays.
SMC	System Management Controller or External Controller. Refers to a separate system management controller that handles reset sequences, sleep state transitions, and other system management tasks.
EHCI	Enhanced Host Controller Interface. A controller interface that, on the Intel® SCH, supports up to eight USB 2.0 high-speed root ports, two of which are to be used internally only.
FSB	Front Side Bus. FSB is synonymous with host bus or processor bus.
FWH	Firmware Hub
Cold Reset	Full reset is when PWROK is deasserted and all system rails except V_{CCRTC} are powered down.
Warm Reset	Warm reset is when both RESET# and PWROK are asserted.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. HDMI transmits all ATSC HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available through: http://www.hdmi.org/).
Host	This term is used synonymously with processor.
Intel Graphics Media Adapter	Internal Graphics Device. Generic name for a graphics accelerator that performs decoding of digital video signals.
Intel® GMA 500	Intel® Graphics Media Accelerator 500. A hardware accelerator for 2D and 3D graphics.
INTx	An interrupt request signal where “x” stands for interrupts A, B, C, and D.
LCD	Liquid Crystal Display.
LVDS	Low Voltage Differential Signaling. LVDS is a high speed, low power data transmission standard used for display connections to LCD panels.
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
PCI Express*	PCI Express* is a high-speed serial interface. The PCI Express configuration is software compatible with the existing PCI specifications.
Processor	Intel® Atom™ processor Z5xx series



Term	Description
Rank	A unit of DRAM corresponding to number of SDRAM devices in parallel such that a full 64-bit data bus is formed.
Intel® SCH	Intel® System Controller Hub: a single-chip component that contains the processor interface, DDR2 SDRAM controller, Intel Graphics Media Accelerator 500 (Intel® GMA 500), various display interfaces, USB, SDIO, PCI Express*, PATA, LPC, and other I/O capabilities.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SDVO	Serial Digital Video Out (SDVO). SDVO is a digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS, TV-Out).
SDVO Device	Third-party codec that use SDVO as an input may have a variety of output formats, including DVI, LVDS, HDMI, TV-Out, etc.
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.
SMI	System Management Interrupt. SMI is used to indicate any of several system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state-related activity).
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface from Silicon Image that is used in DVI and HDMI. TMDS is based on low-voltage differential signaling and converts an 8-bit signal into a 10-bit transition-minimized and DC-balanced signal (equal number of 0's and 1's) in order to reduce EMI generation and improve reliability.
TOLM	Top of Low Memory. The highest address below 4 GB where a processor-initiated memory read or write transaction will create a corresponding cycle to DRAM on the memory interface.
UHCI	Universal Host Controller Interface. A controller interface that supports two USB 1.1 ports. The Intel® SCH contains three UHCI controllers.
UMA	Unified Memory Architecture. UMA describes an Intel Graphics Media Adapter using system memory for its frame buffers.
VCO	Voltage Controlled Oscillator

1.2 Reference Documents

Document	Location
Intel® Atom™ Processor Z5xx Series Datasheet	http://www.intel.com/products/atom/techdocs.htm
Intel® System Controller Hub (Intel® SCH) Specification Update	http://www.intel.com/products/atom/techdocs.htm
PCI Express Base Specification, Revision 1.0a	http://www.pcisig.com/specifications/pciexpress/
Mobile Graphics Low-Power Addendum to the PCI Express® Base Specification Revision 1.0	http://www.pcisig.com/specifications/pciexpress/
Low Pin Count Interface Specification, Revision 1.1 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
System Management Bus Specification, Version 1.0 (SMBus)	http://www.smbus.org/specs/
PCI Local Bus Specification, Revision 2.3 (PCI)	http://www.pcisig.com/specifications
PCI Power Management Specification, Revision 1.1	http://www.pcisig.com/specifications
Advanced Configuration and Power Interface, Version 3.0 (ACPI)	http://www.acpi.info/spec.htm
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
Universal Serial Bus Specification (USB), Revision 2.0	http://www.usb.org/developers/docs
AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org
IA-PC HPET (High Precision Event Timers) Specification, Revision 1.0	http://www.intel.com/hardwaredesign/hpetspec_1.pdf



1.3 Overview

The Intel® SCH is designed for use with Intel Atom processor Z5xx series-based platforms. The Intel® SCH connects to the processor as shown in Figure 1.

The Intel® SCH incorporates a variety of PCI functions as listed in Table 1.

Table 1. PCI Devices and Functions

Device	Function	Function Description
0	0	Host Bridge
2	0	Integrated Graphics and Video Device
26	0	USB Client
27	0	Intel® High Definition Audio (Intel® HD Audio) Controller
28	0	PCI Express Port 1
	1	PCI Express Port 2
29	0	USB Classic UHCI Controller 1
	1	USB Classic UHCI Controller 2
	2	USB Classic UHCI Controller 3
	7	USB2 EHCI Controller
30	0	SDIO/MMC Port 0
	1	SDIO/MMC Port 1
	2	SDIO/MMC Port 2
31	0	LPC Interface
	1	PATA Controller

NOTE: All devices are on PCI Bus 0.

1.3.1 Processor Interface

The Intel® SCH supports the Intel Atom processor Z5xx series subset of the Enhanced Mode Scalable Bus Protocol, and implements a low-power CMOS bus. The Intel® SCH supports a single bus agent with FSB data rates of 400 MT/s and 533 MT/s. The Intel® SCH features include:

- Intel Atom processor Z5xx series support
- CMOS frontside bus signaling for reduced power
- 400-MT/s or 533-MT/s data rate operation
- 64-Byte cache-line size
- 64-bit data bus, 32-bit address bus
- Supports one physical processor attachment with up to two logical processors
- 16 deep IOQ
- 1 deep defer queue
- FSB interrupt delivery
- Power-saving sideband control (DPWR#) for enabling/disabling processor data input sense amplifiers
- 1.05-V V_{TT} operation

1.3.2 System Memory Controller

The Intel® SCH integrates a DDR2 memory controller with a single 64-bit wide interface. Only DDR2 memory is supported. The memory controller interface is fully configurable through a set of control registers. Features of the Intel® SCH memory controller include:

- Supports 1.8-V DDR2 SDRAM, up to 2 ranks
- Supports 1.5-V DDR2 SDRAM, 1 rank only
- Supports 400 MT/s and 533 MT/s data rates
- Single 64-bit wide channel
- Single command per clock (1-N) operation
- Support for a maximum of 2GB of DRAM
- Device density support for 512Mb, 1024Mb, and 2048Mb devices
- Device widths of x16
- Aggressive power management to reduce idle power consumption
- Page closing policies to proactively close pages after idle periods
- No on-die termination (ODT) support
- Supports non-terminated and board-terminated bus topologies

1.3.3 USB Host

The Intel® SCH contains three Universal Host Controller Interface (UHCI) USB 1.1 controllers and an Enhanced Host Controller Interface (EHCI) USB 2.0 controller. Port-routing logic on the Intel® SCH determines which USB controller is used to operate a given USB port.

A total of eight USB ports are supported. All eight of these ports are capable of high-speed data transfers up to 480 MB/s, and six of the ports are also capable of full-speed and low-speed signaling. The two high-speed-only USB ports may only be used internally within the system platform.

1.3.4 USB Client

The Intel® SCH supports USB client functionality on Port 2 of the USB interface. This permits the platform to attach to a separate USB host as a peripheral mass storage volume or RNDIS device.

1.3.5 PCI Express*

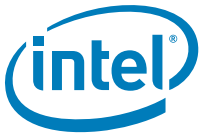
The Intel® SCH has two PCI Express root ports supporting the *PCI Express Base Specification, Revision 1.0a*. PCI Express root Ports 1–2 can be statically configured as two x1 lanes. Each root port supports 2.5 GB/s bandwidth in each direction.

An external graphics device can be used with one of the x1 PCI Express lanes/ports.

1.3.6 LPC Interface

The Intel® SCH implements an LPC interface as described in the *LPC 1.1 Specification*. The LPC bridge function of the Intel® SCH resides in PCI Device 31:Function 0.

The LPC interface has three PCI-based clock outputs that may be provided to different I/O devices, such as Firmware Hub flash memory or a legacy I/O chip. The LPC_CLKOUT signals run at one-fourth of the H_CLKINP/N frequency and support a total of six loads (two loads per clock pair) with no external buffering.



1.3.7 Parallel ATA (PATA)

The PATA Host Controller supports three types of data transfers:

- Programmed I/O (PIO): Processor is in control of the data transfer.
- Multi-word DMA (ATA-5): DMA protocol that resembles the DMA on the ISA bus. Allows transfer rates of up to 66 MB/s.
- Ultra DMA: Synchronous DMA protocol that redefines signals on the PATA cable to allow both host and target throttling of data and transfer rates up to 100 MB/s. Ultra DMA 100/66/33 are supported.

1.3.8 Intel® Graphics Media Accelerator 500 (Intel® GMA 500)

The Intel® SCH provides integrated graphics (2D and 3D) and high-definition video decode capabilities with minimal power consumption.

1.3.8.1 Graphics

The highly compact Intel Graphics Media Adapter contains an advanced shader architecture (model 3.0+) that performs pixel shading and vertex shading within a single hardware accelerator. The processing of pixels is deferred until they are determined to be visible, which minimizes access to memory and improves render performance.

1.3.8.2 Video

The Intel® SCH supports full hardware acceleration of video decode standards, such as H.264, MPEG2, MPEG4, VC1, and WMV9.

1.3.9 Display Interfaces

The Intel Graphics Media Adapter includes LVDS and Serial DVO display ports permitting simultaneous independent operation of two displays, depending on Intel® SCH component.

If external graphics is used instead of the internal graphics device, LVDS and SDVO ports will not function.

1.3.9.1 LVDS

The Intel® SCH supports a Low-Voltage Differential Signaling interface that allows the Intel Graphics Media Adapter to communicate directly to an on-board flat-panel display. The LVDS interface supports pixel color depths of 18 and 24 bits.

1.3.9.2 Serial DVO (SDVO) Display

The Intel® SCH has a digital display channel capable of driving SDVO adapters that provide interfaces to a variety of external display technologies (e.g., DVI, TV-Out, analog CRT).

SDVO lane reversal is not supported.

1.3.10 Secure Digital I/O (SDIO)/Multimedia Card (MMC) Controller

The Intel® SCH contains three SDIO/MMC expansion ports used to communicate with a variety of internal or external SDIO and MMC devices. Each port supports SDIO Revision 1.1 and MMC Revision 4.1 and is backward-compatible with previous interface specifications.

1.3.11 SMBus Host Controller

The Intel® SCH contains an SMBus host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I^2C devices.

The Intel® SCH SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). See the *System Management Bus (SMBus) Specification,* Version 1.0.

1.3.12 Intel® High Definition Audio (Intel® HD Audio) Controller

The *Intel® High Definition Audio Specification* defines a digital interface that can be used to attach different types of codecs (such as audio and modem codecs). The Intel HD Audio controller supports up to four audio streams, two in and two out.

With the support of multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 kHz, the Intel HD Audio controller provides audio quality that can deliver consumer electronic (CE) levels of audio experience. On the input side, the Intel® SCH adds support for an array of microphones.

The Intel HD Audio controller uses a set of DMA engines to effectively manage the link bandwidth and support simultaneous independent streams on the link. The capability enables new exciting usage models with Intel HD Audio (e.g., listening to music while playing a multi-player game on the Internet.) The Intel HD Audio controller also supports isochronous data transfers allowing glitch-free audio to the system.

1.3.13 General Purpose I/O (GPIO)

The Intel® SCH contains a total of 14 GPIO pins. Ten GPIOs are powered by the core power rail and are turned off during sleep modes (S3 and higher). The remaining four GPIOs are powered by the Intel® SCH suspend well power supply. These GPIOs remain active during S3. The suspend well GPIOs can be used to wake the system from the Suspend-to-RAM state.

The GPIOs are not 5-V tolerant.

1.3.14 Power Management

The Intel® SCH contains a mechanism to allow flexible configuration of various device maintenance routines as well as power management functions including enhanced clock control and low-power state transitions (e.g., Suspend-to-RAM and Suspend-to-Disk). A hardware-based thermal management circuit permits software-independent entrance to low-power states. The Intel® SCH contains full support for the *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 3.0.

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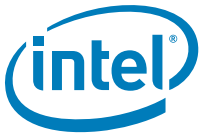


2 Signal Description

This chapter provides a detailed description of the Intel® SCH signals and boot strap definitions. The signals are arranged in functional groups according to their associated interface (see Figure 2).

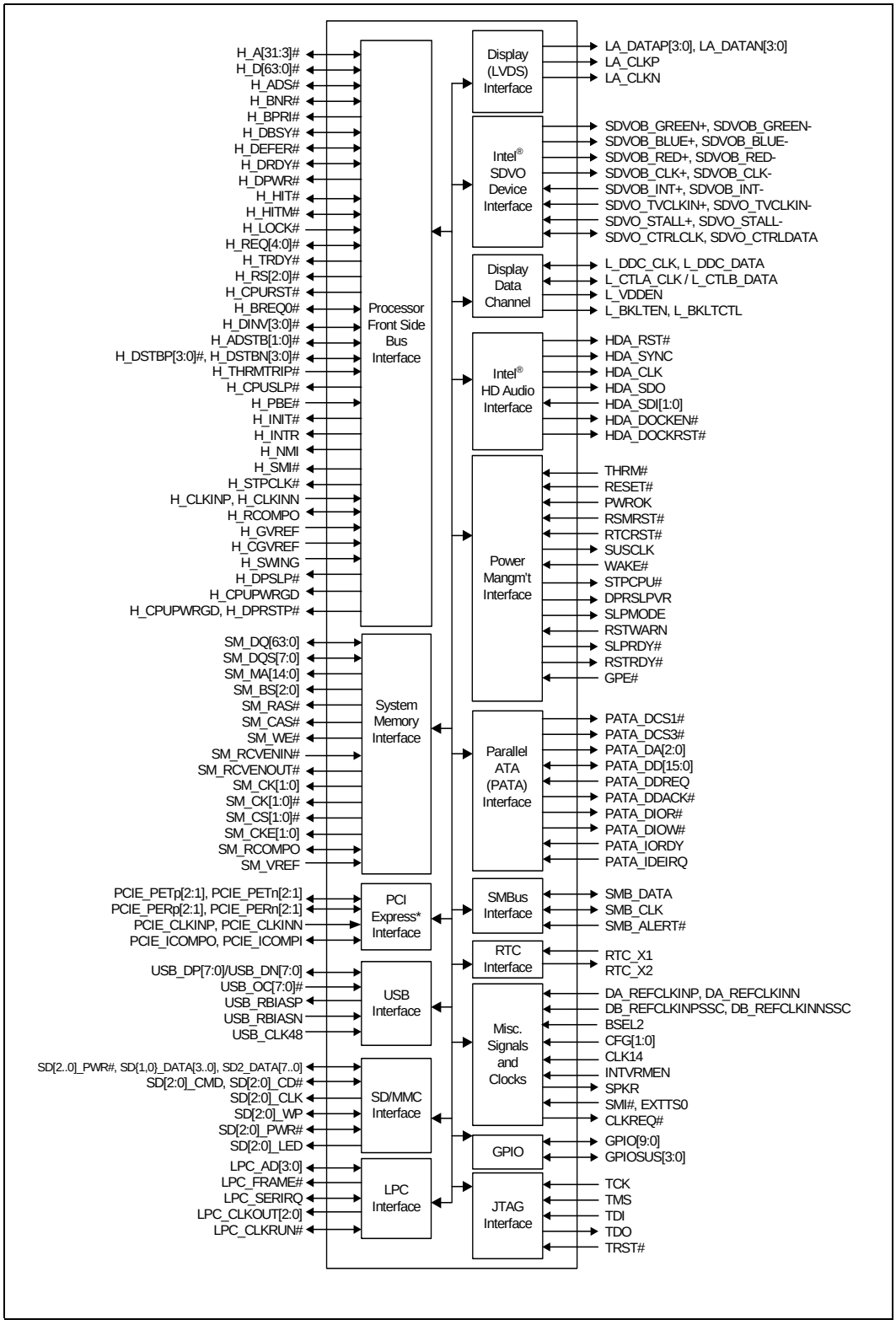
Each signal description table has the following headings:

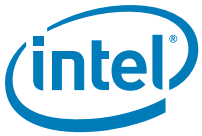
- **Signal**: The name of the signal/pin
- **Type**: the buffer direction and type. Buffer direction can be either input, output, or I/O (bidirectional). See Table 2 for definitions of the different buffer types.
- **Power Well**: the power plane used to supply power to that signal. Choices are Core, DDR, Suspend, and RTC.
- **Description**: A brief explanation of the signal's function

Table 2. Intel® SCH Buffer Types

Buffer Type	Buffer Description
AGTL+	Assisted Gunning Transceiver Logic Plus. CMOS Open Drain interface signals that require termination. Refer to the AGTL+ I/O Specification for complete details.
CMOS, CMOS_OD	1.05-V CMOS buffer, or CMOS Open Drain
CMOS_HDA	CMOS buffers for Intel® HD Audio interface that can be configured for either 1.5-V or 3.3-V operation.
CMOS1.8	1.8-V CMOS buffer. These buffers can be configured as Stub Series Termination Logic (SSTL1.8)
CMOS3.3, CMOS3.3_OD	3.3-V CMOS buffer, or CMOS 3.3-V open drain
CMOS3.3-5	3.3-V CMOS buffer, 5-V tolerant
USB	Compliant with USB 1.1 and USB 2.0 specifications.
PCIE	PCI Express interface signals. These signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant.
SDVO	Serial-DVO differential buffers. These signals are AC coupled. These buffers are not 3.3-V tolerant.
LVDS	Low Voltage Differential Signal output buffers. These pure outputs should drive across a 100-Ω resistor at the receiver when driving.
A	Analog reference or output maybe used as a threshold voltage or for buffer compensation.

Figure 2. Signal Information Diagram

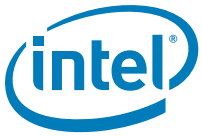




2.1 Host Interface Signals

Signal	Type	Power Well	Description
H_ADS#	I/O AGTL+	Core	**Address Strobe:** The host bus owner asserts H_ADS# to indicate the first of two cycles of a request phase.
H_BNR#	I/O CMOS	Core	**Block Next Request:** This signal is used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the processor bus pipeline depth.
H_BPRI#	O AGTL+	Core	**Priority Agent Bus Request:** The Intel® SCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the H_LOCK# signal was asserted.
H_BREQ0#	I/O CMOS	Core	**Bus Request 0#:** The Intel® SCH pulls the processor bus H_BREQ0# signal low during H_CPURST#. The signal is sampled by the processor on the active-to-inactive transition of H_CPURST#. H_BREQ0# should be tri-stated after the hold time requirement has been satisfied.
H_CPURST#	O AGTL+	Core	**CPU Reset:** H_CPURST# allows the processor to begin execution in a known state. The Intel® SCH asserts H_CPURST# and deasserts H_CPUPWRGD upon exit from its reset. H_CPURST# is deasserted 2–10 ms after H_CPUPWRGD is asserted.
H_DBSY#	I/O AGTL+	Core	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
H_DEFER#	I/O AGTL+	Core	**Defer:** The Intel® SCH will generate a deferred response as defined by the rules of the dynamic defer policy. The Intel® SCH will also use the H_DEFER# signal to indicate a processor retry response.
H_DINV[3:0]#	I/O CMOS	Core	**Dynamic Bus Inversion:** These signals are driven along with the H_D[63:0]# signals. They indicate if the associated data bus signals are inverted or not. H_DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **H_DINV[x]# — Data Bits** H_DINV3# — H_D[63:48] H_DINV2# — H_D[47:32] H_DINV1# — H_D[31:16] H_DINV0# — H_D[15:0]
H_DPWR#	O AGTL+	Core	**Data Power:** Used by Intel® SCH to indicate that a data return cycle is pending within 2 host clock cycles or more. The processor uses this signal during a read-cycle to activate the data input buffers in preparation for H_DRDY# and the related data.
H_DRDY#	I/O AGTL+	Core	**Data Ready:** This signal is asserted for each cycle that data is transferred.

Signal	Type	Power Well	Description
H_A[31:3]#	I/O CMOS	Core	**Host Address Bus:** H_A[31:3]# connect to the processor address bus. During processor cycles, H_A[31:3]# are inputs. Note that the address bus is inverted on the processor bus.
H_ADSTB[1:0]#	I/O AGTL+	Core	**Host Address Strobe:** The source synchronous strobes are used to transfer H_A[31:3]# and H_REQ[4:0]# at the 2x transfer rate. H_ADSTB0# maps to H_A[16:3]#, H_REQ[4:0]# H_ADSTB1# maps to H_A[31:17]#
H_D[63:0]#	I/O CMOS	Core	**Host Data:** These signals are connected to the processor data bus. Note that the data signals are inverted on the processor bus.
H_DSTBP[3:0]# H_DSTBN[3:0]#	I/O AGTL+	Core	**Host Data Strobes:** The source synchronous strobes used to transfer H_D[63:0]# and H_DINV[3:0]# at the 4x transfer rate. **Strobe** — **Data Bits** H_DSTB[P/N]3# — H_D[63:48]#, H_DINV3# H_DSTB[P/N]2# — H_D[47:32]#, H_DINV2# H_DSTB[P/N]1# — H_D[31:16]#, H_DINV1# H_DSTB[P/N]0# — H_D[15:0]#, H_DINV0#
H_HIT#	I/O CMOS	Core	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with H_HITM# by the target to extend the snoop window.
H_HITM#	I/O CMOS	Core	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. This signal is also driven in conjunction with H_HIT# to extend the snoop window.
H_LOCK#	I CMOS	Core	**Host Lock:** All processor bus cycles sampled with the assertion of H_LOCK# and H_ADS#, until the negation of H_LOCK# must be atomic.
H_REQ[4:0]#	I/O CMOS	Core	**Host Request Command:** These signals are asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. The transactions supported by the Intel® SCH are defined in the Host Interface functional description section of this document.
H_TRDY#	O AGTL+	Core	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.

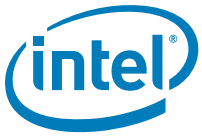


Signal	Type	Power Well	Description
H_RS[2:0]#	O AGTL+	Core	**Response Signals:** These signals indicate the type of response as shown below: 000 = Idle State 001 = Retry Response 010 = Deferred Response 011 = Reserved (not driven by Intel® SCH) 100 = Hard Failure (not driven by Intel® SCH) 101 = No data response 110 = Implicit Writeback 111 = Normal data response
H_THRMTRIP#	I CMOS	Core	**Thermal Trip:** When low, this signal indicates that a thermal trip from the processor occurred, and corrective action will be taken.
H_CPUSLP#	O CMOS	Core	**CPU SLP:** This signal puts the processor into a state that saves power vs. the Stop-Grant state. However, during that time, no snoops occur. It will go active for all other sleep states.
H_PBE#	I CMOS	Core	**Pending Break Event:** This signal can be used in some states for notification by the processor of pending interrupt events.
H_INIT#	O CMOS _OD	Core	**Initialization:** The Intel® SCH can be configured to support a special meaning to the processor during H_CPURST# deassertion. H_INIT# functionality for resetting the processor is not supported. This signal requires a board-level pull-up.
H_INTR	O CMOS	Core	**Processor Interrupt:** H_INTR is asserted by the Intel® SCH to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output normally driven low.
H_NMI	O CMOS	Core	**Non-Maskable Interrupt:** The H_NMI is used to force a non-maskable interrupt to the processor. The processor detects the rising edge of H_NMI. A non-maskable interrupt is reset by setting the corresponding NMI source enable/ disable bit in the NMI Status and Control Register.
H_SMI#	O CMOS	Core	**System Management Interrupt:** The H_SMI# is an output synchronous to LPC clock that is asserted by the Intel® SCH in response to one of many enabled hardware or software events.
H_STPCLK#	O CMOS	Core	**Stop Clock Request:** H_STPCLK# is an active-low output synchronous to LPC clock that is asserted by Intel® SCH in response to one of many hardware or software events. When the processor samples H_STPCLK# asserted, it responds by stopping its internal clock.

Signal	Type	Power Well	Description
H_DPSLP#	O CMOS	Core	**Deep Sleep:** This signal is asserted by the Intel® SCH to the processor. When the signal is low, the processor enters the Deep Sleep state by gating off the processor Core clock inside the processor. When the signal is high (default), the processor is not in the Deep Sleep state. This signal and the H_STPCLK# pin shut the clock in the processor and at the clock generator, respectively. The H_DPSLP# assertion time is wider than the H_STPCLK# assertion time in order for the processor to receive an active clock input whenever H_DPSLP# is deasserted.
H_DPRSTP#	O CMOS	Core	**Deeper Sleep:** When asserted on the platform, this signal causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. To return to the deep sleep state, H_DPRSTP# must be deasserted.
H_CPUPWRGD	O CMOS	Core	**CPU Power Good:** This signal is used for Enhanced Intel SpeedStep® Technology support. H_CPUPWRGD goes to the processor. It is kept high during the Enhanced Intel SpeedStep® Technology state transition to prevent loss of processor context.
Host Interface Reference and Compensation			
H_CLKINP H_CLKINN	I CMOS 0.8	Core	**Differential clock Input for the Host PLL:** This low-voltage differential signal pair is used for FSB transactions. The clock input also supplies a signal to the internal core and memory interface clocks.
H_RCOMPO	I/O A	Core	**Host Resistor Compensation:** This is connected to a reference resistor to dynamically calibrate the driver strengths.
H_SWING	I A	Core	**Voltage Swing Calibration**
H_GVREF H_CGVREF	I A	Core	**Voltage Reference:** These pins are for the input buffer differential amplifier to determine a high versus a low input voltage.

2.2 System Memory Signals

Signal	Type	Power Well	Description
SM_DQ[63:0]	I/O CMOS1.8	DDR	**Data Lines:** The SM_DQ[63:0] signals interface to the DRAM data bus.
SM_DQS[7:0]	I/O CMOS1.8	DDR	**Data Strobes:** These signals are the data strobes used for capturing data. Each strobe signal corresponds to 8 data bits. During writes, SM_DQSx is centered in data. During reads, SM_DQSx is edge aligned with data.
SM_MA[14:0]	O CMOS1.8	DDR	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.



Signal	Type	Power Well	Description
SM_BS[2:0]	O CMOS1.8	DDR	**Bank Select (Bank Address):** These signals define which banks are selected within each SDRAM row. Bank select and memory address signals combine to address every possible location within an SDRAM device.
SM_RAS#	O CMOS1.8	DDR	**Row Address Strobe:** SM_RAS# is used to signify the presence of the row address on SM_MA to the DRAM device being selected.
SM_CAS#	O CMOS1.8	DDR	**Column Address Strobe:** SM_CAS# is used to signify the presence of the column address on SM_MA to the DRAM device being selected.
SM_WE#	O CMOS1.8	DDR	**Write Enable:** SM_WE# tells the DRAM memory that it is performing a write operation on the bus.
SM_RCVENIN#	I CMOS1.8	DDR	**Receive Enable In:** This signal connects to SM_SRCVENOUT# internally. This input (driven from SM_SRCVENOUT#) enables the DQS input buffers during reads.
SM_RCVENOUT#	O CMOS1.8	DDR	**Receive Enable Out:** This signal connects to SM_SRCVENIN# internally. It is part of the feedback used to enable the DQS input buffers during reads.
SM_CK[1:0] SM_CK[1:0]#	O CMOS1.8	DDR	**Differential DDR Clock:** SM_CKx and SM_CKx# pairs are differential clock outputs. The crossing of the positive edge of SM_CKx and the negative edge of SM_CKx# is used to sample the address and control signals on the DRAM.
SM_CS[1:0]#	O CMOS1.8	DDR	**Chip Select:** These signals select particular DRAM components during the active state. There is one SM_CSx# for each DRAM rank, toggled on the positive edge of SM_CKx.
SM_CKE[1:0]	O CMOS1.8	DDR	**Clock Enable:** SM_CKEx is used to initialize DRAM during power-up and to place all DRAM rows into and out of self-refresh during the S3 Suspend-to-RAM low power state. SM_CKEx is also used to dynamically power down inactive DRAM rows. There is one SM_CKEx per SDRAM row, toggled on the positive edge of SM_CKx.
SM_VREF	I A	DDR	**Input Buffer VREF:** This signal is for the input buffer differential amplifier to determine a high versus a low input voltage.
SM_RCOMPO	I/O A	DDR	**Resistor Compensation Output Pin:** This pin is connected to a reference resistor to dynamically calibrate the driver strengths.

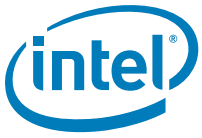
2.3 Integrated Display Interfaces

2.3.1 LVDS Signals

Signal	Type	Power Well	Description
LA_DATAP[3:0] LA_DATAN[3:0]	O LVDS	Core	**Channel A Differential Data Output:** Differential signal pair.
LA_CLKP LA_CLKN	O LVDS	Core	**Channel A Differential Clock Output:** Differential signal pair.

2.3.2 Serial Digital Video Output (SDVO) Signals

Signal Name	Type	Power Well	Description
SDVOB_RED+ SDVOB_RED-	O PCIE	Core	**Serial Digital Video Channel B Red:** SDVOB_RED[±] is a differential data pair that provides red pixel data for the SDVOB channel during Active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK[±] signal pair.
SDVOB_GREEN+ SDVOB_GREEN-	O PCIE	Core	**Serial Digital Video Channel B Green:** SDVOB_GREEN[±] is a differential data pair that provides green pixel data for the SDVOB channel during Active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK[±] signal pair.
SDVOB_BLUE+ SDVOB_BLUE-	O PCIE	Core	**Serial Digital Video Channel B Blue:** SDVOB_BLUE[±] is a differential data pair that provides blue pixel data for the SDVOB channel during Active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVOB_CLK[±] signal pair.
SDVOB_CLK+ SDVOB_CLK-	O PCIE	Core	**Serial Digital Video Channel B Clock:** This differential clock signal pair is generated by the Intel® SCH internal PLL and runs between 100 MHz and 200 MHz. If TV-out mode is used, the SDVO_TVCLKIN[±] clock input is used as the frequency reference for the PLL. The SDVOB_CLK[±] output pair is then driven back to the SDVO device.
SDVOB_INT+ SDVOB_INT-	I PCIE	Core	**Serial Digital Video Input Interrupt:** Differential input pair that may be used as an interrupt notification from the SDVO device to the Intel® SCH. This signal pair can be used to monitor hot plug attach/detach notifications for a monitor driven by an SDVO device.



Signal Name	Type	Power Well	Description
SDVO_TVCLKIN+ SDVO_TVCLKIN-	I PCIE	Core	**Serial Digital Video TV-OUT Synchronization Clock:** Differential clock pair that is driven by the SDVO device to the Intel® SCH. If SDVO_TVCLKIN[±] is used, it becomes the frequency reference for the Intel® SCH dot clock PLL, but will be driven back to the SDVO device through the SDVOB_CLK[±] differential pair. This signal pair has an operating range of 100–200 MHz, so if the desired display frequency is less than 100 MHz, the SDVO device must apply a multiplier to get the SDVO_TVCLKIN[±] frequency into the 100- to 200-MHz range.
SDVO_STALL+ SDVO_STALL-	I PCIE	Core	**Serial Digital Video Field Stall:** Differential input pair that allows a scaling SDVO device to stall the Intel® SCH pixel pipeline.
SDVO_CTRLCLK	I/O CMOS3.3 _OD	Core	**SDVO Control Clock:** Single-ended control clock line from the Intel® SCH to the SDVO device. Similar to I^2C clock functionality, but may run at faster frequencies. SDVO_CTRLCLK is used in conjunction with SDVO_CTRLDATA to transfer device config, PROM, and monitor DDC information. This interface directly connects the Intel® SCH to the SDVO device.
SDVO_CTRLDATA	I/O CMOS3.3 _OD	Core	**SDVO Control Data:** SDVO_CTRLDATA is used in conjunction with SDVO_CTRLCLK to transfer device config, PROM, and monitor DDC information. This interface directly connects the Intel® SCH to the SDVO device.

2.3.3 Display Data Channel (DDC) and GMBus Support

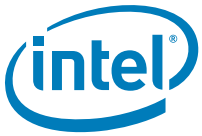
Signal Name	Type	Power Well	Description
L_DDC_CLK	I/O CMOS3.3 _OD	Core	**Display Data Channel Clock:** I^2C-based control signal (Clock) for EDID control.
L_DDC_DATA	I/O CMOS3.3 _OD	Core	**Display Data Channel Data:** I^2C-based control signal (Data) for EDID control.
L_CTLA_CLK	I/O CMOS3.3 _OD	Core	**Control A Clock**: This signal can be used to control external clock chip for SSC - optional.
L_CTLB_DATA	I/O CMOS3.3 _OD	Core	**Control B Data**: This signal can be used to control external clock chip for SSC – optional.
L_VDDEN	O CMOS3.3	Core	**LCD Power Enable:** Panel power enable control.
L_BKLTEN	O CMOS3.3	Core	**LCD Backlight Enable**: Panel backlight enable control.
L_BKLTCTL	O CMOS3.3	Core	**LCD Backlight Control:** This signal allows control of LCD brightness.

2.4 Universal Serial Bus (USB) Signals

Signal Name	Type	Power Well	Description
USB_DP[5:0]/ USB_DN[5:0]	I/O USB	Sus	**USB Port 5:0 Differentials: Bus Data/Address/ Command Bus:** These differential pairs are used to transmit data/address/command signals for Ports 0 through 5. These ports can be routed to either the EHCI controller or one of the three UHCI controllers and are capable of running at either high-, full-, or low-speed.
USB_DP[7:6]/ USB_DN[7:6]	I/O USB	Sus	**USB Port 7:6 Differentials: Bus Data/Address/ Command Bus:** These differential pairs are used to transmit data/address/command signals for Ports 6 and 7. These ports are routed only to the EHCI controller and should be used ONLY for in-system USB 2.0 devices.
USB_RBIASP	O A	Sus	**Resistor Bias P:** This pin is an analog connection point for an external resistor. This signal is used to set transmit currents and internal load resistors.
USB_RBIASN	I A	Sus	**Resistor Bias N:** This pin is an analog connection point for an external resistor. This signal is used to set transmit currents and internal load resistors.
USB_CLK48	I USB	Sus	**48-MHz Clock:** This optional clock is used to run the USB controller. By default, the Intel® SCH uses DA_REFCLKIN to clock the USB logic.
USB_OC[7:0]#	I CMOS3.3	Sus	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. **NOTE:** USB_OC[7:0]# are not 5-V tolerant.
USBCC/ GPIOSUS3	I/O CMOS3.3	Sus	**USB Client Connect:** This signal, on GPIOSUS3, may be used in systems where USB port 2 is configured for client mode. This indicates connection to an external USB host has been established. **NOTE:** If USB Client support is enabled, then this signal is dedicated for USB Client Connect.

2.5 PCI Express* Signals

Signal Name	Type	Power Well	Description
PCIE_PETp[2:1] PCIE_PETn[2:1]	O PCIE	Core	**PCI Express Transmit:** PCIE_PETp[2:1] are PCI Express Ports 2:1 transmit pair (P and N) signals.
PCIE_PERp[2:1] PCIE_PERn[2:1]	I PCIE	Core	**PCI Express Receive:** PCIE_PERp[2:1] PCI Express Ports 2:1 receive pair (P and N) signals.
PCIE_CLKINP PCIE_CLKINN	I PCIE	Core	**PCI Express Input Clock:** 100-MHz differential clock signals.
PCIE_ICOMPO	I/O A	Core	**PCI Express Compensation Pin:** Output compensation for both current and resistance. Also for LVDS and SDVO interfaces.
PCIE_ICOMPI	I/O A	Core	**PCI Express Compensation Pin:** Input compensation for current. Also for LVDS and SDVO interfaces.

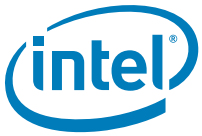


2.6 Secure Digital I/O (SDIO)/MultiMedia Card (MMC) Signals

Signal Name	Type	Power Well	Description
SD0_DATA[3:0] SD1_DATA[3:0] SD2_DATA[7:0]	I/O CMOS3.3	Core	**SDIO Controller 0/1/2 Data:** These signals operate in push-pull mode. The SD card includes internal pull-up resistors for all data lines. By default, after power-up, only SDn_DATA0 is used for data transfer. Wider data bus widths can be configured for data transfer. **NOTE:** Port 0 and 1 are 4 bits wide while ports 2 is 8 bits wide.
SD0_CMD SD1_CMD SD2_CMD	I/O CMOS3.3	Core	**SDIO Controller 0/1/2 Command:** This signal is used for card initialization and transfer of commands. It has two operating modes: open-drain for initialization mode, and push-pull for fast command transfer.
SD0_CLK SD1_CLK SD2_CLK	O CMOS3.3	Core	**SDIO Controller 0/1/2 Clock:** With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal is generated by the Intel® SCH at a maximum frequency of: 24 MHz for SD and SDIO. 48 MHz for MMC.
SD0_WP SD1_WP SD2_WP	I CMOS3.3	Core	**SDIO Controller 0/1/2 Write Protect**: These signals denote the state of the write-protect tab on SD cards.
SD0_CD# SD1_CD# SD2_CD#	I CMOS3.3	Core	**SDIO Controller 0/1/2 Card Detect:** These signals indicates when a card is present in an external slot.
SD0_LED SD1_LED SD2_LED	O CMOS3.3	Core	**SDIO Controller 0/1/2 LED:** These signals can be used to drive an external LED and indicate when transfers are occurring on the bus.
SD0_PWR# SD1_PWR# SD2_PWR#	I/O CMOS3.3	Core	**SDIO/MMC Power Enable:** These pins can be used to enable the power being supplied to an SDIO/MMC device.

2.7 Parallel ATA (PATA) Signals

Signal Name	Type	Power Well	Description
PATA_DD[15:0]	I/O CMOS3.3-5	Core	**Device Data:** These signals drive the corresponding signals on the PATA connector. There is an internal 13.3-kΩ pull-down on PATA_DD7.
PATA_DA[2:0]	O CMOS3.3-5	Core	**Device Address:** These output signals are connected to the corresponding signals on the PATA connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.
PATA_DIOR#	O CMOS3.3-5	Core	**Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the PATA device that it may drive data onto the DD lines. Data is latched by the Intel® SCH on the deassertion edge of PATA_DIOR#. The PATA device is selected either by the ATA register file chip selects (PATA_DCS1# or PATA_DCS3#) and the PATA_DA lines, or the PATA DMA acknowledge (PATA_DDAK#).
PATA_DIOW#	O CMOS3.3-5	Core	**Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the PATA device that it may latch data from the PATA_DD lines. Data is latched by the PATA device on the deassertion edge of PATA_DIOW#. The PATA device is selected either by the ATA register file chip selects (PATA_DCS1# or PATA_DCS3#) and the PATA_DA lines, or the PATA DMA acknowledge (PATA_DDAK#).
PATA_DDACK#	O CMOS3.3-5	Core	**Device DMA Acknowledge:** This signal directly drives the DAK# signals on the PATA connectors. Each is asserted by the Intel® SCH to indicate to PATA DMA slave devices that a given data transfer cycle (assertion of PATA_DIOR# or PATA_DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master PATA function and are not associated with any AT-compatible DMA channel.
PATA_DCS3#	O CMOS3.3-5	Core	**Device Chip Select for 300 Range:** This chip select is for the ATA control register block. This signal is connected to the corresponding signal on the connector.
PATA_DCS1#	O CMOS3.3-5	Core	**Device Chip Selects for 100 Range:** This chip select is for the ATA command register block. This signal is connected to the corresponding signal on the PATA connector.
PATA_DDREQ	I CMOS3.3-5	Core	**Device DMA Request:** This input signal is directly driven from the DRQ signals on the PATA connector. It is asserted by the PATA device to request a data transfer, and used in conjunction with the PCI bus master PATA function and are not associated with any AT-compatible DMA channel. There is an internal 13.3 kΩ pull-down on this pin.
PATA_IORDY	I CMOS3.3-5	Core	**I/O Channel Ready (PIO):** This signal will keep the strobe active (PATA_DIOR# on reads, PATA_DIOW# on writes) longer than the minimum width. It adds waitstates to PIO transfers.



Signal Name	Type	Power Well	Description
PATA_IDEIRQ	I CMOS3.3-5	Core	**IDE Interrupt**: Input from the PATA device indicating request for an interrupt. Tied internally to IRQ14.

2.8 Intel HD Audio Interface

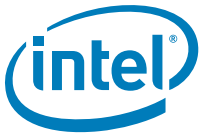
Signal Name	Type	Power Well	Description
HDA_RST#	O CMOS_HDA	Core	**Intel® HD Audio Reset:** This signal is the reset to external Codecs
HDA_SYNC	O CMOS_HDA	Core	**Intel HD Audio Sync:** This signal is an 48-kHz fixed rate sample sync to the Codec(s). It is also used to encode the stream number.
HDA_CLK	O CMOS_HDA	Core	**Intel HD Audio Clock (Output):** This signal is a 24.000-MHz serial data clock generated by the Intel HD Audio controller. This signal contains an integrated pull-down resistor so that it does not float when an Intel HD Audio CODEC (or no CODEC) is connected.
HDA_SDO	O CMOS_HDA	Core	**Intel HD Audio Serial Data Out:** This signal is a serial TDM data output to the Codec(s). The serial output is double-pumped for a bit rate of 48 MB/s for HD Audio.
HDA_SDI[1:0]	I CMOS_HDA	Core	**Intel HD Audio Serial Data In:** These serial inputs are single-pumped for a bit rate of 24 MB/s. They have integrated pull-down resistors that are always enabled.
HDA_DOCKEN#	O CMOS_HDA	Core	**Intel HD Audio Dock Enable:** This active low signal controls the external Intel HD Audio docking isolation logic. When deasserted, the external docking switch is in isolate mode. When asserted, the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Intel SCH signals.
HDA_DOCKRST#	O CMOS_HDA	Core	**Intel HD Audio Dock Reset:** This signal is a dedicated reset signal for the codec(s) in the docking station. It works similar to, but independent of, the normal HDA_RST# signal.

2.9 LPC Interface

Signal Name	Type	Power Well	Description
LPC_AD[3:0]	I/O CMOS3.3	Core	**LPC Address/Data:** Multiplexed Command, Address, Data
LPC_FRAME#	O CMOS3.3	Core	**LPC Frame:** This signal indicates the start of an LPC/FHW cycle.
LPC_SERIRQ	I/O CMOS3.3	Core	**Serial Interrupt Request:** This signal conveys the serial interrupt protocol.
LPC_CLKRUN#	I/O CMOS3.3	Core	**Clock Run:** This signal gates the operation of the LPC_CLKOUTx. Once an interrupt sequence has started, LPC_CLKRUN# should remain asserted to allow the LPC_CLKOUTx to run.
LPC_CLKOUT[2:0]	O CMOS3.3	Core	**LPC Clock:** These signals are the clocks driven by the Intel® SCH to LPC devices. Each clock can support up to two loads. **NOTE:** The primary boot device like FWH and SPI (behind SMC) should be connected to LPC_CLKOUT[0]

2.10 SMBus Interface

Signal Name	Type	Power Well	Description
SMB_DATA	I/O CMOS3.3_OD	Core	**SMBus Data:** This signal is the SMBus data pin. An external pull-up resistor is required.
SMB_CLK	I/O CMOS3.3_OD	Core	**SMBus Clock:** This signal is the SMBus clock pin. An external pull-up resistor is required.
SMB_ALERT#	I CMOS3.3_OD	Core	**SMBus Alert:** This signal can be used to generate an SMI#.



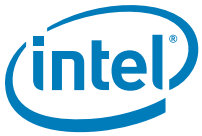
2.11 Power Management Interface

Signal Name	Type	Power Well	Description
THRM#	I CMOS3.3	Core	**Thermal Alarm:** This signal is an active low signal generated by external hardware to generate an SMI or SCI.
RESET#	I CMOS3.3	DDR	**System Reset:** This signal forces a reset after being de-bounced. This signal is powered by V_{CCSM}.
PWROK	I CMOS3.3	RTC	**Power OK:** When asserted, PWROK is an indication to the Intel® SCH that core power is stable. PWROK can be driven asynchronously.
RSMRST#	I CMOS3.3	RTC	**Resume Well Reset:** This signal is used for resetting the resume well. An external RC circuit is required to ensure that the resume well power is valid prior to RSMRST# going high.
RTCRST#	I CMOS3.3	RTC	**RTC Well Reset:** This signal is normally held high (to V_{CC_RTC}), but can be driven low on the motherboard to test the RTC power well and reset some bits in the RTC well registers that are otherwise not reset by SLPMODE or RSMRST#. An external RC circuit on the RTCRST# signal creates a time delay such that RTCRST# will go high some time after the battery voltage is valid. This allows the Intel® SCH to detect when a new battery has been installed. The RTCRST# input must always be high when other non-RTC power planes are on. NOTE: Unlike many previous products, the Intel® SCH does not use RTCRST# to clear CMOS. RTCRST# does not set a bit which BIOS can then read as a directive to clear CMOS. This signal is in the RTC power well.
SUSCLK	O CMOS3.3	Sus	**Suspend Clock:** This signal is an output of the RTC generator circuit (32.768 kHz). SUSCLK can have a duty cycle from 30% to 70%.
WAKE#	I CMOS3.3	Sus	**PCI Express* Wake Event:** This signal indicates a PCI Express port wants to wake the system.
STPCPU#	O CMOS3.3	Core	**Stop CPU Clock:** This signal is used to support the C3 state. Asserting this signal halts the clocks to the processor by controlling the enable of the clock chip.
DPRSLPVR	O CMOS3.3	Core	**Deeper Sleep Voltage Regulator:** This signal is asserted by the Intel® SCH to the processors voltage regulator. When the signal is high, the voltage regulator outputs the lower “Deeper Sleep” voltage. When the signal is low (default), the voltage regulator outputs the higher “Normal” voltage. This signal is in the core I/O plane and has a standard CMOS output (not open drain).
SLPIOVR#	O CMOS3.3	Core	**Sleep I/O Voltage Regulator Disable:** The SLPIOVR# can be connected to an external VR and be used to control power supplied to the processors I/O rail in the C6 state.

Signal Name	Type	Power Well	Description
SLPMODE	O CMOS3.3	Sus	**Sleep Mode:** SLPMODE determines which sleep state is entered. When SLPMODE is high, S3 will be chosen. When SLPMODE is low, S4/S5 will be the selected sleep mode.
RSTWARN	I CMOS3.3	Sus	**Reset Warning**: Asserting the RSTWARN signal tells the Intel® SCH to enter a sleep state or begin to power down. A system management controller might do so after an external event, such as pressing of the power button or occurrence of a thermal event.
SLPRDY#	O CMOS3.3	Sus	**Sleep Ready**: The Intel® SCH will drive the SLPRDY# signal low to indicate to the system management controller that the Intel® SCH is awake and able to placed into a sleep state. deassertion of this signal indicates that a wake is being requested from a system device.
RSTRDY#	O CMOS3.3	Sus	**Reset Ready**: Assertion of the RSTRDY# signal indicates to the system management controller that it is ready to be placed into a low power state. During a transition from S0 to S3/4/5 sleep states, the Intel® SCH asserts RSTRDY# and CPURST# after detecting assertion of the RSTWARN signal from the external system management controller.
GPE#	I CMOS3.3 _OD	Sus	**General Purpose Event**: GPE# is asserted by an external device (typically, the system management controller) to log an event in the Intel® SCH ACPI space and cause an SCI (if enabled).

2.12 Real Time Clock Interface

Signal Name	Type	Power Well	Description
RTC_X1	Special A	RTC	**Crystal Input 1:** This signal is connected to the 32.768-kHz crystal. If no external crystal is used, then RTC_X1 can be driven with the desired clock rate.
RTC_X2	Special A	RTC	**Crystal Output 2:** This signal is connected to the 32.768-kHz crystal. If no external crystal is used, then RTC_X2 should be left floating.



2.13 JTAG Interface

The JTAG interface is accessible only after PWROK is asserted.

Signal Name	Type	Power Well	Description
TCK	I CMOS	Sus	**JTAG Test Clock:** TCK is a clock input used to drive Test Access Port (TAP) state machine during test and debugging. This input may change asynchronous to the host clock.
TDI	I CMOS	Sus	**JTAG Test Data In:** TDI is used to serially shift data and instructions into the TAP.
TDO	O CMOS_OD	Sus	**JTAG Test Data Out:** TDO is used to serially shift data out of the device.
TMS	I CMOS	Sus	**Test Mode Select:** This signal is used to control the state of the TAP controller.
TRST#	I CMOS	Sus	**Test Reset:** This signal resets the controller logic. It should be pulled down unless TCK is active.

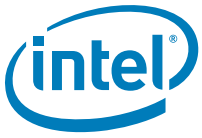
2.14 Miscellaneous Signals and Clocks

Signal Name	Type	Power Well	Description
DA_REFCLKINP/ DA_REFCLKINN	I	Core	**Display PLLA CLK Differential Pair:** 96 MHz, no SSC support.
DB_REFCLKINPSSC/ DB_REFCLKINNSSC	I	Core	**Display PLLB CLK Differential Pair:** display PLL differential clock pair for super SSC.
CLKREQ#	O CMOS3.3 _OD	Core	**Clock Required**: The Intel® SCH will not de-assert CLKREQ# and will not thus enable a power management mode to the clock chip.
CLK14	I CMOS3.3	Core	**Oscillator Clock:** This signal is used for 8254 timers and HPET. It runs at 14.31818 MHz. This clock stops (and should be low) during S3, S4, and S5 states. CLK14 must be accurate to within 500 ppm over 100 µs (and longer periods) to meet HPET accuracy requirements.
INTVRMEN	I CMOS3.3	RTC	**Internal VRM Enable:** This signal is used to enable or disable the integrated 1.5-V Voltage Regulators for the Suspend and Auxiliary wells on the Intel® SCH. When connected to V_{SS}, the VRMs are disabled; when connected to the RTC power well, the VRMs are enabled. This signal is in the RTC well. It is not latched and must remain valid for the VRMs to behave properly.
SPKR	O CMOS3.3	Core	**Speaker:** The SPKR signal is the output of counter 2 and is internally ANDed with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon SLPMODE, its output state is 0.

Signal Name	Type	Power Well	Description
SMI#	I CMOS3.3	Core	**System Management Interrupt:** This signal is generated by the external system management controller.
EXTTS0#	I CMOS3.3	Core	**External Thermal Sensor 0 Event**
EXTTS1#/GPIO9	I CMOS3.3	Core	**External Thermal Sensor 1 Event:** EXTTS1# is multiplexed with GPIO9
BSEL2	I CMOS	Core	**Host Bus Speed Select:** At the deassertion of RESET#, the value sampled on BSEL2 determines the expected frequency of the bus. Refer to Table 3 for more details.
CFG[1:0]	I CMOS	Core	**Configuration:** Strap pins used to configure the graphics/display clock frequency. Refer to Table 3 for more details.

2.15 General Purpose I/O

Signal Name	Type	Power Well	Description
GPIO9/EXTTS1#	I/O CMOS3.3	Core	**General Purpose I/O #9/External Thermal Sensor 1:** This GPIO can function as a second external thermal sensor input.
GPIO8/ PROCHOT#	I/O CMOS3.3 / OD	Core	**General Purpose I/O #8/Processor Hot:** Defaults to a GPIO. As PROCHOT#, this signal can function as an Open-Drain output to the processor or SMC to signify a processor thermal event.
GPIO[6:0]	I/O CMOS3.3	Core	**General Purpose I/O:** These signals are powered off of the core well power plane within the Intel® SCH.
GPIOSUS3/ USBCC	I/O CMOS3.3	Sus	**Resume Well General Purpose I/O #3/USB Client Connect:** This GPIO can function as an input signifying connection to an external USB host. **NOTE:** If a USB Client is enabled in the system, then GPIOSUS3 cannot be used as a general purpose I/O.
GPIOSUS[2:0]	I/O CMOS3.3	Sus	**General Purpose I/O:** These signals are powered from the suspend well power plane within the Intel® SCH. They are accessible during the S3 sleep state.



2.16 Power and Ground Signals

Interface	Ball Name	Nominal Voltage	Description
Common	VCC	1.05	Core supply
	VSS VSS_NCTF[1]	0	Ground
Host	VTT	1.05	Used for FSB input and output devices
	VCCAHPLL	1.5	Analog Power Supply
	VCCDHPLL	1.5	Digital Power Supply
DDR2	VCCSM	1.8 1.5	Driver and Rx supply Configurable for 1.8-V/1.5-V operation
SDVO/ PCIE/ LVDS	VCCLVDS	1.5	Dedicated LVDS supply (must be supplied even if the SDVO only interface is used).
	VCCSDVO	1.5	Dedicated SDVO supply (must be supplied if the interface is used. If SDVO is not used, this supply is not needed for the Intel® SCH).
	VCCPCIE	1.5	Dedicated PCIe* analog/digital supply
	VCCAPCIEPLL	1.5	PCIe PLL
	VCCAPCIEBG	3.3	Band Gap (needs to be enabled for PCIe, SDVO or LVDS)
	VSSAPCIEBG	0	PCIe Band Gap VSS
Display PLL	VCCADPLLA	1.5	Display PLL A power supply (digital and analog) Must be powered even if DPLLA is not used.
	VCCADPLLB	1.5	Display PLL B power supply (digital and analog) Must be powered even if DPLLB is not used.
Intel High Definition Audio	VCC15	1.5	Used for I/O digital logic
	VCCHDA	3.3/1.5	Configurable for 3.3-V or 1.5-V operation
	VCC33	3.3	Used for some internal 3.3-V circuits
SDIO/MMC/ CMOS/LPC/ PATA	VCC15	1.5	Used for I/O digital logic
	VCC33	3.3	Used for I/O analog driver
	VCC5REF	5	Used for 5-V tolerance on core group inputs
USB	VCCAUSBPLL	1.5	USB PLL Supply. Must be powered even if USB is not used
	VCC15USB	1.5	Power for USB Logic and Analogs.
	VCCP33USBSUS	3.3	USB 3.3-V Supply
	VCCAUSBBGSUS	3.3	USB Band Gap
	VSSAUSBBGSUS	0	USB Band Gap V_{SS}
	VCC5REFSUS	5	5-V Supply in Suspend Power Well
CMOS Suspend	VCC33SUS	3.3	3.3-V Suspend Power Supply
	VCC33RTC	3.3	Used for Real Time Clock

NOTE:

1. NCTF (Non-Critical to Function) signals have been designed into the package footprint to enhance the Solder Joint Reliability of our products. The NCTF signals have been designed to absorb some of the stress introduced by the Characteristic Thermal Expansion (CTE)

mismatch between the die-to-package interface. If cracking between the die-to-package interface occurs, product performance or reliability is not affected.

2.17 Functional Straps

The following signals are used to configure certain Intel® SCH features. All strap signals are in the core power well. They are sampled at the rising edge of PWROK and then revert later to their normal usage. Straps should be driven to the desired state at least four LPC (PCI) clocks prior to the rising edge of PWROK.

Table 3. Functional Strap Definitions

<table>
<tr><th>Signal Name</th><th>Strap Function</th><th>Comments</th></tr>
<tr><td>BSEL2
CFG[1:0]</td><td>FSB/DDR Frequency Select
Graphics Frequency Select</td><td>BSEL2: Selects the frequency of the host interface and DDR interface. Normal system configuration will have this signal connected to the processor's BSEL2 signal and will not require external pull-up/pull-down resistors.
CFG[1:0]: Selects the frequency of the internal graphics device.
<table>
<tr><th>BSEL2</th><th>CFG1</th><th>CFG0</th><th>FSB Freq</th><th>GFX Freq</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>100 MHz</td><td>200 MHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>133 MHz</td><td>200 MHz</td></tr>
<tr><td colspan="5">All other combinations are reserved</td></tr>
</table></td></tr>
<tr><td>GPIO3
GPIO0</td><td>CMC (Chipset Microcode) Base Address</td><td>Selects the starting address that the CMC will use to start fetching code (GPIO3 is the most significant).
<table>
<tr><th>GPIO3</th><th>GPIO0</th><th>CMC Base Address</th></tr>
<tr><td>0</td><td>0</td><td>FFFB0000h</td></tr>
<tr><td>0</td><td>1</td><td>FFFC0000h</td></tr>
<tr><td>1</td><td>0</td><td>FFFD0000h (default)</td></tr>
<tr><td>1</td><td>1</td><td>FFFE0000h</td></tr>
</table></td></tr>
<tr><td>RESERVED1</td><td>LPC_CLKOUT[0] Buffer Strength</td><td>Selects the drive strength of the LPC_CLKOUT0 clock.
0 = 1 Load driver strength
1 = 2 Load driver strength</td></tr>
<tr><td>XOR_TEST</td><td>XOR Chain Enable</td><td>Enables XOR chain mode
0 = XOR mode enable
1 = XOR mode disable (default)
NOTE: XOR_TEST includes an internal pullup resistor.</td></tr>
</table>

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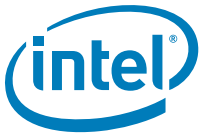


3 Pin States

This chapter describes the states of each Intel® SCH signal in and around reset. It also documents what signals have internal pull-up/pull-down/series termination resistors and their values.

3.1 Pin Reset States

Table 4. Reset State Definitions

Signal State	Description
High-Z	The Intel® SCH places this output in a high-impedance state. For I/Os, external drivers are not expected.
Don't Care	The state of the input (driven or tri-stated) does not effect the Intel® SCH. For I/O, it is assumed the output buffer is in a high-impedance state.
V_{OH}	The Intel® SCH drives this signal high
V_{OL}	The Intel® SCH drives this signal low
VOX–known	The Intel® SCH drives this signal to a level defined by internal function configuration
VOX–unknown	The Intel® SCH drives this signal, but to an indeterminate value
V_{IH}	The Intel® SCH expects/requires the signal to be driven high.
V_{IL}	The Intel® SCH expects/requires the signal to be driven low.
pull-up	This signal is pulled high by a pull-up resistor (internal or external)
pull-down	This signal is pulled low by a pull-down resistor (internal or external)
VIX-unknown	The Intel® SCH expects the signal to be driven by an external source, but the exact electrical level of that input is unknown.
Running	The clock is toggling or signal is transitioning because the function has not stopped.
Off	The power plane for this signal is powered down. The Intel® SCH does not drive outputs and inputs should not be driven to the Intel® SCH.

Table 5. Intel® SCH Reset State (Sheet 1 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
Host Interface					
H_A[31:3]#	I/O	VOH	pull-up	Off	Off
H_D[63:0]#	I/O	VOH	pull-up	Off	Off
H_ADS#	I/O	VOH	pull-up	Off	Off
H_BNR#	I/O	VOH	pull-up	Off	Off
H_BPRI#	O	VOH	pull-up	Off	Off
H_DBSY#	I/O	VOH	pull-up	Off	Off
H_DEFER#	I/O	VOH	pull-up	Off	Off
H_DRDY#	I/O	VOH	pull-up	Off	Off
H_DPWR#	O	VOH	VOL	Off	Off
H_HIT#	I/O	VOH	pull-up	Off	Off
H_HITM#	I/O	VOH	pull-up	Off	Off
H_LOCK#	I	VIH	pull-up	Off	Off
H_REQ[4:0]#	I/O	VOH	pull-up	Off	Off
H_CPUSLP#	O	VOH	VOH	Off	Off
H_TRDY#	O	VOH	pull-up	Off	Off
H_RS[2:0]#	O	VOH	pull-up	Off	Off
H_CPURST#	O	VOL	pull-up	Off	Off
H_BREQ0#	I/O	VIL	pull-up	Off	Off
H_DINV[3:0]#	I/O	VOH	pull-up	Off	Off
H_ADSTB[1:0]#	I/O	VOH	pull-up	Off	Off
H_DSTBP[3:0]#, H_DSTBN[3:0]#	I/O	VOH	pull-up	Off	Off
H_THERMTRIP	I	VIX-unknown	pull-up	Off	Off
H_PBE#	I	VIH	pull-up	Off	Off
H_INIT#	O	VOX-unknown	pull-up	Off	Off
H_INTR	O	VOL	VOL	Off	Off
H_NMI	O	VOL	VOL	Off	Off
H_SMI#	O	VOH	VOH	Off	Off
H_STPCLK#	O	VOH	VOH	Off	Off
H_CLKINP, H_CLKINN	I	Running	Running	Off	Off
H_RCOMPO	I/O-A	High-Z	High-Z	Off	Off
H_GVREF	I-A	VIX-unknown	VIX-unknown	Off	Off
H_GCVREF	I-A	VIX-unknown	VIX-unknown	Off	Off
H_SWING	I-A	VIX-unknown	VIX-unknown	Off	Off
H_DPSLP#	O	VOH	VOH	Off	Off
H_CPUPWRGD	O	VOL	VOL	Off	Off

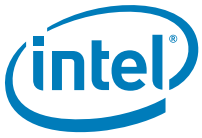


Table 5. Intel® SCH Reset State (Sheet 2 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
H_DPRSTP#	O	VOH	VOH	Off	Off
System Memory Interface					
SM_DQ[63:0]	I/O	High-Z	High-Z	Off	Off
SM_DQS[7:0]	I/O	High-Z	High-Z	Off	Off
SM_MA[14:0]	O	High-Z	VOL	Off	Off
SM_BS[2:0]	O	High-Z	VOL	Off	Off
SM_RAS#	O	High-Z	VOH	Off	Off
SM_CAS#	O	High-Z	VOH	Off	Off
SM_WE#	O	High-Z	VOH	Off	Off
SM_RCEVENIN#	I	High-Z	High-Z	Off	Off
SM_RCVENOUT#	O	High-Z	High-Z	Off	Off
SM_CK[1:0]	O	High-Z	VOH	Off	Off
SM_CK[1:0]#	O	High-Z	VOL	Off	Off
SM_CS[1:0]#	O	High-Z	VOH	Off	Off
SM_CKE[1:0]	O	VOL	VOL	VOL	Off
SM_VREF	I-A	VIX-unknown	VIX-unknown	Don't Care	Off
SM_RCOMP	I-A	High-Z	High-Z	High-Z	Off
LVDS					
LA_DATAP[3:0], LA_DATAN[3:0]	O	VOH	VOH	Off	Off
LA_CLKP/N	O	VOH	VOH	Off	Off
SDVO					
SDVOB_GREEN+, SDVOB_GREEN-	O	pull-up	High-Z	Off	Off
SDVOB_BLUE+, SDVOB_BLUE-	O	pull-up	High-Z	Off	Off
SDVOB_RED+, SDVOB_RED-	O	pull-up	High-Z	Off	Off
SDVOB_CLK+, SDVOB_CLK-	O	pull-up	High-Z	Off	Off
SDVOB_TVCLKIN+, SDVOB_TVCLKIN-	I	Don't care	Don't care	Off	Off
SDVO_INT+, SDVO_INT-	I	Don't care	Don't care	Off	Off
SDVO_STALL+, SDVO_STALL-	I	Don't care	Don't care	Off	Off
SDVO_CTRLCLK	I/O	pull-up	High-Z	Off	Off
SDVO_CTRLDATA	I/O	pull-up	High-Z	Off	Off

Table 5. Intel® SCH Reset State (Sheet 3 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
DDC					
L_DDC_CLK	I/O	pull-up	High-Z	Off	Off
L_DDC_DATA	I/O	pull-up	High-Z	Off	Off
L_CTLCLKA/B	I/O	pull-up	High-Z	Off	Off
L_VDDEN	O	High-Z	High-Z	Off	Off
L_BKLTEN	O	High-Z	High-Z	Off	Off
L_BKLTCTL	O	High-Z	High-Z	Off	Off
USB					
USB_DP[7:0] USB_DN[7:0]	I/O	VOL	VOL	VOX-unknown	Off
USB_OC[7:0]#	I	VIX-unknown	VIX-unknown	VIX-unknown	Off
USB_RBIASP	I-A	High-Z	High-Z	High-Z	Off
USB_RBIASN	I-A	High-Z	High-Z	High-Z	Off
USB_CLK48	I	Don't care	don't care	Off	Off
PCI Express*					
CLKREQ#	O	VOX-known	VOX-known	Off	Off
PCIE_PETp[2:1]	O	pull-up	VOL	Off	Off
PCIE_PETn[2:1]	O	VOH	VOH	Off	Off
PCIE_PERp[2:1]	I	Don't care	Don't care	Off	Off
PCIE_PERn[2:1]	I	Don't care	Don't care	Off	Off
PCIE_CLKINP, PCIE_CLKINN	I	Don't care	Don't care	Off	Off
PCIE_ICOMPO, PCIE_ICOMPI	I/O	High-Z	High-Z	Off	Off
SDIO/MMC					
SD0_DATA[3:0]	I/O	pull-up	High-Z	Off	Off
SD1_DATA[3:0]	I/O	pull-up	High-Z	Off	Off
SD2_DATA[7:0]	I/O	pull-up	High-Z	Off	Off
SD[2:0]_CMD	I/O	pull-up	High-Z	Off	Off
SD[2:0]_CLK	O	VOL	VOL	Off	Off
SD[2:0]_WP	I/O	Don't care	Don't care	Off	Off
SD[2:0]_CD#	I/O	Don't care	Don't care	Off	Off
SD[2:0]_LED	O	VOL	High-Z	Off	Off
SD[2:0]_PWR#	O	VOL	High-Z	Off	Off

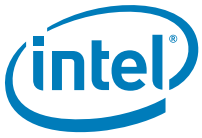


Table 5. Intel® SCH Reset State (Sheet 4 of 5)

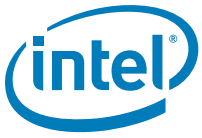
Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
PATA					
PATA_DCS1#	O	VOH	VOH	Off	Off
PATA_DCS3#	O	VOH	VOH	Off	Off
PATA_DA[2:0]	O	VOX-unknown	VOX-unknown	Off	Off
PATA_DD[15:0]	I/O	High-Z	High-Z	Off	Off
PATA_DDREQ	I	VIL	VIL	Off	Off
PATA_DDACK#	O	VOH	VOH	Off	Off
PATA_DIOR#	O	VOH	VOH	Off	Off
PATA_DIOW#	O	VOH	VOH	Off	Off
PATA_IORDY	I	VIH	VIH	Off	Off
PATA_IDEIRQ	I	VIL	VIL	Off	Off
Intel® HD Audio)					
HDA_RST#	O	VOL	VOL	Off	Off
HDA_SYNC	O	High-Z	High-Z	Off	Off
HDA_CLK	O	High-Z	VOL	Off	Off
HDA_SDO	O	High-Z	High-Z	Off	Off
HDA_SDI[1:0]	I	Don't care	Don't care	Off	Off
HDA_DOCKEN#	O	VOH	VOH	Off	Off
HDA_DOCKRST#	O	VOH	VOH	Off	Off
LPC					
LPC_LAD[3:0]	I/O	High-Z	High-Z	Off	Off
LPC_FRAME#	O	VOH	VOH	VOH	Off
LPC_SERIRQ	I/O	High-Z	High-Z	Off	Off
LPC_CLKOUT[2:0]	O	VOL	VOL	VOL	Off
LPC_CLKRUN#	I/O	VOH	VOH	VOH	Off
SMBus					
SMB_DATA	I/O	High-Z	High-Z	Off	Off
SMB_CLK	I/O	High-Z	High-Z	Off	Off
SMB_ALERT#	I	High-Z	High-Z	Off	Off
Power Management					
THRM#	I	VIX-unknown	VIX-unknown	Off	Off
RESET#	I	VIL	VIH	VIL	Off
PWROK	I	VIX-unknown	VIL	VIL	VIL
RSMRST#	I	VIX-unknown	VIH	VIH	VIL
RTCRST#	I	VIX-unknown	VIH	VIH	VIH
SUSCLK	O	Running	Running	Running	Off

Table 5. Intel® SCH Reset State (Sheet 5 of 5)

Signal Name	Direction	Reset	Post-Reset	S3	S4/S5
WAKE#	I	VIX-unknown	VIX-unknown	VIX-unknown	Off
STPCPU#	O	VOH	VOH	Off	Off
DPRSLPVR	O	VOL	VOL	Off	Off
SLPMODE	O	VOL	VOL	VOH	Off
RSTWARN	I	VIH	VIH	VIH	Off
SLPRDY#	O	VOH	VOH	VOL	Off
RSTRDY#	O	VOH	VOH	VOL	Off
GPE#	I	VIX-unknown	VIX-unknown	VIX-unknown	Off
SLPIOVR#	I/O	High-Z	High-Z	Off	Off
Real Time Clock					
RTC_X1	I-A	Running	Running	Running	Running
RTC_X2	I-A	Running	Running	Running	Running
JTAG					
TCK	I	pull-up	pull-up	Off	Off
TMS	I	pull-up	pull-up	Off	Off
TDI	I	pull-up	pull-up	Off	Off
TDO	O	High-Z	High-Z	Off	Off
TRST#	I	pull-up	pull-up	Off	Off
Miscellaneous					
BSEL2	I	VIX-unknown	VIX-unknown	Off	Off
CFG[1:0]	I	VIX-unknown	VIX-unknown	Off	Off
CLK14	I	Running	Running	Off	Off
INTVRMEN	I	VIH	VIH	VIH	VIH
SPKR	O	VOL	VOL	VOL	Off
SMI#,	I	VIX-unknown	VIX-unknown	Off	Off
EXTTS	I	X	X	Off	Off
GPIO					
GPIO[6:0], GPIO[9:8]	I/O	High-Z	High-Z	Off	Off
GPIOSUS[3:0]	I/O	High-Z	High-Z	VIX-unknown	Off

NOTES:

1. The Intel® SCH power-on is a very controlled sequence with several intermediate transitional states before the true reset is reached (this is a reset state from PWROK asserted high to RESET# deasserted high). Pin values are not ensured to be at the specified reset state until all power supplies and input clocks are stable. The 3.3 V I/O pins may glitch, toggle or float.



3.2 Integrated Termination Resistors

Table 6. Intel® SCH Integrated Termination Resistors

Signal	Resistor Type	Nominal Value	Tolerance
GPIO3	pull-up	22 kΩ	±20%
GPIO0	pull-down	22 kΩ	±20%
HDA_CLK	pull-down	22 kΩ	±20%
HDA_DOCKRST#	pull-down	20 kΩ	±20%
HDA_RST#	pull-down	22 kΩ	±20%
HDA_SDI[1:0]	pull-down	22 kΩ	±20%
HDA_SDO	pull-down	22 kΩ	±20%
HDA_SYNC	pull-down	22 kΩ	±20%
LA_CLKN, LA_CLK_P	pull-up	50 Ω	±20%
LA_DATAN[3:0], LA_DATAP[3:0]	pull-up	50 Ω	±20%
LPC_LAD[3:0]	pull-up	20 k	±20%
PATA_DA[2:0]	Series	33 Ω	±20%
PATA_DCS1#	Series	33 Ω	±20%
PATA_DCS3#	Series	33 Ω	±20%
PATA_DD[16:0]	Series	33 Ω	±20%
PATA_DD7	pull-down	13.3 kΩ	±20%
PATA_DDACK#	Series	33 Ω	±20%
PATA_DDREQ	Series	33 Ω	±20%
PATA_DDREQ	pull-down	13.3 kΩ	±20%
PATA_DIOR#	Series	33 Ω	±20%
PATA_DIOW#	Series	33 Ω	±20%
PATA_IDEIRQ	Series	33 Ω	±20%
PATA_IORDY	Series	33 Ω	±20%
PCIE_PERn[2:1], PCIE_PERp[2:1]	pull-down	50 Ω	±20%
PCIE_PETn[2:1], PCIE_PETp[2:1]	pull-up	50 Ω	±20%
RESERVED1	pull-up	300 kΩ	±20%
RESET#	pull-down	50 kΩ	±20%
SD[2:0]_PWR#	pull-up	60 kΩ	±20%
SD2_DATA[7:0] SD[1,0]_DATA[3:0]	pull-up	75 kΩ	±30%
SDVOB_RED, SDVOB_RED#	pull-up	50 Ω	±20%
SDVOB_BLUE, SDVOB_BLUE#	pull-up	50 Ω	±20%
SDVOB_GREEN, SDVOB_GREEN#	pull-up	50 Ω	±20%
SDVOB_CLK, SDVOB_CLK#	pull-up	50 Ω	±20%
SDVOB_CLK#	pull-up	50 Ω	±20%

Table 6. Intel® SCH Integrated Termination Resistors

Signal	Resistor Type	Nominal Value	Tolerance
SDVOB_INT, SDVOB_INT#	pull-down	50 Ω	±20%
SDVOB_STALL, SDVOB_STALL#	pull-down	50 Ω	±20%
SDVOB_TVCLKIN, SDVOB_TVCLKIN#	pull-down	50 Ω	±20%
STPCPU#	pull-down	20 kΩ	±20%
TCK	pull-up	5 kΩ	±40%
TMS	pull-up	5 kΩ	±40%
TDI	pull-up	5 kΩ	±40%
USB_DN[7:0]. USB_DP[7:0]	pull-down	15 kΩ	±20%
USB_DN2, USB_DP2 (Client mode)	pull-up	1.5 kΩ	±20%

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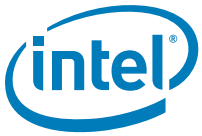

4 System Clock Domains

The Intel® SCH contains many clock frequency domains to support its various interfaces. Table 7 summarizes these domains.

Table 7. Intel® SCH Clock Domains

Clock Domain	Signal Name	Frequency	Source	Usage
FSB	H_CLKINP H_CLKINN	100 MHz or 133 MHz	Main Clock Generator	Used to generate core and SM internal clocks.
PCI Express*	PCIE_CLKIN[P:N]	100 MHz	Main Clock Generator	PCI Express ports
Display Reference Clock	DA_REFCLKIN DB_REFCLKINSSC	96 MHz 100 MHz	Main Clock Generator	Primary clock source for display clocks, USB controllers, SDIO, HD Audio
CLK14	CLK14	14.31818 MHz	Main Clock Generator	Used by ACPI timer and the multimedia timers logic. Stopped during S1 or higher.
RTC	RTC_X1, RTC_X2	32.768 kHz	Cyrstal oscillator	RTC, Power Management. Always running.
Derivative Clocks: See Note				
DDR2	SM_CK[1:0] SM_CK[1:0]#	200 MHz or 266 MHz	Intel® SCH (2x FSB clock)	Drives SDRAM Ranks 0 and 1. Data Rate is 2x the clock rate.
LVDS, SDVO	LA_CLK[P/N] SDVOB_CLK±	100–200 MHz	Intel® SCH (Multiple of DA_REFCLKIN)	Display clock outputs
LPC	LPC_CLKOUT[1:0]	Up to 33 MHz	Intel® SCH (¼ FSB clock)	Supplied for external devices requiring PCICLK
USB2	N/A	480 MHz	Intel® SCH (5x DA_REFCLKIN)	USB PLL
Intel HD Audio	HDA_CLK	24 MHz	Intel® SCH (1/4 DA_REFCLKIN)	Drives external CODECs
SD/SDIO MMC	SD[2:0]_CLK	24 MHz 48 MHz	1/4 DA_REFCLKIN 1/2 DA_REFCLKIN	

NOTE: These are clock domains that are fractional multiples of existing clock frequencies.

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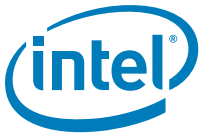


5 Register and Memory Mapping

The Intel® SCH contains registers that are located in the processor's memory and I/O space. It also contains sets of PCI configuration registers that are located in separate configuration space. This chapter describes the Intel® SCH I/O and memory maps at the register-set level. Register-level address maps and individual register-bit descriptions are provided in the following chapters and constitute the bulk of this document.

The following notations and definitions are used in the register/instruction description chapters.

Table 8. Register Access Types and Definitions

Access Type	Meaning	Description
RO	Read Only	In some cases, if a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
WO	Write Only	In some cases, if a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
R/W	Read/Write	A register with this attribute can be read and written.
R/WC	Read/Write Clear	A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.
R/WO	Read/Write-Once	A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
R/WLO	Read/Write, Lock-Once	A register bit with this attribute can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.
Default	Default	When the Intel® SCH is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the Intel® SCH registers accordingly.

5.1 Intel® SCH Register Introduction

The Intel® SCH contains two sets of software accessible registers accessed through the Host processor I/O address space: Control registers and internal configuration registers.

1. Control registers are I/O mapped into the processor I/O space that control access to PCI and PCI Express configuration space (see section entitled I/O Mapped Registers).
2. Internal configuration registers residing within the Intel® SCH are partitioned into eight logical device register sets, one for each PCI device listed in Table 9. (These are “logical” devices because they reside within a single physical device).

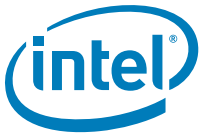
The Intel® SCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the host processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a DWord. All multi-byte numeric fields use little-endian ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in DWord (32-bit) quantities.

Some of the Intel® SCH registers described in this section contain reserved bits. These bits are labeled Reserved. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved-bit positions are preserved. That is, the values of reserved-bit positions must first be read, merged with the new values for other-bit positions and then written back.

Note: The software does not need to perform read, merge, and write operation for the configuration address register.

In addition to reserved bits within a register, the Intel® SCH contains address locations in the configuration space of the Host Bridge entity that are marked either Reserved or Intel Reserved. The Intel® SCH responds to accesses to Reserved address locations by completing the host cycle. When a Reserved register location is read, a zero value is returned. (Reserved registers can be 8, 16, or 32 bits in size). Writes to Reserved registers have no effect on the Intel® SCH. Registers that are marked as Intel Reserved must not be modified by system software. Writes to Intel Reserved registers may cause system failure. Reads from Intel Reserved registers may return a non-zero value.

Upon a Cold Reset, the Intel® SCH sets all configuration registers to predetermined default states. Some default register values are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable and to program the Intel® SCH registers accordingly.



5.2 PCI Configuration Map

The Intel® SCH incorporates a variety of PCI devices and functions, as shown in Table 9.

There are two access mechanisms to the configuration space within the Intel® SCH:

- through I/O ports CF8h/CFCh
- through a direct memory mapped space

Table 9. PCI Devices and Functions

Device	Function	Function Description
0	0	Host Bridge
2	0	Integrated Graphics and Video Device
26	0	USB Client
27	0	HD Audio Controller
28	0	PCI Express Port 1
	1	PCI Express Port 2
29	0	USB Classic UHCI Controller 1
	1	USB Classic UHCI Controller 2
	2	USB Classic UHCI Controller 3
	7	USB2 EHCI Controller
30	0	SDIO/MMC Port 0
	1	SDIO/MMC Port 1
	2	SDIO/MMC Port 2
31	0	LPC Interface
	1	PATA Controller

5.3 System Memory Map

The Intel® SCH supports up to 2 GB of physical DDR2 memory space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1 MB region which is divided into regions that can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. This section describes how the memory space is partitioned and how those partitions are used.

Top of Memory (TOM) is the highest address of physical memory actually installed in the system. TOM greater than 2GB is not supported.

Memory addresses above 2 GB will be routed to internal controllers or external I/O devices. Any memory access between TOM and 2 GB will return indeterminate results, and writes will be ignored.

Figure 3 represents system memory address map in a simplified form.

Figure 3. System Address Ranges

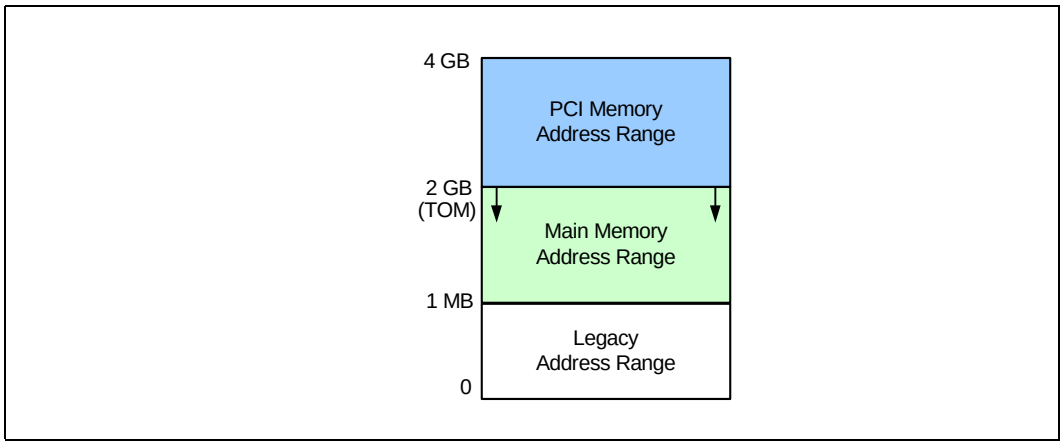


Table 10. Intel® SCH Memory Map (Sheet 1 of 2)

Device	Starting Address	Ending Address	Comment
Legacy Address Range (0 to 1 MB)			
Legacy Video (VGA)	000A0000h	000BFFFFh	Access to this range will be forward to PCI Express if the Intel Graphics Media Adapter is disabled.
Expansion Area	000C0000h	000DFFFFh	
Extended BIOS (LPC)	000E0000h	000EFFFFh	
BIOS (LPC)	000F0000h	000FFFFFh	
LPC	000E0000h	000FFFFFh	
Main Memory[1] (1 MB to Top Of Memory[2])			
TSEG	Variable	Variable	System Management Mode memory
Graphics	Variable	Variable	

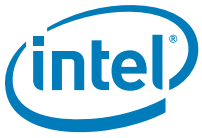


Table 10. Intel® SCH Memory Map (Sheet 2 of 2)

Device	Starting Address	Ending Address	Comment
PCI Configuration Space (2 GB to 4 GB)			
IOxAPIC	FEC00000h	FEC00040h	
HPET	FED00000h	FED003FFh	High Performance Event Timer
TPM 1.2	FEFD40000h	FED4BFFFh	LPC
High BIOS	FFF80000h	FFFFFFFFh	LPC, See **Note** 3 for CMC address space
Configurable Main Memory Configuration Spaces			
PCI Express Port 1	Anywhere in 32-bit range		Configured by D30:F0:MBL
PCI Express Port 1 (prefetchable)	Anywhere in 32-bit range		Configured by D30:F0:PMBL
PCI Express Port 2	Anywhere in 32-bit range		Configured by D30:F1:MBl
PCI Express Port 2 (prefetchable)	Anywhere in 32-bit range		Configured by D30:F1:PMBL
Root Complex Base Register	1 KB anywhere in 32-bit range		Configured by D30:F0:RCBA
USB2 Host Controller	1 KB anywhere in 32-bit range		Configured by D20:F7:MEM_BASE
Intel HD Audio Host Controller	512 KB anywhere in 32-bit range		Configured by D27:F0:LBAR
SDIO 1	1 KB anywhere in 32-bit range		Configured by D30:F0:MEM_BASE
SDIO 2	1 KB anywhere in 32-bit range		Configured by D30:F1:MEM_BASE
SDIO 3	1 KB anywhere in 32-bit range		Configured by D30:F2:MEM_BASE

NOTES:

1. All accesses to addresses within the main memory range will be forwarded by the Intel® SCH to the DRAM unless they fall into one of the optional ranges specified in this section.
2. Top of Memory is determined by examining the contents of the DRAM Rank Population register and calculating the total system memory based on the device width, device density, and number of ranks installed. Up to 2 GB of total system memory is supported.
3. The Chipset Microcode (CMC) base address locates within the LPC space and consumes 64 KB of space. The starting address for the CMC code can be FFFB000h, FFFC000h, FFFD000h, or FFFE000h. Refer to Section 2.17 for selecting the CMC start address. Make sure to avoid using the same starting address for other LPC devices in the system.

5.3.1 Legacy Video Area (A0000h – BFFFFh)

The legacy 128 KB VGA-memory range can be mapped to the Intel Graphics Media Adapter (Device 2) or forwarded to an external graphics device located on one of the two PCI Express I/O ports. The VGA-Disable bit in the Graphics Control register of the Intel Graphics Media Adapter PCI config space can be set to ignore VGA memory or I/O cycles. If that bit is set, the Intel® SCH will steer VGA accesses to the appropriate PCI Express port. If such a device does not exist in the system, the cycles will be ignored.

5.3.2 Expansion Area (C0000h – DFFFFh)

This 128-KB ISA-Expansion region is always mapped to DRAM. This region is typically used by BIOS to shadow (copy) option ROMs, including Video BIOS. This region cannot be write protected.

5.3.3 Extended System BIOS Area (E0000h – EFFFFh)

This area is a single, 64-KB segment that can be assigned independent read/write attributes and is mapped only to main DRAM Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

5.3.4 System BIOS Area (F0000h – FFFFFh)

This area is a single, 64-KB segment that can be assigned read and write attributes. After reset, this region defaults to “disabled” and cycles are forwarded to the LPC interface. By manipulating the Read/Write attributes of this memory range, the Intel® SCH can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

5.3.5 EHCI Controller Area

The EHCI controller (Device 29, Function 7) requires a single, 1-KB to be reserved out of the 1-GB main memory area for configuration purposes. See Chapter 13 for more details.

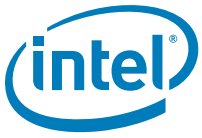
5.3.6 Programmable Attribute Map (PAM)

The two, 64-KB memory regions below 1-MB comprise the PAM Memory Area. See Table 11 for these ranges and default attributes.

Any attempts by the processor or an Intel® SCH device to read a segment marked with the Read Disable attribute will return undefined data.

Table 11. Programmable Attribute Map

Region	Memory Segments	Default Attributes
“Segment E”	0E0000h – 0EFFFFh	R/W
“Segment F”	0F0000h – 0FFFFFh	WE RE



5.3.7 Top of Memory Segment (TSEG)

TSEG is a 1-MB, 2-MB, or 8-MB memory region located below Intel Graphics Media Adapter stolen memory, which is at the top of physical memory (TOM). It is used for System Management Mode accesses by the processor. See Table 10 for more information on SMM.

Processor accesses to the TSEG range without SMM attribute or without WB attribute are forwarded to memory as invalid accesses. Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. The TSEG memory region is not accessible by non-processor bus masters (that is, PCI Express, USB, etc.)

5.3.8 APIC Configuration Space (FEC00000h – FECFFFFFh)

This range is reserved for APIC configuration space which includes an IOxAPIC and a Local (processor) APIC. The IOxAPIC is located at the default address FEC00000h to FEC70FFFh and is part of the LPC bridge controller (Device 31, Function 0). The default Local APIC configuration space goes from FEC80000h to FECFFFFFh.

Processor accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the processor. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each processor should be relocated to the FEC00000h to FECFFFFFh range so that one MTRR can be programmed to 64 KB for the Local and IOxAPIC.

5.3.9 High BIOS Area

The top 2 MB (FFC00000h – FFFFFFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices. The processor begins execution from the High BIOS after reset. This region is mapped to the LPC controller so that the upper subset of this region aliases to the 16-MB through 256-KB range. The actual address space required for the BIOS is less than 2 MB but the minimum processor MTRR range for this region is 2 MB so that full 2 MB must be considered.

5.3.10 Boot Block Update

The Intel® SCH supports a Top-Block Swap mode where the top boot block on the Firmware Hub (FWH) is swapped with a block in a different location. This allows the boot block to be safely updated while protecting the system from a power loss When BC.TS is set, the Intel® SCH inverts A16 for cycles going to the upper two 64 KB blocks in the firmware. When BC.TS is cleared, the Intel® SCH will not invert A16. This bit is cleared by RTCRST#.

The scheme is based on the concept that the top block is reserved as the “boot” block, and the block immediately below the top block is reserved for doing boot-block updates.

The algorithm is as follows:

1. Software copies the contents of the top boot-block to the swap block below it.
2. Software checks that the copy was successful by checksum or other validation technique.
3. Software sets the TOP_SWAP bit. This will invert A16 for cycles going to the Firmware Hub and force the processor to read from the swapped block location. (processor access to FFF**F**0000h through FFF**F**FFFFh will be directed to FFF**E**0000h through FFF**E**FFFFh in the Firmware Hub.)
4. Software erases the top block.
5. Software writes the new top block.
6. Software validates the new top block is correct.
7. Software clears the TOP_SWAP bit allowing normal processor access to the top block address range (FFFF0000h through FFFFFFFFh).
8. Software sets the Top_Swap Lock-Down bit.

If a power failure occurs at any point after step 3, the system will be able to boot from the copy of the boot block that is stored in the block below the top. This is because a copy of the TOP_SWAP bit is stored in the RTC well.

Note: The top-block swap mode may be forced by an external strapping option. When top-block swap mode is forced in this manner, the TOP_SWAP bit cannot be cleared by software.

System Management Mode (SMM) uses main memory for System Management RAM (SMM RAM). SMM uses either a 1-MB, 2-MB, or 8-MB memory region located at the Top of Memory Segment (TSEG) in main memory (above the 1-MB boundary). This memory segment in RAM is available for the SMI handlers and code and data storage, and it is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. The TSEG area can be mapped to any address within the 32-bit address range.

For more details on the location and size of the SMM memory areas, refer to Table 10 or the Host SMM Control (HSMMCTL) Register definition later in this chapter.

Note: Other Intel® SCH bus masters are not allowed to access the SMM space.

5.3.11 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into Intel® SCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. Processor FSB transactions are routed accordingly.

5.3.12 Locked Transactions

Only locked cycles to DRAM are supported by the Intel® SCH. Locked cycles to non-DRAM space are unsupported in the Intel® SCH. This includes all non-physical DRAM address spaces including peripheral device memory, VGA memory, memory-mapped I/O, and other memory spaces besides standard DRAM.

5.4 I/O Address Space

The I/O map is divided into fixed ranges and variable ranges. Fixed ranges cannot be moved, but in some cases can be disabled. Variable ranges can be both moved and disabled.

5.4.1 Fixed I/O Decode Ranges

Table 12 shows the fixed I/O decode ranges from the processor. For each port there may be separate behavior for reads and writes. Processor cycles that go to reserved ranges are internally aborted; if the cycle was a read, all 1s will be returned to the processor.

Table 12. Fixed I/O Decode Ranges (Sheet 1 of 2)

Port Number	Size (Bytes)	Read Target	Write Target	Can Disable?
20h	2	8259 Master	8259 Master	No
24h	2	8259 Master	8259 Master	No
28h	2	8259 Master	8259 Master	No
2Ch	2	8259 Master	8259 Master	No
30h	2	8259 Master	8259 Master	No
34h	2	8259 Master	8259 Master	No
38h	2	8259 Master	8259 Master	No
3Ch	2	8259 Master	8259 Master	No
40h	3	8254	8254	No
43h	1	None	8254	No
50h	3	8254	8254	No
53h	1	None	8254	No
61h	1	NMI Controller	NMI Controller[1]	No
63h	1	NMI Controller	NMI Controller[1]	Yes, alias to 61h
65h	1	NMI Controller	NMI Controller[1]	Yes, alias to 61h
67h	1	NMI Controller	NMI Controller[1]	Yes, alias to 61h
70h	1	None	NMI and RTC	No
71h	1	RTC	RTC	No
72h	1	RTC	NMI and RTC	Yes, w/ 73h
73h	1	RTC	RTC	Yes, w/ 72h
74h	1	RTC	NMI and RTC	No
75h	1	RTC	RTC	No
76h	1	RTC	NMI and RTC	No
77h	1	RTC	RTC	No
84h	3	Internal	Internal/LPC	No
88h	1	Internal	Internal/LPC	No
8Ch	3	Internal	Internal/LPC	No

Table 12. Fixed I/O Decode Ranges (Sheet 2 of 2)

Port Number	Size (Bytes)	Read Target	Write Target	Can Disable?
A0h	2	8259 Slave	8259 Slave	No
A4h	2	8259 Slave	8259 Slave	No
A8h	2	8259 Slave	8259 Slave	No
ACh	2	8259 Slave	8259 Slave	No
B0h	2	8259 Slave	8259 Slave	No
B2h	2	Power Management	Power Management	No
B4h	2	8259 Slave	8259 Slave	No
B8h	2	8259 Slave	8259 Slave	No
BCh	2	8259 Slave	8259 Slave	No
170h	8	PATA	PATA	Yes
1F0h	8	PATA	PATA	Yes
376h	1	PATA	PATA	Yes
3F6h	1	PATA	PATA	Yes
CF8h	4	Internal	Internal	No
CFCh	4	Internal	Internal	No

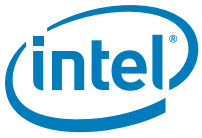
NOTE:
1. Only if the Port 61 Alias-Enable bit (GCS.P61AE) is set—otherwise, none.

5.4.2 Variable I/O Decode Ranges

Table 13 shows the Variable I/O Decode Ranges. They are set using Base Address Registers (BARs) or other configuration bits in the various configuration spaces. The PnP software (PCI or ACPI) can use its configuration mechanism to set and adjust these values. These values should not be mapped on top of fixed address ranges as unpredictable behavior will result.

Table 13. Variable I/O Decode Ranges

Range Name	Mappable	Size (Bytes)	Target
ACPI	Anywhere in 64-K I/O Space	64	Power Management
Bus Master IDE	Anywhere in 64-K I/O Space	16	PATA
SMBus	Anywhere in 64-K I/O Space	32	SMB Unit
GPIO	Anywhere in 64-K I/O space	64	GPIO Unit
USB 1	Anywhere in 64-K I/O Space	32	UHCI Host Controller 1
USB 2	Anywhere in 64-K I/O Space	32	UHCI Host Controller 2
USB 3	Anywhere in 64-K I/O Space	32	UHCI Host Controller 3



5.5 I/O Mapped Registers

The Intel® SCH contains two registers that reside in the processor I/O address space – the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

5.5.1 NSC—NMI Status and Control Register

I/O Offset (Port): 61h Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Access and Default	Description
7	0 RO	**SERR# NMI Status (SNS):** Set on errors from a PCIe port or internal functions that generate SERR#. SNE in this register must be cleared in order for this bit to be set. To reset the interrupt, set Bit 2 to 1 and then set it to 0.
6	0 RO	**IOCHK NMI Status (INS):** Set when SERIRQ asserts IOCHK# and INE in this register is cleared. To reset the interrupt, set Bit 3 to 1 and then set it to 0.
5	0 RO	**Timer Counter 2 Status (T2S):** Reflects the current state of the 8254 Counter 2 output. Counter 2 must be programmed for this bit to have a determinate value.
4	0 RO	**Refresh Cycle Toggle Status (RTS):** This signal toggles from 0 to 1 or 1 to 0 at a rate that is equivalent to when a refresh cycles would occur.
3	0 R/W	**IOCHK NMI Enable (INE):** When set, IOCHK# NMIs are disabled and cleared. When cleared, IOCHK# NMIs are enabled.
2	0 R/W	**SERR# NMI Enable (SNE):** When set, SERR# NMIs are disabled and cleared. When cleared, SERR# NMIs are enabled.
1	0 R/W	**Speaker Data Enable (SDE):** When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0 R/W	**Timer Counter 2 Enable (TC2E):** When cleared, counter 2 counting is disabled. When set, counting is enabled.

5.5.2 NMIE—NMI Enable Register

I/O Offset (Port): 70h Attribute: R/W
Default Value: 00h Size: 8 bits

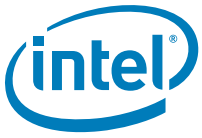
Bit	Access and Default	Description
7	0 WO	**NMI Enable (EN):** 1 = NMI sources disabled. 0 = NMI sources enabled.
6:0	0 WO	**Real Time Clock Index (RIDX):** Selects the RTC register or CMOS RAM address to access.

5.5.3 CONFIG_ADDRESS—Configuration Address Register

I/O Offset (Port): 0CF8h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DW. A Byte or Word reference will pass through the Configuration Address Register and onto the internal Intel® SCH backbone as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access and Default	Description
31	R/W 0b	**Configuration Enable (CFGE):** 0 = Disable accesses to PCI configuration space. 1 = Enable accesses to PCI configuration space.
30:24	RO 00h	Reserved
23:16	R/W 00h	**Bus Number:** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus 0 agent. If this is the case and the Intel® SCH is not the target (i.e., the device number is ≥3 and not equal to 7), then a Type 0 Configuration Cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by Device 1's Secondary Bus Number or Subordinate Bus Number Register, then a Type 1 Configuration Cycle is generated. This field is mapped to Byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the Type 1 configuration cycles.
15:11	R/W 00h	**Device Number:** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is "00" the Intel® SCH decodes the Device Number field. The Intel® SCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0, 1, 2 or 7 the internal Intel® SCH devices are selected. This field is mapped to Byte 6 [7:3] of the request header format during PCI Configuration cycles.
10:8	R/W 000b	**Function Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The Intel® SCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to Byte 6 [2:0] of the request header format during PCI Configuration cycles.
7:2	R/W 00h	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to Byte 7 [7:2] of the request header format for during PCI Configuration cycles.
1:0	RO 00b	Reserved



5.5.4 RSTC—Reset Control Register

I/O Offset (Port): 0CF9h Attribute: R/W, RO
Default Value: 00h Size: 8 bits

Bit	Access and Default	Description
7:4	0 RO	Reserved
3	0 R/W	**Cold Reset (COLD):** This bit will cause a cold reset to the platform, which is performed by driving SLPMODE low, SLPRDY# low, and RSTRDY# low. In response to this, the platform will perform a full power cycle.
2	0 RO	Reserved
1	0 R/W	**Warm Reset (WARM):** This bit will cause a warm reset to the platform, which is performed by driving RSTRDY# low. In response to this, the platform will drive RESET# low to reset the processor and all peripherals.
0	0 R/W	**CPU-Only Reset (CPU):** This bit causes H_CPURST# to be asserted, with processor timing requirements met for minimum pulse width. The processor Power-On-Config register (HPOC) contents will be driven on the host address bus, and latched on the deassertion edge of H_CPURST#.

5.5.5 CONFIG_DATA—Configuration Data Register

I/O Offset (Port): 0CFCh Attribute: R/W
Default Value: 00000000h Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access and Default	Description
31:0	R/W 0000 0000h	**Configuration Data Window (CDW):** If Bit 31 of the CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

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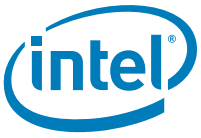
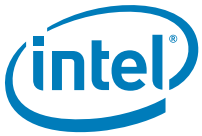




6 General Chipset Configuration

This chapter lists the core registers used to configure the Intel® SCH chipset. These registers are not specific to any particular interface or PCI configuration space, so they are documented here.

There are four groups of registers that meet this description:

- Root complex topology capability
- Interrupt pin and route definitions
- General configuration

The start and end address offsets listed in the following sections are relative to the Root Complex Base Address.

6.1 Root Complex Capability

The root complex is used by PCI Express aware operating systems to identify PCI Express capabilities. It indicates to the OS that the Intel® SCH is capable of isochronous transfers and that an Intel HD Audio controller exists within the Intel® SCH.

The following registers follow the PCI Express capability list structure as defined in the PCI Express specification.

Table 14. Root Complex Configuration Registers

Address	Symbol	Register Name
0000–0003h	RCTCL	Root Complex Topology Capability List
0004–0007h	ESD	Element Self Description
0010–0013h	HDD	Intel® HD Audio Descriptor (Port 15)
0014–0017h	Reserved	Reserved
0018–008Fh	HDBA	Intel HD Audio Base Address (Port 15)

6.1.1 RCTCL—Root Complex Topology Capabilities List

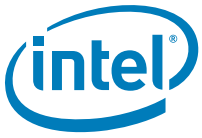
Address Offset: 0000h Attribute: RO
Default Value: 00010005h Size: 32 bits

Bits	Default and Access	Description
31:20	000h RO	**Next Capability (NEXT):** This field indicates next item in the list.
19:16	1h RO	**Capability Version (CV):** This field indicates the version of the capability structure.
15:0	0005h RO	**Capability ID (CID):** This field indicates this is a PCI Express link capability section of an RCRB.

6.1.2 ESD—Element Self Description

Address Offset: 0004h Attribute: RO, R/WO
Default Value: 00000102h Size: 32 bits

Bits	Default and Access	Description
31:24	00h RO	**Port Number (PN):** A value of 0 to indicate the egress port for Intel® SCH.
23:16	00h R/WO	**Component ID (CID):** This field indicates the component ID assigned to this element by software. This is written once by platform BIOS and is locked until a platform reset.
15:08	01h RO	**Number of Link Entries (NLE):** This field indicates that one link entry (corresponding to Intel® HD Audio) is described by this RCRB.
7:4	0 RO	Reserved
3:0	2h RO	**Element Type (ET):** This field indicates that the element type is a root complex internal link.



6.1.3 HDD—Intel HD Audio Description

Address Offset: 0010h Attribute: RO
Default Value: see description Size: 32 bits

Bits	Default and Access	Description
31:24	Fh RO	**Target Port Number (PN):** This field indicates the target port number is 15 (Intel® HD Audio).
23:16	Init RO	**Target Component ID (TCID):** This field returns the value of the ESD.CID field programmed by platform BIOS, since the root port is in the same component as the Root Complex Register Blocks (RCRB).
15:2	0 RO	Reserved
1	1 RO	**Link Type (LT):** This bit indicates that the link points to a root port.
0	1 RO	**Link Valid (LV):** Link is always valid.

6.1.4 HDBA—Intel HD Audio Base Address

Address Offset: 0018h Attribute: RO
Default Value: 00000000 000D8000h Size: 64 bits

Bits	Default and Access	Description
63:32	0h RO	**Config Space Base Address Upper (CBAU):** Reserved
31:28	0h RO	**Config Space Base Address Lower (CBAL):** Reserved
27:20	0h RO	**Bus Number (BN):** Indicates Intel® HD Audio is on Bus 0
19:15	1Bh RO	**Device Number (DN):** Indicates Intel HD Audio is in Device 27
14:12	0h RO	**Function Number (FN):** Indicates Intel HD Audio is in Function 0
11:00	0 RO	Reserved

6.2 Interrupt Pin and Routing Configuration

Configuration of interrupts involves setting both the interrupt pin that a particular device/function should be mapped to, as well as the routing of that pin to the appropriate PIRQx signal that ultimately goes to either the PIC or APIC controller.

6.2.1 Interrupt Pin Configuration

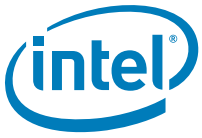
The following registers tell each device which interrupt pin to report in the IPIN register of their configuration space. Each register has one or more 4-bit field assigned to a particular PCI function. This 4-bit field is defined as shown in Table 15.

Table 15. Interrupt Pin Field Bit Decoding

Bits	Pin
0h	No Interrupt
1h	INTA#
2h	INTB#
3h	INTC#
4h	INTD#
5h – Fh	Reserved

Table 16. Interrupt Pin Register Map

Address	Symbol	Register Name	Interface
3100–3103h	D31IP	Device 31 Interrupt Pin	LPC Interface
3104–3107h	D30IP	Device 30 Interrupt Pin	SDIO/MMC (Ports 1-3)
3108–310Bh	D29IP	Device 29 Interrupt Pin	USB Host (UHCI 1-3, EHCI)
310C–310Fh	D28IP	Device 28 Interrupt Pin	PCI Express (Ports 1 and 2)
3110–3113h	D27IP	Device 27 Interrupt Pin	Intel HD Audio
3114–3117h	D26IP	Device 26 Interrupt Pin	USB Target
3118–311Ch	D02IP	Device 2 Interrupt Pin	Intel GMA 500



6.2.1.1 D31IP—Device 31 Interrupt Pin

Offset Address: 3100h–3103h Attribute: R/W, RO
Default Value: 00000210h Size: 32 bits

Bits	Type	Reset	Description
31:4	RO	0	Reserved
3:0	RO	0h	**LPC Bridge Pin (LIP):** The LPC bridge does not generate an interrupt.

6.2.1.2 D30IP—Device 30 Interrupt Pin

Offset Address: 3104–3107h Attribute: R/W, RO
Default Value: 00000321h Size: 32 bits

Bits	Type	Reset	Description
31:12	RO	0	Reserved
11:8	R/W	3h	**SDIO Port 2 Interrupt Pin (SD2):** Indicates which pin SDIO Controller 2 uses.
7:4	R/W	2h	**SDIO Port 1 Interrupt Pin (SD1:** Indicates which pin SDIO Controller 1 uses.
3:0	R/W	1h	**SDIO Port 0 Interrupt Pin (SD0):** Indicates which pin SDIO Controller 0 uses.

6.2.1.3 D29IP—Device 29 Interrupt Pin

Offset Address: 3108–310Bh Attribute: R/W, RO
Default Value: 40000321h Size: 32 bits

Bits	Type	Reset	Description
31:28	R/W	4h	**EHCI Pin (EIP):** Indicates which pin the EHCI controller uses.
27:12	RO	0	Reserved
11:8	R/W	3h	**UHCI 2 Pin (U2P):** Indicates which pin USB Controller 2 uses.
7:4	R/W	2h	**UHCI 1 Pin (U1P):** Indicates which pin USB Controller 1 uses.
3:0	R/W	1h	**UHCI 0 Pin (U0P):** Indicates which pin USB Controller 0 uses.

6.2.1.4 D28IP—Device 28 Interrupt Pin

Offset Address: 310C–310Fh Attribute: R/W, RO
Default Value: 00000021h Size: 32 bits

Bits	Type	Reset	Description
31:8	RO	0	Reserved
7:4	R/W	2h	**PCI Express 2 Pin (P2IP):** Indicates which pin PCI Express Port 2 uses.
3:0	R/W	1h	**PCI Express 1 Pin (P1IP):** Indicates which pin PCI Express Port 1 uses.

6.2.1.5 D27IP—Device 27 Interrupt Pin

Offset Address: 3110–3113h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Bits	Type	Reset	Description
31:4	RO	0	Reserved
3:0	R/W	1h	**Intel HD Audio Pin (HDAIP):** Indicates which pin the Intel® HD Audio controller uses.

6.2.1.6 D26IP—Device 26 Interrupt Pin

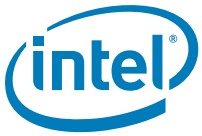
Offset Address: 3114–3117h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Bits	Type	Reset	Description
31:4	RO	0	Reserved
3:0	R/W	1h	**USB Target Pin (UTIP):** Indicates which pin the USB Target controller uses.

6.2.1.7 D02IP—Device 2 Interrupt Pin

Offset Address: 3118–311Bh Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Bits	Type	Reset	Description
31:4	RO	0	Reserved
3:0	R/W	1h	**Graphics Pin (GP):** Indicates which pin the graphics controller uses for interrupts.



6.2.2 Interrupt Route Configuration

The Interrupt Route Configuration registers indicates which PIRQx# pin on the Intel® SCH is connected to the INTA/B/C/D pins reported in the Device X Interrupt Pin register fields. This will be the internal pin/message the device will generate to either the 8259 interrupt controller or the IOxAPIC.

Table 17. Interrupt Route Field Bit Decoding

Bits	Interrupt
0000	PIRQA#
0001	PIRQB#
0010	PIRQC#
0011	PIRQD#
0100	PIRQE#
0101	PIRQF#
0110	PIRQG#
0111	PIRQH#
1000 – 1111	Reserved

Table 18. Interrupt Route Register Map

Address	Symbol	Register Name	Interface
3140–3141h	D31IR	Device 31 Interrupt Route	LPC Interface
3142–3143h	D30IR	Device 30 Interrupt Route	SDIO/MMC (Ports 1-3)
3144–3145h	D29IR	Device 29 Interrupt Route	USB Host (UHCI1-3, EHCI)
3146–3147h	D28IR	Device 28 Interrupt Route	PCI Express (Ports 1 and 2)
3148–3149h	D27IR	Device 27 Interrupt Route	Intel® High Definition Audio
314A–314Bh	D26IR	Device 26 Interrupt Route	USB Target
314C–314Dh	D02IR	Device 2 Interrupt Route	Intel® Graphics Media Accelerator 500

6.2.2.1 D31IR—Device 31 Interrupt Route

Offset Address: 3140-3141h Attribute: R/W
Default Value: 3210h Size: 16 bits

Bits	Default and Access	Description
15:12	3h R/W	**Interrupt D Pin Route (IDR):** Indicates which physical pin INTD# uses for Device 31.
11:8	2h R/W	**Interrupt C Pin Route (ICR):** Indicates which physical pin INTC# uses for Device 31.
7:4	1h R/W	**Interrupt B Pin Route (IBR):** Indicates which physical pin INTB# uses for Device 31.
3:0	0h R/W	**Interrupt A Pin Route (IAR):** Indicates which physical pin INTA# uses for Device 31.

6.2.2.2 D30IR—Device 30 Interrupt Route

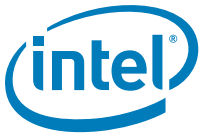
Offset Address: 3142-3143h Attribute: R/W
Default Value: 3210h Size: 16 bits

Bits	Default and Access	Description
15:12	3h R/W	**Interrupt D Pin Route (IDR):** Indicates which physical pin INTD# uses for Device 30.
11:8	2h R/W	**Interrupt C Pin Route (ICR):** Indicates which physical pin INTC# uses for Device 30.
7:4	1h R/W	**Interrupt B Pin Route (IBR):** Indicates which physical pin INTB# uses for Device 30.
3:0	0h R/W	**Interrupt A Pin Route (IAR):** Indicates which physical pin INTA# uses for Device 30.

6.2.2.3 D29IR—Device 29 Interrupt Route

Offset Address: 3144-3145h Attribute: R/W
Default Value: 3210h Size: 16 bits

Bits	Default and Access	Description
15:12	3h R/W	**Interrupt D Pin Route (IDR):** Indicates which physical pin INTD# uses for Device 29.
11:8	2h R/W	**Interrupt C Pin Route (ICR):** Indicates which physical pin INTC# uses for Device 29.
7:4	1h R/W	**Interrupt B Pin Route (IBR):** Indicates which physical pin INTB# uses for Device 29.
3:0	0h R/W	**Interrupt A Pin Route (IAR):** Indicates which physical pin INTA# uses for Device 29.



6.2.2.4 D28IR—Device 28 Interrupt Route

Offset Address: 3146-3147h Attribute: R/W
Default Value: 3210h Size: 16 bits

Bits	Default and Access	Description
15:12	3h R/W	**Interrupt D Pin Route (IDR):** Indicates which physical pin INTD# uses for Device 28.
11:8	2h R/W	**Interrupt C Pin Route (ICR):** Indicates which physical pin INTC# uses for Device 28.
7:4	1h R/W	**Interrupt B Pin Route (IBR):** Indicates which physical pin INTB# uses for Device 28.
3:0	0h R/W	**Interrupt A Pin Route (IAR):** Indicates which physical pin INTA# uses for Device 28.

6.2.2.5 D27IR—Device 27 Interrupt Route

Offset Address: 3148-3149h Attribute: R/W
Default Value: 3210h Size: 16 bits

Bits	Default and Access	Description
15:12	3h R/W	**Interrupt D Pin Route (IDR):** Indicates which physical pin INTD# uses for Device 27.
11:8	2h R/W	**Interrupt C Pin Route (ICR):** Indicates which physical pin INTC# uses for Device 27.
7:4	1h R/W	**Interrupt B Pin Route (IBR):** Indicates which physical pin INTB# uses for Device 27.
3:0	0h R/W	**Interrupt A Pin Route (IAR):** Indicates which physical pin INTA# uses for Device 27.

6.2.2.6 D26IR—Device 26 Interrupt Route

Offset Address: 314A-314Bh Attribute: R/W
Default Value: 3210h Size: 16 bits

Bits	Default and Access	Description
15:12	3h R/W	**Interrupt D Pin Route (IDR):** Indicates which physical pin INTD# uses for Device 26.
11:8	2h R/W	**Interrupt C Pin Route (ICR):** Indicates which physical pin INTC# uses for Device 26.
7:4	1h R/W	**Interrupt B Pin Route (IBR):** Indicates which physical pin INTB# uses for Device 26.
3:0	0h R/W	**Interrupt A Pin Route (IAR):** Indicates which physical pin INTA# uses for Device 26.

6.2.2.7 D02IR—Device 2 Interrupt Route

Offset Address: 314C-314Dh Attribute: R/W
Default Value: 3210h Size: 16 bits

Bits	Default and Access	Description
15:12	3h R/W	**Interrupt D Pin Route (IDR):** Indicates which physical pin INTD# uses for Device 2.
11:8	2h R/W	**Interrupt C Pin Route (ICR):** Indicates which physical pin INTC# uses for Device 2.
7:4	1h R/W	**Interrupt B Pin Route (IBR):** Indicates which physical pin INTB# uses for Device 2.
3:0	0h R/W	**Interrupt A Pin Route (IAR):** Indicates which physical pin INTA# uses for Device 2.

6.3 General Configuration Register

6.3.1 RC—RTC Configuration Register

Offset Address: 3400–3403h Attribute: RO, R/WLO
Default Value: 00000000h Size: 32-bit

Bit	Default and Access	Description
31:3	0000000h RO	Reserved
2	0b R/WLO	Reserved
1	0 R/WLO	**Upper 128-Byte Lock (UL):** When set, bytes 38h–3Fh in the upper 128-byte bank of RTC RAM are locked. Writes will be ignored and reads will not return any ensured data.
0	0 R/WLO	**Lower 128-Byte Lock (LL):** When set, bytes 38h–3Fh in the lower 128-byte bank of RTC RAM are locked. Writes will be ignored and reads will not return any ensured data.

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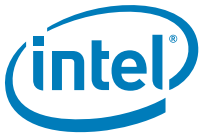


7 Host Bridge (D0:F0)

7.1 Functional Description

The host bridge logic manages many of the Intel® SCH central functions most specifically the FSB controller, memory controller, and thermal and power management.

The host bridge contains all the registers necessary to configure these functions. These registers are organized into two groups, each with its own method of access:

1. PCI configuration space. These registers are accessed using the standard PCI cycle methodology.
2. Custom register space. These registers are accessed through two specific PCI configuration registers, and they are used to issue messages onto the Intel® SCH internal message network.

7.1.1 Dynamic Bus Inversion

When the processor or the Intel® SCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus the corresponding H_DINV# signal will be asserted and the data will be inverted prior to being driven on the bus. Conversely, whenever the processor or the Intel® SCH receives data, it monitors H_DINV[3:0]# to determine if the corresponding data segment should be inverted.

7.1.2 FSB Interrupt Overview

The processor supports FSB interrupt delivery. It does not support the APIC serial bus interrupt delivery mechanism. Interrupt-related messages are encoded on the FSB as “Interrupt Message Transactions”. FSB interrupts may originate from a device part of, or attached to, the Intel® SCH, such as a USB controller or the Intel Graphics Media Accelerator 500. In such a case the Intel® SCH drives the “Interrupt Message Transaction” onto the FSB.

In the IOxAPIC environment, an interrupt is generated from the Intel® SCH IOxAPIC to the processor in the form of a Memory Write to the FSB. Furthermore, the PCI 2.3 specification and PCI Express specification define MSIs (Message Signaled Interrupts) that also take the form of Memory Writes. MSI-capable devices, such as PCI Express or USB, may generate an interrupt using the MSI mechanism, writing the interrupt message directly to the FSB. Alternatively, an Interrupt Message Transaction can be directed to the IOxAPIC which in turn routes the interrupt message to the FSB using the traditional IOxAPIC interrupt Memory Write method. The target of an MSI transaction is dependent upon the target address of the interrupt Memory Write.

Caution: Improperly formed MSIs, including any non-DWord writes to the space reserved for MSI, may cause unexpected system behavior.

7.1.3 CPU BIST Strap

To enter CPU BIST, software first sets the PMSW.CBE (BIST enable) bit, and then does a warm reset by writing to RSTC.WARM. The BIST strap sequence is as follows:

- As part of the boot sequence, the power management controller will check whether PMSW.CBE has been set. If so, it will set the state of the BIST bit in the POC vector accordingly.
- The power management controller prepares the full POC vector and writes it to the HPOC register internally. These values are driven onto the HA[31:3] and INIT# pins.
- CPURST# is deasserted to the processor after ensuring that at least 4 host bus clocks have elapsed after driving POC.
- POC pins all take their normal usage two host clocks after CPURST# deassertion.

7.2 Host PCI Configuration Registers

Table 19. Host Bridge Configuration Register Address Map

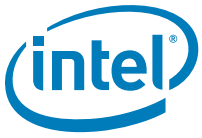
Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor ID	8086	RO
02h–03h	DID	Device ID	8100-8107	RO
04h–05h	PCICMD	PCI Command	0007h	R/W, RO
06h–07h	PCISTS	PCI Status	0280h	R/WC, RO
08h	RID	Revision ID	See description	RO
0Ah–0Bh	CC	Class Codes	0805h	RO
2Ch–2Fh	SS	Subsystem Identifiers	See description	RO

NOTE: Address locations that are not shown should be treated as Reserved.

7.2.1 VID—Identification Register

Offset: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Default and Access	Description
15:0	8086h RO	**Vendor ID (VID):** PCI standard identification for Intel.



7.2.2 DID—Identification Register

Offset: 02h–03h Attribute: RO
Default Value: 810xh Size: 16 bits

Bit	Default and Access	Description
15:0	8100-8107h RO	**Device ID (DID):** This is a 16-bit value assigned to the controller. Refer to the Intel® SCH Specification Update for the DID for various product SKU.

7.2.3 PCICMD—PCI Command Register

Offset: 04h–05h Attribute: R/W, RO
Default Value: 0007h Size: 16 bits

Bit	Default and Access	Description
15:3	0 RO	Reserved
2	1 RO	**Bus Master Enable (BME):** The Intel® SCH is always enabled as a bus master.
1	1 RO	**Memory Space Enable (MSE):** The Intel® SCH is always allowed to access memory.
0	1 RO	**I/O Access Enable (IOAE):** The memory controller always allows access to I/O.

7.2.4 PCISTS—PCI Status Register

Offset: 06h–07h Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:0	0000h RO	Reserved

7.2.5 RID—Revision Identification Register

Offset Address: 08h Attribute: RO
Default Value: TBD Size: 8 bits

Bit	Default and Access	Description
7:0	TBD RO	**Revision ID:** This value is tied to the value in the LPC bridge (Device 31, Function 0).

7.2.6 CC—Class Code Register

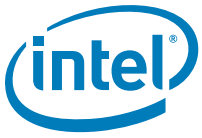
Offset: 0Ah–0Bh Attribute: RO
Default Value: 0600h Size: 16 bits

Bit	Default and Access	Description
15:8	06h RO	**Base Class Code (BCC):** 06h indicates a bridge device.
7:0	00h RO	**Sub Class Code (SCC):** 00h indicates a host bridge.

7.2.7 SS—Subsystem Identifiers Register

Offset: 2Ch–2Fh Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:16	RO	Subsystem ID (SSID)
15:0	RO	Subsystem Vendor ID (SVID)



7.2.7.1 TTB—Thermal Trip Behavior Register

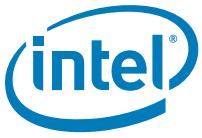
Offset: B6h Attribute: RO, R/W, R/WLO
Default Value: 00000000h Size: 32 bits

(Sheet 1 of 2)

Bit	Default and Access	Description
31	0 R/W	**Internal Thermal Hardware Throttling Enable bit (ITHTE):** This is a master enable for internal thermal sensor-based hardware throttling. Interrupts are not affected by this bit. This is for Hot Trip throttling only.
30:28	000b RO	Reserved
27:26	00b R/W	**Catastrophic Shutdown Select (CSS):** Chooses which option to take upon a catastrophic thermal event. **Bit** / **Definition** 00 — No external assertions—internal hardware throttling only. 01 — **Power-down immediately**: SLPRDY#, SLPMODE, and RSTRDY# are all driven to 0s within 100 µs. This powers off the platform. A system reboot is required. *This is the lowest-latency option.* 10 — **Request S5:** SLPRDY# is asserted after S5-ready; Powers off the platform after sleep-readiness has been checked by the Intel® SCH. A system reboot is required. Once the trip point is reached, SLPRDY# stays asserted even if the trip deasserts before the platform is shut down. *This has the longest latency, but allows for transactions to finish so as to avoid data from being lost/corrupted. However, there is still no assurance of corruption prevention, as functionality to enter S5 is not ensured in the temperature region where catastrophic trip is normally Reserved* 11 — Reserved
25	0 R/WLO	Reserved
24	0 R/W	**PROCHOT# ENABLE (PHE):** When this bit is set, PROCHOT# is asserted on Aux2 trip. 0 = PROCHOT# is not asserted 1 = PROCHOT# can be asserted on Aux2 trip PROCHOT# pulse width has a minimum duration of 500 µs to meet the processor specifications.
23	0 R/W	**SMI on EXTTS1# Thermal Sensor Trip (SME1T):** 1 = SMI is generated on an external Thermal Sensor 1 trip.
22	0 R/W	**SMI on EXTTS0# Thermal Sensor Trip (SME1T):** 1 = SMI is generated on an external Thermal Sensor 0 trip.
21	0 RO	Reserved

(Sheet 2 of 2)

Bit	Default and Access	Description
20	0 R/W	**SMI on Hot Trip (SMHT):** 1 = SMI is generated on a hot trip.
19	0 R/W	**SMI on Aux3 Trip (SMA3T):** 1 = SMI is generated on an Aux3 trip.
18	0 R/W	**SMI on Aux2 Trip (SMA2T):** 1 = SMI is generated on an Aux2 trip.
17	0 R/W	**SMI on Aux1 Trip (SMA1T):** 1 = SMI is generated on an Aux1 trip.
16	0 R/W	**SMI on Aux0 Trip (SMA0T):** 1 = SMI is generated on an Aux0 trip.
15	0 R/W	**SCI on EXTTS1# Thermal Sensor Trip (SCE1T):** 1 = SCI is generated on an external Thermal Sensor 1 trip.
14	0 R/W	**SCI on EXTTS0# Thermal Sensor Trip (SCE1T):** 1 = SCI is generated on an external Thermal Sensor 1 trip.
13	0 RO	Reserved
12	0 R/W	**SCI on Hot Trip (SCHT):** 1 = SCI is generated on a hot trip.
11	0 R/W	**SCI on Aux3 Trip (SCA3T):** 1 = SCI is generated on an Aux3 trip.
10	0 R/W	**SCI on Aux2 Trip (SCA2T):** 1 = SCI is generated on an Aux2 trip.
9	0 R/W	**SCI on Aux1 Trip (SCA1T):** 1 = SCI is generated on an Aux1 trip.
8	0 R/W	**SCI on Aux0 Trip (SCA0T):** 1 = SCI is generated on an Aux0 trip.
7:0	0 RO	Reserved



7.2.7.2 EXTTSCS—External Thermal Sensor Control and Status Register

Offset: B7h Attribute: RO, R/WLO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:6	0000000h RO	Reserved
7	0 R/WLO	**EXTTS1 Enable (EXE1):** 1 = Indicates EXTTS1 is wired and configured for external thermal sensor input.
6:4	0 R/WLO	Reserved
3	00b R/WLO	**EXTTS0 Enable (EXE0):** 1 = Indicates EXTTS0 is wired and configured for external thermal sensor input.
2:0	00b R/WLO	Reserved

7.2.7.3 TSIU[0,1,2,3,4]—Thermal Sensor In Use Register [0,1,2,3,4]

Offset: TSIU0 = C0h Attribute: RO, RS/WC
TSIU1 = C1h
TSIU2 = C2h
TSIU3 = C3h
TSIU4 = C4h
Default Value: 00000000h Size: 32 bits.

Bit	Default and Access	Description
31:1	00000000h RO	Reserved
0	0 RS/WC	**In Use Bit IU[0..4]:** After a full Intel® SCH reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect

7.2.8 Miscellaneous (Port 05h)

Port 05h contains configuration and status registers that don't specifically belong to other ports or interfaces.

7.2.8.1 MSR—Mode and Status Register

Offset: 03h Attribute: RO
Default Value: 0000000Uh Size: 32 bits.

Bit	Default and Access	Description
31:4	0000000h RO	Reserved
3	- RO	**Core Clock Frequency:** This bit indicates the frequency of the core clock and the FSB and Memory interface frequencies. 0 = 100-MHz Core clock, 400-MT/s FSB, 400-MT/s DDR 1 = 133-MHz Core clock, 533-MT/s FSB, 533-MT/s DDR
2:0	- RO	**Graphics Frequency:** This bit indicates the frequency for the graphics core clock. 100 = 200 MHz Others = Reserved

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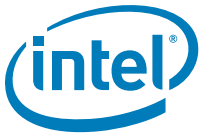


8 Memory Controller (D0:F0)

8.1 Functional Overview

8.1.1 DRAM Frequencies and Data Rates

To reduce design complexity and clock network power, the Intel® SCH maintains a fixed relationship to the FSB clock frequency. The FSB frequency can be 100 MHz or 133 MHz, resulting in support of the following clock frequencies and data rates for DRAM.

FSB Clock	DRAM Clock	DRAM Data Rate	DRAM Type	Peak Bandwidth
100 MHz	200 MHz	400 MT/s	DDR2	3.2 GB/s
133 MHz	266 MHz	533 MT/s	DDR2	4.2 GB/s

8.1.2 DRAM Command Scheduling

The Intel® SCH memory controller operates at the common core clock, which is one half the DDR2 memory clock frequency, or ¼ the DDR data rate. To provide efficient scheduling, the controller is capable of scheduling two operations in the controller core clock to be able to issue a command every memory clock (where scheduling rules for the memory devices allow).

The memory controller operates on up to two requests at a time to provide pipelining for memory commands where possible. It will issue page management commands (activates and precharges) out of order for the later request, but will always service reads and writes (CAS operations) in the order in which they were received by the controller. This provides efficient scheduling while still maintaining in-order rules for compatibility with the FSB IOQ.

The Intel® SCH never uses any additive latency, which is provided for in DDR2 to create a posted CAS effect and improve scheduling efficiency in some memory systems.

8.1.3 Page Management

The memory controller is capable of closing open pages after the pages have been idle for a configurable period of time. This benefits the system for both power and performance (when properly configured). From a performance standpoint, it helps since it can reduce the number of page misses encountered. From a power perspective, it allows the memory devices to reach the precharge power management state (power down when all banks are closed), which has better power saving characteristics on most memory devices than when the pages are left open and the device is in powered down.

Pages that close due to timeout can do so in one of two ways:

- When one or more (but not all) pages in a given rank time out, the pages that have timed out will close provided the rank is awake and timing rules allow. If the rank is powered down, it will be powered up to service individual page closures only if configured to do so. This is not the default behavior; however, this is primarily a performance benefit and can adversely effect power consumption.
- When all of the open pages in a rank have timed out, the memory controller will power up to service page closures.

Note: There is generally a significant power savings by entering the pre-charge powerdown state versus the active powerdown state that is used by the memory devices when pages are still open.

Note: Up to 16 Banks can be independently tracked by the Intel® SCH memory controller.

8.2 DRAM Technologies and Organization

For the Intel® SCH, 512-Mb, 1-Gb and 2-Gb technologies and addressing are supported for x16 devices. The DRAM sub-system supports a single-channel, 64-bits wide, with one or two ranks.

Table 20. DRAM Attributes

Device Size	Width	Page Size	Banks	Bank Addr	Row Addr	Col Addr
512 Mb	X16	2KB	4	BA0-BA1	A0-A12	A0-A9
1024 Mb	X16	2KB	8	BA0-BA2	A0-A12	A0-A9
2048 Mb	X16	2KB	8	BA0-BA2	A0-A13	A0-A9

8.2.1 DRAM Address Mapping

System addresses are decoded by the memory controller to map to the rank, bank, row, and column physical address locations in the populated DRAMs.

8.2.1.1 DRAM Device Address Decode

For any rank, the address range it implements is mapped into the physical address regions of the devices on that rank. This is addressable by bank (B), row (R), and column (C) addresses. Once a rank is selected as described above, the range that it is implementing is mapped into the device's physical address as described in Table 21.

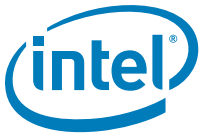


Table 21. DRAM Address Decoder

Topic	Device Density		
	512 Mb	1024 Mb	2048Mb
	x16	x16	x16
Rank Size	256 MB	512 MB	1024MB
Bank Bits	2	3	3
Row Bits	13	13	14
Col Bits	10	10	10
A31	—	—	
A30	—	—	
A29	—	—	R13
A28	—	B2	B2
A27	R12	R12	R12
A26	R11	R11	R11
A25	R10	R10	R10
A24	R9	R9	R9
A23	R8	R8	R8
A22	R7	R7	R7
A21	R6	R6	R6
A20	R5	R5	R5
A19	R4	R4	R4
A18	B1	B1	B1
A17	C9	C9	C9
A16	R3	R3	R3
A15	R2	R2	R2
A14	R1	R1	R1
A13	R0	R0	R0
A12	B0	B0	B0
A11	C8	C8	C8
A10	C7	C7	C7
A9	C6	C6	C6
A8	C5	C5	C5
A7	C4	C4	C4
A6	C3	C3	C3
A5	C2	C2	C2
A4	C1	C1	C1
A3	C0	C0	C0

NOTE: R = Row address bit. C = Column address bit. B = Bank Select bit (SM_BS[2:0]).

8.3 DRAM Clock Generation

The Intel® SCH contains two differential clock pairs (SM_CK[1:0]/SM_CK[1:0]#) that are used to support as many as two ranks of memory on the system board.

8.4 DDR2 On-Die Termination

The Intel® SCH memory controller interface was designed to operate properly without on-die termination. This has resulted is significant power savings, both within the system and within the Intel® SCH. The Intel® SCH contains features to reduce power consumption in the event SSTL termination is used within the system.

8.5 DRAM Power Management

The Intel® SCH supports memory power management in the following conditions:

- C0–C1: CKE Powerdown
- C2–C6: Dynamic Self-Refresh
- S3: Self-Refresh

8.5.1 CKE Powerdown

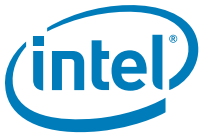
The memory controller employs aggressive use of memory power management features. When a rank is not being accessed, the CKE for that rank is deasserted, bringing the devices into either an active or precharge powerdown state depending on whether any pages are still open in the device.

DDR2 supports slow or fast exit from active powerdown. These options must be configured in the memory devices themselves by BIOS before memory accesses begin. The slower exit improves power savings when in a low power state but comes at a high latency cost. Due to the latency cost this can in some cases have the effect of increasing power consumption if the memory subsystem frequently has to suffer this delay and is consuming full power on the I/O interface in the process. The Intel® SCH will not use the slower exit, opting instead to use the active powerdown as a lighter powerdown mode, but employing page close timers to get to a more power efficient precharge powerdown state when the pages in the rank have been idle for the configured time.

8.5.2 Interface High-Impedance

Although the Intel® SCH is designed to operate properly with no SSTL termination, it provides power saving mechanisms to reduce power consumption if SSTL termination is used. To save power on an SSTL-terminated DDR2 interface, any output signals that are not needed for proper memory operation at that time should be tristated (floated). This is due to the SSTL termination topology which is center-terminated and thus consumes power whenever a signal is driven high or low.

- When both ranks are powered down, address and command pins are tristated.
- Address and command signals are only enabled when a chip select is asserted, floating these signals at all other times.
- When a rank is powered down, the corresponding SM_CS# pins are tristated.
- Data and strobe signals are floated. This occurs whenever the data and strobe are not actively transferring write data (or issuing a preamble or postamble on the strobes).
- The SM_CK/SM_CK# signals are floated whenever both ranks are in self refresh.
- Static disabling is available for preventing unused signals from ever driving. This is provided for SM_BS[2:0], SM_MA[14:13], SM_CK[1:0]/SM_CK[1:0]#, SM_CKE[1:0].



8.5.3 Refresh

The Intel® SCH handles all DRAM refresh operations when the device is not in self-refresh. To reduce the performance impact of DRAM refreshes, the Intel® SCH waits until eight refreshes are required and then issues all of these refreshes. This provides some increase in efficiency (overall lower percentage of impact to the available bandwidth), but there will also be a longer period of time that the memory will be unavailable, roughly 8 x t_{RFC}.

8.5.4 Self-Refresh

Self-refresh can be entered to save power on the memory device and Intel® SCH power to drive the DDR2 differential clock signals. When the memory is in self-refresh, the Intel® SCH disables all output signals, except the SM_CKE signals.

The Intel® SCH will enter self refresh as part of the suspend (S3) sequence. It stays in this the self-refresh state until a resume sequence is initiated.

8.5.5 Dynamic Self-Refresh

In addition, the Intel® SCH can support dynamic self-refresh in C2–C6 states. It wakes the memory from self-refresh state whenever memory access is needed, then re-enter self-refresh state as soon as there are no more requests are needed.

8.5.6 DDR2 Voltage

The Intel® SCH supports 1.8-V and 1.5-V DDR2 memory.

Note: 1.5-V DDR2 support is restricted to single rank operation.

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9 Graphics, Video, and Display (D2:F0)

9.1 Graphics Overview

9.1.1 3-D Core Key Features

Two pipe scaleable unified shader implementation.
- — 3-D Peak Performance
- — Fill Rate: 2 Pixels per clock
- — Vertex Rate: One Triangle 15 clocks (Transform Only)
- — Vertex/Triangle Ratio average = 1 vtx/tri, peak 0.5 vtx/tri

- Texture max size = 2048 x 2048
- Programmable 4x multi-sampling anti-aliasing (MSAA)
  - — Rotated grid
  - — ISP performance related to AA mode, TSP performance unaffected by AA mode
- Optimized memory efficiency using multi-level cache architecture

9.1.2 Shading Engine Key Features

The unified pixel/vertex shader engine supports a broad range of instructions.

- Unified programming model
  - — Multi-threaded with four concurrently running threads
  - — Zero-cost swapping in/out of threads
  - — Cached program execution model – unlimited program size
  - — Dedicated pixel processing instructions
  - — Dedicated vertex processing instructions
  - — 2048 32-bit registers
- SIMD pipeline supporting operations in:
  - — 32-Bit IEEE Float
  - — 2-way, 16-bit fixed point
  - — 4-way, 8-bit integer
  - — 32-bit, bit-wise (logical only)
- Static and Dynamic flow control
  - — Subroutine calls
  - — Loops
  - — Conditional branches
  - — Zero-cost instruction predication
- Procedural Geometry
  - — Allows generation of more primitives on output compared with input data
  - — Effective geometry compression
  - — High order surface support
- External data access
  - — Permits reads from main memory by cache (can be bypassed)
  - — Permits writes to main memory
  - — Data fence facility provided
  - — Dependent texture reads

9.1.3 Vertex Processing

Modern graphics processors perform two main procedures to generate 3-D graphics. First, vertex geometry information is transformed and lit to create a 2-D representation in the screen space. Those transformed and lit vertices are then processed to create display lists in memory. The pixel processor then rasterizes these display lists on a regional basis to create the final image.

The Intel GMA 500 supports DMA data accesses from SDRAM. DMA accesses are controlled by a main scheduler and data sequencer engine. This engine coordinates the data and instruction flow for the vertex processing, pixel processing, and general purpose operations.

Transform and lighting operations are performed by the vertex processing pipeline. A 3-D object is usually expressed in terms of triangles, each of which is made up of three vertices defined by X–Y–Z coordinate space. The transform and lighting process is performed by processing data through the unified shader core. The results of this process are sent to the pixel processing function. The steps to transform and light a triangle or vertex are explained below.

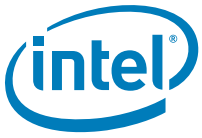
9.1.3.1 Vertex Transform Stages

- **Local space**: Relative to the model itself (e.g., using the model centre at reference point). Prior to being placed into a scene with other objects.
- **World space**: Transform LOCAL to WORLD: This is needed to bring all objects in the scene together into a common coordinate system.
- **Camera space**: Transform WORLD to CAMERA (also called EYE): This is required to transform the world in order to align it with camera view. In OpenGL the local to world and world to camera transformation matrix is combined into one, called the ModelView matrix.
- **Clip space**: Transform CAMERA to CLIP: The projection matrix defines the viewing frustum onto which the scene will be projected. Projection can be orthographic, or perspective. Clip is used because clipping occurs in clip space.
- **Perspective space**: Transform CLIP to PERSPECTIVE: The perspective divide is basically what enables 3-D objects to be projected onto a 2-D space. A divide is necessary to represent distant objects as smaller on the screen. Coordinates in perspective space are called normalized device coordinates ([-1,1] in each axis).
- **Screen space**: Transform PERSPECTIVE to SCREEN: This is where 2-D screen coordinates are finally computed, by scaling and biasing the normalized device coordinates according to the required render resolution.

9.1.3.2 Lighting Stages

Lighting is used to generate modifications to the base color and texture of vertices; examples of different types of lighting are:

- **Ambient** lighting is constant in all directions and the same color to all pixels of an object. Ambient lighting calculations are fast, but objects appear flat and unrealistic.
- **Diffuse** lighting takes into account the light direction relative to the normal vector of the object's surface. Calculating diffuse lighting effects takes more time because the light changes for each object vertex, but objects appear shaded with more three-dimensional depth.
- **Specular** lighting identifies bright reflected highlights that occur when light hits an object surface and reflects back toward the camera. It is more intense than diffuse light and falls off more rapidly across the object surface. Although it takes longer to calculate specular lighting than diffuse lighting, it adds significant detail to the surface of some objects.
- **Emissive** lighting is light that is emitted by an object, such as a light bulb.



9.1.4 Pixel Processing

After vertices are transformed and lit by the vertex processing pipeline, the pixel processor takes the vertex information and generates the final rasterized pixels to be displayed. The steps of this process include removing hidden surfaces, applying textures and shading, and converting pixels to the final display format. The vertex/pixel shader engine is described in Section 9.1.5.

The pixel processing operations also have their own data scheduling function that controls image processor functions and the texture and shader routines.

9.1.4.1 Hidden Surface Removal

The image processor takes the floating-point results of the vertex processing and further converts them to polygons for rasterization and depth processing. During depth processing, the relative positions of objects in a scene, relative to the camera, are determined. The surfaces of objects hidden behind other objects are then removed from the scene, thus preventing the processing of un-seen pixels. This improves the efficiency of subsequent pixel-processing.

9.1.4.2 Applying Textures and Shading

After hidden surfaces are removed, textures and shading are applied. Texture maps are fetched, mipmaps calculated, and either is applied to the polygons. Complex pixel-shader functions are also applied at this stage.

9.1.4.3 Final Pixel Formatting

The pixel formatting module is the final stage of the pixel-processing pipeline and controls the format of the final pixel data sent to the memory. It supplies the unified shader with an address into the output buffer, and the shader core returns the relevant pixel data. The pixel formatting module also contains scaling functions, as well as a dithering and data format packing function.

9.1.5 Unified Shader

The unified shader engine contains a specialized programmable microcontroller with capabilities specifically suited for efficient processing of graphics geometries (vertex shading), graphics pixels (pixel shading), and general-purpose video and image processing programs. In addition to data processing operations, the unified shader engine has a rich set of program-control functions permitting complex branches, subroutine calls, tests, etc., for run-time program execution.

The unified shader core also has a task and thread manager which tries to maintain maximum performance utilization by using a 16-deep task queue to keep the 16 threads full.

The unified store contains 16 banks of 128 registers. These 32-bit registers contain all temporary and output data, as well as attribute information. The store employs features which reduce data collisions such as data forwarding, pre-fetching of a source argument from the subsequent instruction. It also contains a write back queue.

Like the register store, the arithmetic logic unit (ALU) pipelines are 32-bits wide. For floating-point instructions, these correlate to IEEE floating point values. However, for integer instructions, they can be considered as one 32-bit value, two 16-bit values, or four 8-bit values. When considered as four 8-bit values, the integer unit effectively acts like a four-way SIMD ALU, performing four operations per clock. It is expected that in legacy applications pixel processing will be done on 8-bit integers, roughly quadrupling the pixel throughput compared to processing on float formats.

9.1.6 Multi Level Cache

The multi-level cache is a three-level cache system consisting of two modules, the main cache module and a request management and formatting module. The request management module also provides Level-0 caching for texture and unified shader core requests.

The request management module can accept requests from the data scheduler, unified shaders and texture modules. Arbitration is performed between the three data streams, and the cache module also performs any texture decompression that may be required.

9.2 Video Decode Overview

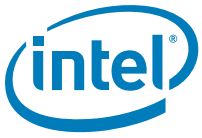
The video decode accelerator improves video performance/power by providing hardware-based acceleration at the macroblock level (variable length decode stage entry point). The Intel® SCH supports full hardware acceleration of the following video decode standards.

Table 22. Hardware-Accelerated Video Codec Support

Codec	Profile	Level	Note
H.264	Baseline profile	L3	
H.264	Main profile	L4.1 (1080i @ 30fps)	
H.264	High profile	L4.1 (1080i @ 30fps)	
MPEG2	Main profile	High	
MPEG4	Simple profile	L3	
MPEG4	Advanced simple profile	L5	
VC1	Simple profile	Medium	
VC1	Main profile	High	
VC1	Advanced profile	L3 up to (1080i @ 30fps)	
WMV9	Simple profile	Medium	
WMV9	Main profile	High	

The video decode function is performed in four processing modules:

- Entropy coding processing
- Motion compensation
- Deblocking
- Final pixel formatting



9.2.1 Entropy Coding

The entropy encoding module serves as the master controller for the video accelerator. The master data stream control and bitstream parsing functions for the macroblock level and below are performed here. Required control parameters are sent to the motion compensation and deblocking modules.

The macroblock bitstream parsing performs the entropy encoding functions for VLC, CALVC, and CABAC techniques used in video codecs. The entropy encoding module also performs the motion vector reconstruction using the motion vector predictors.

After entropy encoding, the iDCT coefficients are extracted and inverse scan ordered. Then inverse quantization, rescaling, and AC/DC coefficient processing is performed.

The re-scaled coefficients are passed to the Inverse Transform engine for processing. The Hadamard transform is also supported and performed here. The inverse-transformed data is connected to the output port of entropy coding module, which provides the residual data to the motion compensation module.

9.2.2 Motion Compensation

The entropy encoder or host can writes a series of commands to define the type of motion predication used. The motion predicated data is then combined with residual data, and the resulting reconstructed data is passed to the de-blocker.

The Motion Compensation module is made-up of four sub-modules:

- The Module Control Unit module controls the overall motion compensation operation. It parses the command stream to detect errors in the commands sent, and extracts control parameters for use in later parts of the processing pipeline. The Module Control Unit also accepts residual data (either direct from VEC or by a system register), and re-orders the frame/field format to match the predicted tile format.
- The Reference Cache module accepts the Inter/Intra prediction commands, along with the motion vectors and index to reference frame in the case of Inter prediction. The module calculates the location of reference data in the frame store (including out-of-bounds processing requirements). The module includes cache memory which is checked before external system memory reads are requested (the cache can significantly reduce system memory bandwidth requirements). In H264 mode, the module also extracts and stores Intra boundary data which is used in Intra prediction. The output of the Reference Cache is passed to the 2-D filter module.
- The 2-D filter module implements up to 8-tap Vertical and Horizontal filters to generate predicted data for sub-pixel motion vectors (to a resolution of up-to 1/8th of a pixel). The 2-D filter module also generates H264 Intra prediction tiles (based on the Intra prediction mode and boundary data extracted by the Reference Cache). For VC1 and WMV9, the 2-D filter module also implements Range scaling and Intensity Compensation on Inter reference data prior to sub-pixel filtering.
- The Pixel Reconstruction Unit combines predicted data from the 2-D filter with the re-ordered residual data from the Module Control Unit. In the case of Bi-directional macroblocks with two motion vectors per tile, the Pixel Reconstruction Unit combines the two tiles of predicted data prior to combining the result with residual data. In the case of H264, the Pixel Reconstruction Unit also implements Weighted Averaging. The final reconstructed data is then passed to the VDEB for de-blocking (as well as being fed-back to Reference Cache so that Intra boundary data can be extracted).

9.2.3 Deblocking

The deblocking module is responsible for codec back-end video filtering. It is the last module within the high definition video decoder module pipeline. The deblocking module performs overlap filtering and in-loop deblocking of the reconstructed data generated by the motion-compensation module. The frames generated are used for display and for reference of subsequent decoded frames.

The deblocking module performs the following specific codec functions:

- H.264 Deblocking, including ASO modes
- VC-1/WMV9 overlap filter and in-loop deblocking
- Range-mapping
- Pass-through of reconstructed data for codec-modes that don't require deblocking (MPEG2, MPEG4).

9.2.4 Output Reference Frame Storage Format

Interlaced pictures (as opposed to progressive pictures) are always stored in system memory as interlaced frames, including interlaced field pictures.

9.2.4.1 Pixel format

The pixel format has the name 420PL12YUV8. This consists of a single plane of luma (Y) and a second plane consisting of interleaved Cr/Cb (V/U) components. For 420PL12YUV8, the number of chroma samples is a quarter of the quantity of luma samples – half as many vertically, half as many horizontally.

Table 23. Pixel Format for the Luma (Y) Plane

Bit	Symbol	Description
63:56	Y7[7:0]	8-bit Y luma component
55:48	Y6[7:0]	8-bit Y luma component
47:40	Y5[7:0]	8-bit Y luma component
39:32	Y4[7:0]	8-bit Y luma component
31:24	Y3[7:0]	8-bit Y luma component
23:16	Y2[7:0]	8-bit Y luma component
15:8	Y1[7:0]	8-bit Y luma component

Table 24. Pixel Formats for the Cr/Cb (V/U) Plane (Sheet 1 of 2)

Bit	Symbol	Description
Format 1		
7:0	Y0[7:0]	8-bit Y luma component
63:56	U3[7:0]	8-bit U/Cb chroma component
55:48	V3[7:0]	8-bit V/Cr chroma component
47:40	U2[7:0]	8-bit U/Cb chroma component
39:32	V2[7:0]	8-bit V/Cr chroma component
31:24	U1[7:0]	8-bit U/Cb chroma component
23:16	V1[7:0]	8-bit V/Cr chroma component
15:8	U0[7:0]	8-bit U/Cb chroma component
7:0	V0[7:0]	8-bit V/Cr chroma component

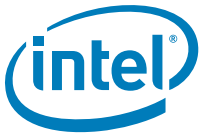


Table 24. Pixel Formats for the Cr/Cb (V/U) Plane (Sheet 2 of 2)

Bit	Symbol	Description
Format 2 (Cr and Cb are reversed relative to Format 1)		
63:56	V3[7:0]	8-bit U/Cr chroma component
55:48	U3[7:0]	8-bit V/Cb chroma component
47:40	V2[7:0]	8-bit U/Cr chroma component
39:32	U2[7:0]	8-bit V/Cb chroma component
31:24	V1[7:0]	8-bit U/Cr chroma component
23:16	U1[7:0]	8-bit V/Cb chroma component
15:8	V0[7:0]	8-bit U/Cr chroma component
7:0	U0[7:0]	8-bit V/Cb chroma component

9.3 Display Overview

The Intel® SCH display output can be divided into three stages:

- Planes
  - — Request/Receive data from memory
  - — Format memory data into pixels
  - — Handle fragmentation, tiling, physical address mapping
- Pipes
  - — Generate display timing
  - — Scaling, LUT
- Ports
  - — Format pixels for output (SDVO, LVDS)
  - — Interface to physical layer

9.3.1 Planes

The Intel® SCH contains a variety of planes (such as, Display and Cursor). A plane consists of rectangular shaped image that has characteristics (such as, source, size, position, method, and format). These planes get attached to source surfaces, which are rectangular areas in memory with a similar set of characteristics. They are also associated with a particular destination pipe.

- Display Plane - The primary and secondary display plane works in an indexed mode, hi-color mode or a true color mode. The true color mode allows for an 8-bit alpha channel. One of the primary operations of the display plane is the set mode operation. The set-mode operation occurs when it is desired to enable a display, change the display timing, or source format. The secondary display plane can be used as a primary surface on the secondary display or as a sprite planes on either the primary or secondary display.
- Cursor Plane - The cursor plane is one of the simplest display planes. With a few exceptions, the cursor plane supports sizes of 64 x 64, 128 x 128 and 256 x 256 fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted.
- VGA Plane - VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. VGA Timings are generated based on the VGA register values (the hi-resolution timing generator registers are not used).

Note: The Intel® SCH has limited support for a VGA Plane. The VGA plane is suitable for usages such as BIOS boot screens, pre-OS splash screens, etc. Other usages of the VGA plane (like DOS-based games, for example) are not supported.

9.3.2 Display Pipes

The display consists of two pipes:

- Display Pipe A
- Display Pipe B

A pipe consists of a set of combined planes and a timing generator. The timing generators provide timing information for each of the display pipes. The Intel® SCH has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe.

Pipe A can operate in a single-wide mode.

The Clock Generator Units (DPLLA and DPLLB) provide a stable frequency for driving display devices. It operates by converting an input reference frequency into an output frequency. The timing generators take their input from internal DPLL devices that are programmable to generate pixel clocks in the range of 25 MHz–180 MHz.

9.3.3 Display Ports

Display ports are the destination for the display pipe. These are the places where the display data finally appears to devices outside the graphics device. The Intel® SCH has one dedicated LVDS port and one SDVO port.

Since the Intel® SCH has two display ports available for its two pipes, it can support up to two different images on two different display devices. Timings and resolutions for these two images may be different.

9.3.3.1 LVDS Port

Display Pipe B supports output to the LVDS display port. The LVDS port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then locked into the registers to prevent unwanted corruption of the values. From that point on, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA. The timing signals will remain stable and active through mode changes. These mode changes include VGA to VGA, VGA to HiRes, HiRes to VGA, and HiRes to HiRes.

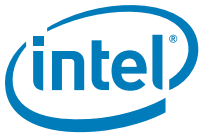
The transmitter can operate in a variety of modes and supports several data formats. The serializer supports 6-bit or 8-bit color per lane (for 18-bit and 24-bit color respectively) and single-channel operating modes. The display stream from the display pipe is sent to the LVDS transmitter port at the dot clock frequency, which is determined by the panel timing requirements. The output of LVDS is running at a fixed multiple of the dot clock frequency.

The single LVDS channel can take 18 or 24 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on four differential data pair outputs.

This display port is normally used in conjunction with the pipe functions of panel up-scaling and 6-to 8-bit dither. This display port is also used in conjunction with the panel power sequencing and additional associated functions.

When enabled, the LVDS constant current drivers consume significant power. Individual pairs or sets of pairs can be selected to be powered down when not being used. When disabled, individual or sets of pairs will enter a low power state. When the port is disabled, all pairs enters a low power mode. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

A maximum pixel clock of 112 MHz is supported for the LVDS interface.



9.3.3.2 SDVO Digital Display Port

Display Pipe A is configured to use the SDVO port. The SDVO port can support a variety of display types (VGA, LVDS, DVI, TV-Out, etc.) by an external SDVO device. SDVO devices translate SDVO protocol and timings to the desired display format and timings.

A maximum pixel clock of 160 MHz is supported on the SDVO interface.

9.3.3.2.1 SDVO DVI/HDMI

DVI (and HDMI), a 3.3-V interface standard supporting the TMDS protocol, is a prime candidate for SDVO. The Intel® SCH provides an unscaled mode where the display data is centered within the attached display area. Monitor Hot Plug functionality is supported.

9.3.3.2.2 SDVO LVDS

The Intel® SCH can use the SDVO port to drive an LVDS transmitter. Flat Panel is a fixed resolution display. The Intel® SCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The Intel® SCH provides an unscaled mode where the display data is centered within the attached display area. Scaling in the LVDS transmitter through the SDVO stall input pair is also supported.

9.3.3.2.3 SDVO TV-Out

The SDVO port supports both standard and high-definition TV displays in a variety of formats. The SDVO port generates the proper blank and sync timing, but the external encoder is responsible for generation of the proper format signal and output timings.

The Intel® SCH will support NTSC/PAL/SECAM standard definition formats. The Intel® SCH will generate the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal.

The TV-out interface on the Intel® SCH is addressable as a master device. This allows an external TV encoder device to drive a pixel clock signal on SDVO_TVCLKIN[+/-] that the Intel® SCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.

9.3.3.2.4 Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing will be generated with pixel granularity to allow more overscan ratios to be supported.

9.3.3.2.5 Control Bus

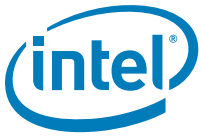
The SDVO port defines a two-wire (SDVO_CTRLCLK and SDVO_CTRLDATA) communication path between the SDVO device and Intel® SCH. Traffic destined for the PROM or DDC will travel across the Control bus, and will then require the SDVO device to act as a switch and direct traffic from the Control bus to the appropriate receiver. The Control bus is able to operate at up to 1 MHz.

9.4 Configuration Registers

Table 25. Graphics and Video PCI Configuration Register Address Map

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	8108h	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0000h	RO
08h	RID	Revision Identification	see description	RO
09h–0Bh	CC	Class Codes	03U000h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	MEM_BASE	Memory Mapped Base Address	00000000h	RO, R/W
14h–17h	IO_BASE	I/O Base Address	00000000h	RO, R/W
18h–1Bh	GMEM_BASE	Graphics Memory Base Address	00000000h	RO, R/W, R/WLOR/WLO
1Ch–1Fh	GTT_BASE	Graphics Translation Table Range Address	00000000h	RO, R/W
2Ch–2Fh	SS	Subsystem Identifiers	See description	RO
34h	CAP_PTR	Capabilities Pointer	D0h	RO
3Ch	INT_LN	Interrupt Line	00h	RO
3Dh	INT_PN	Interrupt Pin	See description	RO
52h–53h	GC	Graphics Control	0030h	RO, R/W
58h–5Bh	SSRW	Software Scratch Read Write	00000000h	R/W
5Ch–5Fh	BSM	Base of Stolen Memory	00000000h	RO, R/W
90h	MSI_CAPID	MSI Capability ID	05h	RO
91h	NXT_PTR3	Next Item Pointer 3	00h	RO
92h–93h	MSI_CTL	MSI Message Control	0000h	RO, R/W
94h–97h	MSI_ADR	MSI Message Address	00000000h	RO, R/W
98h–99h	MSI_DATA	MSI Message Data	0000h	RO, R/W
B0h	VEND_CAPID	Vendor Capability ID	09h	RO
B1h	NXT_PTR2	Next Item Pointer 2	See description	RO
C4h	FD	Function Disable	00000000h	RO, R/W
D0h	PM_CAPID	Power Management Capabilities ID	01h	RO
D1h	NXT_PTR1	Next Item Pointer 1	B0h	RO
D2h–D3h	PM_CAP	Power Management Capabilities	0022h	RO
D4h–D5h	PM_CTL_STS	Power Management Control/Status	0000h	RO, R/W
E0h–E1h	SWSCISMI	Software SCI/SMI	0000h	R/W, R/WO
E4h–E7h	ASLE	System Display Event Register	See description	R/W
F0h	GCR	Graphics Clock Ratio	See description	R/W
F4h–F7h	LBB	Legacy Backlight Brightness	See description	R/W
FCh–FFh	ASLS	ASL Storage	00000000h	R/W

NOTE: Address locations that are not shown should be treated as Reserved.



9.4.1 VID—Vendor Identification Register

Register Address: 00–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Default and Access	Description
15:0	8086h RO	**Vendor Identification Number (VID):** PCI standard identification for Intel.

9.4.2 DID—Device Identification Register

Register Address: 02h Attribute: RO
Default Value: 810xh Size: 16 bits

Bit	Default and Access	Description
15:0	8108-810Fh RO	**Device Identification Number (DID):** This is a 16-bit value assigned to the Graphics controller. Refer to the Intel® SCH Specification Update for the DID for various product SKU.

9.4.3 PCICMD—PCI Command Register

Register Address: 04–05h Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:11	00h RO	Reserved
10	0 R/W	**Interrupt Disable (ID):** This bit disables the device from asserting INTx#. 0 = Enables the assertion of this device's INTx# signal. 1 = Disables the assertion of this device's INTx# signal.
9:3	0 RO	Reserved
2	0 R/W	**Bus Master Enable (BME):** Enables the Intel Graphics Media Adapter to function as a PCI compliant master.
1	0 R/W	**Memory Space Enable (MSE):** When set, accesses to this device's memory space is enabled.
0	0 R/W	**I/O Space Enable (IOSE):** When set, accesses to this device's I/O space is enabled.

9.4.4 PCISTS—PCI Status Register

Register Address: 06-07h Attribute: RO, R/W
Default Value: 00000000h Size: 16 bits

Bit	Default and Access	Description
15:5	0 RO	Reserved
4	1 RO	**Capability List (CAP):** This bit indicates that the register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list.
3	0 RO	**Interrupt Status (IS):** This bit reflects the state of the interrupt in the device in the graphics device.
2:0	000b RO	Reserved

9.4.5 RID—Revision Identification

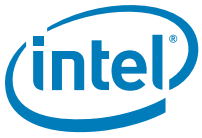
Register Address: 08h Attribute: RO
Default Value: See description Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the value of the Revision ID Register.

9.4.6 CC—Class Codes Register

Register Address: 09–0Bh Attribute: RO
Default Value: 030000h Size: 24 bits

Bit	Default and Access	Description
23:16	03h RO	**Base Class Code (BCC):** Indicates a display controller.
15:8	00h RO	**Sub-Class Code (SCC):** When GC.VD is cleared, this value is 00h. When GC.VD is set, this value is 80h.
7:0	00h RO	**Programming Interface (PI):** Indicates a display controller.



9.4.7 HEADTYP—Header Type Register

Register Address: 0Eh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7	0 RO	**Multi Function Status (MFunc):** Integrated graphics is a single function.
6:0	0000000b RO	**Header Code (HDR):** Indicates a Type 0 header format.

9.4.8 MEM_BASE—Memory Mapped Base Address Register

Register Address: 10h–13h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

This register requests allocation for the Intel Graphics Media Adapter registers and instruction ports. The allocation is for 512 KB.

Bit	Default and Access	Description
31:19	0000h R/W	**Base Address (BA):** Set by the OS, these bits correspond to Address Signals 31:19.
18:1	0000h RO	Reserved
0:0	0 RO	**Resource Type (RTE):** Indicates a request for memory space.

9.4.9 IO_BASE—I/O Base Address Register

Register Address: 14h–17h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

This register provides the base offset of 8 bytes of I/O registers within this device. Access to I/O space is allowed in the D0 state and CMD.IOSE is set. Access is disallowed in states D1–D3 or if CMD.IOSE is cleared or if this device is disabled. Access to this space is independent of VGA functionality.

Bit	Default and Access	Description
31:16	0000h RO	Reserved
15:3	0000h R/W	**Base Address (BA):** Set by the OS, these bits correspond to Address Signals 15:3.
2:1	00b RO	Reserved
0:0	1 RO	**Resource Type (RTE):** Indicates a request for I/O space.

9.4.10 GMEM_BASE—Graphics Memory Base Address Register

Register Address: 18h–1Bh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

This register provides the base address of the graphics aperture within this device. Accesses to the graphics aperture use the address translation logic of the memory management unit within the graphics core.

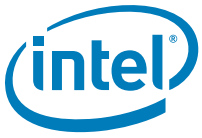
Note: Accesses to the graphics aperture are only permitted if the internal memory requesters of the graphics core are not enabled.

Bit	Default and Access	Description
31:29	000b R/W	**Base Address (BA):** Set by the OS, these bits correspond to Address Signals 31:29.
28	0b RO	Reserved
27	0b R/WLO	**256-MB Address Mask (M256):** This bit is either part of the Memory Base Address (RW) or part of the Address Mask (RO), depending on the value of MSAC.UAS.
26:1	0s RO	Reserved
0	0 RO	**Resource Type (RTE):** Indicates a request for memory space.

9.4.11 GTT_BASE—Graphics Translation Table Base Address Register

Register Address: 1Ch–1Fh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:19	0000h R/W	**Base Address (BA):** Set by the OS, these bits correspond to Address Signals 31:19.
18	0b R/WLO	Reserved
17	0b R/WLO	**256-KB Address Mask (M256):** This bit is either part of the GTT Base Address (RW) or part of the Address Mask (RO), depending on the value of MSAC.UAS
16:1	0s RO	Reserved
0	0 RO	**Resource Type (RTE):** Indicates a request for memory space.



9.4.12 SS—Subsystem Identifiers

This register matches the value written to the LPC bridge.

9.4.13 CAP_PTR—Capabilities Pointer Register

Register Address:	34h	Attribute:	RO, R/W
Default Value:	00D0h	Size:	8 bits

Bit	Default and Access	Description
7:0	D0h RO	**Pointer (PTR):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List.

9.4.14 INT_LN—Interrupt Line Register

Register Address:	3Ch	Attribute:	RO, R/W
Default Value:	00h	Size:	8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Interrupt Line (ILIN):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this bit.

9.4.15 INT_PN—Interrupt Pin Register

Register Address:	3Dh	Attribute:	RO
Default Value:	See Description	Size:	16 bits

Bit	Default and Access	Description
7:0	Desc RO	**Interrupt Pin (IPIN):** This value reflects the value of D02IP.GP in the LPC configuration space.

9.4.16 GC—Graphics Control Register

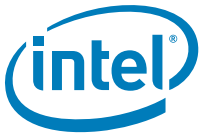
Register Address: 52h–53h
Default Value: 0030h
Attribute: RO, R/W
Size: 16 bits

Bit	Default and Access	Description
15:7	0 RO	Reserved
6:4	011b R/W	**Graphics Mode Select (GMS):** This field is used to select the amount of memory pre-allocated to support the graphics device in VGA (non-linear) and Native (linear) modes. If graphics is disabled, this value must be programmed to 000h. **Bits 6:4 / Description** 000 — No memory pre-allocated. Graphics does not claim VGA cycles (Mem and I/O), and CC.SCC is 80h. 001 — 1 MB of memory pre-allocated for frame buffer. 010 — 4 MB of memory pre-allocated for frame buffer. 011 — 8 MB of memory pre-allocated for frame buffer. others — reserved This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. Hardware does not clear or set any of these bits automatically based on the Intel Graphics Media Adapter being disabled/ enabled.
3:2	00b RO	Reserved
1	0 RO	**VGA Disable (VD)** 0 = VGA memory and I/O cycles are enabled, and CC.SCC is set to 00h. 1 = VGA memory or I/O cycles are not claimed, and CC.SCC is set to 80h.
0	0 RO	Reserved

9.4.17 SSRW—Software Scratch Read / Write Register

Register Address: 58h–5Bh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Default and Access	Description
31:0	0 R/W	**Scratch (S):** Scratchpad bits



9.4.18 BSM—Base of Stolen Memory Register

Register Address: 5Ch–5Fh Attribute: RO, R/W
Default Value: 07800000h Size: 32 bits

Bit	Default and Access	Description
31:20	078h R/W	**Base of Stolen Memory (BSM):** This field contains bits 31:20 of the base address of stolen DRAM memory.
19:0	00000h RO	Reserved

9.4.19 MSAC—Multi Size Aperture Control

Register Address: 62h Attribute: RO, R/W
Default Value: 02hh Size: 8 bits

This register determines the size of the graphics memory aperture. By default, the aperture size is 256 MB. Only BIOS writes this register based on address allocation efforts. Drivers may read this register to determine the correct aperture size. BIOS must restore this data upon S3 resume.

Bit	Default and Access	Description
7:4	0h R/W	**Scratch Bits (SCRATCH):** These bits have no physical effect on hardware.
3:2	00b RO	Reserved
1:0	10b RW	**Untrusted Aperture Size (UAS):** Indicates the size of the untrusted aperture space.

Bits 1:0	Description
11	128 MB. Bits 28 and 27 of GTT_BASE are read-write limiting the address space to 128MB.
10	256 MB. Bit 28 is read-write and bit 27 of GTT_BASE is read-only limiting the address space to 256MB.
01	Reserved
00	Reserved

9.4.20 MSI_CAPID—MSI Capability Register

Register Address: 90h
Default Value: 05h
Attribute: RO
Size: 8 bits

Bit	Default and Access	Description
7:0	05h RO	**Capability ID (ID):** Indicates a Messaged Signal Interrupt capability.

9.4.21 NXT_PTR3—Next Item Pointer #3 Register

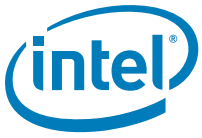
Register Address: 91h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Pointer to Next Capability (NEXT):** 00h indicates this is the last capability in the list.

9.4.22 MSI_CTL—Message Control Register

Register Address: 92h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Default and Access	Description
15:8	00h RO	Reserved
7:7	0 RO	**64-bit Address Capable (C64):** 32-bit capable only
6:4	000b R/W	**Multiple Message Enable (MME):** This field is R/W for software compatibility, but only a single message is ever generated.
3:1	000b RO	**Multiple Message Capable (MMC):** This device is only single message capable.
0	0 R/W	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupts are not used to generate interrupts. CMD.BME must be set for an MSI to be generated.



9.4.23 MSI_ADR—Message Address Register

Register Address: 94-97h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

A read from this register produces undefined results.

Bit	Default and Access	Description
31:2	0 R/W	**Address (ADDR):** Lower 32-bits of the system specified message address, always DWord aligned.
1:0	00b RO	Reserved

9.4.24 MSI_DATA—Message Data Register

Register Address: 98-99h Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:0	0000h R/W	**Data (DATA):** This 16-bit field is programmed by system software and is driven onto the lower word of data during the data phase of the MSI write transaction.

9.4.25 VEND_CAPID—Vendor Capability Register

Register Address: B0h Attribute: RO
Default Value: 09h Size: 8 bits

Bit	Default and Access	Description
7:0	09h RO	**Capability ID (ID):** 09h indicates a vendor-specific capability.

9.4.26 NXT_PTR2—Next Item Pointer #2 Register

Register Address: B1h Attribute: RO
Default Value: 90h/00h Size: 8 bits

Bit	Default and Access	Description
7:0	90h/00h RO	**Pointer to Next Capability (NEXT):** 90h indicates the address of the next capability. However, if the FD.MD bit is set, the MSI capability will be disabled and this register will report 00h indicating the Power Management capability is the last capability in the list.

9.4.27 FD—Function Disable Register

Register Address: C4h–C7h
Default Value: 00000000h
Attribute: RO, R/W
Size: 32 bits

Bit	Default and Access	Description
31:2	0s RO	Reserved
1	0 R/W	**MSI Disable (MD):** When set, the MSI capability pointer is not available. The item which points to the MSI capability (NXT_PTR2) will, instead, indicate that this is the last item in the list.
0	0 R/W	**Disable (D)** 1 = D2:F0 is disabled.

9.4.28 PM_CAPID—Power Management Capabilities ID Register

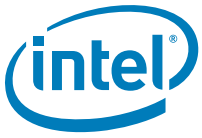
Register Address: D0h
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Default and Access	Description
7:0	01h RO	**Capabilities ID (CAPID):** This ID is 01h for power management.

9.4.29 NXT_PTR1—Next Item Pointer #1 Register

Register Address: D1h
Default Value: B0h
Attribute: RO
Size: 8 bits

Bit	Default and Access	Description
7:0	B0h RO	**Pointer to Next Capability (NEXT):** B0h indicates the address of the next capability.



9.4.30 PM_CAP—Power Management Capabilities Register

Register Address: D2h–D3h
Default Value: 0022h
Attribute: RO, R/W
Size: 16 bits

Bit	Default and Access	Description
15:11	00h RO	**PME Support (PMES):** The Intel Graphics Media Adapter does not generate PME#.
10	0 RO	**D2 Support (D2S):** The D2 power management state is not supported.
9	0 RO	**D1 Support (D1S):** The D1 power management state is not supported.
8:6	000b RO	Reserved
5	1 RO	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the Intel Graphics Media Adapter is required before generic class device driver is to use it.
4:3	00b RO	Reserved
2:0	010b RO	**Version (VS):** Indicates compliance with *PCI Power Management Specification, Revision 1.1*.

9.4.31 PM_CTL_STS—Power Management Control/Status Register

Register Address: D4h–D5h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Default and Access	Description
15:2	0000h RO	Reserved
1:0	00b R/W	**Power State (PS):** This field indicates the current power state of graphics and can be used to set graphics into a new power state. If software attempts to write an unsupported state to this field, the data is discarded and no state change occurs. 00 = D0 (Default) 01 = D1 (Not supported) 10 = D2 (Not supported) 11 = D3

9.4.32 SWSCISMI—Software SCI/SMI Register

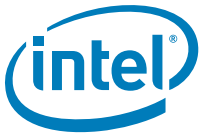
Register Address: E0h–E1h Attribute: R/W, R/WO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15	0 R/WO	**SMI or SC Event Select (MCS):** 0 = SMI is selected. 1 = SCI is selected.
14:1	0s R/W	**Software Scratch Bits (SS):** Used by software. No hardware functionality.
0	0 R/W	**Software SCI Event (SWSCI):** If MCS is set, setting this bit causes an SCI.

9.4.33 ASLE—System Display Event Register

Register Address: E4h–E7h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:24	00h R/W	**ASLE Scratch Trigger 3 (AST3):** When written, this scratch byte triggers an interrupt when IEF-Bit 0 is enabled and IMR-Bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	00h R/W	**ASLE Scratch Trigger 2 (AST2):** Same definition as AST3.
15:8	00h R/W	**ASLE Scratch Trigger 1 (AST1):** Same definition as AST3.
7:0	00h R/W	**ASLE Scratch Trigger 0 (AST0):** Same definition as AST3.



9.4.34 GCR—Graphics Clock Ratio Register

Register Address: F0h–F3h Attribute: RO, R/W
Default Value: 00000002h Size: 32 bits

Bit	Default and Access	Description
31:2	RO	Reserved
3:2	10b R/W	**Graphics 2x Clock to Graphics Clock Ratio:** The field is used to configure the graphics 2-D processing engine. 01 = ratio is 2:1 All other encodings are reserved.
1:0	10b R/W	**Graphics Clock to Core Clock Ratio (GCCR)**: Set by BIOS to correctly configure the graphics clock frequency as a function of the Intel® SCH core clock frequency. 01 = ratio is 1:1 for 100-MHz FSB operation 10 = ratio is 3:2 for 133-MHz FSB operation All other encodings are reserved.

9.4.35 LBB—Legacy Backlight Brightness Register

Register Address: F4h–F7h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:24	00h R/W	**LBPC Scratch Trigger 3 (LST3):** When enabled by internal register bits, a write to this range triggers an display event interrupt. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	00h R/W	**LBPC Scratch Trigger 2 (LST2):** Same definition as LST3
15:8	00h R/W	**LBPC Scratch Trigger 1 (LST1):** Same definition as LST3
7:0	00h R/W	**Legacy Backlight Brightness (LBES):** The value of zero is the lowest brightness setting and 255 is the brightest. If field LBES is written as part of a 16-bit (word) or 32-bit (dword) write to LBB, this will cause a flag to be set (LBES) in the PIPEBSTATUS register and cause an interrupt if Backlight event in the PIPEBSTATUS register and cause an Interrupt if Backlight Event (LBEE) and Display B Event is enabled by software. (If field LBES is written as a (one) byte write to LBB (i.e., if only least significant byte of LBB is written), no flag or interrupt will be generated.)

9.4.36 ASLS—ASL Storage Register

Register Address: FCh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0s R/W	**Scratchpad (SP):** This definition of this scratch register is worked out in common between System BIOS and driver software. Storage for up to six devices is possible. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/Non VGA), one bit for _DGS (enable/disable requested), and two bits for DCS (enabled now/ disabled now, connected or not).

§ §

10 Intel® HD Audio (D27:F0)

10.1 Functional Overview

The controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and an external codec(s). The Intel® SCH controller communicates with the external codec(s) over the Intel HD Audio serial link. The Intel® SCH implements two output DMA engines and two input DMA engines. The output DMA engines move digital data from system memory to a D-A converter in a codec. The Intel® SCH implements a single Serial Data Output signal (HDA_SDOUT) that is connected to all external codecs. The input DMA engines move digital data from the A-D converter in the codec to system memory. The Intel® SCH supports up to two external codecs by implementing two Serial Digital Input signals (HDA_SDI[1:0]).

Audio software renders outbound and processes inbound data to/from buffers in system memory. The location of individual buffers is described by a Buffer Descriptor List (BDL) that is fetched and processed by the controller. The data in the buffers is arranged in a predefined format. The output DMA engines fetch the digital data from memory and reformat it based on the programmed sample rate, bit/sample and number of channels. The data from the output DMA engines is then combined and serially sent to the external codecs over the Intel HD Audio link. The input DMA engines receive data from the codecs over the Intel HD Audio link and format the data based on the programmable attributes for that stream. The data is then written to memory in the predefined format for software to process. Each DMA engine moves one stream of data. A single codec can accept or generate multiple streams of data, one for each A-D or D-A converter in the codec. Multiple codecs can accept the same output stream processed by a single DMA engine.

Codec commands and responses are also transported to and from the codecs by DMA engines. The DMA engine dedicated to transporting commands from the Command Output Ring Buffer (CORB) in memory to the codec(s) is called the CORB engine. The DMA engine dedicated to transporting responses from the codec(s) to the Response Input Ring Buffer in memory is called the RIBR engine. Every command sent to a codec yields a response from that codec. Some commands are “broadcast” type commands in which case a response will be generated from each codec. A codec may also be programmed to generate unsolicited responses, which the ROBR engine also processes. The Intel® SCH also supports Programmed I/O-based Immediate Command/Response transport mechanism that can be used by BIOS for memory initialization.

10.1.1 Docking

The Intel® SCH controls an external switch that is used to isolate a codec in the docking station. When docking occurs, software is notified by ACP, and initiates the docking sequence. The Intel® SCH manages the switch such that the electrical connection between the dock codec and the Intel HD Audio interface occurs during the proper time within the frame sequence and when the signals are not transitioning.

The Intel® SCH drives a dedicated reset signal to dock codec(s). It sequences the switch control and dedicated signal such that the dock codec experiences a “normal” reset as specified in the Intel HD Audio specification.

The user normally requests undocking. Software halts streams to the codecs in the docking station and initiates the undocking sequence. The Intel® SCH asserts dock reset and manages the external switch to electrically isolate the dock codec. Electrical isolation during surprise undocking is handled external to the Intel® SCH, and software invokes the undocking sequence as part of the clean-up process to prepare for a subsequent docking event.

10.1.1.1 Dock Sequence

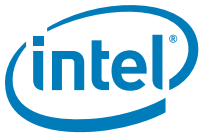
This sequence is followed when the system is running and a docking event occurs as well as when resuming from S3 (RESET# asserted) and Intel HD Audio controller D3.

- ECAP.DS defaults to set. BIOS may clear this bit to effectively turn off the docking feature.
- After reset, GCTL.DA and GSTS.DM are cleared, HDA_DOCK_EN# deasserted and HDA_DOCKRST# asserted. H_CLKIN, HDA_SYNC HDA_SDO may or may not be running.
- A docking event is signaled to software through ACPI control methods. How this is done is outside the scope the spec.
- Software first checks that the docking is supported (ECAP.DS set) and that GSTS.DM is cleared and initiates the docking sequence by setting GCTL.DA.
- The Intel® SCH asserts HDA_DOCK_EN# synchronously to H_CLKIN and timed such that H_CLKIN is low, HDA_SYNC is low, and HDA_SDO is low. In the Intel® SCH, the first 8 bits of the Command field are “reserved” and driven to 0s, creating a predictable point in time to assert HDA_DOCK_EN#.
- After it asserts HDA_DOCK_EN#, it waits for a minimum of 2400 FSB clocks and deasserts HDA_DOCKRST#, synchronous to H_CLKIN and timed such that there are least 4 H_CLKIN clock periods from the deassertion of HDA_DOCKRST# to the first frame HDA_SYNC assertion.
- The Connect/Turnaround/Address Frame hardware initialization sequence occurs on dock codecs' SDI line. A dock codec is detected when SDI is high on the last H_CLKIN cycle of the Frame HDA_SYNC of a Connect Frame. The appropriate bit(s) in the State Change Status (STATESTS) register are set. The Turnaround and Address Frame initialization sequence then occurs on the dock codecs’ SDI(s).
- After the sequence is complete, the Intel® SCH sets GSTS.DM indicating the dock is mated and that software can begin codec discovery, enumeration, and configuration. Software discovers dock codecs by comparing the bits now set in the STATSTS register with the bits that were set prior to docking.

10.1.1.2 Undock Sequence

There are two possible undocking scenarios. The first is the one that is initiated by the user that invokes software and gracefully shuts down the dock codecs before they are undocked. The second is referred to as the “surprise undock” where the user undocks while the dock codec is running. Both of these situations appear the same to the controller as it is not cognizant of the “surprise removal”

- In the docked quiescent state, GCTL.DA and GSTS.DM are asserted. HDA_DOCK_EN# is asserted and HDA_DOCKRST# is deasserted.
- User initiates an undock event through a mechanism outside the scope of this document.
- Software halts the stream to the dock codec and clears GCTL.DA.
- The Intel® SCH asserts HDA_DOCKRST# synchronous to H_CLKIN. HDA_DOCKRST# assertion will occur a minimum of four H_CLKIN ticks after the completion of the current frame. The HD Audio link reset specification requirement that the last Frame sync be skipped will not be met.
- A minimum of four H_CLKIN periods after HDA_DOCKRST#, assertion, the Intel® SCH deasserts HDA_DOCK_EN# to isolate the dock codec. HDA_DOCK_EN# is deasserted synchronously to H_CLKIN and timed such that H_CLKIN, HDA_SYNC, and HDA_SDO are low.
- Hardware clears GSTS.DM. An interrupt can be enabled (DMIS status and DMIE enable bits) to notify software.
- The Intel® SCH is now ready for a subsequent docking event.



10.1.1.3 Relationship between HDA_DOCKRST# and HDA_RST#

HDA_RST# is asserted when RESET# occurs or when the CRST# bit is 0. In both of these cases GCTL.DA and GSTS.DM bits are cleared, HDA_DOCK_EN# is deasserted, and HDA_DOCKRST# is asserted. After reset, software is responsible for initiating the electrical connection, discovery, and enumeration process just as it would for a normal docking event.

10.1.1.4 External Pull-Ups/Pull-Downs

The following table shows the resistors that should be mounted on the dock side of the isolation switch.

Signal	Intel® SCH Resistors[1]	External Resistors
HDA_CLK	Weak Pull-down	Weak Pull-Down
HDA_SYNC	None	Weak Pull-Down
HDA_SDO	None	Weak Pull-Down
HDA_SDI (from docked codec(s))s	Weak Pull-down	None
HDA_RST#	None	NA
HDA_DOCK_EN#	None	NA
HDA_DOCKRST#	None	Weak Pull-Down

NOTE:
1. Weak pull-down resistor is about 10 kΩ.

10.1.2 Low Voltage (LV) Mode

The Intel® SCH does *not* implement an automatic voltage detection circuit to dynamically select the I/O voltage of Intel HD Audio I/O pins. Bit zero of the HD Control Register (Offset 40h) is used to select either high-voltage (3.3 V) or low-voltage (1.5 V) I/O operation. The default mode is 3.3 V.

10.2 PCI Configuration Register Space

The Intel HD Audio controller resides in PCI Device 27, Function 0 on Bus 0. This function contains a set of DMA engines that are used to move samples of digitally encoded data between system memory and external codecs.

All registers in this function (including memory-mapped registers) must be addressable in byte, word, and Dword quantities. The software must always make register accesses on natural boundaries (i.e., Dword accesses must be on Dword boundaries; word accesses on word boundaries, etc.) In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the Intel HD Audio memory-mapped space, the results are undefined.

Table 26. Intel HD Audio PCI Configuration Registers (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Access
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	811Bh	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	RO
08h	RID	Revision Identification	See description	RO
09–0Bh	CC	Class Codes	040300h	RO
0Dh	CLS	Cache Line Size	00h	R/W
0Dh	LT	Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	LBAR	Lower Base Address	00000004h	R/W, RO
14h–17h	UBAR	Upper Base Address	00000000h	R/W
2Ch–2Fh	SS	Subsystem Identifiers	See description	R/WO
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INTLN	Interrupt Line	00h	R/W
3Dh	INTPN	Interrupt Pin	See Description	RO
40h	HDCTL	HD Control	00h	R/W, RO
44h	TCSEL	Traffic Class Select	00h	R/W
4Ch	DCKCTL	Docking Control	00h	R/W, RO
4Dh	DCKSTS	Docking Status	80h	R/WO, RO
50h	PM_CAPID	PCI Power Management Capability ID	01h	RO
51h	NXT_PTR1	Next Capability Pointer #1	70h	RO
52h–53h	PM_CAP	Power Management Capabilities	C842	RO
54h–57h	PM_CTL_STS	Power Management Control and Status	00000000h	R/W, RO, R/WC
60h	MSI_CAPID	MSI Capability ID	05h	RO
61h	NXT_PTR3	Next Capability Pointer #3	70h	RO

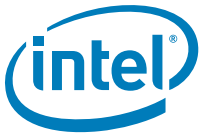


Table 26. Intel HD Audio PCI Configuration Registers (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Access
62h–63h	MSI_CTL	MSI Message Control	0080h	R/W, RO
64h–67h	MSI_ADR	MSI Message Address	00000000h	R/W, RO
68h–69h	MSI_DATA	MSI Message Data	0000h	R/W
70h	PCIE_CAPID	PCI Express Capability ID	10h	RO
71h	NXT_PTR2	Next Capability Pointer #2	60h or 00h	RO
72h–73h	PCIECAP	PCI Express Capabilities	0091h	RO
74h–77h	DEVCAP	Device Capabilities	00000000h	RO
78h–79h	DEVC	Device Control	0800h	R/W, RO
7Ah–7Bh	DEVS	Device Status	0000h	RO, R/W
FCh–FFh	FD	Function Disable Register	00000000h	RO, R/W
100h–103h	VCCAP	Virtual Channel Enhanced Capability Header	13010002h	RO
104h–107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO
108h–10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10Ch–10Dh	PVCCTL	Port VC Control	0000h	RO
10Eh–10Fh	PVCSTS	Port VC Status	0000h	RO
110h–103h	VC0CAP	VC0 Resource Capability	00000000h	RO
114h–117h	VC0CTL	VC0 Resource Control	800000FFh	R/W, RO
11Ah–11Bh	VC0STS	VC0 Resource Status	0000h	RO
11Ch–11Fh	VC1CAP	VC1 Resource Capability	00000000h	RO
120h–123h	VC1CTL	VC1 Resource Control	00000000h	R/W, RO
126h–127h	VC1STS	VC1 Resource Status	0000h	RO
130h–133h	RCCAP	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
134h–137h	ESD	Element Self Description	0F000100h	RO, R/W
140h–143h	L1DESC	Link 1 Description	See Description	RO
148h–14bh	L1ADD	Link 1 Address	See Description	RO, R/W

NOTE: Address locations that are not shown should be treated as Reserved.

10.2.1 VID—Vendor Identification Register

Offset: 00h-01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Default and Access	Description
15:0	RO	**Vendor ID** This is a 16-bit value assigned to Intel. Intel VID = 8086h

10.2.2 DID—Device Identification Register

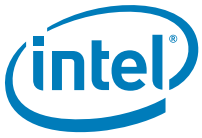
Offset Address: 02h–03h Attribute: RO
Default Value: 811Bh Size: 16 bits

Bit	Default and Access	Description
15:0	811Bh RO	**Device ID:** This is a 16-bit value assigned to the Intel HD Audio controller.

10.2.3 PCICMD—PCI Command Register

Offset Address: 04h–05h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:11	0h RO	Reserved
10	0 R/W	**Interrupt Disable (ID)** 0 = The INTx# signals may be asserted. 1 = The Intel® HD Audio controller INTx# signal will be deasserted **Note**: This bit does not effect the generation of MSI(s).
9:3	00h RO	Reserved
2	0 R/W	**Bus Master Enable (BME)**: Controls standard PCI Express bus mastering capabilities for Memory and I/O, reads and writes. Note that this bit also controls MSI generation since MSIs are essentially memory writes. 0 = Disable 1 = Enable
1	0 R/W	**Memory Space Enable (MSE):** Enables memory space addresses to the Intel HD Audio controller. 0 = Disable 1 = Enable
0	0 RO	Reserved



10.2.4 PCISTS—PCI Status Register

Offset Address: 06h–07h Attribute: RO
Default Value: 0010h Size: 16 bits

Bit	Default and Access	Description
15:5	000h RO	Reserved
4	1 RO	**Capabilities List (CAP_LIST)**: Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0 RO	**Interrupt Status (IS)** 0 = This bit is 0 after the interrupt is cleared. 1 = This bit is 1 when the INTx# is asserted. **NOTE:** This bit is not set by an MSI.
2:0	000b RO	Reserved

10.2.5 RID—Revision Identification Register

Offset: 08h Attribute: RO
Default Value: See description Size: 8 Bits

Bit	Default and Access	Description
7:0	See description RO	**Revision ID (RID).** Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the value of the Revision ID Register

10.2.6 CC—Class Code Register

Offset: 09h–0Bh Attribute: RO
Default Value: 040300h Size: 24 bits

Bit	Default and Access	Description
23:16	04h RO	**Base Class Code (BCC)**: 04h = Multimedia device
8:15	03h RO	**Sub-Class Code (SCC)**: 03h = Audio Device
7:0	00h RO	**Programming Interface (PI):** Indicates Intel® HD Audio programming interface.

10.2.7 CLS—Cache Line Size Register

Address Offset: 0Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Cache Line Size (CLS):** Does not apply to PCI Express. The PCI Express specification requires this to be implemented as a R/W register but has no functional impact on the Intel® SCH.

10.2.8 LT—Latency Timer Register

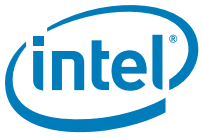
Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Latency Timer:** Hardwired to 00

10.2.9 HEADTYP—Header Type Register

Address Offset: 0Eh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Header Type:** Hardwired to 00.



10.2.10 LBAR—Lower Base Address Register

Address Offset:	10h-13h	Attribute:	R/W, RO
Default Value:	00000004h	Size:	32 bits

Bit	Default and Access	Description
31:14	0000h R/W	**Lower Base Address (LBA):** This field provides the base address for the Intel HD Audio controller's memory mapped configuration registers. 16 KB are requested by hardwiring Bits 13:4 to 0's.
13:4	000h RO	**Reserved:** Hardwired to 0s
3	0 RO	**Prefetchable (PREF):** Hardwired to 0 to indicate that this BAR is NOT prefetchable
2:1	10b RO	**Address Range (ADDRNG):** This field indicates that this BAR can be located anywhere in 64-bit address space.
0	0 RO	**Resource Type (RTE):** Indicates this BAR is located in memory space.

10.2.11 UBAR—Upper Base Address Register

Address Offset:	14h-17h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Default and Access	Description
31:0	0 R/W	**Upper Base Address (UBA):** This field provides the upper 32 bits of the Base address for the Intel® HD Audio controller memory mapped configuration registers.

This register matches the value written to the LPC bridge.

10.2.12 SS—Sub System Identifiers Register

Offset:	2Ch–2Fh	Attribute:	R/WO
Default Value:	00000000h	Size:	32 bits

This register is initialized to Logic 0 by the assertion of RESET#. This register can be written only once after RESET# deassertion.

Bit	Default and Access	Description
31:16	0000h R/WO	**Subsystem ID (SSID):** This field is written by BIOS. No hardware action taken on this value.
15:0	0000h R/WO	**Subsystem Vendor ID (SSVID):** This field is written by BIOS. No hardware action taken on this value.

10.2.13 CAP_PTR—Capabilities Pointer Register

Address Offset: 34h Attribute: RO
Default Value: 50h Size: 8 bits

This register indicates the offset for the capability pointer.

Bit	Default and Access	Description
7:0	50h RO	**Pointer (PTR):** This field indicates that the first capability pointer offset is offset 50h (Power Management Capability).

10.2.14 INTLN—Interrupt Line Register

Address Offset: 3Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Interrupt Line:** This data is not used by the Intel® SCH. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

10.2.15 INTPN—Interrupt Pin Register

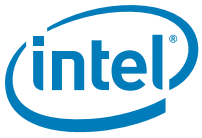
Address Offset: 3Dh Attribute: RO
Default Value: See Description Size: 8 bits

Bit	Default and Access	Description
7:4	0h RO	Reserved
3:0	0h RO	**Interrupt Pin:** This reflects the value of D27IP.ZIP (Chipset Config Registers:Offset 3110h:Bits 3:0).

10.2.16 HDCTL—HD Control Register

Address Offset: 40h Attribute: R/W, RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:1	00h RO	Reserved
0	0 R/W	**Low Voltage Mode Enable (LMVE)** 0 = (Default) The Intel HD Audio controller operates in high voltage mode. 1 = The Intel HD Audio controller's AFE operates in low voltage mode.



10.2.17 DCKCTL—Docking Control Register

Address Offset: 4Ch Attribute: R/W, RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:1	00h RO	Reserved
0	0 R/W, RO	**Dock Attach (DA):** Software writes a 1 to this bit to initiate the docking sequence on the HDA_DOCK_EN# and HDA_DOCKRST# signals. When the docking sequence is complete, hardware will set the Dock Mated (GSTS.DM) status bit to a 1. Software writes a 0 to this bit to initiate the undocking sequence on the HDA_DOCK_EN# and HDA_DOCKRST# signals. When the undocking sequence is complete hardware will set the Dock Mated (GSTS.DM) status bit to a 0. **NOTES:** • Software must check the state of the Dock Mated (GSTS.DM) bit prior to writing to the Dock Attach bit. Software shall only change the DA bit from a 0 to a 1 when DM=0. Likewise, software shall only change the DA bit from 1 to 0 when DM=1. If these rules are violated, the results are undefined. • This bit is Read Only when the DCKSTS.DS bit = 0.

10.2.18 DCKSTS—Docking Status Register

Address Offset: 4Dh Attribute: R/WO, RO
Default Value: 80h Size: 8 bits

Bit	Default and Access	Description
7	1 R/WO	**Docking Supported (DS):** When set, indicates Intel® SCH supports docking. DKCTL.DA is only writeable when this bit is 1. This bit is reset on RESET#, but not on CRST#
6:1	00h RO	Reserved
0	0 RO	**Dock Mated (DM):** This bit indicates that codec is physically and electrically docked.

10.2.19 PM_CAPID—PCI Power Management Capability ID Register

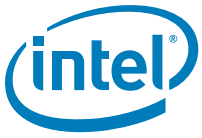
Address Offset: 50h Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Default and Access	Description
15:8	70h RO	**Next Capability (Next):** Hardwired to 70h. Points to the next capability structure (PCI Express).
7:0	01h RO	**Cap ID (CAP):** Hardwired to 01h to indicate that this pointer is a PCI power management capability.

10.2.20 PM_CAP—Power Management Capabilities Register

Address Offset: 52h–53h Attribute: RO
Default Value: 4802h Size: 16 bits

Bit	Default and Access	Description
15:11	01001b RO	**PME Support:** Hardwired to 01001b to indicate PME# can be generated from $D3_{HOT}$ and D0 states.
10:3	0s RO	Reserved
2:0	010b RO	**Version (VS):** Hardwired to 010b to indicate support for *PCI Power Management Specification, Revision 1.1*.



10.2.21 PM_CTL_STS—Power Management Control and Status Register

Address Offset: 54h-57h Attribute: RO, R/W, R/WC
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:16	0000h RO	Reserved
15	0 R/WC	**PME Status (PMES)** 0 = Software clears the bit by writing a 1 to it. 1 = when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PMEE (bit 8 in this register).
14:9	00h RO	Reserved
8	0 R/W	**PME Enable (PMEE)** 0 = Disable 1 = When set, and PMES is set, the audio controller generates an internal Power Management Event (PME).
7:2	00h RO	Reserved
1:0	00b R/W	**Power State (PS):** This field is used both to determine the current power state of the Intel HD Audio controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state Others = reserved **NOTES**: • If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. • When in the $D3_{HOT}$ states, the Intel HD Audio controller configuration space is available, but the I/O and memory space are not. Additionally, interrupts are blocked. • When software changes this value from $D3_{HOT}$ state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

10.2.22 MSI_CAPID—MSI Capability ID Register

Address Offset: 60h Attribute: RO
Default Value: 0005h Size: 16 bits

Bit	Default and Access	Description
15:8	00h RO	**Next Capability (Next):** Points to the next item in the capability list. Wired to 00h to indicate this is the last capability in the list.
7:0	05h RO	**Cap ID (CAP) Hardwired to 05h:** Indicates that this pointer is a MSI capability.

10.2.23 MSI_CTL—MSI Message Control Register

Address Offset: 62h–63h Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:1	0000h RO	Reserved
0	0 R/W	**MSI Enable (ME)** 0 = An MSI may not be generated 1 = An MSI will be generated instead of an INTx signal.

10.2.24 MSI_ADR—MSI Message Address Register

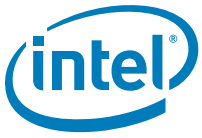
Address Offset: 64h–67h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:2	0s R/W	**Message Lower Address (MLA):** Address used for MSI message.
1:0	00b RO	Reserved

10.2.25 MSI_DATA—MSI Message Data Register

Address Offset: 68h–69h Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:0	0000h R/W	**Message Data (MD):** Data used for MSI message.



10.2.26 PCIE_CAPID—PCI Express Capability ID Register

Address Offset: 70h Attribute: RO
Default Value: 60/00 10h Size: 8 bits

Bit	Default and Access	Description
7:0	60h/00h RO	**Next Capability (Next):** Defaults to 60h, the address of the next capability structure in the list. However, if the FD.MD bit is set, the MSI capability will be disabled and this register will report 00h indicating this capability is the last capability in the list.
7:0	10h RO	**Cap ID (CAP)**: Hardwired to 10h. Indicates that this pointer is a PCI Express capability structure.

10.2.27 PCIECAP—PCI Express Capabilities Register

Address Offset: 72h–73h Attribute: RO
Default Value: 0091h Size: 16 bits

Bit	Default and Access	Description
15:8	00h RO	Reserved
7:4	9h RO	**Device/Port Type (DPT):** Hardwired to 1001b. Indicates that this is a Root Complex Integrated endpoint device.
3:0	1h RO	**Capability Version (CV):** Hardwired to 0001b. Indicates version #1 PCI Express capability.

10.2.28 DEVCAP—Device Capabilities Register

Address Offset: 74h–77h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0 RO	Reserved

10.2.29 DEVC—Device Control Register

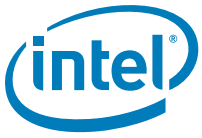
Address Offset: 78h–79h Attribute: R/W, RO
Default Value: 0800h Size: 16 bits

Bit	Default and Access	Description
15	0 RO	Reserved
14:12	000b RO	**Max Read Request Size (MRRS):** Hardwired to 000 enabling 128 B maximum read request size.
11	1 R/W	**No Snoop Enable (NSNPEN):** 0 = The Intel HD Audio controller will not set the No-Snoop bit. In this case, isochronous transfers will not use VC1 (VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use VC0. 1 = The Intel HD Audio controller is permitted to set the No-Snoop bit in the Requester Attributes of a bus master transaction. In this case, VC0 or VC1 may be used for isochronous transfers. **NOTE:** This bit is not reset on $D3_{HOT}$ to D0 transition.
10:4	0 RO	Reserved
3:0	0 R/W	**Error Reporting Bits (ERB):** R/W to pass PCI Express compliance test. no functionality.

10.2.30 DEVS—Device Status Register

Address Offset: 7ah–7bh Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:6	0000h RO	Reserved
5	0 RO	**Transactions Pending (TXP):** 0 = Completions for all Non-Posted Requests have been received. 1 = The Intel HD Audio controller has issued Non-Posted requests which have not been completed.
4:0	00000b R/W	Reserved



10.2.31 FD—Function Disable Register

Address Offset: FCh–FFh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:3	0 RO	Reserved
2	0 R/W	**Clock Gating Disable (GCD)** 0 = Dynamic Clock gating within the function is enabled (Default) 1 = Dynamic Clock gating within the function is disabled.
1	0 R/W	**MSI Disable (MD)** 1 = When set, the MSI capability pointer is hidden.
0	0 R/W	**Disable (D)** 1 = Intel® HD Audio function (D27:F0) is disabled.

10.2.32 VCCAP—Virtual Channel Enhanced Capability Header Register

Address Offset: 100h–103h Attribute: RO
Default Value: 13010002h Size: 32 bits

Bit	Default and Access	Description
31:20	130h RO	**Next Capability Offset (NXTAP):** Points to the next capability header, which is the Root Complex Link Declaration Enhanced Capability Header.
19:16	1h RO	**Capability Version**
15:0	0002h RO	**PCI Express Extended Capability**

10.2.33 PVCCAP1—Port VC Capability Register 1

Address Offset: 104h–107h Attribute: RO
Default Value: 00000001h Size: 32 bits

Bit	Default and Access	Description
31:3	0 RO	Reserved
2:0	001b RO	**Extended VC Count (VCCNT):** Hardwired to 001b. Indicates that 1 extended VC (in addition to VC0) is supported by the Intel® HD Audio controller.

10.2.34 PVCC2—Port VC Capability Register 2

Address Offset: 108h-10Bh Attribute: RO
Default Value: 00000000h Size: 32 Bits

Bit	Default and Access	Description
31:0	0 RO	Reserved

10.2.35 PCCTL—Port VC Control

Address Offset: 10Ch-10Dh Attribute: RO
Default Value: 0000h Size: 16 Bits

Bit	Default and Access	Description
15:0	0 RO	Reserved

10.2.36 PVCSTS—Port VC Status

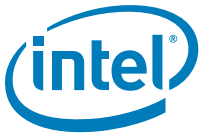
Address Offset: 10Eh-10Fh Attribute: RO
Default Value: 0000h Size: 16 Bits

Bit	Default and Access	Description
15:0	0 RO	Reserved

10.2.37 VC0CAP—VC0 Resource Capability Register

Address Offset: 110h-113h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0 RO	Reserved



10.2.38 VC0CTL—VC0 Resource Control Register

Address Offset: 114h–117h Attribute: R/W, RO
Default Value: 800000FFh Size: 32 bits

Bit	Default and Access	Description
31	1 RO	**VC0 Enable:** Hardwired to 1 for VC0.
30:8	0 RO	Reserved
7:0	FFh R/W, RO	**TC/VC0 Map:** Bit 0 is hardwired to 1 since TC0 is always mapped VC0. Bits [7:1] are implemented as R/W bits.

10.2.39 VCSTS—VC0 Resource Status Register

Address Offset: 11Ah-10Bh Attribute: RO
Default Value: 0000h Size: 16 Bits

Bit	Default and Access	Description
16:0	0 RO	Reserved

10.2.40 VC0CAP—VC0 Resource Capability Register

Address Offset: 11Ch-10Fh Attribute: RO
Default Value: 00000000h Size: 32 Bits

Bit	Default and Access	Description
31:0	0 RO	Reserved

10.2.41 VC1CTL—VC1 Resource Control Register

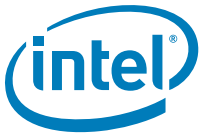
Address Offset: 120h–123h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31	0 R/W	**VC1 Enable** 0 = VC1 is disabled 1 = VC1 is enabled **NOTE:** This bit is not reset on $D3_{HOT}$ to D0 transition.
30:27	0h RO	Reserved
26:24	000b R/W	**VC1 ID:** This field assigns a VC ID to the VC1 resource. This field is not used by the Intel® SCH hardware, but it is R/W to avoid confusing software.
23:8	0h RO	Reserved
7:0	00h R/W, RO	**TC/VC Map:** This field indicates the TCs that are mapped to the VC1 resource. Bit 0 is hardwired to 0 indicating that it cannot be mapped to VC1. Bits [7:1] are implemented as R/W bits. This field is not used by the Intel® SCH, but it is R/W to avoid confusing software.

10.2.42 VC1STS—VC1 Resource Status Register

Address Offset: 126h-127h Attribute: RO
Default Value: 0000h Size: 16 Bits

Bit	Default and Access	Description
15:0	0 RO	Reserved



10.2.43 RCCAP—Root Complex Link Declaration Enhanced Capability Header Register

Address Offset: 130h–133h Attribute: RO
Default Value: 00010005h Size: 32 bits

Bit	Default and Access	Description
31:20	000h RO	**Next Capability Offset:** Indicates this is the last capability.
19:16	1h RO	**Capability Version**
15:0	0005h RO	**PCI Express Extended Capability ID**

10.2.44 ESD—Element Self Description Register

Address Offset: 134h–137h Attribute: RO, R/W
Default Value: 0F000100h Size: 32 bits

Bit	Default and Access	Description
31:24	0Fh RO	**Port Number (PN):** Hardwired to 0Fh indicating that the Intel® HD Audio controller is assigned as Port #15d.
23:16	00h R/W	**Component ID (COMPID):** Set by BIOS to match the value of ESD.CID of the chip configuration section.
15:8	01h RO	**Number of Link Entries (NLE):** The HD Audio controller only connects to the Intel® SCH egress port.
7:4	0h RO	Reserved
3:0	0h RO	**Element Type (ELTYP):** The Intel HD Audio controller is an integrated Root Complex Device. Therefore, the field reports a value of 0h.

10.2.45 L1DESC—Link 1 Description Register

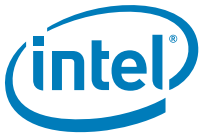
Address Offset: 140h–143h Attribute: RO
Default Value: 00000001h Size: 32 bits

Bit	Default and Access	Description
31:24	RO	**Target Port Number:** The Intel® HD Audio controller targets the Intel® SCH's RCRB egress port, Port 0.
23:16	See Description RO	**Target Component ID:** Returns the value of ESD.COMPID.
15:2	RO	Reserved
1	0 RO	**Link Type (LNKTYP):** Indicates Type 0.
0	1 RO	**Link Valid (LNKVLD)**

10.2.46 L1ADD—Link 1 Address Register

Address Offset: 148h–14Bh Attribute: RO, R/W
Default Value: See Description Size: 32 bits

Bit	Default and Access	Description
31:14	RCBA R/W	**Base (BASE):** Hardwired to match the RCBA register value in the PCI-LPC bridge (D31:F0h).
13:0	0000h RO	Reserved



10.3 Memory Mapped Configuration Registers

The base memory location for these memory mapped configuration registers is specified in the LBAR and UBAR registers (D27:F0:offset 10h and D27:F0:offset 14h). The individual registers are then accessible at LBAR + Offset as indicated in Table 27.

These memory mapped registers must be accessed in byte, word, or Dword quantities.

Table 27. Intel HD Audio Memory Mapped Configuration Registers (Sheet 1 of 3)

LBAR + Offset	Mnemonic	Register Name	Default	Access
00h–01h	GCAP	Global Capabilities	4401h	RO
02h	VMIN	Minor Version	00h	RO
03h	VMAJ	Major Version	01h	RO
04h–05h	OUTPAY	Output Payload Capability	003Ch	RO
06h–07h	INPAY	Input Payload Capability	001Dh	RO
08h–0Bh	GCTL	Global Control	00000000h	R/W
0Ch	WAKEEN	Wake Enable	0000h	R/W, RO
0Eh	STATESTS	State Change Status	0000h	R/W, RO
10h–11h	GSTS	Global Status	0000h	R/WC
18h–19h	OUTSTRMPAY	Output Stream Payload Capability	0030h	RO
1Ah–1Bh	INSTRMPAY	Input Stream Payload Capability	0018h	RO
20h–23h	INTCTL	Interrupt Control	00000000h	R/W, RO
24h–27h	INTSTS	Interrupt Status	00000000h	RO
30h–33h	WALCLK	Wall Clock Counter	00000000h	RO
38h–3Bh	SSYNC	Stream Synchronization	00000000h	R/W, RO
40h–43h	CORBBASE	CORB Base Address	00000000h	R/W, RO
48h–49h	CORBWP	CORB Write Pointer	0000h	R/W, RO
4Ah–4Bh	CORBRP	CORB Read Pointer	0000h	R/W, RO
4Ch	CORBCTL	CORB Control	00h	R/W, RO
4Dh	CORBST	CORB Status	00h	R/WC
4Eh	CORBSIZE	CORB Size	42h	RO
50h–53h	RIRBBASE	RIRB Base Address	00000000h	R/W, RO
58h–59h	RIRBWP	RIRB Write Pointer	0000h	WO, RO
5Ah–5Bh	RINTCNT	Response Interrupt Count	0000h	R/W, RO
5Ch	RIRBCTL	RIRB Control	00h	R/W, RO
5Dh	RIRBSTS	RIRB Status	00h	R/WC, RO
5Eh	RIRBSIZE	RIRB Size	40h	RO
60h–63h	IC	Immediate Command	00000000h	R/W
64h–67h	IR	Immediate Response	00000000h	RO
68h–69h	IRS	Immediate Command Status	0000h	R/W, R/WC, RO

Table 27. Intel HD Audio Memory Mapped Configuration Registers (Sheet 2 of 3)

LBAR + Offset	Mnemonic	Register Name	Default	Access
70h–73h	DPBASE	DMA Position Base Address	00000000h	R/W, RO
80-82h	ISD0CTL	Input Stream Descriptor 0 (ISD0) Control	040000h	R/W, RO
83h	ISD0STS	ISD0 Status	00h	R/WC, RO
84h–87h	ISD0LPIB	ISD0 Link Position in Buffer	00000000h	RO
88h–8Bh	ISD0CBL	ISD0 Cyclic Buffer Length	00000000h	R/W
8Ch–8dh	ISD0LVI	ISD0 Last Valid Index	0000h	R/W, RO
8Eh–8Fh	ISD0FIFOW	ISD0 FIFO Watermark	0004h	R/W, RO
90h–91h	ISD0FIFOS	ISD0 FIFO Size	0077h	RO
92h–93h	ISD0FMT	ISD0 Format	0000h	R/W, RO
98h–9Bh	ISD0BDPL	ISD0 Buffer Descriptor List Pointer	00000000h	R/W, RO, WO
A0h–A2h	ISD1CTL	Input Stream Descriptor 1(ISD01) Control	040000h	R/W, RO
A3h	ISD1STS	ISD1 Status	00h	R/WC, RO
A4h–A7h	ISD1LPIB	ISD1 Link Position in Buffer	00000000h	RO
A8h–ABh	ISD1CBL	ISD1 Cyclic Buffer Length	00000000h	R/W
ACh–ADh	ISD1LVI	ISD1 Last Valid Index	0000h	R/W, RO
AEh–AFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W, RO
B0h–B1h	ISD1FIFOS	ISD1 FIFO Size	0077h	RO
B2-B3h	ISD1FMT	ISD1 Format	0000h	R/W, RO
B8-BBh	ISD1BDPL	ISD1 Buffer Descriptor List Pointer	00000000h	R/W, RO, WO
C0h–C2h	OSD0CTL	Output Stream Descriptor 0 (OSD0) Control	040000h	R/W, RO
C3h	OSD0STS	OSD0 Status	00h	R/WC, RO
C4h–C7h	OSD0LPIB	OSD0 Link Position in Buffer	00000000h	RO
C8h–CBh	OSD0CBL	OSD0 Cyclic Buffer Length	00000000h	R/W
CCh–CDh	OSD0LVI	OSD0 Last Valid Index	0000h	R/W, RO
CEh–CFh	OSD0FIFOW	OSD0 FIFO Watermark	0004h	R/W, RO
D0h–D1h	OSD0FIFOS	OSD0 FIFO Size	00BFh	R/W, RO
D2h-D3h	OSD0FMT	OSD0 Format	0000h	R/W, RO
D8h–DBh	OSD0BDPL	OSD0 Buffer Descriptor List Pointer	00000000h	R/W, RO, WO
E0h–E2h	OSD1CTL	Output Stream Descriptor 1 (OSD1) Control	040000h	R/W, RO
123h	OSD1STS	OSD1 Status	00h	R/WC, RO

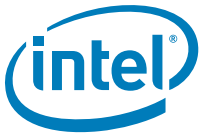


Table 27. Intel HD Audio Memory Mapped Configuration Registers (Sheet 3 of 3)

LBAR + Offset	Mnemonic	Register Name	Default	Access
E4h–E7h	OSD1LPIB	OSD1 Link Position in Buffer	00000000h	RO
E8h–EBh	OSD1CBL	OSD1 Cyclic Buffer Length	00000000h	R/W
ECh–EDh	OSD1LVI	OSD1 Last Valid Index	0000h	R/W, RO
EEh–EFh	OSD1FIFOW	OSD1 FIFO Watermark	0004h	R/W, RO
F0h–F1h	OSD1FIFOS	OSD1 FIFO Size	00BFh	R/W, RO
F2h–F3h	OSD1FMT	OSD1 Format	0000h	R/W, RO
F8h–FBh	OSD1BDPL	OSD1 Buffer Descriptor List Pointer	00000000h	R/W, RO
Vendor-Specific Memory Mapped Registers[1]				
1030h–1033h	EM1	Extended Mode 1	0C00000h	R/W, RO
1004h–1007h	INRC	Input Stream Repeat Count	00000000h	RO
1008h–100Bh	OUTRC	Output Stream Repeat Count	00000000h	RO
100Ch–100Fh	FIFOTRK	FIFO Tracking	000FF800h	RO, R/W
1010h–1013h	I0DPIB	Input Stream 0 DMA Position in Buffer	00000000h	RO
1014h–1017h	I1DPIB	Input Stream 1 DMA Position in Buffer	00000000h	RO
1020h–1023h	O0DPIB	Output Stream 0 DMA Position in Buffer	00000000h	RO
1024h–1027h	O1DPIB	Output Stream 1 DMA Position in Buffer	00000000h	RO
1030h–1033h	EM2	Extended Mode 2	00000000h	R/W, RO
2030h–2033h	WLCLKA	Wall Clock Counter Alias	00000000h	RO
2084h–2087h	ISD0LPIBA	ISD0 Link Position in Buffer Alias	00000000h	RO
20A4h–20A7h	ISD1LPIBA	ISD1 Link Position in Buffer Alias	00000000h	RO
2104h–2107h	OSD0LPIBA	OSD0 Link Position in Buffer Alias	00000000h	RO
2124h–2127h	OSD1LPIBA	OSD1 Link Position in Buffer Alias	00000000h	RO

NOTES:
1. The 4-KB memory-mapped range starting at LBAR + 4 KB is reserved in the Intel HD Audio specification for Vendor-specific registers.
2. Address locations that are not shown should be treated as Reserved.

10.3.1 GCAP—Global Capabilities Register

Memory Address: LBAR + 00h Attribute: RO
Default Value: 4401h Size: 16 bits

Bit	Default and Access	Description
15:12	0010b RO	**Output Stream Supported (OSS):** Indicates that the Intel® HD Audio controller supports 2 output streams.
11:8	0010b RO	**Input Stream Supported (ISS):** Indicates that the Intel HD Audio controller supports 2 input streams.
7:3	00000b RO	**Bidirectional Stream Supported:** Indicates that the Intel HD Audio controller supports 0 bidirectional stream.
2	RO	Reserved
1	0b RO	**Serial Data Out Signals (NSDO):** Indicates that the Intel HD Audio controller supports 1 serial data output signal.
0	0b RO	**64-bit Address Supported (64OK):** 64-bit addressing is not supported.

10.3.2 VMIN—Minor Version Register

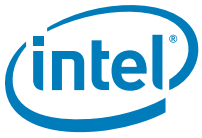
Memory Address: LBAR + 02h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Minor Version (MAJ):** Indicates that the Intel® SCH supports minor revision number 00h of the Intel® HD Audio specification.

10.3.3 VMAJ—Major Version Register

Memory Address: LBAR + 03h Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Default and Access	Description
7:0	01h RO	**Major Version (MAJ):** Indicating that the Intel® SCH supports major revision number 01h of the Intel® HD Audio specification.



10.3.4 OUTPAY—Output Payload Capability Register

Memory Address: LBAR + 04h Attribute: RO
Default Value: 003Ch Size: 16 bits

Bit	Default and Access	Description
15:7	0 RO	Reserved
6:0	3Ch RO	**Output Payload Capability (OUT):** Indicates the total output payload available on the link as 60 words (120 bytes). This field indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48-MHz frame. The default link clock of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. 00h = 0 word 01h = 1 word payload ..... FFh = 256 word payload

10.3.5 INPAY—Input Payload Capability Register

Memory Address: LBAR + 06h Attribute: RO
Default Value: 001dh Size: 16 bits

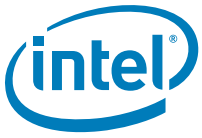
Bit	Default and Access	Description
15:7	0 RO	Reserved
6:0	1Dh RO	**Input Payload Capability (IN):** Hardwired to 1Dh indicating 29 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48-MHz frame. The default link clock of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words available for data payload. 00h = 0 word 01h = 1 word payload ..... FFh = 256 word payload

10.3.6 GCTL—Global Control Register

Memory Address: LBAR + 08h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

(Sheet 1 of 2)

Bit	Default and Access	Description
31:9	0 RO	Reserved
8	0 R/W	**Accept Unsolicited Response Enable (AURE)** 0 = Unsolicited responses from the codecs are not accepted. 1 = Unsolicited response from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.
7:2	000000b RO	Reserved
1	0 R/W	**Flush Control (FLUSH)**: Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer Bit 0 needs not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be a 0. When the flush is initiated, the controller will flush the pipelines to memory to ensure that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFIOs is not critical.



(Sheet 2 of 2)

Bit	Default and Access	Description
0	0 R/W	**Controller Reset #** 0 = Writing a 0 to this bit causes the Intel HD Audio controller to be reset. All state machines, FIFOs and non-resume well memory mapped configuration registers (not PCI configuration registers) in the controller will be reset. The Intel HD Audio link RESET# signal will be asserted, and all other link signals will be driven to their default values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify the controller is in reset. 1 = Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. This bit defaults to a 0 after Hardware reset, therefore, software needs to write a 1 to this bit to begin operation. **NOTES:** • The CORB/RIRB RUN bits and all stream RUN bits must be verified cleared to 0 before writing a 0 to this bit in order to assure a clean re-start. • When setting or clearing this bit, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. • When this bit is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is this register itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# (this bit) is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with RESET# or on a $D3_{HOT}$ to D0 transition.

10.3.7 WAKEEN-Wake Enable

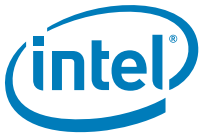
Memory Address: LBAR + 0Ch Attribute: RO, RW
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:2	0 RO	Reserved
1:0	00b RWC	**SDIN Wake Enable Flags (SDIWEN):** These bits control which SDI signal(s) may generate a wake event. A 1 in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. Bit 0 is for SDI0, Bit 1 is for SDI1 These bits are in the suspend well and only cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

10.3.8 STATESTS - State Change Status

Memory Address: LBAR + 0Eh Attribute: RO
Default Value: 001dh Size: 16 bits

Bit	Default and Access	Description
15:3	0 RO	Reserved
1:0	00b RWC	**SDIN State Change Status Flags (SDIWAKE):** Flag bits that indicate which SDI signal(s) received a "State Change" event. The bits are cleared by writing a 1 to them. Bit 0 is for SDI0, Bit 1 is for SDI1 Bit 2 is for SDI2. These bits are in the suspend well and only cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.



10.3.9 GSTS—Global Status Register

Memory Address: LBAR + 10h Attribute: R/WC, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:4	000h RO	Reserved
3	0 R/WC	**Dock Mated Interrupt Status (DMIS):** A 1 indicates that the dock mating or unmating process has completed. For the docking process it indicates that dock is electrically connected and that software may detect and enumerate the docked codecs. For the undocking process it indicates that the dock is electrically isolated and that software may report to the user that physical undocking may commence. This bit gets set to a 1 by hardware when the DM bit transitions from a 0 to a 1 (docking) or from a 1 to a 0 (undocking). Note that this bit is set regardless of the state of the DMIE bit. Software clears this bit by writing a 1 to it. Writing a 0 to this bit has no effect.
2	0 RO	**Dock Mated (DM):** This bit effectively communicates to software that an Intel HD Audio docked codec is physically and electrically attached. Controller hardware sets this bit to 1 after the docking sequence triggered by writing a 1 to the Dock Attach (GCTL.DA) bit is completed (HDA_DOCKRST# deassertion). This bit indicates to software that the docked codec(s) may be discovered by the STATESTS register and then enumerated. Controller hardware sets this bit to 0 after the undocking sequence triggered by writing a 0 to the Dock Attach (GCTL.DA) bit is completed (DOCK_EN# deasserted). This bit indicates to software that the docked codec(s) may be physically undocked. This bit is Read Only. Writes to this bit have no effect.
1	0 R/WC	**Flush Status:** This bit is set to 1 by hardware to indicate that the flush cycle initiated when the Flush Control bit (LBAR + 08h, Bit 1) was set has completed. Software must write a 1 to clear this bit before the next time the Flush Control bit is set to clear the bit.
0	0 RO	Reserved

10.3.10 ECAP—Extended Capabilities

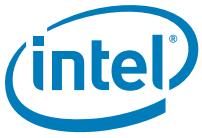
Memory Address: LBAR + 14h Attribute: RO
Default Value: 00000001h Size: 32 bits

Bit	Default and Access	Description
31:1	0 RO	Reserved
1	000b R/WO	**Docking Supported (DS):** A 1 indicates that Intel® SCH supports Intel HD Audio Docking. The GCTL.DA bit is only writable when this bit is 1. This bit is reset to its default value only on RESET#, but not on a CRST# or D3HOT-to-D0 transition.

10.3.11 STRMPAY—Stream Payload Capability

Memory Address: LBAR + 18h Attribute: RO
Default Value: 00180030h Size: 32 bits

Bit	Default and Access	Description
31:24	00h RO	Reserved
23:16	18h RO	**Input (IN):** Indicates the number of words per frame for the input streams is 24 words. This measurement is in 16-bit word quantities per 48-kHz frame.
15:8	00h RO	Reserved
7:0	30h RO	**Output (OUT):** Indicates the number of words per frame for output streams is 48 words. This measurement is in 16-bit word quantities per 48-kHz frame.



10.3.12 INTCTL—Interrupt Control Register

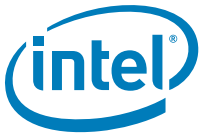
Memory Address: LBAR + 20h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31	0 R/W	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. 1 = Intel® HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI configuration space. **NOTE:** This bit is not affected by the $D3_{HOT}$ to D0 transition.
30	0 R/W	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. 1 = Controller generates an interrupt when the corresponding status bit gets set due to a Response Interrupt, a Response Buffer Overrun, and State Change events. **NOTE:** This bit is not affected by the $D3_{HOT}$ to D0 transition.
29:4	0 RO	Reserved
3	0 R/W	**Output Stream 2 (OS2):** This bit set and GE set enables INTSTS.OS2 to generate an interrupt.
2	0 R/W	**Output Stream 1 (OS1):** This bit set and GE set enables INTSTS.OS1 to generate an interrupt.
1	0 R/W	**Input Stream 2 (IS2):** This bit set and GE set enables INTSTS.IS2 to generate an interrupt.
0	0 R/W	**Input Stream 1 (IS1):** This bit set and GE set enables INTSTS.IS1 to generate an interrupt.

10.3.13 INTSTS—Interrupt Status Register

Memory Address: LBAR + 24h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31	0 RO	**Global Interrupt Status (GIS):** This bit is an OR of all the interrupt status bits in this register. **NOTE:** This bit is not affected by the $D3_{HOT}$ to D0 transition.
30	0 RO	**Controller Interrupt Status (CIS):** Status of general controller interrupt. 1 = Indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. This bit is an OR of all of the stated interrupt status bits for this register. **NOTES:** 1. This bit is set regardless of the state of the corresponding Interrupt Enable bit, but a hardware interrupt will not be generated unless the corresponding enable bit is set. 2. This bit is not affected by the $D3_{HOT}$ to D0 transition.
29:4	0 RO	Reserved
3	0 RO	**Output Stream 2 (OS2):** 1 = Interrupt occurred on Output Stream 2.
2	0 RO	**Output Stream 1 (OS1):** 1 = Interrupt occurred on Output Stream 1.
1	0 RO	**Input Stream 2 (IS2):** 1 = Interrupt occurred on Input Stream 2.
0	0 RO	**Input Stream 1 (IS1):** 1 = Interrupt occurred on Input Stream 1.



10.3.14 WALCLK—Wall Clock Counter Register

Memory Address: LBAR + 30h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0s RO	**Wall Clock Counter:** This field is a 32-bit counter that is incremented on each link H_CLKIN period and rolls over from FFFF FFFFh to 0000 0000h. This counter will roll over to 0 with a period of approximately 179 seconds. This counter is enabled while the H_CLKIN bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

10.3.15 SSYNC—Stream Synchronization Register

Memory Address: LBAR + 38h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bits	Default and Access	Description
31:4	0 RO	Reserved
3	0 R/W	**Output Stream 2 Sync (OS2):** When set, this bit blocks data from being sent for output stream 2.
2	0 R/W	**Output Stream 1 Sync (OS1):** When set, this bit blocks data from being sent for output stream 1.
1	0 R/W	**Input Stream 2 Sync (IS2):** When set, this bit blocks data from being received from input stream 2.
0	0 R/W	**Input Stream 1 Sync (IS1):** When set, this bit blocks data from being received from input stream 1.

10.3.16 CORBBASE—CORB Base Address Register

Memory Address: LBAR + 40h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:7	0 R/W	**CORB Base Address:** This field is the lower address of the Command Output Ring Buffer, allowing the CORB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0 RO	Reserved

10.3.17 CORBWP—CORB Write Pointer Register

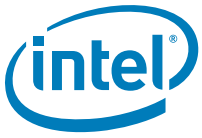
Memory Address: LBAR + 48h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:8	00h RO	Reserved
7:0	00h R/W	**CORB Write Pointer:** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read pointer matches the Write pointer. Supports 256 CORB entries (256 x 4 byte = 1 KB). This register field may be written when the DMA engine is running.

10.3.18 CORBRP—CORB Read Pointer Register

Memory Address: LBAR + 4Ah Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15	0 R/W	**CORB Read Pointer Reset:** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual prefetched commands in the CORB hardware buffer within the Intel HD Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	00h RO	Reserved
7:0	00h RO	**CORB Read Pointer (CORBRP):** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4 byte =1 KB). This field may be read while the DMA engine is running.



10.3.19 CORBCTL—CORB Control Register

Memory Address: LBAR + 4Ch Attribute: R/W, RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:2	00h RO	Reserved
1	0 R/W	**Enable CORB DMA Engine:** 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	0 R/W	**CORB Memory Error Interrupt Enable:** If this bit is set, the controller will generate an interrupt if the CMEI status bit (LBAR + 4Dh: bit 0) is set.

10.3.20 CORBST—CORB Status Register

Memory Address: LBAR + 4dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h	Reserved

10.3.21 CORBSIZE—CORB Size Register

Memory Address: LBAR + 4Eh Attribute: RO
Default Value: 42h Size: 8 bits

Bit	Default and Access	Description
7:4	0100b RO	**CORB Size Capability:** Hardwired to 0100b indicating that the Intel® SCH only supports a CORB size of 256 CORB entries (1024B).
3:2	00b RO	Reserved
1:0	10b RO	**CORB Size:** Hardwired to 10b which sets the CORB size to 256 entries (1024 B).

10.3.22 RIRBBASE—RIRB Base Address Register

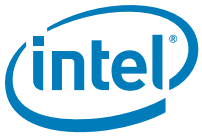
Memory Address: LBAR + 50h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:7	0s R/W	**CORB Lower Base Address:** This field is the lower address of the Response Input Ring Buffer, allowing the RIRB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	00h RO	Reserved

10.3.23 RIRBWP—RIRB Write Pointer Register

Memory Address: LBAR + 58h Attribute: WO, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15	0 WO	**RIRB Write Pointer Reset:** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit is always read as 0.
14:8	00h RO	Reserved
7:0	00h RO	**RIRB Write Pointer (RIRBWP):** This field is the indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2-DWord RIRB entry units (since each RIRB entry is 2 dwords long). Supports up to 256 RIRB entries (256 x 8 bytes = 2KB). This register field may be written when the DMA engine is running.



10.3.24 RINTCNT—Response Interrupt Count Register

Memory Address: LBAR + 5Ah Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:8	00h RO	Reserved
7:0	00h R/W	**N Response Interrupt Count** 0000 0001b = 1 response sent to RIRB ..... 1111 1111b = 255 responses sent to RIRB 0000 0000b = 256 responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each response occupies 2 DWords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codecs responds in one frame, then the count is increased by the number of responses received in the frame.

10.3.25 RIRBCTL—RIRB Control Register

Memory Address: LBAR + 5Ch Attribute: R/W, RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:3	0h RO	Reserved
2	0 R/W	**Response Overrun Interrupt Control:** If this bit is set, the hardware will generate an interrupt when the Response Overrun Interrupt Status bit (LBAR + 5Dh: bit 2) is set.
1	0 R/W	**Enable RIRB DMA Engine:** 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	0 R/W	**Response Interrupt Control**: 0 = Disable Interrupt 1 = Generate an interrupt after N number of responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

10.3.26 RIRBSTS—RIRB Status Register

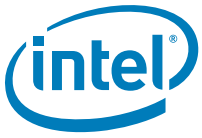
Memory Address: LBAR + 5Dh Attribute: R/WC, RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:3	0h RO	Reserved
2	0 R/WC	**Response Overrun Interrupt Status:** Software sets this bit to 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.
1	0 RO	Reserved
0	0 R/WC	**Response Interrupt:** Hardware sets this bit to 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.

10.3.27 RIRBSIZE—RIRB Size Register

Memory Address: LBAR + 5Eh Attribute: RO
Default Value: 40h Size: 8 bits

Bit	Default and Access	Description
7:4	0100b RO	**RIRB Size Capability:** Hardwired to 0100b indicating that the Intel® SCH only supports a RIRB size of 256 RIRB entries (2048 B).
3:2	00b RO	Reserved
1:0	00b RO	**RIRB Size:** Hardwired to 10b which sets the CORB size to 256 entries (2048 B).



10.3.28 IC—Immediate Command Register

Memory Address: LBAR + 60h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0 R/W	**Immediate Command Write:** The command to be sent to the codec by the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit (LBAR + 68h: bit 0).

10.3.29 IR—Immediate Response Register

Memory Address: LBAR + 64h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0 RO	**Immediate Response Read (IRR):** This register contains the response received from a codec resulting from a command sent by the Immediate Command mechanism. If multiple codecs responded in the same time, there is no assurance as to which response will be latched. Therefore, broadcast-type commands must not be issued by the Immediate Command mechanism.

10.3.30 IRS—Immediate Command Status Register

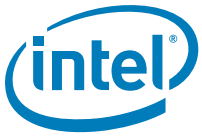
Memory Address: LBAR + 68h Attribute: R/W, R/WC, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:2	0 RO	Reserved
1	0 R/WC	**Immediate Result Valid (IRV):** This bit is set to 1 by hardware when a new response is latched into the Immediate Response register (LBAR + 64). This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit by writing a 1 to it before issuing a new command so that the software may determine when a new response has arrived.
0	0 R/W	**Immediate Command Busy (ICB):** When this bit is read as 0, it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (by software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. **NOTE:** An Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

10.3.31 DPBASE—DMA Position Base Address Register

Memory Address: LBAR + 70h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:7	0 R/W	**DMA Position Base Address:** This field is the lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control and must be programmed with a valid value before the Flush Control bit (LBAR+08h:Bit 1) is set.
6:1	00000b RO	Reserved
0	0 R/W	**DMA Position Buffer Enable:** When this bit is set to 1, the controller will write the DMA positions of each of the DMA engines to the buffer in the main memory periodically (typically once per frame). Software can use this value to know what data in memory is valid data.



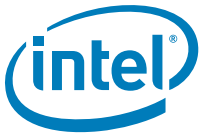
10.3.32 SDCTL—Stream Descriptor Control Register

Memory Address: Input Stream[0]: LBAR + 80h
Input Stream[1]: LBAR + A0h
Output Stream[0]: LBAR + C0h
Output Stream[1]: LBAR + E0h
Attribute: R/W, RO

Default Value: 040000h
Size: 24 bits

Bit	Default and Access	Description
23:20	0h R/W	**Stream Number:** This value reflect the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have its stream number encoded on the HDA_SYNC signal. When an input stream is detected on any of the SDI signals that match this value, the data samples are loaded into FIFO associated with this descriptor. Note that while a single SDI input may contain data from more than one stream number, two different SDI inputs may not be configured with the same stream number. 0000 = Reserved 0001 = Stream 1 ..... 1110 = Stream 14 1111 = Stream 15
19	0 RO	**Bidirectional Direction Control:** This bit is only meaningful for bidirectional streams; therefore, this bit is hardwired to 0.
18	1 RO	**Traffic Priority:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled through the PCI Express registers.
17:16	00 RO	**Stripe Control:** This bit is only meaningful for input streams; therefore, this bit is hardwired to 0.
15:5	0 RO	Reserved
4	0 R/W	**Descriptor Error Interrupt Enable** 0 = Disable 1 = An interrupt is generated when the Descriptor Error Status bit is set.
3	0 R/W	**FIFO Error Interrupt Enable:** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, Bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0 R/W	**Interrupt on Completion Enable:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, Bit 2 in the Status register will be set, but the interrupt will not occur.

Bit	Default and Access	Description
1	0 R/W	**Stream Run (RUN):** 0 = The DMA engine associated with this input stream will be disabled. The hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine. 1 = The DMA engine associated with this input stream will be enabled to transfer data from the FIFO to the main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.
0	0 R/W	**Stream Reset (SRST):** 0 = Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. 1 = Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFOs for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. The RUN bit must be cleared before SRST is asserted.



10.3.33 SDSTS—Stream Descriptor Status Register

Memory Address: Input Stream[0]: LBAR + 83h
Input Stream[1]: LBAR + A3h
Output Stream[0]: LBAR + C3h
Output Stream[1]: LBAR + E3h
Attribute: R/WC, RO

Default Value: 00h
Size: 8 bits

Bit	Default and Access	Description
7:6	00b RO	Reserved
5	0 RO	**FIFO Ready (FIFORDY):** For output streams, the controller hardware will set this bit to 1 while the output DMA FIFO contains enough data to maintain the stream on the link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
4	0 R/WC	**Descriptor Error:** When set, this bit indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor list useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stopped. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0 R/WC	**FIFO Error:** This bit is set when a FIFO error occurs. This bit is set even if an interrupt is not enabled. The bit is cleared by writing a 1 to it. For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers do not increment and the incoming data is not written into the FIFO, thereby being lost. For an output stream, this indicates a FIFO underrun when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0 R/WC	**Buffer Completion Interrupt Status:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to it.
1:0	00 RO	Reserved

10.3.34 SDLPIB—Stream Descriptor Link Position in Buffer Register

Memory Address: Input Stream[0]: LBAR + 84h; Input Stream[1]: LBAR + A4h; Output Stream[0]: LBAR + C4h; Output Stream[1]: LBAR + E4h — Attribute: RO

Default Value: 00000000h — Size: 32 bits

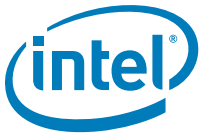
Bit	Default and Access	Description
31:0	0 RO	**Link Position in Buffer:** This field indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

10.3.35 SDCBL—Stream Descriptor Cyclic Buffer Length Register

Memory Address: Input Stream[0]: LBAR + 88h; Input Stream[1]: LBAR + A8h; Output Stream[0]: LBAR + C8h; Output Stream[1]: LBAR + E8h — Attribute: R/W

Default Value: 00000000h — Size: 32 bits

Bit	Default and Access	Description
31:0	0 R/W	**Cyclic Buffer Length:** Indicates the number of bytes in the complete cyclic buffer. This register represents an integer number of samples. Link Position in Buffer will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should be only modified when the RUN bit is 0. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfer may be corrupted.



10.3.36 SDLVI—Stream Descriptor Last Valid Index Register

Memory Address: Input Stream[0]: LBAR + 8Ch; Input Stream[1]: LBAR + ACh; Output Stream[0]: LBAR + CCh; Output Stream[1]: LBAR + ECh — Attribute: R/W, RO

Default Value: 0000h — Size: 16 bits

Bit	Default and Access	Description
15:8	00h RO	Reserved
7:0	00h R/W	**Last Valid Index:** The value written to this register indicates the index for the last valid Buffer Descriptor in BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. This field must be at least 1 (i.e., there must be at least 2 valid entries in the buffer descriptor list before DMA operations can begin). This value should only modified when the RUN bit is 0.

10.3.37 SDFIFOW—Stream Descriptor FIFO Watermark Register

Memory Address: Input Stream[0]: LBAR + 8Eh; Input Stream[1]: LBAR + AEh; Output Stream[0]: LBAR + CEh; Output Stream[1]: LBAR + EEh — Attribute: R/W, RO

Default Value: 0004h — Size: 16 bits

Bit	Default and Access	Description
15:3	0 RO	Reserved
2:0	100b R/W	**FIFO Watermark (FIFOW).** Indicates the minimum number of bytes accumulated/free in the FIFO before the controller will start a fetch/ eviction of data. 010 = 8 B 011 = 16 B 100 = 32 B (Default) Others = Unsupported **NOTE:** When the bit field is programmed to an unsupported size, the hardware sets itself to the default value. Software must read the bit field to test if the value is supported after setting the bit field.

10.3.38 SDFIFOS—Stream Descriptor FIFO Size Register

Memory Address:	Input Stream[0]: LBAR + 90h Input Stream[1]: LBAR + B0h Output Stream[0]: LBAR + D0h Output Stream[1]: LBAR + F0h	Attribute: Output:	Input: RO R/W, RO
Default Value:	Input Stream: 0077h Output Stream: 00BFh	Size:	16 bits

Bit	Default and Access	Description
15:8	00h RO	Reserved
7:0	77h RO (input) BFh R/W (output)	**FIFO Size — RO (Input stream), R/W (Output stream):** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. The value in this field is different for input and output streams. It is also dependent on the Bits per Samples setting for the corresponding stream. Following are the values read/written from/to this register for input and output streams, and for non-padded and padded bit formats: *Output Stream R/W value*:

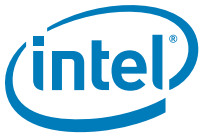
Value	Output Streams
0Fh = 16B	8, 16, 20, 24, or 32 bit Output Streams
1Fh = 32B	8, 16, 20, 24, or 32 bit Output Streams
3Fh = 64B	8, 16, 20, 24, or 32 bit Output Streams
7Fh = 128B	8, 16, 20, 24, or 32 bit Output Streams
BFh = 192B	8, 16, or 32 bit Output Streams
FFh = 256B	20, 24 bit Output Streams

NOTES:
1. All other values not listed are not supported.
2. When the output stream is programmed to an unsupported size, the hardware sets itself to the default value (BFh).
3. Software must read the bit field to test if the value is supported after setting the bit field.

Input Stream RO value:

Value	Input Streams
77h = 120B	8, 16, 32 bit Input Streams
9Fh = 160B	20, 24 bit Input Streams

NOTE: The default value is different for input and output streams, and reflects the default state of the BITS fields (in Stream Descriptor Format registers) for the corresponding stream.



10.3.39 SDFMT—Stream Descriptor Format Register

Memory Address: Input Stream[0]: LBAR + 92h
Input Stream[1]: LBAR + B2h
Output Stream[0]: LBAR + D2h
Output Stream[1]: LBAR + F2h
Attribute: R/W, RO

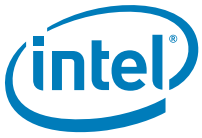
Default Value: 0000h
Size: 16 bits

Bit	Default and Access	Description
15	0 RO	Reserved
14	0 R/W	**Sample Base Rate:** R/W 0 = 48 kHz 1 = 44.1 kHz
13:11	000b R/W	**Sample Base Rate Multiple:** R/W 000 = 48 kHz, 44.1 kHz or less 001 = x2 (96 kHz, 88.2 kHz, 32 kHz) 010 = x3 (144 kHz) 011 = x4 (192 kHz, 176.4 kHz) Others = Reserved.
10:8	000b R/W	**Sample Base Rate Divisor:** 000 = Divide by 1(48 kHz, 44.1 kHz) 001 = Divide by 2 (24 kHz, 22.05 kHz) 010 = Divide by 3 (16 kHz, 32 kHz) 011 = Divide by 4 (11.025 kHz) 100 = Divide by 5 (9.6 kHz) 101 = Divide by 6 (8 kHz) 110 = Divide by 7 111 = Divide by 8 (6 kHz)
7	0 RO	Reserved
6:4	000b R/W	**Bits per Sample (BITS):** 000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries Others = Reserved.
3:0	0h R/W	**Number of Channels (CHAN):** Indicates number of channels in each frame of the stream. 0000 =1 0001 =2 ..... 1111 =16

10.3.40 SDBDPL—Stream Descriptor Buffer Descriptor Pointer List Base Register

Memory Address:	Input Stream[0]: LBAR + 98h Input Stream[1]: LBAR + B8h Output Stream[0]: LBAR + D8h Output Stream[1]: LBAR + F8h	Attribute:	R/W, RO, WO
Default Value:	00000000h	Size:	32 bits

Bit	Default and Access	Description
31:7	0 R/W	**Buffer Descriptor List Pointer Lower Base Address:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.
6:1	00h RO	Reserved
0	0 RW/WO	**Protect (PROT):** When set, all bits of this register are WO and return 0 when read. When cleared, bits are RW. Tis bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value.



10.4 Vendor Specific Memory Mapped Registers

10.4.1 EM1—Extended Mode 1 Register

Memory Address: 1000h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:24	0 RO	Reserved
28:28	00b RW	**Loopback Enable (LPBKEN):** When set, output data is rerouted to the input. Each input has its own loopback enable.
27:26	00 RW	**Free Count Request (FREECNTREQ):** This field determines the clock in which freecnt will be requested from the XFR layer. BIOS or software must set FREECNTREQ to “11” Any other selection will cause RIRB failures.
25	0b RW	**Phase Select (PSEL):** Sets the input data sample point within phyclk. 1 = Phase C, 0 = Phase D
24	1b RW	**Boundary Break (128_4K):** Sets the break boundary for reads. 0 = 4KB 1 = 128B
23:21	000b RW	**CORB Pace (CORBPACE):** Determines the rate at which CORB commands are issued on the link. 000 = Every Frame 001 = Every 2 Frames ..... 111 = Every 8 Frames
20	0b RW	**FIFO Ready Select (FRS):** When cleared, SDS.FRDY is asserted when there are 2 or more packets available in the FIFO. When set, SDS.FRDY is asserted when there are one or more packets available in the FIFO.
19:15	00000b RO	Reserved
14	0b RW	**48 KHz Enable:** When set, Intel® SCH adds one extra bitclk to every twelfth frame. When cleared, it will use the normal functionality and send 500 bitclks per frame.
13	0b RW	**Dock Enable Signal Transition Select (DETS):** When set, DOCK_EN# transitions off the falling edge of BCLK (phase C). When cleared, DOCK_EN# transitions 1/4 BCLK after the falling edge of BCLK (phase D).
12:6	0s RO	Reserved
5:4	00b WO	**Input Repeat Count Resets (IRCR):** Software writes a 1 to clear the respective Repeat Count to 00h. Reads from these bits return 0. Bit 5 = Input Stream 1 Repeat Count Reset Bit 4 = Input Stream 0 Repeat Count Reset
3:2	00b RO	Reserved
1:0	00b WO	**Output Repeat Count Resets (ORCR):** Software writes a 1 to clear the respective Repeat Count to 00h. Reads from these bits return 0. Bit 1 = Output Stream 1 Repeat Count Reset Bit 0 = Output Stream 0 Repeat Count Reset

10.4.2 INRC—Input Stream Repeat Count Register

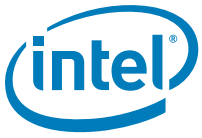
Memory Address: 1004h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:24	0 RO	Reserved
15:8	00h RO	**Stream 1 (S1):** Reports the number of times a buffer descriptor list has been repeated.
7:0	00h RO	**Stream 0 (S0):** Reports the number of times a buffer descriptor list has been repeated.

10.4.3 OUTRC—Output Stream Repeat Count Register

Memory Address: 1008h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:16	0 RO	Reserved
15:8	00h RO	**Stream 1 (S1):** Reports the number of times a buffer descriptor list has been repeated.
7:0	00h RO	**Stream 0 (S0):** Reports the number of times a buffer descriptor list has been repeated.



10.4.4 FIFOTRK – FIFO Tracking Register

Memory Address: 100Ch Attribute: R/W, RO
Default Value: 000FF800h Size: 32 bits

Bit	Default and Access	Description
31:20	000h RO	Reserved
19:11	1FFh RO	**Minimum Status (MSTS):** Tracks the minimum FIFO free count for inbound engines, and the minimum avail count for outbound engines when EN is set and R is deasserted. The FIFO of the DMA selected by SEL is tracked.
10:5	000h RO	**Error Count (EC):** Increments each time a FIFO error occurs in the FIFO which the DMA select is pointing to when the enable bit is set and R is deasserted. When EC reaches a max count of 1FFh (63), the count saturates and holds the max count until it is reset.
4:2	000b R/W	**Select (SEL):** MSTS and EC track the FIFO for the DMA select by this register, as follows: 000 = Output DMA 0 001 = Output DMA 1 010 = Reserved 011 = Reserved 100 = Input DMA 0 101 = Input DMA 1 110 = Reserved 111 = Reserved
1	0 R/W	**Enable (EN):** When set, MSTS and EC track the minimum FIFO status or error count. When cleared, MSTS and EC hold its previous value.
0	0 R/W	**Reset (R):** When set, MSTS and EC are reset to their default value.

10.4.5 SDPIB—Stream DMA Position in Buffer Register

Memory Address: Input Stream 0: 1010h Attribute: RO
Input Stream 1: 1014h
Output Stream 0: 1020h
Output Stream 2: 1024h
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0 RO	**Position (POS):** Indicates the number of bytes processed by the DMA engine from the beginning of the BDL. For output streams, it is incremented when data is loaded into the FIFO.

10.4.6 EM2—Extended Mode 2 Register

Memory Address: 1030h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:9	0 RO	Reserved
8	0 R/W	**CORB Reset Pointer Change Disable (CORPRPDIS):** When cleared, CORBRP.RPR works as described. When this bit is set, the CORB FIFO is not reset and CORBRP.RPR is WO and always read as 0.
7:0	0h RO	Reserved

10.4.7 WLCLKA—Wall Clock Counter Alias Register

Memory Address: 2030h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0 RO	**Wall Clock Counter Alias (CounterA):** Alias of WALCK. 32-bit counter that is incremented on each link H_CLKIN period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the H_CLKIN bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

10.4.8 SLPIB—Stream Link Position in Buffer Register

Memory Address: Input Stream 0: 2084h Attribute: RO
Input Stream 1: 20A4h
Output Stream 0: 2104h
Output Stream 2: 2124h
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0 RO	**Position (POS):** Alias of the corresponding LPIB. Indicates the number of bytes that have been received off the link. It counts from 0 to the value in the Cyclic Buffer Length register and wraps.

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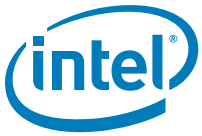


11 PCI Express* (D28:F0, F1)

11.1 Functional Description

There are two PCI Express root ports available in the Intel® SCH. They reside in device 28 and take function 0 and 1. Port 1 is function 0 and Port 2 is function 1.

11.1.1 Interrupt Generation

If enabled to do so, the Intel® SCH PCI Express root port generates interrupts as a result of hot-plug and power management events. These interrupts can be communicated either by legacy interrupt pins (internal to the Intel® SCH), or as Message Signal Interrupt messages to the FSB. For the legacy pin behavior, the D28IP (Base address + 310Ch) and D28IR (Base address + 3146h) registers can be configured to drive a particular internal interrupt signal.

The following table summarizes interrupt behavior for MSI and wire modes. In the table, “bits” refers to the hot-plug and PME interrupt bits.

Table 28. MSI vs. PCI IRQ Actions

Interrupt Register	Wire-Mode Action	MSI Action
All bits are 0	Wire inactive	No action
One or more bits set to 1	Wire active	Send message
One or more bits set to 1, new bit gets set to 1	Wire active	Send message
One or more bits set to 1, software clears some (but not all) bits	Wire active	Send message
One or more bits set to 1, software clears all bits	Wire inactive	No action
Software clears one or more bits, and one or more bits are set on the same clock	Wire active	Send message

11.1.2 Power Management

11.1.2.1 Sleep State Support

Software initiates the transition to S3/S4/S5 by performing an I/O write to the Power Management Control register. After the I/O write completion has been returned to the processor, each root port will send a PME_Turn_Off TLP (Transaction Layer Packet) message on it's downstream link. The device attached to the link will eventually respond with a PME_TO_Ack TLP message followed by sending a PM_Enter_L23 DLLP (Data Link Layer Packet) request to enter the L2/L3 Ready state. When all of the Intel® SCH root ports links are in the L2/L3 Ready state, the Intel® SCH power management control logic will proceed with the entry into S3/S4/S5.

Prior to entering S3, software is required to put each device into D3HOT. When a device is put into D3HOT it will initiate entry into a L1 link state by sending a PM_Enter_L1 DLLP. Thus under normal operating conditions when the root ports sends the PME_Turn_Off message the link will be in state L1. However, when the root port is instructed to send the PME_Turn_Off message, it will send it whether or not the link was in L1. Endpoints attached to ICH can make no assumptions about the state of the link prior to receiving a PME_Turn_Off message.

11.1.2.2 Resuming From Suspended State

The root port can detect a wake event through the WAKE# signal and wake the system. When the root port detects a WAKE# assertion, an internal signal is sent to the power management controller of the Intel® SCH to cause the system to wake up. This internal message is not logged in any register, nor is an interrupt/GPE generated.

11.1.2.3 Device Initiated PM_PME Message

When the system has returned to a working state from a previous low power state, a device requesting service will send a PM_PME message continuously, until acknowledge by the root port. The root port will take different actions depending upon whether this is the first PM_PME has been received, or whether a previous message has been received but not yet serviced by the operating system.

If this is the first message received (RSTS.PS - D28:F0/F1:Offset 60h:bit 16 is cleared), the root port will set RSTS.PS, and log the PME Requester ID into RSTS.RID (D28:F0/F1:Offset 60h:bits 15:0). If an interrupt is enabled by RCTL.PIE (D28:F0/F1:Offset 5Ch:bit 3), an interrupt will be generated. This interrupt can be either a pin or an MSI if MSI is enabled by MSI_CTL.MSIE (D28:F0/F1:Offset 82h:bit 0). See Section 11.1.2.4 for SMI/SCI generation.

If this is a subsequent message received (RSTS.PS is already set), the root port will set RSTS.PP (D28:F0/F1:Offset 60h:bit 17) and log the PME Requester ID from the message in a hidden register. No other action will be taken.

When the first PME event is cleared by software clearing RSTS.PS, the root port will set RSTS.PS, clear RSTS.PP, and move the requester ID from the hidden register into RSTS.RID.

If RCTL.PIE is set, generate an interrupt. If RCTL.PIE is not set, send over to the power management controller so that a GPE can be set. If messages have been logged (RSTS.PS is set), and RCTL.PIE is later written from a 0 to a 1, and interrupt must be generated. This last condition handles the case where the message was received prior to the operating system re-enabling interrupts after resuming from a low power state.

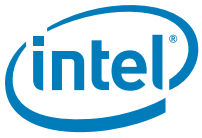
11.1.2.4 SMI/SCI Generation

Interrupts for power management events are not supported on legacy operating systems. To support power management on non-PCI Express aware operating systems, PM events can be routed to generate SCI. To generate SCI, MPC.PMCE must be set. When set, a power management event will cause SMSCS.PMCS (D28:F0/F1:Offset DCh:bit 31) to be set.

Additionally, BIOS workarounds for power management can be supported by setting MPC.PMME (D28:F0/F1:Offset D8h:bit 0). When this bit is set, power management events will set SMSCS.PMMS (D28:F0/F1:Offset DCh:bit 0), and SMI # will be generated. This bit will be set regardless of whether interrupts or SCI is enabled. The SMI# may occur concurrently with an interrupt or SCI.

11.1.3 Hot-Plug

The Intel® SCH does not support PCI Express Hot-Plug.



11.1.4 Additional Clarifications

11.1.4.1 Non-Snoop Cycles Are Not Supported

The Intel® SCH does not support No Snoop cycles on PCIe. DCTL.ENS can never be set. Platform BIOS must disable generation of these cycles in all installed PCIe devices. Generation of a No Snoop request by a PCIe device may result in a protocol violation and lead to errors.

For example, a no-snoop read by a device may be returned by a snooped completion, and this attribute difference, a violation of the specification, will cause the device to ignore the completion.

11.2 PCI Express* Configuration Registers

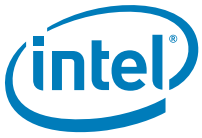
Table 29. PCI Express* Register Address Map (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See Description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See Description	RO
09h–0Bh	CC	Class Codes	060400h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	81h	RO
18h–1Ah	BNUM	Bus Number	000000h	R/W
1Bh	SLT	Secondary Latency Timer	0h	RO
1Ch–1Dh	IOBL	I/O Base and Limit	0000h	R/W, RO
1Eh–1Fh	SSTS	Secondary Status	0000h	R/WC, RO
20h–23h	MBL	Memory Base and Limit	00000000h	R/W, RO
24h–27h	PMBL	Prefetchable Memory Base and Limit	00010001h	R/W, RO
34h	CAP_PTR	Capabilities Pointer	40h	RO
3ch	INT_LN	Interrupt Line	00h	R/W
3dh	INT_PN	Interrupt Pin	See description	RO
3Eh–3Fh	BCTRL	Bridge Control	0000h	R/W, RO
40h	PCIE_CAPID	PCI Express Capability ID	10	RO
41h	NXT_PTR1	Next Item Pointer #1	90h	RO
42h–43h	PCIECAP	PCI Express Capabilities	0041	R/WO, RO
44h–47h	DCAP	Device Capabilities	00000FE0h	RO

Table 29. PCI Express* Register Address Map (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
48h–49h	DCTL	Device Control	0000h	R/W, RO
4ah–4bh	DSTS	Device Status	0010h	R/WC, RO
4Ch–4Fh	LCAP	Link Capabilities	00054C11h	RO, R/WO
50h–51h	LCTL	Link Control	0000h	R/W, WO, RO
52h–53h	LSTS	Link Status	See description	RO
54h–57h	SLCAP	Slot Capabilities	00000060h	R/WO, RO
58h–59h	SLCTL	Slot Control	0000h	R/W, RO
5Ah–5Bh	SLSTS	Slot Status	See description	R/WC, RO
5Ch–5Dh	RCTL	Root Control	0000h	R/W, RO
5Eh	RCAP	Root Capabilities	xxxxh	RO
60h–63h	RSTS	Root Status	00000000h	R/WC, RO
90h	SV_CAPID	Subsystem Vendor Capability ID	0dh	RO
91h	NXT_PTR3	Next Item Pointer #3	A0h	RO
94h–97h	SVID	Subsystem Vendor Identification	00h	R/WO
A0h	PM_CAPID	Power Management Capability ID	01h	RO
A1h	NXT_PTR4	Next Item Pointer #4	00h	RO
A2h–A3h	PM_CAP	Power Management Capabilities	C802h	RO
A4–A7h	PM_CNTL_STS	Power Management Control/ Status	00000000h	R/W, RO
D8–Dbh	MPC	Miscellaneous Port Configuration	00110000h	R/W, RO
DC–DFh	SMSCS	SMI/SCI Status	00000000h	R/WC, RO
FCh–FFh	FD	Function Disable	00000000h	R/W, RO

NOTE: Address locations that are not shown should be treated as Reserved.



11.2.1 VID—Vendor Identification Register

Address Offset: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Default and Access	Description
15:0	8086h RO	**Vendor ID (VID):** This is a 16-bit value assigned to Intel.

11.2.2 DID—Device Identification Register

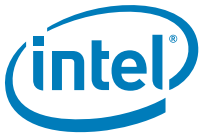
Address Offset: 02h–03h Attribute: RO
Default Value: See Description Size: 16 bits

Bit	Default and Access	Description
15:0	See Description RO	**Device ID (DID)**: This is a 16-bit value assigned to the Intel® SCH PCI Express controller. Port 1 = 8110h Port 2 = 8112h

11.2.3 PCICMD—PCI Command Register

Address Offset: 04h–05h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:11	0h RO	Reserved
10	0 R/W	**Interrupt Disable (ID)**: This bit disables pin-based INTx# interrupts on enabled hot-plug and power management events. 0 = Internal INTx# messages are generated if there is an interrupt for hot-plug or power management. 1 = Internal INTx# messages will not be generated. This bit does not effect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	0 RO	Reserved
8	0 R/W	**SERR# Enable (SEE)**: Hardwired to 0 to indicate this port cannot generate SERR# messages.
7:3	0h RO	Reserved
2	0 R/W	**Bus Master Enable (BME)** 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a PCI Express device.
1	0 R/W	**Memory Space Enable (MSE)** 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI Express device.
0	0 R/W	**I/O Space Enable (IOSE)**: This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI Express device.



11.2.4 PCISTS—PCI Status Register

Address Offset: 06h–07h Attribute: R/WC, RO
Default Value: 0010h Size: 16 bits

Note: There is a secondary status register (SSTS) located at offset 1Eh.

Bit	Default and Access	Description
15	0 RO	Reserved
14	0 R/WC	**Signaled System Error (SSE)** 0 = No system error signaled. 1 = Set when the root port signals a system error to the internal SERR# logic.
13:5	000h RO	Reserved
4	1 RO	**Capabilities List (CLIST)**: Hardwired to 1 indicating the presence of a capabilities list (at offset 34h)
3	0 RO	**Interrupt Status (IS):** Indicates status of hot-plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. This bit is set regardless of the state of PCICMD.Interrupt Disable bit (D28:F0/F1:04h:bit 10).
2:0	000b RO	Reserved

11.2.5 RID—Revision Identification Register

Offset Address: 08h Attribute: RO
Default Value: See description Size: 8 bits

Bit	Default and Access	Description
7:0	See Description RO	**Revision ID (RID):** Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the value of the Revision ID Register.

11.2.6 CC—Class Codes Register

Address Offset: 09h–0Bh Attribute: RO
Default Value: 060400h Size: 24 bits

Bit	Default and Access	Description
23:16	06h RO	**Base Class Code (BCC)**: 06h indicates the device is a bridge device.
15:8	04h RO	**Sub Class Code (SCC)**: 04h indicates this is a PCI-to-PCI bridge.
7:0	00h RO	**Programming Interface (PI)**: No specific register level programming interface defined.

11.2.7 CLS—Cache Line Size Register

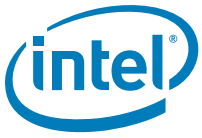
Address Offset: 0Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Cache Line Size (CLS)**: This is read/write but contains no functionality, per the *PCI Express Base Specification*.

11.2.8 PLT—Primary Latency Timer Register

Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:3	0h RO	**Latency Count (CT)**: Reserved per the *PCI Express Base Specification*.
2:0	000b RO	Reserved



11.2.9 HEADTYP—Header Type Register

Address Offset: 0Eh Attribute: RO
Default Value: 81h Size: 8 bits

Bit	Default and Access	Description
7	1 RO	**Multi-Function Device (MFD)** 0 = Single-function device. 1 = Multi-function device.
6:0	01h RO	**Configuration Layout (CL):** Indicates the header layout of the configuration space, which is a PCI-to-PCI bridge, indicated by 1h in this field.

11.2.10 BNUM—Bus Number Register

Address Offset: 18–1Ah Attribute: R/W
Default Value: 000000h Size: 24 bits

Bit	Default and Access	Description
23:16	00h R/W	**Subordinate Bus Number (SBBN)**: Indicates the highest PCI bus number below the bridge.
15:8	00h R/W	**Secondary Bus Number (SCBN)**: Indicates the bus number the port.
7:0	00h R/W	**Primary Bus Number (PBN)**: Indicates the bus number of the backbone.

11.2.11 SLT—Secondary Latency Timer

Address Offset: 1Bh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Secondary Latency Timer (SLT)**: Reserved for a Root Port per the *PCI Express Base Specification.*

11.2.12 IOBL—I/O Base and Limit Register

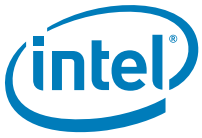
Address Offset: 1Ch–1Dh
Attribute: R/W, RO
Default Value: 0000h
Size: 16 bits

Bit	Default and Access	Description
15:12	0h R/W	**I/O Limit Address (IOLA)**: I/O Base bits corresponding to address lines 15:12 for 4 KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC)**: Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h R/W	**I/O Base Address (IOBA)**: I/O Base bits corresponding to address lines 15:12 for 4 KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC)**: Indicates that the bridge does not support 32-bit I/O addressing.

11.2.13 SSTS—Secondary Status Register

Address Offset: 1Eh–1Fh
Attribute: R/WC, RO
Default Value: 0000h
Size: 16 bits

Bit	Default and Access	Description
15	0 R/WC	**Detected Parity Error (DPE)** 0 = No error. 1 = The port received a poisoned TLP.
14	0 R/WC	**Received System Error (RSE)** 0 = No error. 1 = The port received an ERR_FATAL or ERR_NONFATAL message from the device.
13	0 R/WC	**Received Master Abort (RMA)** 0 = Unsupported Request not received. 1 = The port received a completion with “Unsupported Request” status from the device.
12	0 R/WC	**Received Target Abort (RTA)** 0 = Completion Abort not received. 1 = The port received a completion with “Completion Abort” status from the device.
11	0 RO	**Signaled Target Abort (STA)**: Reserved. The Intel® SCH cannot generate a target abort.
10:9	00 RO	**Secondary DEVSEL# Timing Status (SDTS)**: Reserved per *PCI Express Base Specification*.
8	0 R/WC	**Data Parity Error Detected (DPD)** 0 = Conditions below did not occur. 1 = Set when the BCTRL.PERE (D28:F0/F13E: bit 0) is set, and either of the following two conditions occurs: • Port receives completion marked poisoned. • Port poisons a write request to the secondary side.
7:0	00h RO	Reserved



11.2.14 MBL—Memory Base and Limit Register

Address Offset:	20h–23h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Accesses that are within the ranges specified in this register will be sent to the attached device if the Memory Space Enable bit of PCICMD is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the internal Intel® SCH message network if the Bus Master enable bit of PCICMD is set.

Bit	Default and Access	Description
31:20	000h R/W	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1 MB aligned value of the range.
19:16	0h RO	Reserved
15:4	000h R/W	**Memory Base (MB)**: These bits are compared with bits 31:20 of the incoming address to determine the lower 1 MB aligned value of the range.
3:0	0h RO	Reserved

11.2.15 PMBL—Prefetchable Memory Base and Limit Register

Address Offset:	24h–27h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Accesses that are within the ranges specified in this register will be sent to the device if the Memory Space Enable bit of PCICMD is set. The comparison performed is:

$$PMBU32.PMB \geq AD[63:32]:AD[31:20] \leq PMLU32.PML.$$

Accesses from the device that are outside the ranges specified will be forwarded to the backbone if the Bus Master enable bit of PCICMD is set.

Bit	Default and Access	Description
31:20	000h R/W	**Prefetchable Memory Limit (PML)**: These bits are compared with bits 31:20 of the incoming address to determine the upper 1 MB aligned value of the range.
19:16	0h RO	**64-bit Indicator (I64L)**: Indicates support for 64-bit addressing
15:4	000h R/W	**Prefetchable Memory Base (PMB)**: These bits are compared with bits 31:20 of the incoming address to determine the lower 1 MB aligned value of the range.
3:0	0h RO	**64-bit Indicator (I64B)**: Indicates support for 64-bit addressing

11.2.16 CAP_PTR—Capabilities Pointer Register

Address Offset: 34h Attribute: R0
Default Value: 40h Size: 8 bits

Bit	Default and Access	Description
7:0	40h RO	**Pointer (PTR)**: Indicates that the pointer for the first entry in the capabilities list is at offset 40h in configuration space.

11.2.17 INT_LN—Interrupt Line Register

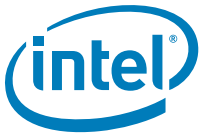
Address Offset: 3Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Interrupt Line (INT_LN)**: This data is not used by the Intel® SCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

11.2.18 INT_PN—Interrupt Pin Register

Address Offset: 3Dh Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Default and Access	Description
7:0	0xh RO	**Interrupt Pin (IPIN)**: This value tells the software which interrupt pin each PCI Express port uses. The upper 4 bits are hardwired to 0000b; bits 3:0 are determined by the Interrupt Pin default values programmed in the memory-mapped configuration space as follows: Port 1 D28IP.P1IP (Offset 310Ch, bits 3:0) Port 2 D28IP.P2IP (Offset 310Ch, bits 7:4) **NOTE:** This does not determine the mapping to the PIRQ pins.



11.2.19 BCTRL—Bridge Control Register

Address Offset: 3Eh–3Fh Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:12	0h RO	Reserved
11	0 RO	**Discard Timer SERR# Enable (DTSE)**: Reserved per *PCI Express Base Specification*, Revision 1.0a
10	0 RO	**Discard Timer Status (DTS)**: Reserved per *PCI Express Base Specification*, Revision 1.0a.
9	0 RO	**Secondary Discard Timer (SDT)**. Reserved per *PCI Express Base Specification*, Revision 1.0a.
8	0 RO	**Primary Discard Timer (PDT)**: Reserved per *PCI Express Base Specification*, Revision 1.0a.
7	0 RO	**Fast Back to Back Enable (FBE)**: Reserved per *PCI Express Base Specification*, Revision 1.0a.
6	0 R/W	**Secondary Bus Reset (SBR)**: Triggers a hot reset on the PCI Express port.
5	0 RO	**Master Abort Mode (MAM)**: Reserved per Express specification.
4	0 R/W	**VGA 16-Bit Decode (V16)** 0 = VGA range is enabled. 1 = The I/O aliases of the VGA range (see BCTRL:VE definition in Bit 3) are not enabled, and only the base I/O ranges can be decoded.
3	0 R/W	**VGA Enable (VE)** 0 = The ranges below will not be claimed off the backbone by the root port. 1 = The following ranges will be claimed off the backbone by the root port: • Memory ranges A0000h–BFFFFh • I/O ranges 3B0h – 3BBh and 3C0h – 3DFh, and all aliases of bits 15:10 in any combination of 1s
2	0 R/W	**ISA Enable (IE)**: This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. 0 = The root port will not block any forwarding from the backbone as described below. 1 = The root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1 KB block (offsets 100h to 3FFh).
1	0 R/W	**SERR# Enable (SE)** 0 = The messages described below are not forwarded to the backbone. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone.
0	0 R/W	**Parity Error Response Enable (PERE)** 0 = Poisoned write TLPs and completions indicating poisoned TLPs will not set the SSTS.DPD (D28:F0/F1:1Eh, bit 8). 1 = Poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD (D28:F0/F1:1Eh, bit 8).

11.2.20 PCIE_CAPID—PCI Express Capability ID Register

Address Offset: 40h Attribute: RO
Default Value: 10h Size: 8 bits

Bit	Default and Access	Description
7:0	10h RO	**Capability ID (CID)**: This field indicates this is a PCI Express capability.

11.2.21 NXT_PTR1—Next Item Pointer #1 Register

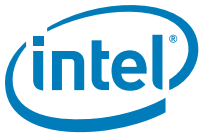
Address Offset: 41h Attribute: RO
Default Value: 90h Size: 8 bits

Bit	Default and Access	Description
7:0	90h RO	**Next Capability (NEXT):** This field indicates the location of the next capability.

11.2.22 PCIECAP—PCI Express Capabilities Register

Address Offset: 42h–43h Attribute: RO, R/WO
Default Value: 0041h Size: 16 bits

Bit	Default and Access	Description
15:14	00b RO	Reserved
13:9	00h RO	**Interrupt Message Number (IMN)**: The Intel® SCH does not have multiple MSI interrupt numbers.
8	0 R/WO	**Slot Implemented (SI)**: Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
7:4	4h RO	**Device/Port Type (DT)**: This field indicates this is a PCI Express root port.
3:0	1h RO	**Capability Version (CV)**: This field indicates PCI Express 1.0.



11.2.23 DCAP—Device Capabilities Register

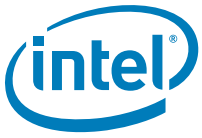
Address Offset: 44h–47h Attribute: RO
Default Value: 00008FC0h Size: 32 bits

Bit	Default and Access	Description
31:28	0h RO	Reserved
27:26	00b RO	**Captured Slot Power Limit Scale (CSPS)**: Not supported.
25:18	00h RO	**Captured Slot Power Limit Value (CSPV):** Not supported.
17:16	00b RO	Reserved
15	1 RO	**Role Based Error Reporting (RBER):** Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 specification.
14	0 RO	**Power Indicator Present (PIP)**: This bit indicates no power indicator is present on the root port.
13	0 RO	**Attention Indicator Present (AIP)**: This bit indicates no attention indicator is present on the root port.
12	0 RO	**Attention Button Present (ABP)**: This bit indicates no attention button is present on the root port.
11:9	111b RO	**Endpoint L1 Acceptable Latency (E1AL)**: This field indicates more than 4 µs. This field essentially has no meaning for root ports since root ports are not endpoints.
8:6	111b RO	**Endpoint L0 Acceptable Latency (E0AL)**: This field indicates more than 64 µs. This field essentially has no meaning for root ports since root ports are not endpoints.
5	0 RO	**Extended Tag Field Supported (ETFS)**: This bit indicates that 8-bit tag fields are supported.
4:3	00b RO	**Phantom Functions Supported (PFS)**: No phantom functions supported.
2:0	000b RO	**Max Payload Size Supported (MPS)**: This field indicates the maximum payload size supported is 128 Bytes.

11.2.24 DCTL—Device Control Register

Address Offset: 48h–49h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15	0 RO	Reserved
14:12	000b RO	**Max Read Request Size (MRRS)**: Hardwired to 0.
11	0 RO	**Enable No Snoop (ENS)**: Not supported. The root port will never issue non-snoop requests.
10	0 R/W	**Aux Power PM Enable (APME)**: The OS will set this bit to 1 if the device connected has detected aux power. It has no effect on the root port otherwise.
9	0 RO	**Phantom Functions Enable (PFE)**: Not supported.
8	0 RO	**Extended Tag Field Enable (ETFE)**: Not supported.
7:5	000b R/W	**Max Payload Size (MPS)**: The root port only supports 128-B payloads, regardless of the programming of this field.
4	0 RO	**Enable Relaxed Ordering (ERO)**: Not supported.
3	0 R/W	**Unsupported Request Reporting Enable (URE)**: 0 = The root port will ignore unsupported request errors. 1 = Allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0 R/W	**Fatal Error Reporting Enable (FEE)**: 0 = The root port will ignore fatal errors. 1 = Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0 R/W	**Non-Fatal Error Reporting Enable (NFE)**: 0 = The root port will ignore non-fatal errors. 1 = Enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0 R/W	**Correctable Error Reporting Enable (CEE)**: 0 = The root port will ignore correctable errors. 1 = Enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.



11.2.25 DSTS—Device Status Register

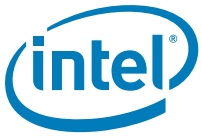
Address Offset: 4Ah–4Bh Attribute: R/WC, RO
Default Value: 0010h Size: 16 bits

Bit	Default and Access	Description
15:6	00h RO	Reserved
5	0 RO	**Transactions Pending (TDP)**: This bit has no meaning for the root port since only one transaction may be pending to the Intel® SCH, so a read of this bit cannot occur until it has already returned to 0.
4	1 RO	**AUX Power Detected (APD):** The root port contains AUX power for wake up.
3	0 R/WC	**Unsupported Request Detected (URD)**: This bit indicates an unsupported request was detected.
2	0 R/WC	**Fatal Error Detected (FED)**: This bit indicates a fatal error was detected. 0 = No fatal errors have occurred. 1 = A fatal error occurred from a data link protocol error, link training error, buffer overflow, or malformed TLP.
1	0 R/WC	**Non-Fatal Error Detected (NFED)**: This bit indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout.
0	0 R/WC	**Correctable Error Detected (CED)**: This bit indicates a correctable error was detected. 0 = Correctable has not occurred. 1 = The port received an internal correctable error from receiver errors/ framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

11.2.26 LCAP—Link Capabilities Register

Address Offset: 4Ch–4Fh Attribute: R/WO, RO
Default Value: 00054C11h Size: 32 bits

Bit	Default and Access	Description
31:24	00h RO	**Port Number (PN)**: Indicates the port number for the root port. This value is different for each implemented port. Port 1 = 01h. Port 2 = 02h.
23:21	00b RO	Reserved
20	1b RO	**Link Active Reporting Capable (LARC)**: Hardwired to 1 to indicate that this port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0b RO	Reserved
18	1 RO	**Clock Power Management (CPM):** Indicates clock power management is supported.
17:15	010b RO	**L1 Exit Latency (EL1)**: Set to 010b to indicate an exit latency of 2 µs to 4 µs.
14:12	100b RO	**L0s Exit Latency (EL0)**: Indicates an exit latency based upon common-clock configuration. 0 = Use MPC.UCEL. 1 = Use MPC.CCEL
11:10	11b R/WO	**Active State Link PM Support (APMS)**: Indicates what level of active state link power management is supported on the root port. 11b = both L0s and L1 entry are supported.
9:4	01h RO	**Maximum Link Width (MLW)**: Single lane only
3:0	1h RO	**Maximum Link Speed (MLS)**. Set to 1h to indicate the link speed is 2.5 GB/s.



11.2.27 LCTL—Link Control Register

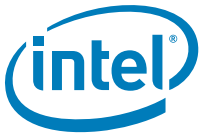
Address Offset: 50h-51h Attribute: R/W, WO, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:9	00h RO	Reserved
8	0 RO	Reserved
7	0 R/W	**Extended Synch (ES)** 0 = Extended synch disabled. 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	0 R/W	**Common Clock Configuration (CCC)** 1 = The Intel® SCH and device are operating with a distributed common reference clock.
5	0 R0/WO	**Retrain Link (RL)**: When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT and LSTS.LTE to check the status of training.
4	0 R/W	**Link Disable (LD)** 0 = Link enabled. 1 = The root port will disable the link.
3	0 RO	**Read Completion Boundary Control (RCBC)**: Indicates the read completion boundary is 64 bytes.
2	0 RO	Reserved
1:0	00b R/W	**Active State Link PM Control (APMC)**: Indicates whether the root port should enter L0s or L1 or both. Bits / Definition: 00b – Disabled 01b – L0s Entry is Enabled 10b – L1 Entry is Enabled 11b – L0s and L1 Entry Enabled

11.2.28 LSTS—Link Status Register

Address Offset: 52h–53h Attribute: RO
Default Value: See bit description Size: 16 bits

Bit	Default and Access	Description
15:14	00b RO	Reserved
13	0 RO	**Data Link Layer Active (DLLA)** 0 = Data Link Control and Management State Machine is not in the DL Active state 1 = Data Link Control and Management State Machine is in the DL Active state
12	1 RO	**Slot Clock Configuration (SCC)** 1 = indicate that the Intel® SCH uses the same reference clock as on the platform and does not generate its own clock.
11	0 RO	**Link Training (LT)**: Not supported. Hardwired to 0.
10	0 RO	**Link Training Error (LTE)**: The root port sets this bit whenever link training is occurring. It clears the bit upon completion of link training.
9:4	00h RO	**Negotiated Link Width (NLW)**: May only take the value of a single link (01h). The value of this register is undefined if the link has not successfully trained.
3:0	1h RO	**Link Speed (LS)**: This field indicates the negotiated Link speed of the given PCI Express link. 01h = Link speed is 2.5 GB/s.



11.2.29 SLCAP—Slot Capabilities Register

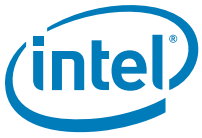
Address Offset: 54h–57h Attribute: R/WO, RO
Default Value: 00000060h Size: 32 bits

Bit	Default and Access	Description
31:19	0000h R/WO	**Physical Slot Number (PSN)**: This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18:17	00b RO	Reserved
16:15	00b R/WO	**Slot Power Limit Scale (SLS)**: Specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:7	00h R/WO	**Slot Power Limit Value (SLV)**: These bits, in conjunction with SLS, specify the upper limit on power supplied by the slot. The two values Together, SLV and SLS indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1 RO	**Hot Plug Capable (HPC)** 1 = Indicates that hot-plug is supported.
5	1 RO	**Hot Plug Surprise (HPS)** 1 = Indicates the device may be removed from the slot without prior notification.
4	0 RO	**Power Indicator Present (PIP)** 0 = Indicates that a power indicator LED is not present for this slot.
3	0 RO	**Attention Indicator Present (AIP)** 0 = Indicates that an attention indicator LED is not present for this slot.
2	0 RO	**MRL Sensor Present (MSP)** 0 = Indicates that an MRL sensor is not supported
1	0 RO	**Power Controller Present (PCP)** 0 = Indicates that a power controller is not supported for this slot.
0	0 RO	**Attention Button Present (ABP)** 0 = Indicates that an attention button is not supported for this slot.

11.2.30 SLCTL—Slot Control Register

Address Offset: 58h–59h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:13	000b RO	Reserved
12	0 R/W	**Link Active Changed Enable (LACE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field (D28:F0/F1:52h:bit 13) is changed.
11	0 RO	Reserved
10	0 RO	**Power Controller Control (PCC)**: This bit has no meaning for module based hot-plug.
9:8	00b R/W	**Power Indicator Control (PIC)**: When read, the current state of the power indicator is returned. When written, the appropriate POWER_INDICATOR_* messages are sent. Defined encodings are: Bits / Definition 00b Reserved 01b On 10b Blink 11b Off
7:6	00b R/W	**Attention Indicator Control (AIC)**: When read, the current state of the attention indicator is returned. When written, the appropriate ATTENTION_INDICATOR_* messages are sent. Defined encodings are the same as the PIC bits above.
5	0 R/W	**Hot Plug Interrupt Enable (HPE)** 0 = Hot plug interrupts based on hot-plug events is disabled. 1 = Enables generation of a hot-plug interrupt on enabled hot-plug events.
4	0 R/W	**Command Completed Interrupt Enable (CCE)** 0 = Hot plug interrupts based on command completions is disabled. 1 = Enables the generation of a hot-plug interrupt when a command is completed by the hot-plug controller.
3	0 R/W	**Presence Detect Changed Enable (PDE)** 0 = Hot plug interrupts based on presence detect logic changes is disabled. 1 = Enables the generation of a hot-plug interrupt or wake message when the presence detect logic changes state.
2	0 R/W	**MRL Sensor Changed Enable (MSE)** 0 = Indicates that an MRL sensor is not supported.
1	0 R/W	**Power Fault Detected Enable (PFE)** 0 = PFE not supported.
0	0 R/W	**Attention Button Pressed Enable (ABE)**: ABE is not supported, but is read/write for ease of implementation and to easily draft off of the PCI-Express specification.



11.2.31 SLSTS—Slot Status Register

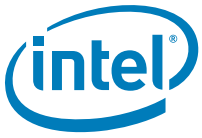
Address Offset: 5Ah–5Bh Attribute: R/WC, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:9	00h	Reserved
8	0 R/WC	**Link Active State Changed (LASC)**: This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register (D28:F0/F1:52h:bit 13) is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
7	0 RO	Reserved
6	See description RO	**Presence Detect State (PDS)**: If XCAP.SI (D28:F0/F1:42h:bit 8) is set (indicating that this root port spawns a slot), then this bit: 0 = Indicates the slot is empty. 1 = Indicates the slot has a device connected. Otherwise, if XCAP.SI is cleared, this bit is always set (1).
5	0 RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
4	0 RO	**Command Completed (CC)**: Hardcoded to 0. These messages are not supported.
3	0 R/WC	**Presence Detect Changed (PDC)** 0 = No change in the PDS bit. 1 = The PDS bit changed states.
2	0 RO	**MRL Sensor Changed (MSC)**: Reserved as the MRL sensor is not implemented.
1	0 RO	**Power Fault Detected (PFD)**: Reserved as a power controller is not implemented.
0	0 RO	**Attention Button Pressed (ABP)**: Hardcoded to 0. Attention button messages are not supported.

11.2.32 RCTL—Root Control Register

Address Offset: 5Ch–5Dh Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:4	000h RO	Reserved
3	0 R/W	**Power Management Event Interrupt Enable (PIE)** 0 = Interrupt generation disabled. 1 = Interrupt generation enabled when PCISTS.IS is in a set state (either due to a 0 to 1 transition, or due to this bit being set with RSTS.IS already set).
2	0 R/W	**System Error on Fatal Error Enable (SFE)** 0 = An SERR# will not be generated.
1	0 R/W	**System Error on Non-Fatal Error Enable (SNE)** 0 = An SERR# will not be generated.
0	0 R/W	**System Error on Correctable Error Enable (SCE)** 0 = An SERR# will not be generated.



11.2.33 RCAP—Root Capabilities

Address Offset: 5Eh Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:1	000h RO	Reserved
0	0b RO	**CRS Software Visibility (CSV):** This bit is not supported by the Intel® SCH. This bit, when set, indicates that the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software.

11.2.34 RSTS—Root Status Register

Address Offset: 60h–63h Attribute: R/WC, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:18	0000h RO	Reserved
17	0 RO	**PME Pending (PP)**: Hardcoded to 0.
16	0 R/WC	**PME Status (PS)** 0 = PME was not asserted. 1 = PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0 RO	**PME Requestor ID (RID)**: Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set.

11.2.35 RCAP—Root Capabilities Register

Address Offset: 5eh Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:1	0000h RO	Reserved
0	0 RO	**Software Visibility of Configuration Retry (SVCR)**: Maintained for compatibility

11.2.36 SV_CAPID—Subsystem Vendor Capability ID Register

Address Offset: 90h Attribute: RO
Default Value: 0Dh Size: 8 bits

Bit	Default and Access	Description
7:0	0Dh RO	**Capability Identifier (CID)**: Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

11.2.37 NXT_PTR3—Next Item Pointer #3 Register

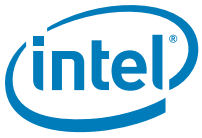
Address Offset: 91h Attribute: RO
Default Value: A0h Size: 8 bits

Bit	Default and Access	Description
7:0	A0h RO	**Next Capability (NEXT):** This field indicates the location of the next capability.

11.2.38 SVID—Subsystem Vendor Identification Register

Address Offset: 94h–97h Attribute: R/WO
Default Value: 0000h Size: 32 bits

Bit	Default and Access	Description
31:16	00h R/WO	**Subsystem Identifier (SID)**: This field indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs.
15:0	00h R/WO	**Subsystem Vendor Identifier (SVID)**: This field indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs.



11.2.39 PCI—Power Management Capability ID Register

Address Offset: A0h Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Default and Access	Description
7:0	01h RO	**Capability Identifier (CID)**: Value of 01h indicates this is a PCI power management capability.

11.2.40 NXT_PTR4—Next Item Pointer #4 Register

Address Offset: A1h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Next Capability (NEXT):** This field indicates this is the last capability in the list.

11.2.41 PM_CAP—Power Management Capabilities Register

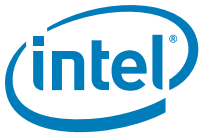
Address Offset: A2h–A3h Attribute: RO
Default Value: C802h Size: 16 bits

Bit	Default and Access	Description
15:11	11001b RO	**PME_Support (PMES)**: This field indicates PME# is supported for states D0, $D3_{HOT}$ and $D3_{COLD}$. The root port does not generate PME#, but reporting that it does is necessary for some legacy operating systems to enable PME# in devices connected behind this root port.
10	0 RO	**D2_Support (D2S)**: The D2 state is not supported.
9	0 RO	**D1_Support (D1S):** The D1 state is not supported.
8:6	000b RO	**Aux_Current (AC)**: Reports 375 mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	0 RO	**Device Specific Initialization (DSI)**: This bit indicates that no device-specific initialization is required.
4	0 RO	Reserved
3	0 RO	**PME Clock (PMEC)**: This bit indicates that PCI clock is not required to generate PME#.
2:0	010b RO	**Version (VS)**: This field indicates support for *Revision 1.1 of the PCI Power Management Specification*.

11.2.42 PM_CNTL_STS—Power Management Control and Status Register

Address Offset: A4h–A7h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:16	00h RO	Reserved
15	0 RO	**PME Status (PMES)**: This bit indicates a PME was received on the downstream link.
14:9	00h RO	Reserved
8	0 R/W	**PME Enable (PMEE)**: This bit indicates PME is enabled. The root port takes no action on this bit, but it must be R/W for some legacy operating systems to enable PME# on devices connected to this root port. This bit is sticky and resides in the resume well. The reset for this bit is RSMRST# which is not asserted during a warm reset.
7:2	00h RO	Reserved
1:0	00b R/W	**Power State (PS)**: This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state **NOTE:** When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into $D3_{HOT}$. If software attempts to write a 10 or 01 to these bits, the write will be ignored.



11.2.43 MPC—Miscellaneous Port Configuration Register

Address Offset: D8h–DBh Attribute: R/W, RO
Default Value: 00110000h Size: 32 bits

Bit	Default and Access	Description
31	0 R/W	**Power Management SCI Enable (PMCE)** 0 = SCI generation based on a power management event is disabled. 1 = Enables the root port to generate SCI whenever a power management event is detected.
30	0 R/W	**Hot Plug SCI Enable (HPCE)** 0 = SCI generation based on a hot-plug event is disabled. 1 = Enables the root port to generate SCI whenever a hot-plug event is detected.
29	0 R/W	**Link Hold Off (LHO):** When set, the port will not take any TLP. This is used during loopback mode to fill up the downstream queue.
28	0 R/W	**Address Translator Enable (ATE):** Used to enable address translation by the AT bits in this register during loopback mode.
27:21	0h RO	Reserved
20:18	100b R/W	**Unique Clock Exit Latency (UCEL)**: L0s Exit Latency when LCAP.CCC is cleared.
17:15	010b R/W	**Common Clock Exit Latency (CCEL)**: L0s Exit Latency LCAP.CCC is set.
14:12	000b R/W	Reserved
11:8	0 R/W	**Address Translator (AT)**: During loopback, these bits are XOR'd with bits [31:28] of the receive address, if the ATE bit in this register is enabled.
7:2	0 RO	Reserved
1	0 R/W	**Hot Plug SMI Enable (HPME)** 0 = SMI generation based on a Hot-Plug event is disabled. 1 = Enables the root port to generate SMI whenever a Hot-Plug event is detected.
0	0 R/W	**Power Management SMI Enable (PMME)** 0 = SMI generation based on a power management event is disabled. 1 = Enables the root port to generate SMI whenever a power management event is detected.

11.2.44 SMSCS—SMI/SCI Status Register

Address Offset: DCh–DFh Attribute: R/WC, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31	0 R/WC	**Power Management SCI Status (PMCS)**: This bit is set if the PME control logic needs to generate an interrupt, and this interrupt has been routed to generate an SCI.
30	0 R/WC	**Hot Plug SCI Status (HPCS)**: This bit is set if the Hot-Plug controller needs to generate an interrupt, and has this interrupt been routed to generate an SCI.
29:5	000000h R/WC	Reserved
4	0 R/WC	**Hot Plug Link Active State Changed SMI Status (HPLAS)**: This bit is set when SLSTS.LASC (D28:F0/F1:5A, bit 8) transitions from 0 to 1, and MPC.HPME (D28:F0/F1:D8h, bit 1) is set. When this bit is set, an SMI# will be generated.
3:2	00b RO	Reserved
1	0 R/WC	**Hot Plug Presence Detect SMI Status (HPPDM)**: This bit is set when SLSTS.PDC (D28:F0/F1:5A, bit 3) transitions from 0 to 1, and MPC.HPME (D28:F0/F1:D8h, bit 1) is set. When this bit is set, an SMI# will be generated.
0	0 R/WC	**Power Management SMI Status (PMMS)**: This bit is set when RSTS.PS (D28:F0/F1:60h, bit 16) transitions from 0 to 1, and MPC.PMME (D28:F0/F1:D8, bit 1) is set.

11.2.45 FD—Function Disable Register

Address Offset: FCh–FFh Attribute: R/W, R0
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:3	0 RO	Reserved
2	0 R/W	**Clock Gating Disable (CGD)** 0 = Clock gating within this function is enabled. 1 = Clock gating within this function is disabled.
1	0 RO	Reserved
0	0 R/W	**Disable (D)** 0 = This function is enabled. 1 = This function is disabled.

§ §

12 UHCI Host Controller (D29:F0, F1, F2)

12.1 Functional Description

The Intel® SCH contains three controllers supporting the Universal Host Controller Interface (UHCI). Each Universal Host Controller (UHC) includes a root hub with two separate USB 1.1 ports, for a total of 6 USB ports.

- Overcurrent detection on all six USB ports is supported. The overcurrent inputs are *not* 5-V tolerant, and can be used as GPIs if not needed.
- The UHCs are arbitrated differently than standard PCI devices to improve arbitration latency.
- The UHCs use the Analog Front End (AFE) embedded cell that allows support for USB full-speed signaling rates, instead of USB I/O buffers.

12.1.1 Bus Protocol

Refer to the *Universal Serial Bus Specification, Revision 1.1*, Chapter 8 for full details on the USB bus protocol.

12.1.2 USB Interrupts

There are two general groups of USB interrupt sources: those resulting from execution of transactions in the schedule, and those resulting from an Intel® SCH operation error. For more information on transaction-based and operational error-based interrupts, refer to chapter 4 of *Universal Host Controller Interface Specification, Revision 1.1.*

When the Intel® SCH drives an interrupt for USB, it internally drives one of the virtual PIRQ# pins as configured by the Interrupt Pin and Interrupt Route registers defined for that device in the Intel® SCH root register complex.

12.1.3 USB Power Management

The UHC can be put into a suspended state and its power can be removed. This requires that certain bits of information be retained in the resume power plane of the Intel® SCH so that a device on a port may wake the system. Such a device may be a fax-modem, which will wake up the machine to receive a fax or take a voice message. The settings of the following bits in I/O space will be maintained when the Intel® SCH enters the S3, S4, or S5 states.

Table 30. Bits Maintained in Low Power States

Register	Offset	Bit	Description
Command	00h	3	Enter Global Suspend Mode (EGSM)
Status	02h	2	Resume Detect
Port Status and Control	10h and 12h	2	Port Enabled/Disabled
		6	Resume Detect
		8	Low-speed Device Attached
		12	Suspend

When the Intel® SCH detects a resume event on any of its ports, it sets the corresponding USB_STS bit in ACPI space. If USB is enabled as a wake/break event, the system wakes up and an SCI generated.

12.1.4 USB Legacy Keyboard Operation

When a USB keyboard is plugged into the system, and a standard keyboard is not, the system may not boot, and MS-DOS legacy software will not run because the keyboard will not be identified. The Intel® SCH implements a series of trapping operations that will snoop accesses that go to the keyboard controller and put the expected data from the USB keyboard into the keyboard controller.

Note: The scheme described below assumes that the keyboard controller (8042 or equivalent) is on the LPC bus.

This legacy operation is performed through SMM space. The latched SMI source (60R, 60W, 64R, 64W) is available in the Status Register. Because the enable is after the latch, it is possible to check for other events that did not necessarily cause an SMI. It is the software's responsibility to logically AND the value with the appropriate enable bits.

Note also that the SMI is generated before the PCI cycle completes (e.g., before H_TRDY# goes active) to ensure that the processor doesn't complete the cycle before the SMI is observed. This method is used on MPIIX and has been validated.

The logic also needs to block the accesses to the 8042 by simply not activating the 8042 CS. This is done by logically ANDing the four enables (60R, 60W, 64R, 64W) with the 4 types of accesses to determine if 8042CS should go active. An additional term is required for the pass-through case.

Figure 4 shows the Enable and Status path. The state table for the diagram is shown in Table 31.

Figure 4. USB Legacy Keyboard Flow Diagram

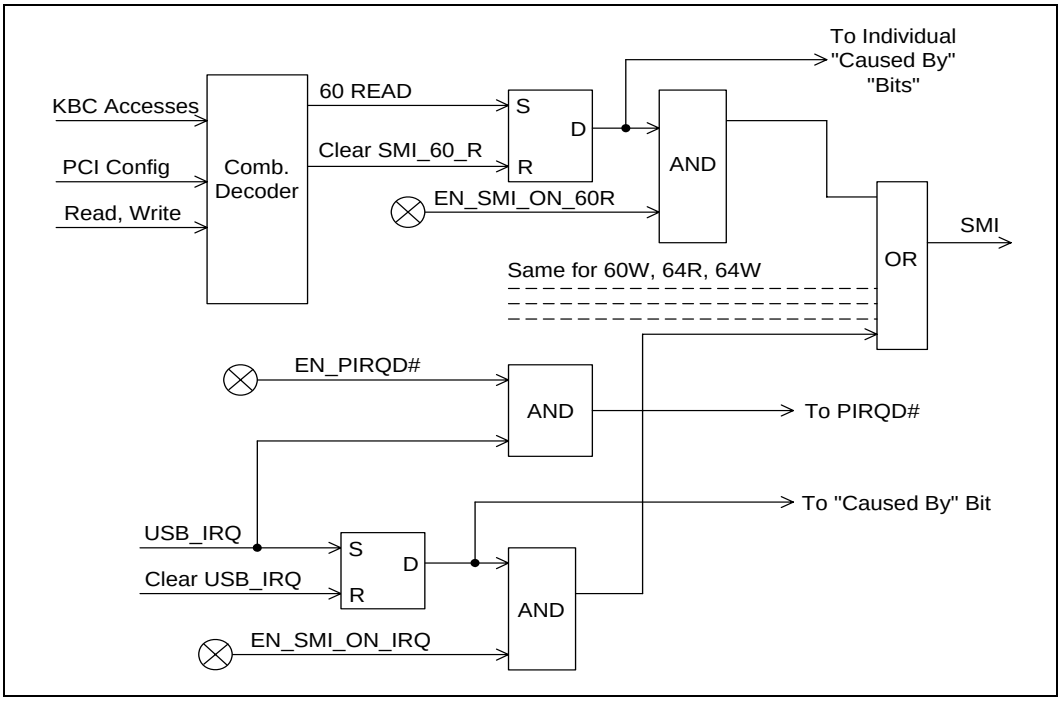
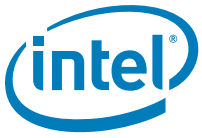


Table 31. USB Legacy Keyboard State Transitions (Sheet 1 of 2)

Current State	Action	Data Value	Next State	Comment
IDLE	64h/Write	D1h	GateState1	Standard D1 command. Cycle passed through to 8042. SMI# doesn't go active. PSTATE (offset C0, bit 6) goes to 1.
IDLE	64h/Write	Not D1h	IDLE	Bit 3 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	64h/Read	N/A	IDLE	Bit 2 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	60h/Write	Don't Care	IDLE	Bit 1 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	60h/Read	N/A	IDLE	Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated.
GateState 1	60h/Write	XXh	GateState2	Cycle passed through to 8042, even if trap enabled in Bit 1 in Config Register. No SMI# generated. PSTATE remains 1. If data value is not DFh or DDh then the 8042 may chose to ignore it.
GateState 1	64h/Write	D1h	GateState1	Cycle passed through to 8042, even if trap enabled by Bit 3 in Config Register. No SMI# generated. PSTATE remains 1. Stay in GateState1 because this is part of the double-trigger sequence.

Table 31. USB Legacy Keyboard State Transitions (Sheet 2 of 2)

Current State	Action	Data Value	Next State	Comment
GateState 1	64h/Write	Not D1h	ILDE	Bit 3 in Config space determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState 1	60h/Read	N/A	IDLE	This is an invalid sequence. Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState 1	64h/Read	N/A	GateState1	Just stay in same state. Generate an SMI# if enabled in Bit 2 of Config Register. PSTATE remains 1.
GateState 2	64/Write	FFh	IDLE	Standard end of sequence. Cycle passed through to 8042. PSTATE goes to 0. Bit 7 in Config Space determines if SMI# should be generated.
GateState 2	64h/Write	Not FFh	IDLE	Improper end of sequence. Bit 3 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState 2	64h/Read	N/A	GateState2	Just stay in same state. Generate an SMI# if enabled in Bit 2 of Config Register. PSTATE remains 1.
GateState 2	60h/Write	See Comment	IDLE	Improper end of sequence. Bit 1 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.
GateState 2	60h/Read	N/A	IDLE	Improper end of sequence. Bit 0 in Config Register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in Config Register is set, then SMI# should be generated.



12.2 PCI Configuration Registers

Table 32. UHCI Controller PCI Register Address Map (D29:F0/F1/F2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0000h	R/WC, RO
08h	RID	Revision Identification	Reserved	RO
09h–0Bh	CC	Class Codes	0C0300h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	See description	RO
20h–23h	BASE	Base Address	00000001h	R/W, RO
2Ch–2Fh	SSID	Subsystem Identifiers	See description	R/WO
34h	CAP_PTR	Capabilities Pointer	00h	RO
3Ch	INT_LN	Interrupt Line	00h	RO
3Dh	INT_PN	Interrupt Pin	See description	RO
60h	USB_RELNUM	Serial Bus Release Number	10h	RO
C4h	USB_RES	USB Resume Enable	00h	R/W, RO
FCh	FD	Function Disable	00000000h	RO. R/W

NOTE: Address locations that are not shown should be treated as Reserved.

12.2.1 VID—Vendor Identification Register

Address Offset: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Default and Access	Description
15:0	8086 RO	**Vendor ID (VID)**: This is a 16-bit value assigned to Intel.

12.2.2 DID—Device Identification Register

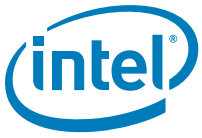
Address Offset: 02h–03h Attribute: RO
Default Value: See bit description Size: 16 bits

Bit	Default and Access	Description
15:0	See description RO	**Device ID (DID)**: This is a 16-bit value assigned to the UHC. UHCI #1 (D29:F0): 8114h UHCI #2 (D29:F1): 8115h UHCI #3 (D29:F2): 8116h

12.2.3 PCICMD—PCI Command Register

Address Offset: 04h–05h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:11	0 RO	Reserved
10	0 R/W	**Interrupt Disable** 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
9:3	00h RO	Reserved
2	0 R/W	**Bus Master Enable (BME)** 0 = Disable 1 = Enable. The Intel® SCH can act as a master on the PCI bus for USB transfers.
1	0 RO	Reserved
0	0 R/W	**I/O Space Enable (IOSE)**: This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the USB I/O registers. The Base Address register for USB should be programmed before this bit is set.



12.2.4 PCISTS—PCI Status Register

Address Offset: 06h–07h Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:4	000h RO	Reserved
3	0 RO	**Interrupt Status**: This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	000b RO	Reserved

12.2.5 RID—Revision Identification Register

Offset Address: 08h Attribute: RO
Default Value: see description Size: 8 bits

Bit	Default and Access	Description
7:0	see description RO	**Revision ID**: Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the value of the Revision ID Register.

12.2.6 CC—Class Code Register

Address Offset: 09h–0Bh Attribute: RO
Default Value: 0C0300h Size: 24 bits

Bit	Default and Access	Description
23:16	0Ch RO	**Base Class Code (BCC)**: 0Ch = Serial Bus controller.
8:15	03h RO	**Sub Class Code (SCC)**: 03h = USB host controller.
7:0	00h RO	**Programming Interface (PI)**: 00h = No specific register level programming interface defined.

12.2.7 MLT—Master Latency Timer Register

Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Master Latency Timer (MLT)**: Hardwired to 00h. The USB controller is implemented internal to the Intel® SCH and not arbitrated as a PCI device.

12.2.8 HEADTYP—Header Type Register

Address Offset: 0Eh Attribute: RO
Default Value: See Bit Description Size: 8 bits

Bit	Default and Access	Description
7	See Desc. RO	**Multi-Function Device** 0 = Single-function device. 1 = Multi-function device. (Default) For UHCI #2 and #3 (D29:F1 and F2 respectively) this register is hardwired to 00h. For UHCI #1 (D29:F0), bit 7 always reports 1.
6:0	00h RO	**Configuration Layout**: Hardwired to 00h, which indicates the standard PCI configuration layout.

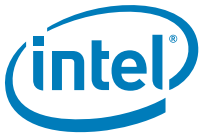
12.2.9 BASE—Base Address Register

Address Offset: 20h–23h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Bit	Default and Access	Description
31:16	0000h RO	Reserved
15:5	000h R/W	**Base Address**: Bits 15:5 correspond to I/O address signals AD[15:5], respectively. This gives 32 bytes of relocatable I/O space.
4:1	000b RO	Reserved
0	1 RO	**Resource Type Indicator (RTE)**: Hardwired to 1 to indicate that the base address field in this register maps to I/O space.

12.2.10 SSID—Subsystem Identifiers Register

This register matches the value written to the LPC bridge.



12.2.11 SID—Subsystem Identification Register

Address Offset: 2Eh–2Fh Attribute: R/WO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:0	R/WO	**Subsystem ID (SID)**: BIOS sets the value in this register to identify the Subsystem ID. The SID register, in combination with the SVID register (D29:F0/F1/F2:2C), enables the operating system to distinguish each subsystem from other(s). The value read in this register is the same as what was written to the LPC's SSID register. **NOTE:** The software can write to this register only once per core well reset. Writes should be done as a single, 16-bit cycle.

12.2.12 CAP_PTR—Capabilities Pointer Register

Address Offset: 34h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Pointer (PTR):** 00h indicates this device has no additional capabilities.

12.2.13 INT_LN—Interrupt Line Register

Address Offset: 3Ch Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Interrupt Line (INT_LN)**: This data is not used by the Intel® SCH. It is to communicate to software the interrupt line that the interrupt pin is connected to.

12.2.14 INT_PN—Interrupt Pin Register

Address Offset: 3Dh Attribute: RO
Default Value: See Description Size: 8 bits

Bit	Default and Access	Description
7:0	See Description RO	**Interrupt Line (INT_LN)**: This value tells the software which interrupt pin each USB host controller uses. The upper 4 bits are hardwired to 0000b; the lower 4 bits are determine by the Interrupt Pin default values that are programmed in the memory-mapped configuration space as follows: UHCI #1 — D29IP.U0P (Chipset Config Registers:Offset 3108h:bits 3:0) UHCI #2 — D29IP.U1P (Chipset Config Registers:Offset 3108h:bits 7:4) UHCI #3 — D29IP.U2P (Chipset Config Registers:Offset 3108h:bits 11:8) **NOTE:** This does not determine the mapping to the PIRQ pins.

12.2.15 USB_RELNUM—Serial Bus Release Number Register

Address Offset: 60h Attribute: RO
Default Value: 10h Size: 8 bits

Bit	Default and Access	Description
7:0	10h RO	**Serial Bus Release Number** 10h = USB controller supports the *USB Specification*, Release 1.0.

12.2.16 USB_RES—USB Resume Enable Register

Address Offset: C4h Attribute: R/W, RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:2	0h RO	Reserved
1	0 R/W	**PORT0EN**: Enable port 0 of the USB controller to respond to wakeup events. 0 = The USB controller will not look at this port for a wakeup event. 1 = The USB controller will monitor this port for remote wakeup and connect/disconnect events.
0	0 R/W	**PORT1EN**: Enable port 1 of the USB controller to respond to wakeup events. 0 = The USB controller will not look at this port for a wakeup event. 1 = The USB controller will monitor this port for remote wakeup and connect/disconnect events.

12.2.17 FD—Function Disable Register

Address Offset: FCh Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:3	0 RO	Reserved
2	0 R/W	**Clock Gating Disable (CGD)** 0 = Clock gating within this function is enabled 1 = Clock gating within this function is disabled
1	0 RO	Reserved
0	0 R/W	**Disable (D)** 0 = This function is enabled 1 = This function is disabled and the configuration space is not accessible.

12.3 I/O Registers

Some of the read/write register bits that deal with changing the state of the USB hub ports function such that on read back they reflect the current state of the port, and not necessarily the state of the last write to the register. This allows the software to poll the state of the port and wait until it is in the proper state before proceeding. A host controller reset, global reset, or port reset will immediately terminate a transfer on the affected ports and disable the port. This affects the USBCMD register, bit 4 and the PORT[7:0]SC registers, bits [12,6,2]. See individual bit descriptions for more detail.

Table 33. USB I/O Registers

Offset[1]	Mnemonic	Register Name	Default	Type[2]
00h–01h	USBCMD	USB Command	0000h	R/W, RO
02h–03h	USBSTS	USB Status	0020h	R/WC
04h–05h	USBINTR	USB Interrupt Enable	0000h	R/W
06h–07h	FRNUM	Frame Number	0000h	R/W (see **Note**)
08h–0Bh	FRBASEADD	Frame List Base Address	Undefined	R/W
0Ch	SOFMOD	Start of Frame Modify	40h	R/W
10h–11h	PORTSC0	Port 0 Status/Control	0080h	R/WC, RO, R/W (see **Note**)
12h–13h	PORTSC1	Port 1 Status/Control	0080h	R/WC, RO, R/W (see **Note**)

NOTES:
1. Register offsets are with respect to BASE.
2. Registers that are writable are WORD writable only. Byte writes to these registers.

12.3.1 USBCMD—USB Command Register

I/O Offset:	BASE + (00h–01h)	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

The USB Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed. The table following the bit description provides additional information on the operation of the Run/Stop and Debug bits.

Bit	Default and Access	Description
15:7	00h RO	Reserved
8	0 R/W	**Loop Back Test Mode:** 0 = Disable loop back test mode. 1 = The Intel® SCH is in loop back test mode. When both ports are connected together, a write to one port will be seen on the other port and the data will be stored in I/O offset 18h.
7	0 R/W	**Max Packet (MAXP)**: This bit selects the maximum packet size that can be used for full speed bandwidth reclamation at the end of a frame. This value is used by the host controller to determine whether it should initiate another transaction based on the time remaining in the SOF counter. Use of reclamation packets larger than the programmed size will cause a Babble error if executed during the critical window at frame end. The Babble error results in the offending endpoint being stalled. Software is responsible for ensuring that any packet which could be executed under bandwidth reclamation be within this size limit. 0 = 32 bytes 1 = 64 bytes
6	0 R/W	**Configure Flag (CF)**: This bit has no effect on the hardware. It is provided only as a semaphore service for software. 0 = Indicates that software has not completed host controller configuration. 1 = HCD software sets this bit as the last action in the process of configuring the host controller.
5	0 R/W	**Software Debug (SWDBG)**: The SWDBG bit must only be manipulated when the controller is in the stopped state. This can be determined by checking the HCHalted bit in the USBSTS register. 0 = Normal Mode. 1 = Debug mode. In SW Debug mode, the host controller clears the Run/Stop bit after the completion of each USB transaction. The next transaction is executed when software sets the Run/Stop bit back to 1.
4	0 R/W	**Force Global Resume (FGR)**: 0 = Software resets this bit to 0 after 20 ms has elapsed to stop sending the Global Resume signal. At that time all USB devices should be ready for bus activity. The 1 to 0 transition causes the port to send a low speed EOP signal. This bit will remain a 1 until the EOP has completed. 1 = Host controller sends the Global Resume signal on the USB, and sets this bit to 1 when a resume event (connect, disconnect, or K-state) is detected while in global suspend mode.

Bit	Default and Access	Description
3	0 R/W	**Enter Global Suspend Mode (EGSM)** 0 = Software resets this bit to 0 to come out of Global Suspend mode. Software writes this bit to 0 at the same time that Force Global Resume (bit 4) is written to 0 or after writing bit 4 to 0. 1 = Host controller enters the Global Suspend mode. No USB transactions occur during this time. The Host controller is able to receive resume signals from USB and interrupt the system. Software must ensure that the Run/Stop bit (bit 0) is cleared prior to setting this bit.
2	0 R/W	**Global Reset (GRESET)** 0 = This bit is reset by the software after a minimum of 10 ms has elapsed as specified in Chapter 7 of the USB Specification. 1 = Global Reset. The host controller sends the global reset signal on the USB and then resets all of its logic, including the internal hub registers. The hub registers are reset to their power on state. Chip Hardware Reset has the same effect as Global Reset (bit 2), except that the host controller does not send the Global Reset on USB.
1	0 R/W	**Host Controller Reset (HCRESET)**: The effects of HCRESET on Hub registers are slightly different from Chip Hardware Reset and Global USB Reset. The HCRESET affects bits [8,3:0] of the Port Status and Control Register (PORTSC) of each port. HCRESET resets the state machines of the host controller including the Connect/Disconnect state machine (one for each port). When the Connect/Disconnect state machine is reset, the output that signals connect/disconnect are negated to 0, effectively signaling a disconnect, even if a device is attached to the port. This virtual disconnect causes the port to be disabled. This disconnect and disabling of the port causes bit 1 (connect status change) and bit 3 (port enable/disable change) of the PORTSC to get set. The disconnect also causes bit 8 of PORTSC to reset. About 64 bit times after HCRESET goes to 0, the connect and low-speed detect will take place, and bits 0 and 8 of the PORTSC will change accordingly. 0 = Reset by the host controller when the reset process is complete. 1 = Reset. When this bit is set, the host controller module resets its internal timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated.
0	0 R/W	**Run/Stop (RS)**: When set to 1, the Intel® SCH proceeds with execution of the schedule. The Intel® SCH continues execution as long as this bit is set. When this bit is cleared, the Intel® SCH completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The host controller clears this bit when the following fatal errors occur: consistency check failure, PCI Bus errors. 0 = Stop 1 = Run **NOTE:** This bit should only be cleared if there are no active Transaction Descriptors in the executable schedule or software will reset the host controller prior to setting this bit again.

Table 34. Run/Stop, Debug Bit Interaction SWDBG (Bit 5), Run/Stop (Bit 0) Operation

SWDBG (Bit 5)	Run/Stop (Bit 0)	Description
0	0	If executing a command, the host controller completes the command and then stops. The 1.0 ms frame counter is reset and command list execution resumes from start of frame using the frame list pointer selected by the current value in the FRNUM register. (While Run/Stop=0, the FRNUM register (BASE + 06h) can be reprogrammed).
0	1	Execution of the command list resumes from Start Of Frame using the frame list pointer selected by the current value in the FRNUM register. The host controller remains running until the Run/Stop bit is cleared (by software or hardware).
1	0	If executing a command, the host controller completes the command and then stops and the 1.0 ms frame counter is frozen at its current value. All status are preserved. The host controller begins execution of the command list from where it left off when the Run/Stop bit is set.
1	1	Execution of the command list resumes from where the previous execution stopped. The Run/Stop bit is set to 0 by the host controller when a TD is being fetched. This causes the host controller to stop again after the execution of the TD (single step). When the host controller has completed execution, the HC Halted bit in the Status Register is set.

When the USB host controller is in Software Debug Mode (USBCMD Register bit 5=1), the single stepping software debug operation is as follows:

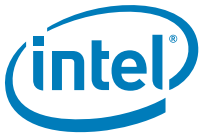
To Enter Software Debug Mode:

1. HCD puts host controller in Stop state by setting the Run/Stop bit to 0.
2. HCD puts host controller in Debug Mode by setting the SWDBG bit to 1.
3. HCD sets up the correct command list and Start Of Frame value for starting point in the Frame List Single Step Loop.
4. HCD sets Run/Stop bit to 1.
5. Host controller executes next active TD, sets Run/Stop bit to 0, and stops.
6. HCD reads the USBCMD register to check if the single step execution is completed (HCHalted=1).
7. HCD checks results of TD execution. Go to step 4 to execute next TD or step 8 to end Software Debug mode.
8. HCD ends Software Debug mode by setting SWDBG bit to 0.
9. HCD sets up normal command list and Frame List table.
10. HCD sets Run/Stop bit to 1 to resume normal schedule execution.

In Software Debug mode, when the Run/Stop bit is set, the host controller starts. When a valid TD is found, the Run/Stop bit is reset. When the TD is finished, the HCHalted bit in the USBSTS register (bit 5) is set.

The SW Debug mode skips over inactive TDs and only halts after an active TD has been executed. When the last active TD in a frame has been executed, the host controller waits until the next SOF is sent and then fetches the first TD of the next frame before halting.

This HCHalted bit can also be used outside of Software Debug mode to indicate when the host controller has detected the Run/Stop bit and has completed the current transaction. Outside of the Software Debug mode, setting the Run/Stop bit to 0 always resets the SOF counter so that when the Run/Stop bit is set the host controller starts over again from the frame list location pointed to by the Frame List Index (see FRNUM Register description) rather than continuing where it stopped.



12.3.2 USBSTS—USB Status Register

I/O Offset: BASE + (02h–03h) Attribute: R/WC, RO
Default Value: 0020h Size: 16 bits

This register indicates pending interrupts and various states of the host controller. The status resulting from a transaction on the serial bus is not indicated in this register.

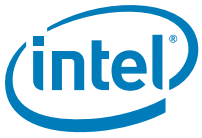
Bit	Default and Access	Description
15:6	00h RO	Reserved
5	1 R/W	**HCHalted** 0 = Software clears this bit by writing a 1 to it. 1 = The host controller has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the host controller hardware (debug mode or an internal error). Default.
4	0 R/WC	**Host Controller Process Error** 0 = Software clears this bit by writing a 1 to it. 1 = The host controller has detected a fatal error. This indicates that the host controller suffered a consistency check failure while processing a Transfer Descriptor. An example of a consistency check failure would be finding an invalid PID field while processing the packet header portion of the TD. When this error occurs, the host controller clears the Run/Stop bit in the Command register (D29:F0/F1/F2:BASE + 00h, bit 0) to prevent further schedule execution. A hardware interrupt is generated to the system.
3	0 R/WC	**Host System Error** 0 = Software clears this bit by writing a 1 to it. 1 = A serious error occurred during a host system access involving the host controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the host controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system.
2	0 R/WC	**Resume Detect (RSM_DET)** 0 = Software clears this bit by writing a 1 to it. 1 = The host controller received a “RESUME” signal from a USB device. This is only valid if the Host controller is in a global suspend state (Command register, D29:F0/F1/F2:BASE + 00h, bit 3 = 1).
1	0 R/WC	**USB Error Interrupt** 0 = Software clears this bit by writing a 1 to it. 1 = Completion of a USB transaction resulted in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit (D29:F0/F1/F2:BASE + 04h, bit 2) set, both this bit and Bit 0 are set.
0	0 R/WC	**USB Interrupt (USBINT)** 0 = Software clears this bit by writing a 1 to it. 1 = The host controller sets this bit when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. Also set when a short packet is detected (actual length field in TD is less than maximum length field in TD), and short packet detection is enabled in that TD.

12.3.3 USBINTR—USB Interrupt Enable Register

I/O Offset:	BASE + (04h–05h)	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Fatal errors (host controller processor error, (D29:F0/F1/F2:BASE + 02h, bit 4, USBSTS Register) cannot be disabled by the host controller. Interrupt sources that are disabled in this register still appear in the Status Register to allow the software to poll for events.

Bit	Default and Access	Description
15:5	0000h RO	Reserved
4	0 R/W	**Scratchpad (SP)**
3	0 R/W	**Short Packet Interrupt Enable** 0 = Disabled 1 = Enabled
2	0 R/W	**Interrupt on Complete Enable (IOC)** 0 = Disabled 1 = Enabled
1	0 R/W	**Resume Interrupt Enable** 0 = Disabled 1 = Enabled
0	0 R/W	**Timeout/CRC Interrupt Enable** 0 = Disabled 1 = Enabled



12.3.4 FRNUM—Frame Number Register

I/O Offset:	BASE + (06–07h)	Attribute:	R/W (Writes must be Word writes)
Default Value:	0000h	Size:	16 bits

Bits [10:0] of this register contain the current frame number that is included in the frame SOF packet. This register reflects the count value of the internal frame number counter. Bits [9:0] are used to select a particular entry in the Frame List during scheduled execution. This register is updated at the end of each frame time.

This register must be written as a word. Byte writes are not supported. This register cannot be written unless the host controller is in the STOPPED state as indicated by the HCHalted bit (D29:F0/F1/F2:BASE + 02h, bit 5). A write to this register while the Run/Stop bit is set (D29:F0/F1/F2:BASE + 00h, bit 0) is ignored.

Bit	Default and Access	Description
15:11	00h RO	Reserved
10:0	000h R/W	**Frame List Current Index/Frame Number**: This field provides the frame number in the SOF Frame. The value in this register increments at the end of each time frame (approximately every 1 ms). In addition, bits 9:0 are used for the Frame List current index and correspond to memory address signals 11:2.

12.3.5 FRBASEADD—Frame List Base Address Register

I/O Offset:	BASE + (08h–0Bh)	Attribute:	R/W
Default Value:	Undefined	Size:	32 bits

This 32-bit register contains the beginning address of the Frame List in the system memory. HCD loads this register prior to starting the schedule execution by the host controller. When written, only the upper 20 bits are used. The lower 12 bits are written as 0s (4 KB alignment). The contents of this register are combined with the frame number counter to enable the host controller to step through the Frame List in sequence. The two least significant bits are always 00. This requires dword-alignment for all list entries. This configuration supports 1024 Frame List entries.

Bit	Default and Access	Description
31:12	R/W	**Base Address**: These bits correspond to memory address signals 31:12, respectively.
11:0	000h RO	Reserved

12.3.6 SOFMOD—Start of Frame Modify Register

I/O Offset:	Base + (0Ch)	Attribute:	R/W
Default Value:	40h	Size:	8 bits

This register is used to modify the value used in the generation of SOF timing on the USB. When a new value is written to bits 7:0, the SOF timing of the next frame will be adjusted. This feature can be used to adjust out any offset from the clock source that generates the clock that drives the SOF counter. This register can also be used to maintain real time synchronization with the rest of the system so that all devices have the same sense of real time. Using this register, the frame length can be adjusted across the full range required by the USB specification. The initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. It may be reprogrammed by USB system software at any time. The value will take effect from the beginning of the next frame. This register is reset upon a host controller reset or global reset. Software must maintain a copy of the value for reprogramming if necessary.

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>7</td><td>0, RO</td><td>Reserved</td></tr>
<tr><td>6:0</td><td>40h
R/W</td><td>SOF Timing Value: Guidelines for the modification of frame time are contained in Chapter 7 of the USB Specification. The SOF cycle time (number of SOF counter clock periods to generate a SOF frame length) is equal to 11936 + value in this field. The default value is decimal 64 which gives a SOF cycle time of 12000. For a 12-MHz SOF counter clock input, this produces a 1-ms Frame period. The following table indicates what SOF Timing Value to program into this field for a certain frame period.
<table>
<tr><th>Frame Length (# 12 MHz Clocks) (decimal)</th><th>SOF Timing Value (this register) (decimal)</th></tr>
<tr><td>11936</td><td>0</td></tr>
<tr><td>11937</td><td>1</td></tr>
<tr><td>—</td><td>—</td></tr>
<tr><td>11999</td><td>63</td></tr>
<tr><td>12000</td><td>64</td></tr>
<tr><td>—</td><td>—</td></tr>
<tr><td>12063</td><td>127</td></tr>
</table>
</td></tr>
</table>

12.3.7 PORTSC[0,1]—Port Status and Control Registers

I/O Offset: Port 0,2,4: BASE + (10h–11h)
Port 1,3,5: BASE + (12h–13h)
Attribute: R/WC, RO, R/W (Word writes only)
Default Value: 0080h
Size: 16 bits

After a power-up reset, global reset, or host controller reset, the initial conditions of a port are: no device connected, Port disabled, and the bus line status is 00 (single-ended 0).

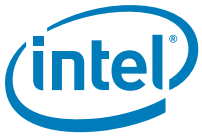
Port Reset and Enable Sequence

When software wishes to reset a USB device it will assert the Port Reset bit in the Port Status and Control register. The minimum reset signaling time is 10 ms and is enforced by software. To complete the reset sequence, software clears the port reset bit. The UHCI controller must re-detect the port connect after reset signaling is complete before the controller will allow the port enable bit to reset. This time is approximately 5.3 µs. Software has several possible options to meet the timing requirement and a partial list is enumerated below:

- Iterate a short wait, setting the port enable bit and reading it back to see if the enable bit is set.
- Poll the connect status bit and wait for the hardware to recognize the connect prior to enabling the port.
- Wait longer than the hardware detect time after clearing the port reset and prior to enabling the port.

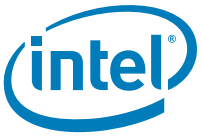
Bit	Default and Access	Description
15:13	0 RO	Reserved
12	0 R/W	**Suspend (SUS)**: This bit should not be written to a 1 if global suspend is active (bit 3=1 in the USBCMD register). Bit 2 and bit 12 of this register define the hub states as follows: Bits [12,2] / Hub State: X,0 — Disable 0, 1 — Enable 1, 1 — Suspend When in suspend state, downstream propagation of data is blocked on this port, except for single-ended 0 resets (global reset and port reset). The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. 1 = Port in suspend state. 0 = Port not in suspend state **NOTE:** Normally, if a transaction is in progress when this bit is set, the port will be suspended when the current transaction completes.
11	0 R/WC	**Overcurrent Indicator**: Set by hardware. Software clears this bit by writing a 1. 0 = No inactive to active transition has occurred 1 = Overcurrent pin has gone from inactive to active on this port

Bit	Default and Access	Description
10	0 RO	**Overcurrent Active**: This bit is set and cleared by hardware. 0 = Indicates that the overcurrent pin is inactive (high) 1 = Indicates that the overcurrent pin is active (low)
9	0 R/W	**Port Reset (PR)** 0 = Port is not in Reset 1 = Port is in Reset. When set, the port is disabled and sends the USB Reset signaling.
8	0 RO	**Low Speed Device Attached (LS)** 0 = Full speed device is attached 1 = Low speed device is attached to this port
7	1 RO	Reserved. Hardwired to 1
6	0 R/W	**Resume Detect (RSM_DET)**: Software sets this bit to a 1 to drive resume signaling. The host controller sets this bit to a 1 if a J-to-K transition is detected for at least 32 microseconds while the port is in the Suspend state. The Intel® SCH will then reflect the K-state back onto the bus as long as the bit remains a 1, and the port is still in the suspend state (bit 12,2 are 11). Writing a 0 (from 1) causes the port to send a low speed EOP. This bit will remain a 1 until the EOP has completed. 0 = No resume (K-state) detected/driven on port. 1 = Resume detected/driven on port.
5:4	0 RO	**Line Status**: These bits reflect the D+ (bit 4) and D– (bit 5) signals lines' logical levels. These bits are used for fault detect and recovery as well as for USB diagnostics. This field is updated at EOF2 time (See Chapter 11 of the USB Specification).
3	0 R/WC	**Port Enable/Disable Change**: For the root hub, this bit gets set only when a port is disabled due to disconnect on that port or due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification). 0 = No change. Software clears this bit by writing a 1 to the bit location. 1 = Port enabled/disabled status has changed.
2	0 R/W	**Port Enabled/Disabled (PORT_EN)**: Ports can be enabled by host software only. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes and that there may be a delay in disabling or enabling a port if there is a transaction currently in progress on the USB. 0 = Disable 1 = Enable



Bit	Default and Access	Description
1	0 R/WC	**Connect Status Change**: This bit indicates that a change has occurred in the port's Current Connect Status (see bit 0). The hub device sets this bit for any changes to the port device connect status, even if system software has not cleared a connect status change. If, for example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be setting" an already-set bit (i.e., the bit will remain set). However, the hub transfers the change bit only once when the host controller requests a data transfer to the Status Change endpoint. System software is responsible for determining state change history in such a case. 0 = No change. Software clears this bit by writing a 1 to it. 1 = Change in Current Connect Status.
0	0 RO	**Current Connect Status**: This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. 1 = Device is present on port.

§ §



13 EHCI Host Controller (D29:F7)

13.1 Functional Description

The Intel® SCH contains an Enhanced Host Controller Interface (EHCI), which supports up to eight USB 2.0 high-speed root ports. USB 2.0 allows data transfers up to 480 MB/s. Ports 0-5 of the EHCI share the same pins as the six USB full-speed/low-speed ports detailed in Chapter 12. The two other high-speed ports, Ports 6 and 7, only support USB 2.0. The Intel® SCH contains port-routing logic that determines whether a USB port is controlled by one of the three UHCI controllers or by the EHCI controller. A USB 2.0-based debug port is also implemented in Intel® SCH and is documented in this chapter.

A summary of the key architectural differences between the UHCI and EHCI host controllers are shown in Table 35.

Table 35. UHCI vs. EHCI

Parameter	USB UHCI	USB EHCI
Accessible by	I/O space	Memory Space
Memory Data Structure	Single linked list	Separated into periodic and asynchronous lists
Differential Signaling Voltage	3.3 V	400 mV
Ports per Controller	2	8

13.1.1 EHCI Initialization

The expected initialization sequence of the EHCI begins with a complete power cycle during which the suspend well and core well have been off. After core power wells have been powered up and stabilized, the BIOS performs a number of platform customization steps to configure the Intel® SCH and its attached devices. This makes the system ready for the first operating system drivers to be loaded and initialized. (See Chapter 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 for more information on USB driver initialization.)

In addition to the standard Intel® SCH hardware resets, portions of the EHCI are reset by the HCRESET bit and the transition from the $D3_{HOT}$ device power management state to the D0 state. The effects of each of these resets are as follows:

Reset	Does Reset	Does not Reset	Comments
HCRESET bit set.	Memory space registers except Structural Parameters (which is written by BIOS).	Configuration registers.	The HCRESET must only effect registers that the EHCI driver controls. PCI Configuration space and BIOS-programmed parameters cannot be reset.
Software writes the Device Power State from $D3_{HOT}$ (11b) to D0 (00b).	Core well registers (except BIOS-programmed registers).	Suspend well registers; BIOS-programmed core well registers.	The D3-to-D0 transition must not cause wake information (suspend well) to be lost. It also must not clear BIOS-programmed registers because BIOS may not be invoked following the D3-to-D0 transition.

Any exceptions mentioned in the detailed register descriptions supersede the rules given above. This summary is provided to help explain the reasons for the reset policies.

13.1.2 USB 2.0 Interrupts and Error Conditions

Section 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 goes into detail on the EHCI interrupts and the error conditions that cause them. All error conditions that the EHCI detects can be reported through the EHCI Interrupt status bits. Only Intel® SCH-specific interrupt and error-reporting behavior is documented in this section. The EHCI Interrupts Section must be read first, followed by this section to fully comprehend the EHCI interrupt and error-reporting functionality.

- Based on the EHCI's Buffer sizes and buffer management policies, the Data Buffer Error can never occur on the Intel® SCH.
- Master Abort and Target Abort responses from hub interface on EHCI-initiated read packets will be treated as Fatal Host Errors. The EHCI halts when these conditions are encountered.
- The Intel® SCH may assert the interrupts which are based on the interrupt threshold as soon as the status for the last complete transaction in the interrupt interval has been posted in the internal write buffers. The requirement in the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0.
- Since the Intel® SCH supports the 1024-element Frame List size, the Frame List Rollover interrupt occurs every 1024 milliseconds.
- The Intel® SCH delivers interrupts using PIRQH#.
- The Intel® SCH does not modify the CERR count on an Interrupt IN when the "Do Complete-Split" execution criteria are not met.
- For complete-split transactions in the Periodic list, the "Missed Microframe" bit does not get set on a control-structure-fetch that fails the late-start test. If subsequent accesses to that control structure do not fail the late-start test, then the "Missed Microframe" bit will get set and written back.

13.1.2.1 Aborts on USB 2.0—Initiated Memory Reads

If a read initiated by the EHCI is aborted, the EHCI treats it as a fatal host error. The following actions are taken when this occurs:

- The Host System Error status bit is set
- The DMA engines are halted after completing up to one more transaction on the USB interface
- If enabled (by the Host System Error Enable), then an interrupt is generated
- If the status is Master Abort, then the Received Master Abort bit in configuration space is set
- If the status is Target Abort, then the Received Target Abort bit in configuration space is set
- If enabled (by the SERR Enable bit in the function's configuration space), then the Signaled System Error bit in configuration bit is set.

13.1.3 USB 2.0 Power Management

13.1.3.1 Pause Feature

This feature allows platforms (especially mobile systems) to dynamically enter low-power states during brief periods when the system is idle (i.e., between keystrokes). This is useful for enabling power management features like Enhanced Intel SpeedStep® Technology in the Intel® SCH. The policies for entering these states typically are based on the recent history of system bus activity to incrementally enter deeper power management states. Normally, when the EHCI is enabled, it regularly accesses main memory while traversing the DMA schedules looking for work to do; this activity is viewed by the power management software as a non-idle system, thus preventing the power managed states to be entered.

Suspending all of the enabled ports can prevent the memory accesses from occurring, but there is an inherent latency overhead with entering and exiting the suspended state on the USB ports that makes this unacceptable for the purpose of dynamic power management. As a result, the EHCI software drivers are allowed to pause the EHCI's DMA engines when it knows that the traffic patterns of the attached devices can afford the delay. The pause only prevents the EHCI from generating memory accesses; the SOF packets continue to be generated on the USB ports (unlike the suspended state).

13.1.3.2 Suspend Feature

The *Enhanced Host Controller Interface (EHCI) For Universal Serial Bus Specification*, Section 4.3 describes the details of Port Suspend and Resume.

13.1.3.3 ACPI Device States

The USB 2.0 function only supports the D0 and D3 PCI Power Management states. Notes regarding the Intel® SCH implementation of the Device States:

1. The EHCI hardware does not inherently consume any more power when it is in the D0 state than it does in the D3 state. However, software is required to suspend or disable all ports prior to entering the D3 state such that the maximum power consumption is reduced.
2. In the D0 state, all implemented EHCI features are enabled.
3. In the D3 state, accesses to the EHCI memory-mapped I/O range will master abort.
   NOTE: Since the Debug Port uses the same memory range, the Debug Port is only operational when the EHCI is in the D0 state.
4. In the D3 state, the EHCI interrupt must never assert for any reason. The internal PME# signal is used to signal wake events, etc.
5. When the Device Power State field is written to D0 from D3, an internal reset is generated. See section EHCI Resets for general rules on the effects of this reset.
6. Attempts to write any other value into the Device Power State field other than 00b (D0 state) and 11b (D3 state) will complete normally without changing the current value in this field.

13.1.3.4 ACPI System States

The EHCI behavior as it relates to other power management states in the system is summarized in the following list:

- The System is always in the S0 state when the EHCI is in the D0 state. However, when the EHCI is in the D3 state, the system may be in any power management state (including S0).
- When in D0, the Pause feature (See Section 13.1.3.1) enables dynamic processor low-power states to be entered.
- The PLL in the EHCI is disabled when entering the S3/S4/S5 states (core power turns off).
- All core well logic is reset in the S3/S4/S5 states.

13.1.3.5 Activity During C-States

The USB2 host controller can operating while the processor is in low C-states, causing pop-up to C2.

13.1.3.6 Mobile Considerations

The Intel® SCH USB 2.0 implementation does not behave differently in the mobile configurations versus the desktop configurations. However, some features may be especially useful for the mobile configurations.

- If a system (e.g., mobile) does not implement all ten USB 2.0 ports, the Intel® SCH provides mechanisms for changing the structural parameters of the EHCI and hiding unused UHCI controllers.
- Mobile systems may want to minimize the conditions that will wake the system. The Intel® SCH implements the “Wake Enable” bits in the Port Status and Control registers, as specified in the EHCI spec, for this purpose.
- Mobile systems may want to cut suspend well power to some or all USB ports when in a low-power state. The Intel® SCH implements the optional Port Wake Capability Register in the EHCI Configuration Space for this platform-specific information to be communicated to software.

13.1.4 Interaction with UHCI Host Controllers

The Enhanced Host controller shares its ports with UHCI Host controllers in the Intel® SCH. The UHC at D29:F0 shares Ports 0 and 1; the UHC at D29:F1 shares Ports 2 and 3; the UHC at D29:F2 shares Ports 4 and 5.

There is very little interaction between the Enhanced and the UHCI controllers other than the multiplexing control which is provided as part of the EHCI. Figure 5 shows the USB Port Connections at a conceptual level.

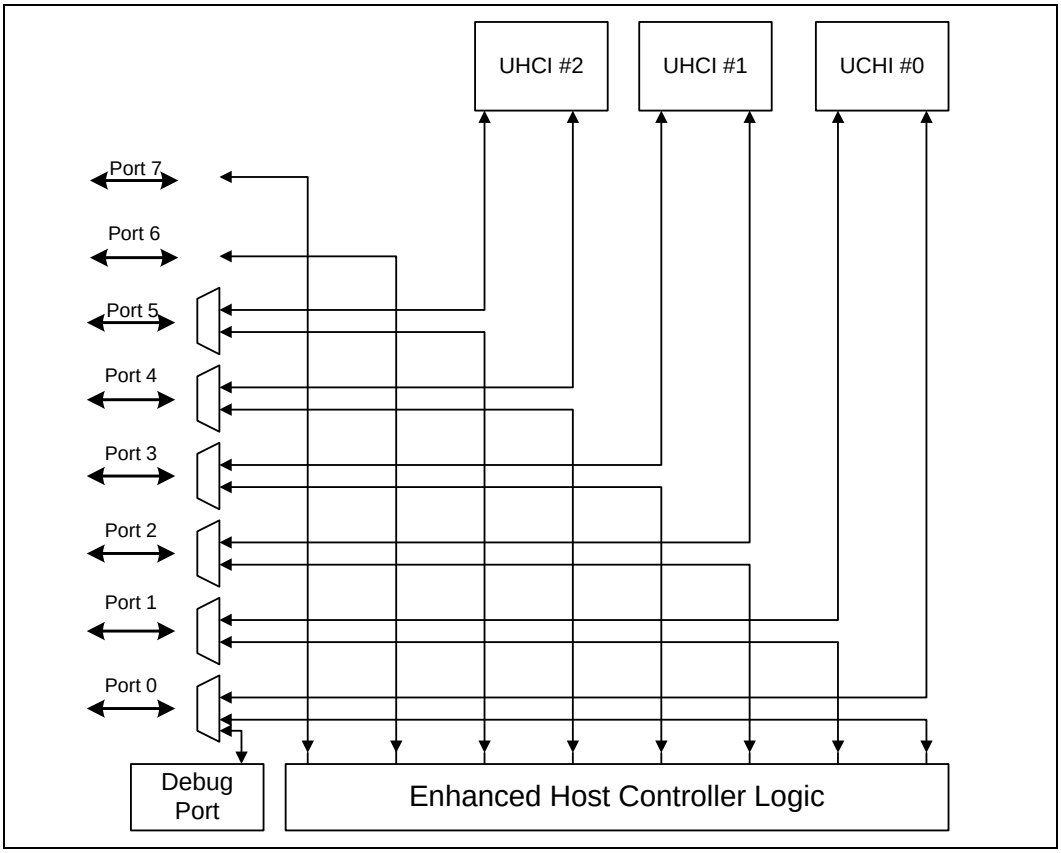
Note: Ports 6 and 7 are not multiplexed onto a UHCI controller, so they are only capable of high-speed operation. This means they can only be used for internal device attachment as USB 2.0 spec requires that external ports be backward compatible with USB 1.1 devices.

13.1.4.1 Port-Routing Logic

Integrated into the EHCI functionality is port-routing logic, which performs the multiplexing between the UHCI and EHCI host controllers. The Intel® SCH conceptually implements this logic as described in Section 4.2 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0. If a device is connected that is not capable of USB 2.0’s high-speed signaling protocol or if the EHCI software

drivers are not present as indicated by the Configured Flag, then the UHCI controller owns the port. Owning the port means that the differential output is driven by the owner and the input stream is only visible to the owner. The host controller that is not the owner of the port internally sees a disconnected port.

Figure 5. Intel® SCH USB Port Connections



Note: The port-routing logic is the only block of logic within the Intel® SCH that observes the physical (real) connect/disconnect information. The port status logic inside each of the host controllers observes the electrical connect/disconnect information that is generated by the port-routing logic.

Only the differential signal pairs are multiplexed/de-multiplexed between the **UHCI and EHCI** host controllers. The other USB functional signals are handled as follows:

- The Overcurrent inputs (OC[7:0]#) are directly routed to both controllers. An overcurrent event is recorded in both controllers' status registers.

The Port-Routing logic is implemented in the Suspend power well so that re-enumeration and re-mapping of the USB ports is not required following entering and exiting a system sleep state in which the core power is turned off.

The Intel® SCH also allows the USB Debug Port traffic to be routed in and out of Port 0. When in this mode, the Enhanced Host controller is the owner of Port 0.

13.1.4.2 Device Connects

The *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 describes the details of handling Device Connects in Section 4.2. There are four general scenarios that are summarized below.

1. Configure Flag = 0 and a full-speed/low-speed-only Device is connected
   - In this case, the UHC is the owner of the port both before and after the connect occurs. The EHCI (except for the port-routing logic) never sees the connect occur. The UHCI driver handles the connection and initialization process.
2. Configure Flag = 0 and a high-speed-capable Device is connected
   - In this case, the UHC is the owner of the port both before and after the connect occurs. The EHCI (except for the port-routing logic) never sees the connect occur. The UHCI driver handles the connection and initialization process. Since the UHC does not perform the high-speed chirp handshake, the device operates in compatible mode.
3. Configure Flag = 1 and a full-speed/low-speed-only Device is connected
   - In this case, the EHCI is the owner of the port before the connect occurs. The EHCI driver handles the connection and performs the port reset. After the reset process completes, the EHCI hardware has cleared (not set) the Port Enable bit in the EHC's PORTSC register. The EHCI driver then writes a 1 to the Port Owner bit in the same register, causing the UHC to see a connect event and the EHCI to see an "electrical" disconnect event. The UHCI driver and hardware handle the connection and initialization process from that point on. The EHCI driver and hardware handle the perceived disconnect.
4. Configure Flag = 1 and a high-speed-capable Device is connected
   - In this case, the EHCI is the owner of the port before, and remains the owner after, the connect occurs. The EHCI driver handles the connection and performs the port reset. After the reset process completes, the EHCI hardware has set the Port Enable bit in the EHC's PORTSC register. The port is functional at this point. The UHC continues to see an unconnected port.

13.1.4.3 Device Disconnects

The *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0 describes the details of handling Device Connects in Section 4.2. There are three general scenarios that are summarized below.

1. Configure Flag = 0 and the device is disconnected
   - In this case, the UHC is the owner of the port both before and after the disconnect occurs. The EHCI (except for the port-routing logic) never sees a device attached. The UHCI driver handles disconnection process.
2. Configure Flag = 1 and a full-speed/low-speed-capable Device is disconnected
   - In this case, the UHC is the owner of the port before the disconnect occurs. The disconnect is reported by the UHC and serviced by the associated UHCI driver. The port-routing logic in the EHCI cluster forces the Port Owner bit to 0, indicating that the EHCI owns the unconnected port.
3. Configure Flag = 1 and a high-speed-capable Device is disconnected
   - In this case, the EHCI is the owner of the port before, and remains the owner after, the disconnect occurs. The EHCI hardware and driver handle the disconnection process. The UHC never sees a device attached.

13.1.4.4 Effect of Resets on Port-Routing Logic

As mentioned above, the Port Routing logic is implemented in the suspend power well so that remuneration and re-mapping of the USB ports is not required following entering and exiting a system sleep state in which the core power is turned off.

Reset Event	Effect on Configure Flag	Effect on Port Owner Bits
Suspend Well Reset	cleared (0)	set (1)
Core Well Reset	no effect	no effect
D3-to-D0 Reset	no effect	no effect
HCRESET	cleared (0)	set (1)

13.1.5 USB 2.0 Legacy Keyboard Operation

The Intel® SCH supports a keyboard downstream from either a full-speed/low-speed or a high-speed port. The description of the legacy keyboard support is unchanged from USB 1.1 (See Section 12.1.4).

13.1.6 USB 2.0 Based Debug Port

The Intel® SCH supports the elimination of the legacy COM ports by providing the ability for new debugger software to interact with devices on a USB 2.0 port.

For details on the debug port, refer to Appendix C of *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0.

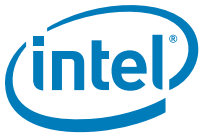
13.2 USB EHCI Configuration Registers

Note: All bit descriptions in this chapter assume the default configuration of Device 29 supporting USB Ports 0-2.

Table 36. USB EHCI PCI Register Address Map

Offset	Mnemonic	Register Name	Default Value	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	8117h	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/W, RO
08h	RID	Revision Identification	See description	RO
09h–0Bh	CC	Class Codes	0C0320h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	MEM_BASE	Memory Base Address	00000000h	R/W, RO
2Ch–2Dh	SVID	USB EHCI Subsystem Vendor Identification	UUUUh	R/W (special)
2Eh–2Fh	SID	USB EHCI Subsystem Identification	UUUUh	R/W (special)
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See description	RO
50h	PM_CAPID	PCI Power Management Capability ID	01h	RO
51h	NXT_PTR1	Next Item Pointer	58h	R/W (special)
52h–53h	PM_CAP	Power Management Capabilities	C9C2h	R/W (special)
54h–55h	PM_CTL_STS	Power Management Control/Status	0000h	R/W, R/WC, RO
58h	DEBUG_CAPID	Debug Port Capability ID	0Ah	RO
59h	NXT_PTR2	Next Item Pointer #2	00h	RO
5Ah–5Bh	DEBUG_BASE	Debug Port Base Offset	20A0h	RO
60h	USB_RELNUM	USB Release Number	20h	RO
61h	FL_ADJ	Frame Length Adjustment	20h	R/W
62h–63h	PWAKE_CAP	Port Wake Capabilities	03FDh	RO
64h–65h	CUO	Classic USB Override	0000h	RO, R/W
68h–6Bh	LEG_EXT_CAP	USB EHCI Legacy Support Extended Capability	00000001h	R/W, RO
6Ch–6Fh	LEG_EXT_CS	USB EHCI Legacy Extended Support Control/Status	00000000h	R/W, R/WC, RO
70h–73h	SPECIAL_SMI	Intel specific USB 2.0 SMI	00000000h	R/W, R/WC
80h	ACCESS_CNTL	Access Control	00h	R/W
C0h–C3h	FD	Function Disable	00000000h	RO, R/W

NOTE: All configuration registers in this section are in the core well and reset by a core well reset and the D3-to-D0 warm reset, except as noted.



13.2.1 VID—Vendor Identification Register

Offset Address: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Default and Access	Description
15:0	8086 RO	**Vendor ID**: This is a 16-bit value assigned to Intel.

13.2.2 DID—Device Identification Register

Offset Address: 02h–03h Attribute: RO
Default Value: 8117h Size: 16 bits

Bit	Default and Access	Description
15:0	8117h RO	**Device ID**: The value 8117h corresponds to the Intel® SCH EHCI controller.

13.2.3 PCICMD—PCI Command Register

Address Offset: 04h–05h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:11	0 RO	Reserved
10	0 R/W	**Interrupt Disable** 0 = The function is capable of generating interrupts. 1 = The function cannot generate its interrupt to the interrupt controller. **Note** that the corresponding Interrupt Status bit (D29:F7:06h, bit 3) is not affected by the interrupt enable.
9:3	00h RO	Reserved
2	0 R/W	**Bus Master Enable (BME)** 0 = Disables this functionality. 1 = Enables the Intel® SCH to act as a master on the PCI bus for USB transfers.
1	0 R/W	**Memory Space Enable (MSE)**: This bit controls access to the USB 2.0 Memory Space registers. 0 = Disables this functionality. 1 = Enables accesses to the USB 2.0 registers. The Base Address register (D29:F7:10h) for USB 2.0 should be programmed before this bit is set.
0	0 RO	Reserved

13.2.4 PCISTS—PCI Status Register

Address Offset: 06h–07h Attribute: R/W, RO
Default Value: 0010h Size: 16 bits

Bit	Default and Access	Description
15:5	000h RO	Reserved
4	1 RO	**Capabilities List (CAP_LIST)**: Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0 RO	**Interrupt Status**: This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = This bit will be 0 when the interrupt is deasserted. 1 = This bit is a 1 when the interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	0 RO	Reserved

13.2.5 RID—Revision Identification Register

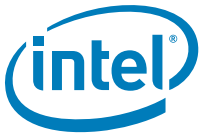
Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Revision ID**: Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the value of the Revision ID Register

13.2.6 CC—Class Codes Register

Address Offset: 09h–0Bh Attribute: RO
Default Value: 0C0320h Size: 24 bits

Bit	Default and Access	Description
23:16	0Ch RO	**Base Class Code (BCC)** 0Ch = Serial bus controller.
15:8	03h RO	**Sub Class Code (SCC)** 03h = Universal serial bus host controller.
7:0	20h RO	**Programming Interface (PI)**: A value of 20h indicates that this USB 2.0 host controller conforms to the EHCI Specification.



13.2.7 MLT—Master Latency Timer Register

Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Master Latency Timer (MLT)**: Hardwired to 00h. Because the EHCI controller is internally implemented with arbitration on an interface (and not PCI), it does not need a master latency timer.

13.2.8 HEADTYP—Header Type Register

Address Offset: 0Eh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7	0 RO	**Multi-Function Device**: Hardwired to 0h indicating this is a single function device.
6:0	00h RO	**Configuration Layout**. Hardwired to 00h, which indicates the standard PCI configuration layout.

13.2.9 MEM_BASE—Base Address Register

Address Offset: 10h–13h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:10	0000h R/W	**Memory Base Address**: Bits 31:10 correspond to memory address signals 31:10, respectively. This gives 1 KB of locatable memory space aligned to 1 KB boundaries.
9:4	00h RO	Reserved
3	0 RO	**Prefetchable**: Hardwired to 0 indicating that this range should not be prefetched.
2:1	00b RO	**Type**: Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
0	0 RO	**Resource Type Indicator (RTE)**: Hardwired to 0 indicating that the base address field in this register maps to memory space.

13.2.10 SVID—USB EHCI Subsystem Vendor ID Register

Address Offset: 2Ch–2Dh Attribute: R/W (special)
Default Value: UUUUh Size: 16 bits
Reset: None

Bit	Default and Access	Description
15:0	R/W	**Subsystem Vendor ID (SVID)** (special): This register, in combination with the USB 2.0 Subsystem ID register, enables the operating system to distinguish each subsystem from the others. **NOTE:** Writes to this register are enabled when the WRT_RDONLY bit (D29:F7:80h, bit 0) is set to 1.

13.2.11 SID—USB EHCI Subsystem ID Register

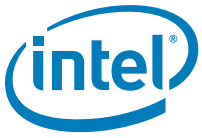
Address Offset: 2Eh–2Fh Attribute: R/W (special)
Default Value: UUUUh Size: 16 bits
Reset: None

Bit	Default and Access	Description
15:0	R/W	**Subsystem ID (SID)** (special): BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). **NOTE:** Writes to this register are enabled when the WRT_RDONLY bit (D29:F7:80h, bit 0) is set to 1.

13.2.12 CAP_PTR—Capabilities Pointer Register

Address Offset: 34h Attribute: RO
Default Value: 50h Size: 8 bits

Bit	Default and Access	Description
7:0	50h RO	**Pointer (PTR)**: This register points to the starting offset of the USB 2.0 capabilities ranges.



13.2.13 INT_LN—Interrupt Line Register

Address Offset: 3Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Interrupt Line (INT_LN)**: This data is not used by the Intel® SCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

13.2.14 INT_PN—Interrupt Pin Register

Address Offset: 3Dh Attribute: RO
Default Value: See Description Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Interrupt Pin**. This reflects the value of D29IP.EIP (Chipset Config Registers:Offset 3108:bits 31:28). **NOTE:** Bits 7:4 are always 0.

13.2.15 PM_CAPID—PCI Power Management Capability ID Register

Address Offset: 50h Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Default and Access	Description
7:0	01h RO	**Power Management Capability ID**: A value of 01h indicates that this is a PCI Power Management capabilities field.

13.2.16 NXT_PTR1—Next Item Pointer #1 Register

Address Offset: 51h Attribute: R/W (special)
Default Value: 58h Size: 8 bits

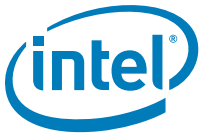
Bit	Default and Access	Description
7:0	58h R/W	**Next Item Pointer 1 Value** (special): This register defaults to 58h, which indicates that the next capability registers begin at configuration offset 58h. This register is writable when the WRT_RDONLY bit (D29:F7:80h, bit 0) is set. This allows BIOS to effectively hide the Debug Port capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Only values of 58h (Debug Port visible) and 00h (Debug Port invisible) are expected to be programmed in this register. **NOTE:** Register not reset by D3-to-D0 warm reset.

13.2.17 PM_CAP—Power Management Capabilities Register

Address Offset: 52h–53h Attribute: R/W (special), RO
Default Value: C9C2h Size: 16 bits

Bit	Default and Access	Description
15:11	11001b R/W	**PME Support (PME_SUP)** (special): This 5-bit field indicates the power states in which the function may assert PME#. The EHCI does not support the D1 or D2 states. For all other states, the EHCI is capable of generating PME#. Software should never need to modify this field.
10	0 RO	**D2 Support (D2_SUP)**. 0 = D2 State is not supported
9	0 RO	**D1 Support (D1_SUP)**. 0 = D1 State is not supported
8:6	111b R/W	**Auxiliary Current (AUX_CUR).** The EHCI reports 375 mA maximum suspend well current required when in the $D3_{COLD}$ state. This value may be rewritten by BIOS when a better current value is known.
5	0 RO	**Device Specific Initialization (DSI**). The Intel® SCH reports 0, indicating that no device-specific initialization is required.
4	0 RO	Reserved
3	0 RO	**PME Clock (PME_CLK)**. The Intel® SCH reports 0, indicating that no PCI clock is required to generate PME#.
2:0	010b RO	**Version (VER)**. The Intel® SCH reports 010b, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

NOTES:
1. Normally, this register is read-only to report capabilities to the power management software. To report different power management capabilities, depending on the system in which the Intel® SCH is used, bits 15:11 and 8:6 in this register are writable when the WRT_RDONLY bit (D29:F7:80h, bit 0) is set. The value written to this register does not effect the hardware other than changing the value returned during a read.
2. This register is reset during a core well reset, but not D3-to-D0 state transition.



13.2.18 PWR_CNTL_STS—Power Management Control/Status Register

Address Offset: 54h–55h
Default Value: 0000h
Attribute: R/W, R/WC, RO
Size: 16 bits

Bit	Default and Access	Description
15	0 R/WC	**PME Status (STS)** 0 = Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). 1 = This bit is set when the EHCI would normally assert the PME# signal independent of the state of the PME_En bit. **NOTE:** This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	00b RO	**Data Scale (DSCA)**: Hardwired to 00b indicating it does not support the associated Data register.
12:9	0h RO	**Data Select (DSEL)**: Hardwired to 0000b indicating it does not support the associated Data register.
8	0 R/W	**PME Enable (EN)** 0 = Disable. 1 = Enable. Enables EHCI to generate an internal PME signal when PME_Status is 1. **NOTE:** This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:2	00h RO	Reserved
1:0	00b R/W	**Power State**: This 2-bit field is used both to determine the current power state of EHCI function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = $D3_{HOT}$ state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the $D3_{HOT}$ state, the Intel® SCH must not accept accesses to the EHCI memory range; but the configuration space must still be accessible. When software changes this value from the $D3_{HOT}$ state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

NOTE: Reset (bits 15, 8): suspend well, and not D3-to-D0 warm reset nor core well reset.

13.2.19 DEBUG_CAPID—Debug Port Capability ID Register

Address Offset: 58h Attribute: RO
Default Value: 0Ah Size: 8 bits

Bit	Default and Access	Description
7:0	0Ah RO	**Debug Port Capability ID**: Hardwired to 0Ah indicating that this is the start of a Debug Port Capability structure.

13.2.20 NXT_PTR2—Next Item Pointer #2 Register

Address Offset: 59h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h RO	**Next (NEXT)**: Hardwired to 00h to indicate there are no more capability structures in this function.

13.2.21 DEBUG_BASE—Debug Port Base Offset Register

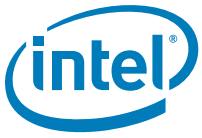
Address Offset: 5Ah–5Bh Attribute: RO
Default Value: 20A0h Size: 16 bits

Bit	Default and Access	Description
15:13	02h RO	**BAR Number**: Hardwired to 001b to indicate the memory BAR begins at offset 10h in the EHCI configuration space.
12:0	A0h RO	**Debug Port Offset**: Hardwired to 0A0h to indicate that the Debug Port registers begin at offset A0h in the EHCI memory range.

13.2.22 USB_RELNUM—USB Release Number Register

Address Offset: 60h Attribute: RO
Default Value: 20h Size: 8 bits

Bit	Default and Access	Description
7:0	20h RO	**USB Release Number**: A value of 20h indicates that this controller follows *Universal Serial Bus (USB) Specification, Revision 2.0*.



13.2.23 FL_ADJ—Frame Length Adjustment Register

Address Offset:	61h	Attribute:	R/W
Default Value:	20h	Size:	8 bits

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit (D29:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 1. Changing value of this register while the host controller is operating yields undefined results. It should not be reprogrammed by USB system software unless the default or BIOS programmed values are incorrect, or the system is restoring the register while returning from a suspended state.

These bits in suspend well and not reset by a D3-to-D0 warm rest or a core well reset.

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>7:6</td><td>00b
RO</td><td>Reserved. These bits are reserved for future use and should read as 00b.</td></tr>
<tr><td>5:0</td><td>20h
R/W</td><td>Frame Length Timing Value: Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000.
<table>
<tr><th>Frame Length (# 480 MHz Clocks) (decimal)</th><th>Frame Length Timing Value (this register) (decimal)</th></tr>
<tr><td>59488</td><td>0</td></tr>
<tr><td>59504</td><td>1</td></tr>
<tr><td>59520</td><td>2</td></tr>
<tr><td>—</td><td>—</td></tr>
<tr><td>59984</td><td>31</td></tr>
<tr><td>60000</td><td>32</td></tr>
<tr><td>—</td><td>—</td></tr>
<tr><td>60480</td><td>62</td></tr>
<tr><td>60496</td><td>63</td></tr>
</table></td></tr>
</table>

13.2.24 PWAKE_CAP—Port Wake Capability Register

Address Offset:	62–63h	Attribute:	RO
Default Value:	01FFh	Size:	16 bits

This register is in the suspend power well. A one in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect/connect or over-current events as wake-up events. This is an information-only mask register.

Reset: Suspend well, and not D3-to-D0 warm reset nor core well reset.

Bit	Default and Access	Description
15:9	0 RO	Reserved
8:1	1FFh RO	**Port Wake Up Capability Mask**: Bit positions 1 through 8 (Device 29) correspond to a physical port implemented on this host controller. For example, Bit Position 1 corresponds to Port 1, Bit Position 2 corresponds to Port 2, etc.
0	1b RO	**Port Wake Implemented**: A 1 in this bit indicates that this register is implemented to software.

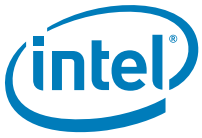
13.2.25 CUO—Classic USB Override Register

Address Offset:	64h	Attribute:	RO, R/W
Default Value:	00h	Size:	16 bits

This 16-bit register provides a bit corresponding to each of the ports on the EHCI host controller. When a bit is set to 1, the corresponding USB port is routed to the classic (UHCI) host controller and will only operate using the classic signaling rates. The feature is implemented with the following requirements:

- The associated Port Owner bit does not reflect the value in this new override register. This ensures compatibility with EHCI drivers.
- BIOS must only write to this register during initialization (while the Configured Flag is 0).
- The register is implemented in the Suspend well to maintain port-routing when the core power goes down
- When a 1 is present in the CUO register, then the classic controller operates the port regardless of the EHCI port routing logic. The corresponding EHCI port will always appear disconnected in this mode.
- Port 0 must not be programmed into Classic USB Override mode as this is the Debug Port.

Bit	Default and Access	Description
15:8	00h RO	Reserved
7:1	00h R/W	**Classic USB Port Owner**: A 1 in a bit position forces the corresponding USB port to the classic host controller.
0	0 RO	Reserved



13.2.26 LEG_EXT_CAP—USB EHCI Legacy Support Extended Capability Register

Address Offset:	68–6Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset. This register lives in the resume power well.

Bit	Default and Access	Description
31:25	00h RO	Reserved. Hardwired to 00h
24	0 R/W	**HC OS Owned Semaphore**: System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as clear.
23:17	00h RO	Reserved. Hardwired to 00h
16	0 R/W	**HC BIOS Owned Semaphore**: The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will clear this bit in response to a request for ownership of the EHCI controller by system software.
15:8	00h RO	**Next EHCI Capability Pointer**: Hardwired to 00h to indicate that there are no EHCI Extended Capability structures in this device.
7:0	01h RO	**Capability ID**: Hardwired to 01h to indicate that this EHCI Extended Capability is the Legacy Support Capability.

13.2.27 LEG_EXT_CS—USB EHCI Legacy Support Extended Control/Status Register

Address Offset:	6C–6Fh	Attribute:	R/W, R/WC, RO
Default Value:	00000000h	Size:	32 bits
Power Well:	Suspend		

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Default and Access	Description
31	0 R/WC	**SMI on BAR**: Software clears this bit by writing a 1 to it. 0 = Base Address Register (BAR) not written. 1 = This bit is set to 1 when the Base Address Register (BAR) is written.
30	0 R/WC	**SMI on PCI Command**: Software clears this bit by writing a 1 to it. 0 = PCI Command (PCICMD) Register Not written. 1 = This bit is set to 1 when the PCI Command (PCICMD) Register is written.
29	0 R/WC	**SMI on OS Ownership Change**: Software clears this bit by writing a 1 to it. 0 = No HC OS Owned Semaphore bit change. 1 = This bit is set to 1 when the HC OS Owned Semaphore bit in the LEG_EXT_CAP register (D29:F7:68h, bit 24) transitions from 1-to-0 or 0-to-1.

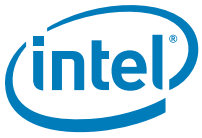
Bit	Default and Access	Description
28:22	00h RO	Reserved. Hardwired to 00h
21	0 RO	**SMI on Async Advance**: This bit is a shadow bit of the Interrupt on Async Advance bit (D29:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the Interrupt on Async Advance bit in the USB2.0_STS register.
20	0 RO	**SMI on Host System Error**: This bit is a shadow bit of Host System Error bit in the USB2.0_STS register (D29:F7:CAPLENGTH + 24h, bit 4). **NOTE:** To clear this bit system software must write a 1 to the Host System Error bit in the USB2.0_STS register.
19	0 RO	**SMI on Frame List Rollover**: This bit is a shadow bit of Frame List Rollover bit (D29:F7:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the Frame List Rollover bit in the USB2.0_STS register.
18	0 RO	**SMI on Port Change Detect**: This bit is a shadow bit of Port Change Detect bit (D29:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the Port Change Detect bit in the USB2.0_STS register.
17	0 RO	**SMI on USB Error**: This bit is a shadow bit of USB Error Interrupt (USBERRINT) bit (D29:F7:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the USB Error Interrupt bit in the USB2.0_STS register.
16	0 RO	**SMI on USB Complete**: This bit is a shadow bit of USB Interrupt (USBINT) bit (D29:F7:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register. **NOTE:** To clear this bit system software must write a 1 to the USB Interrupt bit in the USB2.0_STS register.
15	0 R/W	**SMI on BAR Enable** 0 = Disable. 1 = Enable. When this bit is 1 and SMI on BAR (D29:F7:6Ch, bit 31) is 1, then the host controller will issue an SMI.
14	0 R/W	**SMI on PCI Command Enable** 0 = Disable. 1 = Enable. When this bit is 1 and SMI on PCI Command (D29:F7:6Ch, bit 30) is 1, then the host controller will issue an SMI.
13	0 R/W	**SMI on OS Ownership Enable** 0 = Disable. 1 = Enable. When this bit is a 1 and the OS Ownership Change bit (D29:F7:6Ch, bit 29) is 1, the host controller will issue an SMI.
12:6	00h RO	Reserved: Hardwired to 00h

Bit	Default and Access	Description
5	0 R/W	**SMI on Async Advance Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Async Advance bit (D29:F7:6Ch, bit 21) is a 1, the host controller will issue an SMI immediately.
4	0 R/W	**SMI on Host System Error Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Host System Error (D29:F7:6Ch, bit 20) is a 1, the host controller will issue an SMI.
3	0 R/W	**SMI on Frame List Rollover Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Frame List Rollover bit (D29:F7:6Ch, bit 19) is a 1, the host controller will issue an SMI.
2	0 R/W	**SMI on Port Change Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Port Change Detect bit (D29:F7:6Ch, bit 18) is a 1, the host controller will issue an SMI.
1	0 R/W	**SMI on USB Error Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on USB Error bit (D29:F7:6Ch, bit 17) is a 1, the host controller will issue an SMI immediately.
0	0 R/W	**SMI on USB Complete Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on USB Complete bit (D29:F7:6Ch, bit 16) is a 1, the host controller will issue an SMI immediately.

13.2.28 SPECIAL_SMI—Intel Special USB 2.0 SMI Register

Address Offset: 70h–73h Attribute: R/W, R/WC
Default Value: 00000000h Size: 32 bits
Power Well: Suspend

Bit	Default and Access	Description
31:30	00b RO	Reserved. Hardwired to 00b
29:22	0 R/WC	**SMI on PortOwner**: Software clears these bits by writing a 1 to it. 0 = No Port Owner bit change. 1 = Bits 29:22 correspond to the Port Owner bits for Ports 8 (29) through 1 (22). These bits are set to 1 when the associated Port Owner bits transition from 0 to 1 or 1 to 0.
21	0 R/WC	**SMI on PMCSR**C: Software clears these bits by writing a 1 to it. 0 = Power State bits Not modified. 1 = Software modified the Power State bits in the Power Management Control/Status (PMCSR) register (D29:F7:54h).
20	0 R/WC	**SMI on Async**: Software clears these bits by writing a 1 to it. 0 = No Async Schedule Enable bit change 1 = Async Schedule Enable bit transitioned from 1-to-0 or 0-to-1.
19	0 R/WC	**SMI on Periodic**: Software clears this bit by writing a 1 it. 0 = No Periodic Schedule Enable bit change. 1 = Periodic Schedule Enable bit transitions from 1-to-0 or 0-to-1.
18	0 R/WC	**SMI on CF**: Software clears this bit by writing a 1 it. 0 = No Configure Flag (CF) change. 1 = Configure Flag (CF) transitions from 1-to-0 or 0-to-1.
17	0 R/WC	**SMI on HCHalted**: Software clears this bit by writing a 1 it. 0 = HCHalted did Not transition to 1 (as a result of the Run/Stop bit being cleared). 1 = HCHalted transitions to 1 (as a result of the Run/Stop bit being cleared).
16	0 R/WC	**SMI on HCReset**: Software clears this bit by writing a 1 it. 0 = HCRESET did Not transitioned to 1. 1 = HCRESET transitioned to 1.
15:14	00b RO	Reserved: Hardwired to 00b
13:6	00h R/W	**SMI on PortOwner Enable** 0 = Disable. 1 = Enable. When any of these bits are 1 and the corresponding SMI on PortOwner bits are 1, then the host controller will issue an SMI. Unused ports should have their corresponding bits cleared.
5	0 R/W	**SMI on PMSCR Enable** 0 = Disable. 1 = Enable. When this bit is 1 and SMI on PMSCR is 1, then the host controller will issue an SMI.



Bit	Default and Access	Description
4	0 R/W	**SMI on Async Enable** 0 = Disable. 1 = Enable. When this bit is 1 and SMI on Async is 1, then the host controller will issue an SMI
3	0 R/W	**SMI on Periodic Enable** 0 = Disable. 1 = Enable. When this bit is 1 and SMI on Periodic is 1, then the host controller will issue an SMI.
2	0 R/W	**SMI on CF Enable** 0 = Disable. 1 = Enable. When this bit is 1 and SMI on CF is 1, then the host controller will issue an SMI.
1	0 R/W	**SMI on HCHalted Enable** 0 = Disable. 1 = Enable. When this bit is a 1 and SMI on HCHalted is 1, then the host controller will issue an SMI.
0	0 R/W	**SMI on HCReset Enable** 0 = Disable. 1 = Enable. When this bit is a 1 and SMI on HCReset is 1, then host controller will issue an SMI.

NOTE: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

13.2.29 ACCESS_CNTL—Access Control Register

Address Offset: 80h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:1	00h RO	Reserved
0	0 R/W	**WRT_RDONLY**: When set to 1, this bit enables a select group of normally read-only registers in the EHCI function to be written by software. Registers that may only be written when this mode is entered are noted in the summary tables and detailed description as “Read/Write-Special”. The registers fall into two categories: System-configured parameters and Status bits.

13.2.30 FD—Function Disable Register

Address Offset: C0h–C3h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:3	0s RO	Reserved
2	0 R/W	**Clock Gating Disable (CGD)** 0 = Clock gating within this function is enabled 1 = Clock gating within this function is disabled
1	0 RO	Reserved
0	0 R/W	**Disable (D)** 0 = This function is enabled 1 = This function is disabled and the configuration space is not accessible.

13.3 Memory-Mapped I/O Registers

The EHCI memory-mapped I/O space is composed of two sets of registers: Capability Registers and Operational Registers.

Note: The Intel® SCH EHCI controller will not accept memory transactions (neither reads nor writes) as a target that are locked transactions. The locked transactions should not be forwarded to PCI as the address space is known to be allocated to USB.

Note: When the EHCI function is in the D3 PCI power state, accesses to the USB 2.0 memory range are ignored and result a master abort. Similarly, if the Memory Space Enable (MSE) bit (D29:F7:04h, bit 1) is not set in the Command register in configuration space, the memory range will not be decoded by the Intel® SCH enhanced host controller (EHC). If the MSE bit is not set, then the Intel® SCH must default to allowing any memory accesses for the range specified in the BAR to go to PCI. This is because the range may not be valid and, therefore, the cycle must be made available to any other targets that may be currently using that range.

13.3.1 Host Controller Capability Registers

These registers specify the limits, restrictions and capabilities of the host controller implementation. Within the host controller capability registers, only the structural parameters register is writable. These registers are implemented in the suspend well and is only reset by the standard suspend-well hardware reset, not by HCRESET or the D3-to-D0 reset.

Note: The EHCI controller does not support as a target memory transactions that are locked transactions. Attempting to access the EHCI controller Memory-Mapped I/O space using locked memory transactions will result in undefined behavior.

Note: When the USB2 function is in the D3 PCI power state, accesses to the USB2 memory range are ignored and will result in a master abort Similarly, if the Memory Space Enable (MSE) bit is not set in the Command register in configuration space, the memory range will not be decoded by the Enhanced Host Controller (EHC). If the MSE bit is not set, then the EHCI will not claim any memory accesses for the range specified in the BAR.

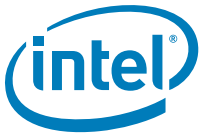


Table 37. EHCI Capability Registers

MEM_BASE + Offset	Mnemonic	Register	Default	Type
00h	CAPLENGTH	Capabilities Registers Length	20h	RO
02h–03h	HCIVERSION	Host Controller Interface Version Number	0100h	RO
04h–07h	HCSPARAMS	Host Controller Structural Parameters	00104208h	R/W (special), RO
08h–0Bh	HCCPARAMS	Host Controller Capability Parameters	00006871h	RO

NOTE: Read/Write Special means that the register is normally read-only, but may be written when the WRT_RDONLY bit is set. Because these registers are expected to be programmed by BIOS during initialization, their contents must not get modified by HCRESET or D3-to-D0 internal reset.

13.3.1.1 CAPLENGTH—Capability Registers Length Register

Offset: MEM_BASE + 00h Attribute: RO
Default Value: 20h Size: 8 bits

Bit	Default and Access	Description
7:0	20h RO	**Capability Register Length Value:** This register is used as an offset to add to the Memory Base Register (D29:F7:10h) to find the beginning of the Operational Register Space. This field is hardwired to 20h indicating that the Operation Registers begin at offset 20h.

13.3.1.2 HCIVERSION—Host Controller Interface Version Number Register

Offset: MEM_BASE + 02h–03h Attribute: RO
Default Value: 0100h Size: 16 bits

Bit	Default and Access	Description
15:0	0100h RO	**Host Controller Interface Version Number:** This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

13.3.1.3 HCSPARAMS—Host Controller Structural Parameters

Offset: MEM_BASE + 04h–07h Attribute: R/W (special), RO
Default Value: 00103206h Size: 32 bits

Note: This register is reset by a suspend well reset and not a D3-to-D0 reset or HCRESET.

Bit	Default and Access	Description
31:24	00h RO	Reserved
23:20	1h RO	**Debug Port Number (DP_N)** (special): Hardwired to 1h indicating that the Debug Port is on the lowest numbered port on the EHCI.
19:16	0h RO	Reserved
15:12	3h R/W	**Number of Companion Controllers (N_CC)**: This field indicates the number of companion controllers associated with this USB EHCI host controller. A 0 in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value of 1 or more in this field indicates there are companion USB UHCI host controller(s). Port-ownership hand-offs are supported. High, Full- and Low-speed devices are supported on the host controller root ports. The Intel® SCH allows the default value of 3h to be over-written by BIOS. When removing classic controllers, they must be disabled in the following order: Function 2, Function 1, and Function 0, which correspond to Ports 5:4, 3:2, and 1:0, respectively for Device 29.
11:8	2h RO	**Number of Ports per Companion Controller (N_PCC)**: Hardwired to 2h. This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software.
7	0h RO	**Port Routing Rules (PRR)**: Indicating the first NPCC ports are routed to the lowest numbered function companion host controller, the next NPCC ports are routed to the next lowest function companion controller, and so on. Hardwired to 0.
6:4	000b RO	Reserved
3:0	8h R/W	**Number of Ports (N_PORTS)**: This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1h to Fh. The Intel® SCH reports 8h by default. However, software may write a value less than the default for some platform configurations. A 0 in this field is undefined.

NOTE: This register is writable when the WRT_RDONLY bit is set.

13.3.1.4 HCCPARAMS—Host Controller Capability Parameters Register

Offset: MEM_BASE + 08h–0Bh Attribute: RO
Default Value: 00016871h Size: 32 bits

Bit	Default and Access	Description
31:17	0000h RO	Reserved
16	1 RO	**Periodic Schedule Update Capability (PSUC)**: Indicates the EHCI supports ECMD.PUE.
15:8	68h RO	**EHCI Extended Capabilities Pointer (EECP)**: This field is hardwired to 68h, indicating that the EHCI capabilities list exists and begins at offset 68h in the PCI configuration space.
7:4	7h RO	**Isochronous Scheduling Threshold**: This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit 7 is 0, the value of the least significant 3 bits indicates the number of micro-frames a host controller hold a set of isochronous data structures (one or more) before flushing the state. When bit 7 is a 1, then host software assumes the host controller may cache an isochronous data structure for an entire frame. Refer to the EHCI specification for details on how software uses this information for scheduling isochronous transfers. This field is hardwired to 7h.
3	0 RO	Reserved. These bits are reserved and should be set to 0.
2	0 RO	**Asynchronous Schedule Park Capability**: This bit is hardwired to 0 indicating that the host controller does not support this optional feature.
1	0 RO	**Programmable Frame List Flag**: 0 = System software must use a frame list length of 1024 elements with this host controller. The USB2.0_CMD register (D29:F7:CAPLENGTH + 20h, bits 3:2) *Frame List Size* field is a read-only register and must be set to 0. 1 = System software can specify and use a smaller frame list and configure the host controller by the USB2.0_CMD register *Frame List Size* field. The frame list must always be aligned on a 4-K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	1 RO	**64-bit Addressing Capability**: This field documents the addressing range capability of this implementation. The value of this field determines whether software should use the 32-bit or 64-bit data structures. Values for this field have the following interpretation: 0 = Data structures using 32-bit address memory pointers 1 = Data structures using 64-bit address memory pointers This bit is hardwired to 1. **NOTE:** The Intel® SCH only implements 44 bits of addressing. Bits 63:44 will always be 0.

13.3.2 Host Controller Operational Registers

This section defines the enhanced host controller operational registers. These registers are located after the capabilities registers. The operational register base must be dword-aligned and is calculated by adding the value in the first capabilities register (CAPLENGTH) to the base address of the enhanced host controller register address space (MEM_BASE). Since CAPLENGTH is always 20h, Table 38 already accounts for this offset. All registers are 32 bits in length.

The first set of registers in Table 38 (offsets MEM_BASE + 20:3Bh) are implemented in the core power well. These core well registers are reset by either a core well hardware reset, manually resetting the EHCI controller by the HCRESET bit in the USB2.0_CMD register.

The second set of registers (offsets MEM_BASE + 60:83h) are powered by the suspend power well and remain powered during the S3 sleep state. These registers are reset either during a suspend well hardware reset or by resetting the EHCI controller (by the USB2.0_CMD.HCRESET bit).

Table 38. Enhanced Host Controller Operational Register Address Map

MEM_BASE + Offset	Mnemonic	Register Name	Default	Type
20h–23h	USB2.0_CMD	USB 2.0 Command	00080000h	R/W, RO
24h–27h	USB2.0_STS	USB 2.0 Status	00001000h	R/WC, RO
28h–2Bh	USB2.0_INTR	USB 2.0 Interrupt Enable	00000000h	R/W
2Ch–2Fh	FRINDEX	USB 2.0 Frame Index	00000000h	R/W,
30h–33h	CTRLDSSEGMENT	Control Data Structure Segment	00000000h	R/W, RO
34h–37h	PERODICLISTBASE	Period Frame List Base Address	00000000h	R/W
38h–3Bh	ASYNCLISTADDR	Current Asynchronous List Address	00000000h	R/W
60h–63h	CONFIGFLAG	Configure Flag	00000000h	R/W
64h–67h	PORT0SC	Port 0 Status and Control	00003000h	R/W, R/WC, RO
68h–6Bh	PORT1SC	Port 1 Status and Control	00003000h	R/W, R/WC, RO
6Ch–6Fh	PORT2SC	Port 2 Status and Control	00003000h	R/W, R/WC, RO
70h–73h	PORT3SC	Port 3 Status and Control	00003000h	R/W, R/WC, RO
74h–77h	PORT4SC	Port 4 Status and Control	00003000h	R/W, R/WC, RO
78h–7Bh	PORT5SC	Port 5 Status and Control	00003000h	R/W, R/WC, RO
7Ch–7Fh	PORT6SC	Port 6 Status and Control	00003000h	R/W, R/WC, RO
80h–83h	PORT7SC	Port 7 Status and Control	00003000h	R/W, R/WC, RO

13.3.2.1 USB2.0_CMD—USB 2.0 Command Register

Offset: MEM_BASE + 20–23h Attribute: R/W, RO
Default Value: 00080000h Size: 32 bits

Bit	Default and Access	Description
31:24	00h RO	Reserved. These bits are reserved and should be set to 0 when writing this register.
23:16	08h R/W	**Interrupt Threshold Control**: System software uses this field to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. Value / Maximum Interrupt Interval: 00h – Reserved 01h – 1 micro-frame 02h – 2 micro-frames 04h – 4 micro-frames 08h – 8 micro-frames (= ~1 ms) (default) 10h – 16 micro-frames (2 ms) 20h – 32 micro-frames (4 ms) 40h – 64 micro-frames (8 ms)
15:12	0h RO	Reserved. These bits are reserved and should be set to 0 when writing this register.
11:8	0h RO	**Unimplemented Asynchronous Park Mode**: Hardwired to 0h indicating the host controller does not support this optional feature.
7	0 RO	**Light Host Controller Reset**: Hardwired to 0. The Intel® SCH does not implement this optional reset.
6	0 R/W	**Interrupt on Async Advance Doorbell**: This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. 0 = The host controller sets this bit to a 0 after it has set the Interrupt on Async Advance status bit (D29:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register to a 1. 1 = Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USB2.0_STS register. If the *Interrupt on Async Advance Enable* bit in the USB2.0_INTR register (D29:F7:CAPLENGTH + 28h, bit 5) is a 1 then the host controller will assert an interrupt at the next interrupt threshold. See the EHCI specification for operational details. **NOTE:** Software should not write a 1 to this bit when the asynchronous schedule is inactive. Doing so will yield undefined results.
5	0 R/W	**Asynchronous Schedule Enable**: Default 0b. This bit controls whether the host controller skips processing the Asynchronous Schedule. 0 = Do not process the Asynchronous Schedule 1 = Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
4	0 R/W	**Periodic Schedule Enable**: Default 0b. This bit controls whether the host controller skips processing the Periodic Schedule. 0 = Do not process the Periodic Schedule 1 = Use the PERIODICLISTBASE register to access the Periodic Schedule.

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>3:2</td><td>0
RO</td><td>Frame List Size: The Intel® SCH hardwires this field to 00b because it only supports the 1024-element frame list size.</td></tr>
<tr><td>1</td><td>0
R/W</td><td>Host Controller Reset (HCRESET): This control bit used by software to reset the host controller. The effects of this on root hub registers are similar to a Chip Hardware Reset (i.e., RSMRST# assertion and PWROK deassertion on the Intel® SCH).
When software writes a 1 to this bit, the host controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.

NOTE: PCI configuration registers and Host controller capability registers are not effected by this reset.
All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s), with the side effects described in the EHCI spec. Software must re-initialize the host controller in order to return the host controller to an operational state.
This bit is set to 0 by the host controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this register.
Software should not set this bit to a 1 when the HCHalted bit (D29:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 0. Attempting to reset an actively running host controller will result in undefined behavior. This reset me be used to leave EHCI port test modes.</td></tr>
<tr><td>0</td><td>0
R/W</td><td>Run/Stop (RS):
0 = Stop (default)
1 = Run. When set to a 1, the Host controller proceeds with execution of the schedule. The Host controller continues execution as long as this bit is set. When this bit is set to 0, the Host controller completes the current transaction on the USB and then halts. The HCHalted bit in the USB2.0_STS register indicates when the Host controller has finished the transaction and has entered the stopped state.
Software should not write a 1 to this field unless the host controller is in the Halted state
(i.e., HCHalted in the USBSTS register is a 1). The Halted bit is cleared immediately when the Run bit is set.
The following table explains how the different combinations of Run and Halted should be interpreted:

<table>
<tr><th>Run/Stop</th><th>Halted</th><th>Interpretation</th></tr>
<tr><td>0b</td><td>0b</td><td>In the process of halting</td></tr>
<tr><td>0b</td><td>1b</td><td>Halted</td></tr>
<tr><td>1b</td><td>0b</td><td>Running</td></tr>
<tr><td>1b</td><td>1b</td><td>Invalid - the HCHalted bit clears immediately</td></tr>
</table>

Memory read cycles initiated by the EHCI that receive any status other than Successful will result in this bit being cleared.</td></tr>
</table>

NOTE: The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

13.3.2.2 USB2.0_STS—USB 2.0 Status Register

Offset: MEM_BASE + 24h–27h Attribute: R/WC, RO
Default Value: 00001000h Size: 32 bits

This register indicates pending interrupts and various states of the EHCI controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in Section 4 of the EHCI specification for additional information concerning USB 2.0 interrupt conditions.

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Bit	Default and Access	Description
31:16	0000h RO	Reserved. These bits are reserved and should be set to 0 when writing this register.
15	0 RO	**Asynchronous Schedule Status**: This bit reports the current real status of the Asynchronous Schedule. 0 = Status of the Asynchronous Schedule is disabled. (Default) 1 = Status of the Asynchronous Schedule is enabled. **NOTE:** The Host controller is not required to *immediately* disable or enable the Asynchronous Schedule when software transitions the *Asynchronous Schedule Enable* bit (D29:F7:CAPLENGTH + 20h, bit 5) in the USB2.0_CMD register. When this bit and the *Asynchronous Schedule Enable* bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	0 RO	**Periodic Schedule Status**: This bit reports the current real status of the Periodic Schedule. 0 = Status of the Periodic Schedule is disabled. (Default) 1 = Status of the Periodic Schedule is enabled. **NOTE:** The Host controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit (D29:F7:CAPLENGTH + 20h, bit 4) in the USB2.0_CMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	0 RO	**Reclamation** 0 = This read-only status bit is used to detect an empty asynchronous schedule. The operational model and valid transitions for this bit are described in Section 4 of the EHCI Specification.
12	1 RO	**HCHalted** 0 = This bit is a 0 when the Run/Stop bit is a 1. 1 = The Host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host controller hardware (e.g., internal error). (Default)
11:6	00h RO	Reserved
5	0 R/WC	**Interrupt on Async Advance**: 0=Default. System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the *Interrupt on Async Advance Doorbell* bit (D29:F7:CAPLENGTH + 20h, bit 6) in the USB2.0_CMD register. This bit indicates the assertion of that interrupt source.

Bit	Default and Access	Description
4	0 R/WC	**Host System Error** 0 = No serious error occurred during a host system access involving the Host controller module 1 = The Host controller sets this bit to 1 when a serious error occurs during a host system access involving the Host controller module. A hardware interrupt is generated to the system. Memory read cycles initiated by the EHCI that receive any status other than Successful will result in this bit being set. When this error occurs, the Host controller clears the Run/Stop bit in the USB2.0_CMDregister (D29:F7:CAPLENGTH + 20h, bit 0) to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system (if enabled in the Interrupt Enable Register).
3	0 R/WC	**Frame List Rollover** 0 = No *Frame List Index* rollover from its maximum value to 0. 1 = The Host controller sets this bit to a 1 when the *Frame List Index* (see Section) rolls over from its maximum value to 0. Since the Intel® SCH only supports the 1024-entry Frame List Size, the *Frame List Index* rolls over every time FRNUM13 toggles.
2	0 R/WC	**Port Change Detect**: This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/ disable change and connect status change). Regardless of the implementation, when this bit is readable (i.e., in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the *Port Owner* bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.
1	0 R/WC	**USB Error Interrupt (USBERRINT)** 0 = No error condition. 1 = The Host controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set. See the EHCI specification for a list of the USB errors that will result in this interrupt being asserted.
0	0 R/WC	**USB Interrupt (USBINT)** 0 = No completion of a USB transaction whose Transfer Descriptor had its IOC bit set. No short packet is detected. 1 = The Host controller sets this bit to 1 when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. The Host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

13.3.2.3 USB2.0_INTR—USB 2.0 Interrupt Enable Register

Offset: MEM_BASE + 28h–2Bh Attribute: R/W
Default Value: 00000000h Size: 32 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USB2.0_STS Register to allow the software to poll for events. Each interrupt enable bit description indicates whether it is dependent on the interrupt threshold mechanism (see Section 4 of the EHCI specification), or not.

Bit	Default and Access	Description
31:6	0000000h RO	Reserved. These bits are reserved and should be 0 when writing this register.
5	0 R/W	**Interrupt on Async Advance Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the Interrupt on Async Advance bit (D29:F7:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	0 R/W	**Host System Error Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the Host System Error Status bit (D29:F7:CAPLENGTH + 24h, bit 4) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	0 R/W	**Frame List Rollover Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the Frame List Rollover bit (D29:F7:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	0 R/W	**Port Change Interrupt Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the Port Change Detect bit (D29:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
1	0 R/W	**USB Error Interrupt Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the USBERRINT bit (D29:F7:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBERRINT bit in the USB2.0_STS register.
0	0 R/W	**USB Interrupt Enable** 0 = Disable. 1 = Enable. When this bit is a 1, and the USBINT bit (D29:F7:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBINT bit in the USB2.0_STS register.

13.3.2.4 FRINDEX—Frame Index Register

Offset:	MEM_BASE + 2Ch–2Fh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

The SOF frame number value for the bus SOF token is derived or alternatively managed from this register. Refer to Section 4 of the EHCI specification for a detailed explanation of the SOF value management requirements on the host controller. The value of FRINDEX must be within 125 µs (1 micro-frame) ahead of the SOF token value. The SOF value may be implemented as an 11-bit shadow register. For this discussion, this shadow register is 11 bits and is named SOFV. SOFV updates every 8 micro-frames (1 millisecond). An example implementation to achieve this behavior is to increment SOFV each time the FRINDEX[2:0] increments from 0 to 1.

Software must use the value of FRINDEX to derive the current micro-frame number, both for high-speed isochronous scheduling purposes and to provide the **get** micro-frame number function required to client drivers. Therefore, the value of FRINDEX and the value of SOFV must be kept consistent if chip is reset or software writes to FRINDEX. Writes to FRINDEX must also **write-through** FRINDEX[13:3] to SOFV[10:0]. To keep the update as simple as possible, software should never write a FRINDEX value where the three least significant bits are 111b or 000b.

Note: This register is used by the host controller to index into the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits 12:3 are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index is fixed at 10 for the Intel® SCH since it only supports 1024-entry frame lists. This register must be written as a dword. Word and byte writes produce undefined results. This register cannot be written unless the Host controller is in the Halted state as indicated by the *HCHalted* bit (D29:F7:CAPLENGTH + 24h, bit 12). A write to this register while the Run/Stop bit (D29:F7:CAPLENGTH + 20h, bit 0) is set to a 1 (USB2.0_CMD register) produces undefined results. Writes to this register also effect the SOF value. See Section 4 of the EHCI specification for details.

Bit	Default and Access	Description
31:14	00000h RO	Reserved
13:0	0000h R/W	**Frame List Current Index/Frame Number**: The value in this register increments at the end of each time frame (e.g., micro-frame). Bits 12:3 are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index.

13.3.2.5 CTRLDSSEGMENT—Control Data Structure Segment Register

Offset:	MEM_BASE + 30h–33h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

This 32-bit register corresponds to the most significant address bits 63:32 for all EHCI data structures. Since the Intel® SCH hardwires the 64-bit Addressing Capability field in HCCPARAMS to 1, then this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from either the PERIODICLISTBASE, ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address. This register allows the host software to locate all control data structures within the same 4 GB memory segment.

Bit	Default and Access	Description
31:12	00000h R/W	**Upper Address[63:44]**: Hardwired to 0s. The EHCI is only capable of generating addresses up to 16 terabytes (44 bits of address).
11:0	000h R/W	**Upper Address[43:32]**: This 12-bit field corresponds to address bits 43:32 when forming a control data structure address.

13.3.2.6 PERIODICLISTBASE—Periodic Frame List Base Address Register

Offset:	MEM_BASE + 34h–37h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. Since the Intel® SCH host controller operates in 64-bit mode (as indicated by the 1 in the 64-bit Addressing Capability field in the HCCSPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4 KB aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host controller to step through the Periodic Frame List in sequence.

Bit	Default and Access	Description
31:12	00000h R/W	**Base Address (Low)**: These bits correspond to memory address signals 31:12, respectively.
11:0	000h R/W	Reserved: Must be written as 0s. During runtime, the value of these bits are undefined.

13.3.2.7 ASYNCLISTADDR—Current Asynchronous List Address Register

Offset: MEM_BASE + 38h–3Bh Attribute: R/W
Default Value: 00000000h Size: 32 bits

This 32-bit register contains the address of the next asynchronous queue head to be executed. Since the Intel® SCH host controller operates in 64-bit mode (as indicated by a 1 in 64-bit Addressing Capability field in the HCCPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register (offset 08h). Bits 4:0 of this register cannot be modified by system software and will always return 0s when read. The memory structure referenced by this physical memory pointer is assumed to be 32-byte aligned.

Bit	Default and Access	Description
31:5	0000000h R/W	**Link Pointer Low (LPL)**: These bits correspond to memory address signals 31:5, respectively. This field may only reference a Queue Head (QH).
4:0	0h RO	Reserved: These bits are reserved and their value has no effect on operation.

13.3.2.8 CONFIGFLAG—Configure Flag Register

Offset: MEM_BASE + 60h–63h Attribute: R/W
Default Value: 00000000h Size: 32 bits

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

Bit	Default and Access	Description
31:1	00000000h RO	Reserved. Read from this field will always return 0.
0	0 R/W	**Configure Flag (CF)**: Host software sets this bit as the last action in its process of configuring the Host controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. See Section 4 of the EHCI spec for operation details. Port routing control logic default-routes each port to the UHCIs (default). Port routing control logic default-routes all ports to this host controller.

13.3.2.9 PORT[7:0]SC—Port N Status and Control Register

Offset:	PORT0SC:	MEM_BASE + 64h–67h	
	PORT1SC:	MEM_BASE + 68h–6Bh	
	PORT2SC:	MEM_BASE + 6Ch–6Fh	
	PORT3SC:	MEM_BASE + 70h–73h	
	PORT4SC:	MEM_BASE + 74h–77h	
	PORT5SC:	MEM_BASE + 78h–7Bh	
	PORT6SC:	MEM_BASE + 7Ch–7Fh	
	PORT7SC:	MEM_BASE + 80h–83h	
Attribute:	R/W, R/WC, RO		
Default Value:	00003000h	Size:	32 bits

A host controller must implement one or more port registers. Software uses the N_PORTS information from the Structural Parameters Register to determine how many ports need to be serviced. All ports have the structure defined below. Software must not write to unreported Port Status and Control Registers.

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No device connected
- Port disabled

When a device is attached, the port state transitions to the attached state and system software will process this as with any status change notification. Refer to Section 4 of the EHCI specification for operational requirements for how change events interact with port suspend mode.

Bit	Default and Access	Description
31:23	0000h RO	Reserved. These bits are reserved for future use and will return a value of 0s when read.
22	0 R/W	**Wake on Overcurrent Enable (WKOC_E)**: 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the overcurrent Active bit (bit 4 of this register) is set.
21	0 R/W	**Wake on Disconnect Enable (WKDSCNNT_E)**: 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1-to-0).
20	0 R/W	**Wake on Connect Enable (WKCNNT_E)**: 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0-to-1).

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>19:16</td><td>0h
R/W</td><td>Port Test Control (PTC): When this field is 0s, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b – 1111b are reserved):

<table>
<tr><th>Value</th><th>Maximum Interrupt Interval</th></tr>
<tr><td>0000b</td><td>Test mode not enabled (default)</td></tr>
<tr><td>0001b</td><td>Test J_STATE</td></tr>
<tr><td>0010b</td><td>Test K_STATE</td></tr>
<tr><td>0011b</td><td>Test SE0_NAK</td></tr>
<tr><td>0100b</td><td>Test Packet</td></tr>
<tr><td>0101b</td><td>FORCE_ENABLE</td></tr>
</table>
Refer to USB Specification Revision 2.0, Chapter 7 for details on each test mode.</td></tr>
<tr><td>15:14</td><td>00b
RO</td><td>Reserved</td></tr>
<tr><td>13</td><td>1
R/W</td><td>Port Owner (PO): Default = 1b. This bit unconditionally goes to a 0 when the Configured Flag bit in the USB2.0_CMD register makes a 0 to 1 transition.
System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.</td></tr>
<tr><td>12</td><td>1
RO</td><td>Port Power (PP): Read-only with a value of 1. This indicates that the port does have power.</td></tr>
<tr><td>11:10</td><td>00b
RO</td><td>Line Status (LS): These bits reflect the current logical levels of the D+ (bit 11) and D– (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is 0 and the current connect status bit is set to a 1.
00 = SE0
10 = J-state
01 = K-state
11 = Undefined. Not low speed device, perform EHCI reset.</td></tr>
<tr><td>9</td><td>0
RO</td><td>Reserved. This bit will return a 0 when read.</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>8</td><td>0
R/W</td><td>Port Reset (PR): Default = 0. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0.
1 = Port is in Reset.
0 = Port is not in Reset.

NOTE: When software writes a 0 to this bit, there may be a delay before the bit status changes to a 0. The bit status will not read as a 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g., set the Port Enable bit to a 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from 0-to-1.

For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2 ms of software writing this bit to a 0. The HCHalted bit (D29:F7:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register should be a 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a 1. This bit is 0 if Port Power is 0.

NOTE: System software should not attempt to reset a port if the HCHalted bit in the USB2.0_STS register is a 1. Doing so will result in undefined behavior.</td></tr>
<tr><td>7</td><td>0
R/W</td><td>Suspend (SUS)
0 = Port not in suspend state.(Default)
1 = Port in suspend state.
Port Enabled Bit and Suspend bit of this register define the port states as follows:

<table>
<tr><th>Port Enabled</th><th>Suspend</th><th>Port State</th></tr>
<tr><td>0</td><td>X</td><td>Disabled</td></tr>
<tr><td>1</td><td>0</td><td>Enabled</td></tr>
<tr><td>1</td><td>1</td><td>Suspend</td></tr>
</table>
When in suspend state, downstream propagation of data is blocked on this port, except for port reset. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port depending on the activity on the port.
The host controller will unconditionally set this bit to a 0 when software sets the Force Port Resume bit to a 0 (from a 1). A write of 0 to this bit is ignored by the host controller.
If host software sets this bit to a 1 when the port is not enabled (i.e., Port enabled bit is a 0) the results are undefined.</td></tr>
</table>

Bit	Default and Access	Description
6	0 R/W	**Force Port Resume(FPR)** 0 = No resume (K-state) detected/driven on port. (Default) 1 = Resume detected/driven on port. Software sets this bit to a 1 to drive resume signaling. The Host controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the Port Change Detect bit (D29:F7:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the Port Change Detect bit. **NOTE:** When the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification, Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a 1. Software must appropriately time the Resume and set this bit to a 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to the high-speed idle.
5	0 R/WC	**Overcurrent Change (OCC)**: The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
4	0 RO	**Overcurrent Active (OCA)** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the over current condition is removed. The Intel® SCH automatically disables the port when the overcurrent active bit is 1.
3	0 R/WC	**Port Enable/Disable Change (PEDC)**: For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. 0 = No change in status. (Default). 1 = Port enabled/disabled status has changed.
2	0 R/W	**Port Enabled/Disabled (PED)**: Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. **Note** that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable 1 = Enable (Default)

Bit	Default and Access	Description
1	0 R/WC	**Connect Status Change (CSC)**: This bit indicates a change has occurred in the port's Current Connect Status. Software sets this bit to 0 by writing a 1 to it. 0 = No change (Default). 1 = Change in Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (i.e., the bit will remain set).
0	0 RO	**Current Connect Status (CCS)**: This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

13.3.3 USB 2.0 Based Debug Port Register

The Debug port's registers are located in the same memory area, defined by the Base Address Register (MEM_BASE), as the standard EHCI registers. The base offset for the debug port registers (A0h) is declared in the Debug Port Base Offset Capability Register at Configuration offset 5Ah (D29:F7:offset 5Ah). The address map of the Debug Port registers is shown in Table 39.

Table 39. Debug Port Register Address Map

MEM_BASE + Offset	Mnemonic	Register Name	Default	Type
A0–A3h	CNTL_STS	Control/Status	00000000h	R/W, R/WC, RO, WO
A4–A7h	USBPID	USB PIDs	00000000h	R/W, RO
A8–ABh	DATABUF[3:0]	Data Buffer (Bytes 3:0)	00000000h	R/W
AC–AFh	DATABUF[7:4]	Data Buffer (Bytes 7:4)	00000000h	R/W
B0–B3h	CONFIG	Configuration	00007F01h	R/W

NOTES:
1. All of these registers are implemented in the core well and reset by RESET#, EHCI HCRESET, and a EHCI D3-to-D0 transition.
2. The hardware associated with this register provides no checks to ensure that software programs the interface correctly. How the hardware behaves when programmed in an invalid manner is undefined.

13.3.3.1 CNTL_STS—Control/Status Register

Offset: MEM_BASE + A0h Attribute: R/W, R/WC, RO, WO
Default Value: 0000h Size: 32 bits

Bit	Default and Access	Description
31	RO	Reserved
30	R/W	**OWNER_CNT** 0 = Ownership of the debug port is NOT forced to the EHCI controller (Default) 1 = Ownership of the debug port is forced to the EHCI controller (i.e., immediately taken away from the companion Classic USB Host controller) If the port was already owned by the EHCI controller, then setting this bit has no effect. This bit overrides all of the ownership-related bits in the standard EHCI registers.
29	RO	Reserved
28	R/W	**ENABLED_CNT** 0 = Software can clear this by writing a 0 to it. The hardware clears this bit for the same conditions where the Port Enable/Disable Change bit (in the PORTSC register) is set. (Default) 1 = Debug port is enabled for operation. Software can directly set this bit if the port is already enabled in the associated PORTSC register (this is enforced by the hardware).
27:17	RO	Reserved
16	R/WC	**DONE_STS**: Software can clear this by writing a 1 to it. 0 = Request Not complete 1 = Set by hardware to indicate that the request is complete.
15:12	RO	**LINK_ID_STS**: This field identifies the link interface. 0h = Hardwired. Indicates that it is a USB Debug Port.
11	RO	Reserved. This bit returns 0 when read. Writes have no effect.
10	R/W	**IN_USE_CNT**: Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software. This bit is cleared after reset. (This bit has no effect on hardware.)
9:7	RO	**EXCEPTION_STS**: This field indicates the exception when the ERROR_GOOD#_STS bit is set. This field should be ignored if the ERROR_GOOD#_STS bit is 0. 000 = No Error. (Default) **NOTE**: This should not be seen, since this field should only be checked if there is an error. 001 = Transaction error: indicates the USB 2.0 transaction had an error (CRC, bad PID, timeout, etc.) 010 = Hardware error. Request was attempted (or in progress) when port was suspended or reset. All Other combinations are reserved

Bit	Default and Access	Description
6	RO	**ERROR_GOOD#_STS** 0 = Hardware clears this bit to 0 after the proper completion of a read or write. (Default) 1 = Error has occurred. Details on the nature of the error are provided in the Exception field.
5	WO R/W	**GO_CNT — WO** 0 = Hardware clears this bit when hardware sets the DONE_STS bit. (Default) 1 = Causes hardware to perform a read or write request. **NOTE:** Writing a 1 to this bit when it is already set may result in undefined behavior.
4	0 R/W	**WRITE_READ#_CNT**: Software clears this bit to indicate that the current request is a read. Software sets this bit to indicate that the current request is a write. 0 = Read (Default) 1 = Write
3:0	R/W	**DATA_LEN_CNT**: This field is used to indicate the size of the data to be transferred. default = 0h. For write operations, this field is set by software to indicate to the hardware how many bytes of data in Data Buffer are to be transferred to the console. A value of 0h indicates that a zero-length packet should be sent. A value of 1–8 indicates 1–8 bytes are to be transferred. Values 9–Fh are invalid and how hardware behaves if used is undefined. For read operations, this field is set by hardware to indicate to software how many bytes in Data Buffer are valid in response to a read operation. A value of 0h indicates that a zero length packet was returned and the state of Data Buffer is not defined. A value of 1–8 indicates 1–8 bytes were received. Hardware is not allowed to return values 9–Fh. The transferring of data always starts with byte 0 in the data area and moves toward byte 7 until the transfer size is reached.

NOTES:
1. Software should do Read-Modify-Write operations to this register to preserve the contents of bits not being modified. This include Reserved bits.
2. To preserve the usage of RESERVED bits in the future, software should always write the same value read from the bit until it is defined. Reserved bits will always return 0 when read.

13.3.3.2 USBPID—USB PIDs Register

Offset: MEM_BASE + A4h Attribute: R/W, RO
Default Value: 0000h Size: 32 bits

This DWORD register is used to communicate PID information between the USB debug driver and the USB debug port. The debug port uses some of these fields to generate USB packets, and uses other fields to return PID information to the USB debug driver.

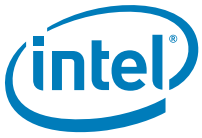
Bit	Default and Access	Description
31:24	00h RO	Reserved: These bits will return 0 when read. Writes will have no effect.
23:16	00h RO	**RECEIVED_PID_STS**: Hardware updates this field with the received PID for transactions in either direction. When the controller is writing data, this field is updated with the handshake PID that is received from the device. When the host controller is reading data, this field is updated with the data packet PID (if the device sent data), or the handshake PID (if the device NAKs the request). This field is valid when the hardware clears the GO_DONE#_CNT bit.
15:8	00h R/W	**SEND_PID_CNT:** Hardware sends this PID to begin the data packet when sending data to USB (i.e., WRITE_READ#_CNT is asserted). Software typically sets this field to either DATA0 or DATA1 PID values.
7:0	00h R/W	**TOKEN_PID_CNT**: Hardware sends this PID as the Token PID for each USB transaction. Software typically sets this field to either IN, OUT, or SETUP PID values.

13.3.3.3 DATABUF[7:0]—Data Buffer Bytes [7:0] Register

Offset: MEM_BASE + A8h–AFh Attribute: R/W
Default Value: 0000000000000000h Size: 64 bits

This register can be accessed as 8 separate 8-bit registers or 2 separate 32-bit register.

Bit	Default and Access	Description
63:0	0s R/W	**DATABUFFER[63:0]**: This field is the 8 bytes of the data buffer. Bits 7:0 correspond to least significant byte (byte 0). Bits 63:56 correspond to the most significant byte (byte 7). The bytes in the Data Buffer must be written with data before software initiates a write request. For a read request, the Data Buffer contains valid data when DONE_STS bit (offset A0, bit 16) is cleared by the hardware, ERROR_GOOD#_STS (offset A0, bit 6) is cleared by the hardware, and the DATA_LENGTH_CNT field (offset A0, bits 3:0) indicates the number of bytes that are valid.

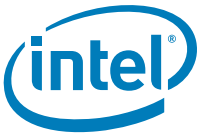


13.3.3.4 CONFIG—Configuration Register

Offset: MEM_BASE + B0–B3h Attribute: R/W
Default Value: 00007F01h Size: 32 bits

Bit	Default and Access	Description
31:15	0000h RO	Reserved
14:8	7Fh R/W	**USB_ADDRESS_CNF**: The USB device address used by the controller for all Token PID generation.
7:4	0h RO	Reserved
3:0	1h R/W	**USB_ENDPOINT_CNF**: This 4-bit field identifies the endpoint of all Token PIDs.

§ §



14 USB Client Controller (D26:F0)

The Intel® SCH USB Client implements a software defined USB device. This allows a platform based on the Intel® SCH chipset to connect to other platforms implementing a USB Host interface for purposes of file transfer, network connectivity, or any other functionality that can be implemented as a USB Device.

This USB Client implementation provides very little hardware acceleration or assistance, and is optimized for flexibility and hardware simplicity. Software is responsible for almost all behaviors above the USB protocol layer and DMA, including handling USB Descriptors, Transaction level formatting, and implementing defined Device Classes.

14.1 Functional Description

The Intel® SCH contains a Universal Serial Bus 2.0 client controller. The USB client is configured to operate on USB port 2.

The serial information transmitted and received by the USB Client contains layers of communication protocols. These communication protocols are defined by *Universal Serial Bus Specification*, *Revision 2.0*. The most basic of these protocols are defined within fields. Examples of these USB fields include: Sync, Packet Identifier, Address, Endpoint, Frame Number, Data, and CRC.

Fields are used to produce *packets*. Depending on the packet function, a different combination and number of fields can be used. Packet types include: Token, Data, and Handshake. Token packets may be of several types including Start of Frame, and PING (high-speed).

Packets are assembled to produce *transactions*. Transactions fall into six groups: Data In, Data Out, SOF, Setup, Status and Ping (HS). Data flow is relative to the USB host controller. In packets represent data flow from the USB Client to the USB host controller. Out packets represent data flow from the USB host controller to the USB Client. SOF transactions signify the start of a new frame. Setup and Status transactions are used for control transfers. Ping transactions are used in high-speed mode to assist with bulk transfers.

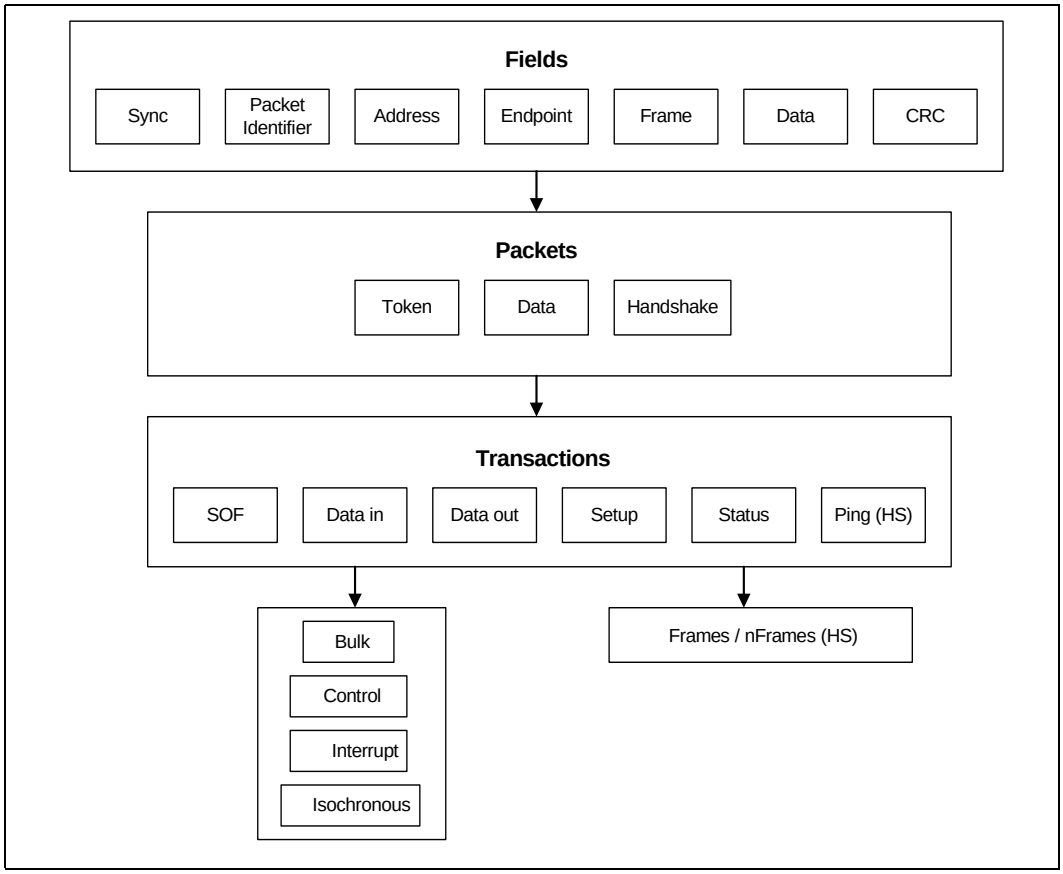
Some sets of transactions together make up *transfers* and are used to transfer data between the host and device. Transfers fall into four groups: bulk, control, interrupt, and isochronous. SOF and PING transactions are not components of transfers. The term *transfer* may refer to a set of related data transfer transactions within a single frame/μframe (HS) such as for a bulk transfer which may transfer an amount of data split into many packets of related data within a single frame/μframe (HS), or it may refer to related data transferred across several frames/μframes (HS), such as for an interrupt transfer.

Transactions are strung together into *frames* for low-speed and full-speed operation modes, or *μframes* during high-speed mode. While a transfer refers to transactions with related data, but not necessarily in any specific order, frames and μframes represent a series of transactions put together in the order which will be observed on the USB bus, but not necessarily having related data.

Figure 6 graphically represents the communication layers in the protocol. See *Universal Serial Bus Specification*, Revision 2.0 for more details on USB protocol.

The USB host controller referenced in this chapter refers to any *Universal Serial Bus Specification*-compliant USB host controller.

Figure 6. Communication Protocol Layers in the USB Client Controller



Software is responsible for handling all transactions, including Setup transactions, with the exception of the SET_ADDRESS transaction. In contrast to other hardware designs available in the industry which may rely on hardware to handle USB interface descriptor requests and Property Get/Set operations, the Intel® SCH USB Client relies on software to handle these operations. Software must, in a timely manner, process all packets received on OUT endpoints, and where required provide the requested data through the appropriate IN endpoint.

14.2 Operation

The Intel® SCH USB Client device is constructed of a series of endpoints which use DMA engines to transfer data between the USB controller and memory. Endpoints 0_IN and 0_OUT are always implemented as the Default Control endpoint and represent the default way that the host software communicates with the device to determine capabilities, configure options, and select interfaces.

The Intel® SCH supports six other end points, known as 1_IN, 1_OUT, 2_IN, 2_OUT, 3_IN, and 3_OUT. These additional endpoints may be configured as needed, such as a set of Bulk In and Bulk Out endpoints, to facilitate data transfer. As an example, a Communications Class device will use the Endpoint 0 In and Out as a control pipe, and Endpoint 1_IN and 1_OUT as a Data Class pipe to transfer packets.

DMA engines are associated with the endpoints which transfer the data being transferred to or from the Host from the Client system RAM. The DMA engine for a particular endpoint must be configured before data can be exchanged with the host.

Transfers (exchanges between client and host) are comprised of zero to many Data packets which contain a number of bytes equal to the Max Packet Size, and a last packet containing fewer bytes (including zero-length packets) known as a Short Packet. For instance, to transfer a 1500-byte Ethernet frame, a Client may provide a 1024-byte packet followed by a 478-byte Short Packet. In many interface class definition, the receiver implicitly understands that the Transfer is complete when it sees the Short packet.

In other usage models (such as streaming video) the stream may simply be a large number of bytes, where the transfer framing information is contained within the data format itself. A Bulk In endpoint may be used to send available bytes when the host asks for them.

Packets are made of individual phases.

Different phases and Token types to different endpoint types:

- Control Endpoint use SETUP PID, DATA0/1 phases, and ACK phase
- Bulk Endpoints use IN/OUT PID, DATA0/1 phases, and ACK phase
- Isoch Endpoints use IN/OUT PID and DATA0 phases only
- Interrupt Endpoints use IN/OUT PID, DATA0/1 Phases, and ACK phase.

Important hardware requirements:

- Hardware must identify destination by matching packet address on packet and handling based on endpoint address and direction.
- Hardware must handle DATA0/1 toggling for Control, Interrupt, and Bulk endpoints
- Hardware must generate (IN) or check (OUT) CRC of packet (except in Control DMA Mode)
- Hardware must handle the SOF token by placing the Frame number in the Frame register
- Hardware must detect short packets
- Hardware must ACK packets received properly, and NAK packets with errors
- Hardware must NAK packets if there is no data to send or no room in the receive buffer
- Hardware must detect bus conditions, such as Suspend, Resume, and Reset, and report the conditions to the software.

14.2.1 USB Features

- USB Revision 2.0, high-speed/full-speed compliant device
- Eight, concurrent programmable endpoints
  - — Programmable endpoint type: bulk, isochronous, or interrupt
  - — Programmable endpoint maximum packet size
  - — 4 ‘IN’ Endpoints, and 4 ‘OUT’ endpoints
  - — Interface and endpoint requests handled entirely by software
  - — 1 IN and 1 OUT endpoint used as EP0 Control Pipe
  - — Automatic hardware handling of SET_ADDRESS

14.2.2 DMA Features

- Supports aligned and unaligned transfers to and from system memory.
- Supports 4 IN (client memory to USB) and 4 OUT (USB to client memory) Endpoints.
- Supports Control, Linear, and Scatter Gather modes of operation to allow efficient use of client system memory.
- Retrieves trailing bytes in the receive endpoint FIFOs.
- Supports up to 4 GBytes of data transfer per descriptor. Packets longer than the defined Max Packet Size are automatically transferred as multiple packets.
- Control Mode DMA supports placing all packet information (including PID) from a single transaction in the DMA buffer
- Linear and Scatter/Gather DMA modes for OUT/IN endpoints place/fetch the DATA phase of multiple USB transactions to/from the same endpoint linearly in memory to optimize lengthy transfers.
- Automatic NAK support for endpoints which do not yet have data ready.

14.2.3 Reset

The USB client port may be reset by either a Device Reset message from the Intel® SCH's internal message bus or using a USB Reset packet from the USB host.

14.2.4 PCI Device Reset

Clear all MMIO registers to reset values, flush FIFO, and initialize all state machines to their power on condition.

On the USB bus, if the Client is currently connected to the USB host, the Client signal disconnect/reconnect

14.2.5 Wake of Client

The Intel® SCH USB client does not issue PME# interrupts which would wake the system from a sleep state.

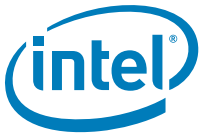
14.2.6 Wake of Host (USB Resume)

The Dev_CTRL.SignalResume bit allows the Client device to signal Resume to the Host while the link is in the Suspend state. This may allow the client to bring the host to S0, or merely resume a link suspended for power reasons.

Before software sets this bit, it must make sure that the client has been enabled to signal wake. The Host OS will write a 1 to the "Remote Wakeup" bit in the bmAttributes field of the Standard Configuration Descriptor to signal that the client may generate Resume signaling. Software must also make sure that the Link has been in the Suspend state for at least 5 ms, per USB spec requirements. Software may determine that more than 5 ms has elapsed by monitoring the SUSPEND bit in the Device Status register.

When software writes a 1 to this bit, hardware will generate resume signaling on the link if the link is in the Suspend state. Software is responsible for knowing whether the device has been enabled to generate the signaling by the Host system, and for ensuring that the link has been in the Suspend state for the 5-ms minimum, per *USB 2.0 Specification,* Section 7.1.7.7.

Hardware is responsible for asserting the resume signaling on the link for the requisite amount of time. When the resume signaling is completed, hardware will clear this bit to a 0. While resume signaling is enabled, software writes to this bit will be ignored.



14.3 PCI Configuration Registers

Table 40. USB Client Controller PCI Register Address Map (D26:F0)

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	8118h	RO
04–05h	PCICMD	PCI Command	0000h	R/W, RO
06–07h	PCISTS	PCI Status	0010h	RO
08h	RID	Revision Identification	See **Note**	RO
09h–0Bh	CC	Class Codes	0C0380h	RO
0Eh	HTYPE	Header Type	00h	RO
10–13h	MEM_BASE	Memory Base Address	00000000h	RO, R/W
2C–2Fh	SS	Subsystem Identification	00000000h	R/W
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INT_LN	Interrupt Line	00h	RO
3Dh	INT_PN	Interrupt Pin	see description	R/W
40h	USBPR	USB Port Routing	02h	RO, R/W
50h	PM_CAPID	PCI Power Management Capability ID	01h	RO
51h	NXT_PTR	Next Item Pointer	00h	RO
52h–53h	PM_CAP	Power Management Capabilities	0000h	RO
54h–55h	PM_CNTL_STS	Power Management Control/ Status	00000000h	RO, R/W
C4h	URE	USB Resume Enable	00h	RO, R/W
FCh	FD	Function Disable	00000000h	RO, R/W

NOTE: Address locations that are not shown should be treated as Reserved.

14.3.1 VID—Vendor Identification Register

Offset Address: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Default and Access	Description
15:0	8086 RO	**Vendor ID:** This is a 16-bit value assigned to Intel.

14.3.2 DID—Device Identification Register

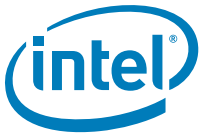
Offset Address: 02h–03h Attribute: RO
Default Value: 8118h Size: 16 bits

Bit	Default and Access	Description
15:0	8118h RO	**Device ID:** 8118h assigned to the USB client controller in the Intel® SCH.

14.3.3 PCICMD—PCI Command Register

Address Offset: 04h–05h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:11	0 RO	Reserved
10	0 R/W	**Interrupt Disable (ID)** 0 = The function is capable of generating interrupts. 1 = The function cannot generate its interrupt to the interrupt controller and it may not generate an MSI. **Note** that the corresponding Interrupt Status bit (PCISTS, bit 3) is not affected by the interrupt enable.
9	0 RO	Reserved
2	0 R/W	**Bus Master Enable (BME)** 0 = Disables this functionality. 1 = Enables the USB client to generate bus master cycles. It also controls MSI generation since MSI are essentially memory writes.
1	0 R/W	**Memory Space Enable (MSE):** This bit controls access to the USB 2.0 Memory Space registers. 0 = Disables this functionality. 1 = Enables accesses to the USB 2.0 registers. The Base Address register (D29:F7:10h) for USB 2.0 should be programmed before this bit is set.
0	0 RO	Reserved



14.3.4 PCISTS—PCI Status Register

Address Offset: 06h–07h Attribute: R/W, RO
Default Value: 0010h Size: 16 bits

Bit	Default and Access	Description
15:5	0 RO	Reserved
4	1 RO	**Capabilities List (CAP_LIST):** Hardwired to 1 indicating that the USB client controller contains a capabilities pointer list at offset 34h.
3	0 RO	**Interrupt Status:** This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = This bit will be 0 when the interrupt is cleared 1 = This bit is a 1 when the interrupt is asserted The value reported in this bit is independent of the value in the Interrupt Disable (ID) bit in the PCICMD register.
2:0	0 RO	Reserved

14.3.5 RID—Revision Identification Register

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Revision ID:** Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the value of the Revision ID Register.

14.3.6 CC—Class Codes Register

Address Offset: 09h–0Bh Attribute: RO
Default Value: 0C0380h Size: 24 bits

Bit	Default and Access	Description
23:16	0Ch RO	**Base Class Code (BCC):** This register indicates that the function implements a Serial Bus Controller device.
15:8	03h RO	**Sub Class Code (SCC):** Indicates that the Programming Interface is 'Not a Host', i.e., it's not EHCI, UHCI, or OHCI.
7:0	80h RO	**Programming Interface (PI):** Universal Serial Bus with no specific programming interface.

14.3.7 HTYPE - Header Type Register

Address Offset: 0E Attribute: RO
Default Value: 00h Size: 8 bits

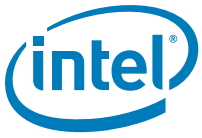
Bit	Default and Access	Description
7:0	00h RO	**Header Type (HTYPE):** Implements a Type 0 Configuration header.

14.3.8 MEM_BASE— USB Client Memory Base Address Register

Address Offset: 10h–17h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

This base address register creates 2048 bytes of memory space to signify the base address of USB Client memory mapped configuration registers.

Bit	Default and Access	Description
63:32	0s RW	**Upper Address (UA):** Upper 32 bits of the Base address for the USB Client controller's memory mapped configuration registers. This may be Read-Only 0's if 64b address decode is not supported.
31:11	0s R/W	**Lower Address (LA):** Base address for the USB Client controller's memory mapped configuration registers. 2048 bytes are requested by hardwiring bits 10:4 to 0s.
10:4	0s RO	Reserved
3	0 RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	10 RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64 bit address space. Note that this needs to be adjusted if the USBCBARU is implemented as Read Only to indicate that 64b address decode is not supported.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space



14.3.9 SID—Subsystem ID Register

Address Offset: 2Ch–2Fh Attribute: R/W
Default Value: 00000000h Size: 32 bits

This register matches the value written to the LPC bridge.

Bit	Default and Access	Description
31:15	0000h RW	**Subsystem ID (SSID):** These RW bits have no hardware functionality.
15:0	0000h RW	**Subsystem Vendor ID (SVID):** These RW bits have no hardware functionality.

14.3.10 CAP_PTR—Capabilities Pointer Register

Address Offset: 34h Attribute: RO
Default Value: 50h Size: 8 bits

Bit	Default and Access	Description
7:0	50h RO	**Capability Pointer (CP):** Indicates that the first capability pointer offset is offset 50h

14.3.11 INT_LN—Interrupt Line Register

Address Offset: 3Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Interrupt Line (INT_LN):** This data is not used by the Intel® SCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

14.3.12 INT_PN—Interrupt Pin Register

Address Offset: 3Dh Attribute: RO
Default Value: See Description Size: 8 bits

Bit	Default and Access	Description
7:4	0h RO	Reserved
3:0	RO	**Interrupt Pin:** This reflects the value of D26IP.UTIP (Chipset Config Registers:Offset 3114, bits 3:0).

14.3.13 USBPR—USB Port Routing Register

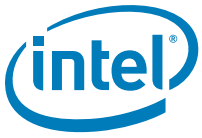
Address Offset: 40h Attribute: RO
Default Value: 02h Size: 8 bits

Bit	Default and Access	Description
7	0 R/W	**EnablePortRouting** 0 = USB port 2 will be routed to the USB host controller 1 = USB port 2 will be routed to the USB client controller
6	0 R/W	**ForcePortRouting** 1 = The USB port indicated by PID will always be routed to the USB Client controller, regardless of the state of the external ID pin. 0 = The USB port indicated by PID will be routed to the USB controller only when the input GPIOSUS3 is set to a 1. If is set to 0 and there is a 0 at the GPIOSUS3 input, the USB Client controller will consider the port disconnected.
5:4	00b RO	Reserved
3:0	02h R/W	**Port ID (PID):** Denotes the binary encoding of the port number to be configured as a client. Port 2 is the default. All other values are reserved.

14.3.14 PM_CAPID—PCI Power Management Capability ID Register

Address Offset: 50h Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Default and Access	Description
7:0	01h RO	**Power Management Capability ID:** A value of 01h indicates that this is a PCI Power Management capabilities field.



14.3.15 NXT_PTR—Next Item Pointer Register

Address Offset: 51h Attribute: R/W (special)
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Next Item Pointer 1 Value (NXT_PTR1):** This register indicates that this is the last capability in the list.

14.3.16 PM_CAP—Power Management Capabilities Register

Address Offset: 52h–53h Attribute: R/W (special), RO
Default Value: 0002h Size: 16 bits

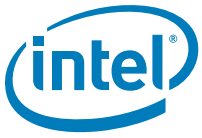
Bit	Default and Access	Description
15:11	11001b RO	**PME Support (PME_SUP):** Indicates PME# can be generated from only D0 states.
10	0b RO	**D2_Support:** The D2 state is not supported.
9	0b RO	**D1_Support:** The D1 state is not supported.
8:6	000b RO	**Auxiliary Current (AUX_CUR) (special):** Reports 0mA maximum Suspend well current required when in the D3 cold state.
5	0 RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0 RO	Reserved
4	0 RO	**PME Clock (PMEC):** Does not apply. Hardwired to 0.
2:0	010b RO	**Version (VER):** Indicates that it complies with Revision 1.1 of the *PCI Power Management Specification*.

14.3.17 PM_CNTL_STS—Power Management Control/Status Register

Address Offset: 54h–55h Attribute: R/W, RO
Default Value: 00000000h Size: 32bits

Bit	Default and Access	Description
31:24	00h RO	**Data:** No data
23	0b RO	**Bus Power/Clock Control Enable (BPCCE):** Does not apply. Hardwired to 0.
22	0b RO	**B2/B3 Support (B23):** Does not apply. Hardwired to 0.
21:2	0...0b RO	Reserved
1:0	00b R/W	Power State (PS): This field is used both to determine the current power state of the USB Client controller and to set a new power state. The values are: 00 = D0 state 01 = Reserved 10 = Reserves 11 = $D3_{HOT}$ state When in $D3_{HOT}$, the USB Client controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from $D3_{HOT}$ to D0, an internal warm (soft) reset is generated, and software must re-initialize the function.

NOTE: Reset (bits 15, 8): suspend well, and not D3-to-D0 warm reset nor core well reset.



14.3.18 URE—USB Resume Enable

Address Offset: C4h Attribute: R/W, RO
Default Value: 00000000h Size: 32bits

Bit	Default and Access	Description
7:1	0s RO	Reserved
0	0b R/W	**Port 0 Enable (P0E):** When set, UHC monitors port 0 for wakeup and connect/disconnect events.

14.3.19 FD—Function Disable Register

Address Offset: FCh Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:3	0000h RO	Reserved
2	0 R/W	**Clock Gating Disable (CGD):** When set, clock gating within the function is disabled. When cleared, clock gating within the function is enabled.
1	0 RO	Reserved
0	0 R/W	**Disable (D):** When set, the function is disabled (configuration space is disabled).

14.4 Memory-Mapped I/O Registers

Table 41. USB Client I/O Registers (Sheet 1 of 2)

MEM_BASE + Offset	Mnemonic	Register	Default	Type
000–003h	GCAP	Global Capabilities	4007000h	RO
100–103h	DEV_STS	Device Status	00000000h	RO
104–107h	FRAME	Frame Number	00000000h	RO
10C–10Fh	INT_STS	Interrupt Status	00000000h	RO, R/WC
110–113h	INT_CTRL	Interrupt Control	00000000h	RO, R/W
000–003h	GCAP	Global Capabilities	4007000h	RO
100–103h	DEV_STS	Device Status	00000000h	RO
104–107h	FRAME	Frame Number	00000000h	RO
10C–10Fh	INT_STS	Interrupt Status	00000000h	RO, R/WC
110–113h	INT_CTRL	Interrupt Control	00000000h	RO, R/W
114–117h	DEV_CTRL	Device Control	00000000h	RO, R/W
200–207h 220–227h 240–247h 260–267h 280–287h 2A0–2A7h 2C0–2C7h 2E0–2E7h	EP0IB EP0OB EP1IB EP1OB EP2IB EP2OB EP3IB EP3OB	Endpoint 0 IN Base Endpoint 0 OUT Base Endpoint 1 IN Base Endpoint 1 OUT Base Endpoint 2 IN Base Endpoint 2 OUT Base Endpoint 3 IN Base Endpoint 3 OUT Base	00000000 00000000h	RO, R/W
208–209h 228–229h 248–249h 268–269h 288–289h 2A8–2A9h 2C8–2C9h 2E8–2E9h	EP0IL EP0OL EP1IL EP1OL EP2IL EP2OL EP3IL EP3OL	Endpoint 0 IN Length Endpoint 0 OUT Length Endpoint 1 IN Length Endpoint 1 OUT Length Endpoint 2 IN Length Endpoint 2 OUT Length Endpoint 3 IN Length Endpoint 3 OUT Length	0000h	R/W
20A–20Bh 22A–22Bh 24A–24Bh 26A–26Bh 28A–28Bh 2AA–2ABh 2CA–2CBh 2EA–2EBh	EP0IPB EP0OPB EP1IPB EP1OPB EP2IPB EP2OPB EP3IPB EP3OPB	Endpoint 0 IN Position in Buffer Endpoint 0 OUT Position in Buffer Endpoint 1 IN Position in Buffer Endpoint 1 OUT Position in Buffer Endpoint 2 IN Position in Buffer Endpoint 2 OUT Position in Buffer Endpoint 3 IN Position in Buffer Endpoint 3 OUT Position in Buffer	0000h	RO, WC
20C–20Dh 22C–22Dh 24C–24Dh 26C–26Dh 28C–28Dh 2AC–2ADh 2CC–2CDh 2EC–2EDh	EP0IDL EP0ODL EP1IDL EP1ODL EP2IDL EP2ODL EP3IDL EP3ODL	Endpoint 0 IN Descriptor in List Endpoint 0 OUT Descriptor in List Endpoint 1 IN Descriptor in List Endpoint 1 OUT Descriptor in List Endpoint 2 IN Descriptor in List Endpoint 2 OUT Descriptor in List Endpoint 3 IN Descriptor in List Endpoint 3 OUT Descriptor in List	0000h	RO, WC

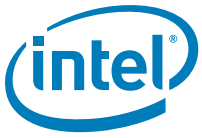


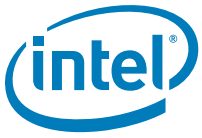
Table 41. USB Client I/O Registers (Sheet 2 of 2)

MEM_BASE +Offset	Mnemonic	Register	Default	Type
20E–20Fh 22E–22Fh 24E–24Fh 26E–26Fh 28E–28Fh 2AE–2AFh 2CE–2CFh 2EE–2EFh	EP0ITQ EP0OTQ EP1ITQ EP1OTQ EP2ITQ EP2OTQ EP3ITQ EP3OTQ	Endpoint 0 IN Transfer in Queue Endpoint 0 OUT Transfer in Queue Endpoint 1 IN Transfer in Queue Endpoint 1 OUT Transfer in Queue Endpoint 2 IN Transfer in Queue Endpoint 2 OUT Transfer in Queue Endpoint 3 IN Transfer in Queue Endpoint 3 OUT Transfer in Queue	0000h	RO, WC
210–211h 230–231h 250–251h 270–271h 290–291h 2B0–2B1h 2D0–2D1h 2F0–2F1h	EP0IMPS EP0OMPS EP1IMPS EP1OMPS EP2IMPS EP2OMPS EP3IMPS EP3OMPS	Endpoint 0 IN Max Packet Size Endpoint 0 OUT Max Packet Size Endpoint 1 IN Max Packet Size Endpoint 1 OUT Max Packet Size Endpoint 2 IN Max Packet Size Endpoint 2 OUT Max Packet Size Endpoint 3 IN Max Packet Size Endpoint 3 OUT Max Packet Size	0040h	RO, R/W
212–213h 232–233h 252–253h 272–273h 292–293h 2B2–2B3h 2D2–2D3h 2F2–2F3h	EP0IS EP0OS EP1IS EP1OS EP2IS EP2OS EP3IS EP3OS	Endpoint 0 IN Status Endpoint 0 OUT Status Endpoint 1 IN Status Endpoint 1 OUT Status Endpoint 2 IN Status Endpoint 2 OUT Status Endpoint 3 IN Status Endpoint 3 OUT Status	0000h	RO, R/WC
214–214h 234–234h 254–254h 274–274h 294–294h 2B4–2B4h 2D4–2D4h 2F4–2F4h	EP0IC EP0OC EP1IC EP1OC EP2IC EP2OC EP3IC EP3OC	Endpoint 0 IN Configuration Endpoint 0 OUT Configuration Endpoint 1 IN Configuration Endpoint 1 OUT Configuration Endpoint 2 IN Configuration Endpoint 2 OUT Configuration Endpoint 3 IN Configuration Endpoint 3 OUT Configuration	0000h	RO, R/W
237h 277h 2B7h 2F7h	EP0OSPS EP1OSPS EP2OSPS EP3OSPS	Endpoint 0 Output Setup Package Status Endpoint 1Output Setup Package Status Endpoint 2 Output Setup Package Status Endpoint 3 Output Setup Package Status	00h	RO, R/WC
238–23Fh 278–27Fh 2B8–2BFh 2F8–2FFh	EP0OSP EP1OSP EP2OSP EP3OSP	Endpoint 0 Output Setup Packet Endpoint 1Output Setup Packet Endpoint 2 Output Setup Packet Endpoint 3 Output Setup Packet	0	R/W

14.4.1 GCAP—Global Capabilities Register

Address Offset: 000h–003h Attribute: RO
Default Value: 40000003h Size: 32 bits

Bit	Default and Access	Description
31:28	4h RO	**Endpoint Cap:** Indicates the number of Endpoints supported by this device. One 'IN' and one 'OUT' pair is considered an endpoint, so the minimum device configuration would have a default value of '1', indicating that only the Endpoint 0 IN and Endpoint 0 OUT are supported. (Reset value may vary if other than four endpoint pairs are supported.)
27:5	0s RO	Reserved
4	0b RO	**Interrupt on Completion Capable (IOCC)** 1 = the hardware has the capability of generating an interrupt based on the Transfer or Scatter Gather DMA mode Buffer Descriptor IOC bit.
3	0 RO	**Transfer Mode Capable (TM)** 1 = the device supports Transfer Mode DMA operation.
2	0 RO	**Scatter Gather Mode Capable (SGM)** 1 = indicates the device supports Scatter Gather Mode DMA operation
1	1 RO	**Linear Mode Capable (LM)** 1 = indicates the device supports Buffer Mode DMA operation.
0	1 RO	**Control Mode Capable (CM)** 1 = indicates the device supports Control Mode DMA operation



14.4.2 DEV_STS—Device Status Register

Address Offset: 100h–103h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:15	0000h RO	Reserved
14:8	00h RO	**Address (ADDR):** This field provides the address of the device on the bus. At initialization, this is zero, and will reset to zero if the device is disconnected from the bus or a Bus Reset event is detected on the link. This register will reflect the address assigned to the device by the controller when the address has been assigned. This is read/write to facilitate testing - software should not write under normal operation
7:4	0h RO	Reserved
3	0 RO	**Rate (R):** The Intel® SCH assigns this bit after negotiating with a USB host. 0 = Device is operating in Full-Speed (12 Mbps) mode. 1 = Device is operating in High-Speed (480 Mbps) mode. A second read maybe required after Connected is read asserted in order to read the correct Rate value.
2	0 RO	Reserved
1	0 RO	**Connected (C):** 0 = The device is not electrically connected to a USB host or hub device. 1 = The hardware is electrically connected to a USB host or hub device based on D+/D- signaling and if has determined whether the connection is high speed or full speed. If the host resets the device, this bit is reset to a “0” and it is set back to a “1” only after the speed mode is established.
0	0 RO	**Suspend (S):** 0 = a link Resume is seen to take the device out of reset. 1 = The hardware has detected that more than 3 ms have elapsed since the last activity on the bus, indicating that the device should enter USB “suspend” state.

14.4.3 FRAME—Frame Number Register

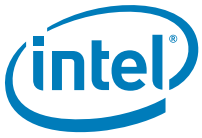
Address Offset: 104h–107h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:12	00000h RO	Reserved
11:0	000h RO	**Number (NUM):** Indicates the last 11b frame number received in a SOF packet on the bus

14.4.4 INT_STS—Interrupt Status Register

Address Offset: 10Ch–10Fh Attribute: RO, R/WC
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:19	000h RO	Reserved
18	0 R/WC	**Reset (R):** A Device Reset signal on the USB port has been detected. When a bus reset is received, the Intel® SCH must immediately stop any transmissions. Endpoint FIFOs are flushed. All Endpoint Enable bits should transition to a '0' at the detection of USB Bus reset, but all other endpoint bits should NOT be affected. While the Reset is being signaled on the USB Bus, software may set the Enable bit on endpoints so that they are ready when bus activity resumes.
17	0 R/WC	**Connect (C):** Set by hardware when the Device Status CONNECTED bit (100h:1) transitions from 0-to-1 OR 1-to-0.
16	0 R/WC	**Suspend (S):** Set by hardware when the Device Status SUSPEND bit (100h:0) transitions from 0-to-1 OR 1-to-0.
15:8	000h RO	Reserved
7:0	00h RO	**Endpoint Status (EPSTS):** These are status bits only; the actual interrupt(s) are cleared by writing a 1 to the appropriate bit(s) in the EP0_IN_STS Register. **Bit** **Endpoint** 7 EP3_OUT 6 EP3_IN 5 EP2_OUT 4 EP2_IN 3 EP1_OUT 2 EP1_IN 1 EP0_OUT 0 EP0_IN



14.4.5 INT_CTRL—Interrupt Control Register

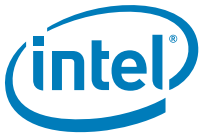
Address Offset: 110h–113h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:19	000h RO	Reserved
18	0 R/W	**Reset Interrupt Enable (RIEN):** When set, and INT_STS.R is set, an interrupt is generated.
17	0 R/W	**Connect Interrupt Enable(CIEN):** When set and INT_STS.C is set, an interrupt is generated.
16	0 R/W	**Suspend Interrupt Enable(SIEN):** When set and INT_STS.S is set, an interrupt is generated.
15:8	000h R/W	Reserved
7:0	00h R/W	**Endpoint Interrupt Enable (EPINTEN):** When one of the Endpoint Interrupt Enable bits is set and the corresponding interrupt status bit (INT_STS.EPSTS) is set, an interrupt is generated. Each bit maps to a particular endpoint as shown below: **Bit Endpoint** 7 EP3_IN 6 EP3_OUT 5 EP2_IN 4 EP2_OUT 3 EP1_IN 2 EP1_OUT 1 EP0_IN 0 EP0_OUT

14.4.6 DEV_CTRL—Device Control Register

Address Offset: 114h–117h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31	0 R/W	**Enable (EN):** While cleared, any writes to any bit(s) in any register other than this bit are ignored. They complete, but will have no effect on any registers. Hardware must not drive D+/D- to signal a connection to the host. When software sets this bit, hardware transitions to the running state. Software must poll this bit and not perform any reads or writes to the register space until the bit is read as a '1'. If the bit is not read as a '1' within 5 ms, software may assume that there is a hardware fault. When software clears this bit, hardware transitions all registers to their reset values (except register "Offset 104h: FRAME - Frame Number" which keeps the last frame number received), and deasserts any interrupts, clears any FIFOs, and performs a device reset.
30	0 R/W	**Connection Enable (CE):** 0 = D+/D- must not be pulled up to indicate to a host that a device is connected, and should appear as not connected. 1 = appropriate pull-ups are enabled to signal a connection to a host. When transitioning from '1' to '0', the device shall appear to the host to Disconnect, as defined in section 7.1.7.3 of the *USB 2.0 specification*.
29:0	0 RO	Reserved
8	0 R/W	**TestMode:** When set to a 1, the USB Client will respond with fast CHIRP's to speed test time.
7	0b R/W	**Test_se0_nak_mode:** When set to a '1', the USB Client will be configured in high-speed mode and will respond with NAK to all incoming IN packets.
6:5	000b RO	Reserved
4	0 R/W	**SignalResume (SR):** When software writes a 1 to this bit, hardware will generate resume signaling on the link if the link is in the Suspend state. Software is responsible for knowing whether the device has been enabled to generate the signaling by the Host system, and for ensuring that the link has been in the suspend state for the 5 ms minimum, per *USB 2.0 Specification,* Section 7.1.7.7. Hardware is responsible for asserting the resume signaling on the link for the requisite amount of time. When the resume signaling is completed, hardware will clear this bit to a '0'. While resume signaling is enabled, software writes to this bit will be ignored.



Bit	Default and Access	Description
3:1	000b R/W	**Charge Enable (CGE):** Software will program the maximum number of unit loads that the device may consume from the bus. Software will determine this based on the Device Configuration selected by the Host software. This value may be from 000b to 101b, representing 0 to 5 unit loads. Since a unit load is defined as 100 mA, hardware may then proceed to draw up to the indicated amount of current. Hardware may assume that 1 unit load (100 mA) of current will be available, and up to 500 mA may be available if the Client Device is plugged into a Host or Powered Hub. Hardware may optionally use this software provided value to charge a battery or draw power off the link for other purposes, or it may ignore the value if it has no need for link power. If hardware does not implement this functionality, it may be Read-Only '000b'.
0	0 R/W	**Force Full Speed (FFS):** If set, the Intel® SCH will not attempt to negotiate High-Speed operation, and will fall back to default Full-Speed operation.

14.5 Device Endpoint Register Map

The following provides the Device Endpoint register map.

Byte Offset 7	6	5	4	3	2	1	0	Address Offset
Input Base Address								00h
Transfer in Queue		Descriptor in List		Position in Buffer		Input Length		08h
Reserved		Status		Configuration		MaxData Packet Size		10h
Reserved								18h
Output Base Address								20h
Transfer in Queue		Descriptor in List		Position in Buffer		Output Length		28h
Setup Packet Status	Reserved	Status		Configuration		MaxData Packet Size		30h
Setup Packet								38h

14.5.1 EPnIB—Endpoint [0..3] Input Base Address Register

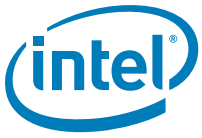
Address Offset:	EP0_IN_BASE	200h–207h	Attribute: RO, R/W
	EP1_IN_BASE	240h–247h	
	EP2_IN_BASE	280h–287h	
	EP3_IN_BASE	2C0h–2C7h	
Default Value:	0000000000000000h		Size: 64 bits

Bit	Default and Access	Description
63:0	000000000h R/W	**Base Address (BA):** Must be 64B aligned. This register may be implemented as a 32b register, with the upper 32b Read Only 00000000h.

14.5.2 EPnIL—Endpoint [0,1] Input Length Register

Address Offset:	EP0IL	208h–209h	Attribute: R/W
	EP1IL	248h–249h	
	EP2IIL	288h–289h	
	EP3IL	2C8h–2C9h	
	Default Value:	0000h	Size: 16 bits

Bit	Default and Access	Description
15:0	0000h R/W	**Length (LEN):** If EPnIC.MD is Buffer, this field indicates the length of the data buffer. If EPnIC.MD is ScatterGather or Transfer, this field indicates the number of entries in the Descriptor List.



14.5.3 EPnIPB—Endpoint [0..3] Input Position in Buffer Register

Address Offset:	EP0IPB	20Ah–20Bh	Attribute: RO, W/C
	EP1IPB	24Ah–24Bh	
	EP2IPB	28Ah–28Bh	
	EP3IPB	2CAh–2CBh	
	Default Value:	0000h	Size:16 bits

Bit	Default and Access	Description
15:0	0000h R/WC	**Position (POS):** Byte offset of the last byte fetched by the DMA engine within the current buffer.

14.5.4 EPnIDL—Endpoint [0..3] Input Descriptor in List Register

Address Offset:	EP0IDL	20Ch–20Dh	Attribute: RO, W/C
	EP1IDL	24Ch–24Dh	
	EP2IDL	28Ch–28Dh	
	EP3IDL	2CCh–2CDh	
Default Value:	0000h		Size:16 bits

Bit	Default and Access	Description
15:0	0000h R/WC	**Position (POS):** If EPnIC.MD is Linear, this is field is RO and not used. If EPnIC.MD is Transfer or Scatter Gather, this field indicates the offset of the current Descriptor in the Descriptor List.

14.5.5 EPnITQ—Endpoint [0..3] Input Transfer in Queue Register

Address Offset:	EP0ITQ	20Eh–20Fh	Attribute: RO, W/C
	EP1ITQ	24Eh–24Fh	
	EP2ITQ	28Eh–28Fh	
	EP3ITQ	2CEh–2CFh	
Default Value:	0000h		Size:16 bits

Bit	Default and Access	Description
15:0	0000h R/WC	**Position (POS):** If EPnIC.MD is Linear this, this field is RO and not used. If EPnIC.MD is Transfer, this field indicates the offset of the current Transfer in the Transfer Queue.

14.5.6 EPnIMPS—Endpoint [0..3] Input Maximum Packet Size Register

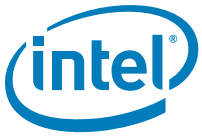
Address Offset:	EP0IMPS	210h–211h	Attribute: RO, R/W
	EP1IMPS	250h–251h	
	EP2IMPS	290h–291h	
	EP3IMPS	2D0h–2D1h	
Default Value:	0040h		Size: 16 bits

Bit	Default and Access	Description
15:11	00h RO	Reserved
10:0	040h R/W	**Size (S):** This field indicates the maximum number of data bytes that may be sent in each inbound DATA packet, up to 1024 Bytes. Software is responsible for making sure that the value programmed here does not break the USB protocol (such as setting to 1024B on a Control endpoint). This defaults to 64 Bytes, which is the default size of a Control Endpoint.

14.5.7 EPnIS—Endpoint [0..3] Input Status Register

Address Offset:	EP0IS	212h–213h	Attribute: RO, R/WC
	EP1IS	252h–253h	
	EP2IS	292h–293h	
	EP3IS	2D2h–2D3h	
	Default Value:	0000h	Size:16 bits

Bit	Default and Access	Description
15	0 R/WC	**Bad PID Type Detected (BP):** An inappropriate PID type was seen; for instance, a SETUP PID to an endpoint configured as a BULK endpoint.
14	0 R/WC	**CRC Error (CE):** A CRC error on the packet from the USB host detected.
13	0 R/WC	**FIFO Error (FE):** Data over-run. The packet received may have been corrupted.
12	0 R/WC	**DMA Error (DE):** There was an error fetching descriptors, or writing buffer data. Hardware may STALL transactions targeted at this endpoint (rather than NAKing them) to indicate to the Host that a serious problem as occurred.
11	0 R/WC	**Transfer Complete (TC):** LENGTH bytes have been sent, or one queue descriptor is complete and IOC was set
10	0 RO	Reserved
9	0 R/WC	**Interrupt on Completion (IOC):** If GC.IOCC is set, when in Scatter Gather or Transfer mode, indicates that a DMA buffer which has IOC set in the descriptor has been completely transferred. If GC.IOCC is cleared, this bit is read-only 0.
8:0	00h RO	Reserved



14.5.8 EPnIC—Endpoint [0..3] Input Configuration Register

Address Offset:	EP0IC	214h–215h	Attribute: RO, R/W
	EP1IC	254h–255h	
	EP2IC	294h–295h	
	EP3IC	2D4h–2D5h	
Default Value:	0000h		Size:16 bits

Bit	Default and Access	Description
15	0 R/W	**Interrupt on Bad PID Type (BP):** Enables EPnIS.BPT to generate an interrupt when set.
14	0 R/W	**Interrupt on CRC Error (ICE):** Enables EPnIS.CE to generate an interrupt when set.
13	0 R/W	**Interrupt on FIFO Error (IFE):** Enables EPnIS.FE to generate an interrupt when set.
12	0 R/W	**Interrupt on DMA Error (IDE):** Enables EPnIS.DE to generate an interrupt when set.
11	0 R/W	**Interrupt on Transfer Complete (ITC):** Enables EPnIS.TC to generate an interrupt when set.
10	0 RO	Reserved
9	0 RW	**Interrupt on DMA Interrupt on Completion (IDIOC):** Enables EPnIS.IOC to generate an interrupt when set.
8	0 RO	Reserved
7:6	00b R/W	**Mode (MD):** Indicates the way the address and Length fields are interpreted, and the way the data is fetched. See section Error! Reference source not found. for a description of these modes. 00 = Linear Mode, Only Linear Mode and Control Mode are supported by the Intel® SCH 01 = Scatter Gather Mode 10 = Transfer Mode 11 = Control Mode
5:4	00b R/W	**Type (TYP):** Changes some endpoint behaviors based on the type of the endpoint. In particular, Isochronous endpoints do not send ACK/NAK packets, and do not perform error checking. The transfer limits for Control and Interrupt are also smaller than the limits for Isoch or Bulk (but only software cares). 00 = Control/Message 01 = Isochronous 10 = Bulk 11 = Interrupt When Control/Message, software should set MD to Linear Mode so that the software can handle each arriving packet. Endpoints 0_IN and 0_OUT (the default Control pipe) will always be used in Control/Message mode.

Bit	Default and Access	Description
3:2	00b RO	Reserved
1	0 R/W	**Enable (EN)** 1 = hardware will send data from the data buffer (fetching from DMA as needed) for as long as there is data remaining to be sent in the buffer. The size of each individual transfer is limited by the EPnIMPS. If IN_Enable is set when the Length register is zero (indicating no bytes or no descriptors), a zero length packet will be sent on the next transfer. 0 = input from this Endpoint is not enabled. If V is set, hardware will send a NAK for any packet addressed to this endpoint. If v is cleared, hardware will STALL any IN transfer to indicate a problem with the Endpoint. On a transition from 1-to-0 the FIFO must be flushed so that the next data transmission is fetched from memory.
0	0 R/W	**Valid (V):** This bit indicates whether this is a valid and configured Endpoint on this device. Clearing this bit causes an endpoint reset. During the reset: • All register values associated with this endpoint must return to their default values. • The DATA0/1 sequence toggling for this endpoint defaults back to DATA0 • All interrupts and status bits associated with this endpoint are cleared. • All DMA FIFOs and state machines are cleared and reset, including any FIFO errors • Intel® SCH minimizes power usage to the extent possible

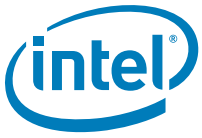
14.5.9 EPnOB—Endpoint [0..3] Output Base Address Register

Address Offset: Attribute: RO, R/W

EP0OB	220h–227h
EP1OB	260h–267h
EP2OB	2A0h–2A7h
EP3OB	2E0h–2E7h

Default Value: 0000000000000000h Size: 64 bits

Bit	Default and Access	Description
63:0	000000000h R/W	**Base Address (BA):** Must be 64B aligned. This register may be implemented as a 32b register, with the upper 32b Read Only 00000000h.



14.5.10 EPnOL—Endpoint [0..3] Output Length Register

Address Offset:

EP0OL	228h–229h	Attribute: R/W
EP1OL	268h–269h	
EP2OL	2A8h–2A9h	
EP3OL	2E8h–2E9h	
Default Value: 0000h		Size: 16 bits

Bit	Default and Access	Description
15:0	0000h R/W	**Length (LEN):** If EPnIC.MD is Buffer, this field indicates the length of the data buffer. If EPnIC.MD is ScatterGather or Transfer, this field indicates the number of entries in the Descriptor List.

14.5.11 EPnOPB—Endpoint [0..3] Output Position in Buffer Register

Address Offset:

EP0OPB	22Ah–22Bh	Attribute: RO, W/C
EP1OPB	26Ah–24Bh	
EP2OPB	2AAh–2ABh	
EP3OPB	2EAh–2EBh	
Default Value: 0000h		Size:16 bits

Bit	Default and Access	Description
15:0	0000h R/WC	**Position (POS):** Byte offset of the last byte written to by the DMA engine within the current buffer.

14.5.12 EPnODL—Endpoint [0..3] Output Descriptor in List Register

Address Offset:

EP0ODL	22Ch–20Dh	Attribute: RO, W/C
EP1ODL	26Ch–24Dh	
EP2ODL	2ACh–28Dh	
EP3ODL	2ECh–2CDh	
Default Value: 0000h		Size:16 bits

Bit	Default and Access	Description
15:0	0000h R/WC	**Position (POS):** If EPnIC.MD is Linear, this field is RO and not used. If EPnIC.MD is Transfer or Scatter Gather, this field indicates the offset of the current Descriptor in the Descriptor List.

14.5.13 EPnOTQ—Endpoint [0..3] Output Transfer in Queue Register

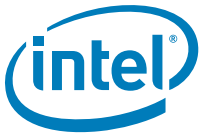
Address Offset:	EP0OTQ	20Eh–20Fh	Attribute: RO, W/C
	EP1OTQ	24Eh–24Fh	
	EP2OTQ	28Eh–28Fh	
	EP3OTQ	2CEh–2CFh	
Default Value:	0000h		Size:16 bits

Bit	Default and Access	Description
15:0	0000h R/WC	**Position (POS):** If EPnIC.MD is Linear this field is RO and not used. If EPnIC.MD is Transfer, this field indicates the offset of the current Transfer in the Transfer Queue.

14.5.14 EPnOMPS—Endpoint [0..3] Output Maximum Packet Size Register

Address Offset:	EP0OMPS	230h–231h	Attribute: RO, R/W
	EP1OMPS	270h–271h	
	EP2OMPS	2B0h–2B1h	
	EP3OMPS	2F0h–2F1h	
Default Value:	0040h		Size: 16 bits

Bit	Default and Access	Description
15:11	00h RO	Reserved
10:0	040h R/W	**Size (S):** This field indicates the maximum number of data bytes than may be sent in each inbound DATA packet, up to 1024 Bytes. Software is responsible for making sure that the value programmed here does not break the USB protocol (such as setting to 1024B on a Control endpoint). This defaults to 64 Bytes, which is the default size of a Control Endpoint.



14.5.15 EPnOS—Endpoint [0..3] Output Status Register

Address Offset:	EP0OS	232h–233h	Attribute: RO, R/WC
	EP1OS	272h–273h	
	EP2OS	2B2h–2B3h	
	EP3OS	2F2h–2F3h	
Default Value:	0000h		Size:16 bits

Bit	Default and Access	Description
15	0 R/WC	**Bad PID Type Detected (BPTD):** An inappropriate PID type was seen; for instance, a SETUP PID to an endpoint configured as a BULK endpoint
14	0 R/WC	**CRC Error (CE):** A CRC error on the packet from the USB host detected.
13	0 R/WC	**FIFO Error (FE):** Data under-run. The packet received may have been corrupted.
12	0 R/WC	**DMA Error (DE):** There was an error fetching descriptors, or fetching buffer data. Hardware may STALL transactions targeted at this endpoint (rather than NAKing them) to indicate to the Host that a serious problem as occurred.
11	0 R/WC	**Transfer Complete (TC):** Short Packet detected, meaning less than EPnOMPS bytes were sent in a Data0/1 phase. This includes zero length packets. This will also be set if or one queue descriptor is complete and IOC was set.
10	0 RO	**Ping NAK Sent (PNS):** Set if hardware responds to a PING with a NAK. Software can use this bit as an indication that the buffer size is insufficient, and that the host is waiting to send a larger packet than can be accommodated.
9	0 R/WC	**Interrupt on Completion (IOC):** If GC.IOCC is set, when in Scatter Gather or Transfer mode, indicates that a DMA buffer which has IOC set in the descriptor has been completely transferred. If GC.IOCC is cleared, this bit is read-only '0'.
8:0	00h RO	Reserved

14.5.16 EPnOC—Endpoint [0..3] Output Configuration Register

Address Offset:	EP0OC	234h–235h	Attribute: RO, R/W
	EP1OC	274h–275h	
	EP2OC	2B4h–2B5h	
	EP3OC	2F4h–2F5h	
Default Value:	0000h		Size:16 bits

Bit	Default and Access	Description
15	0 R/W	**Interrupt on Bad PID Type (IBPT):** Enables EPnOS.BPT to generate an interrupt when set.
14	0 R/W	**Interrupt on CRC Error (ICE):** Enables EPnOS.CE to generate an interrupt when set.
13	0 R/W	**Interrupt on FIFO Error (IFE):** Enables EPnOS.FE to generate an interrupt when set.

Bit	Default and Access	Description
12	0 R/W	**Interrupt on DMA Error (IDE):** Enables EPnOS.DE to generate an interrupt when set.
11	0 R/W	**Interrupt on Transfer Complete (ITC):** Enables EPnOS.TC to generate an interrupt when set.
10	0 RO	**Interrupt on PingNAKSent (IPNS):** Enables EPnOS.PNS to generate an interrupt when set.
9	0 RW	**Interrupt on DMA Interrupt on Completion (IDIOC):** Enables EPnOS.IOC to generate an interrupt when set.
8	0 RO	Reserved
7:6	00b R/W	**Mode (MD):** Indicates the way the address and Length fields are interpreted, and the way the data is fetched. 00 = Linear Mode, Only Linear Mode and Control Mode are supported by the Intel® SCH 01 = Scatter Gather Mode 10 = Transfer Mode 11 = Control Mode
5:4	00b R/W	**Type (TYP):** Changes some endpoint behaviors based on the type of the endpoint. In particular, Isochronous endpoints do not send ACK/NAK packets, and do not perform error checking. The transfer limits for Control and Interrupt are also smaller than the limits for Isoch or Bulk (but only software cares). 00 = Control/Message 01 = Isochronous 10 = Bulk 11 = Interrupt When Control/Message, software should set MD to Linear Mode so that the software can handle each arriving packet. Endpoints 0_IN and 0_OUT (the default Control pipe) will always be used in Control/Message mode.
3:2	00b RO	Reserved
1	0 R/W	**Enable (EN)** 1 = hardware will receive data into the data buffer for as long as there is space in the buffer. 0 = Output on this Endpoint is not enabled. If V is set, hardware will send a NAK for any packet addressed to this endpoint. If V is cleared, hardware will STALL any IN transfer to indicate a problem with the Endpoint. On a transition from 1-to-0, the DMA FIFO must be flushed so that all of the data received is flushed to memory. On a transition from 0-to-1, the Position In Buffer register, and the Description Descriptor in List and Transaction in Queue registers, if implemented, will be reset to zero to cause the DMA to begin transferring the next transaction at the beginning of the buffer.

Bit	Default and Access	Description
0	0 R/W	**Valid (V):** Indicates whether this is a valid and configured Endpoint on this device. Clearing this bit causes an endpoint reset. During the reset: • All register values associated with this endpoint must return to their default values. • The DATA0/1 sequence toggling for this endpoint defaults back to DATA0 • All interrupts and status bits associated with this endpoint are cleared. • All DMA FIFOs and state machines are cleared and reset, including any FIFO errors • Intel® SCH minimizes power usage to the extent possible

14.5.17 EPnOSPS—Endpoint [0..3] Output Setup Package Status Register

Address Offset:	EP0OSPS EP1OSPS EP2OSPS EP3OSPS	237h 277h 2B7h 2F7h	Attribute: RO, R/W
Default Value:	00h		Size:8 bits

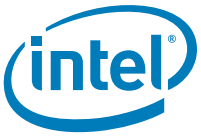
Bit	Default and Access	Description
7:1	00h RO	Reserved
0	0 R/WC	**Valid (V):** Indicates that a valid Setup Packet is in EPnOSP.

14.5.18 EPnOSP—Endpoint [0..3] Output Setup Packet Register

Address Offset:	EP0OSP EP1OSP EP2OSP EP3OSP	238h-23Fh 278h-27Fh 2B8h-2BFh 2F8h-2FFh	Attribute: RO,
Default Value:	0000000000000000h	Size:	64 bits

Bit	Default and Access	Description
63:0	0 RO	Received Setup Packet Data

§ §



15 SDIO/MMC (D30:F0, F1, F2)

15.1 SDIO Functional Description (D30:F0, F1, F2)

The Intel® SCH contains three SDIO/MMC ports.

- Port 0 and Port 1 are 4-bits wide. Port 2 is 8-bits wide.

The controller supports MMC 4.1 and SDIO 1.1 specifications.

- MMC 4.1 transfer rates can be up to 48 MHz and bus widths of 1, 4, or 8 bits.
- SDIO 1.1 supports transfer rates up to 24 MHz and bus widths of 1 or 4 bits.

15.1.1 Protocol Overview

The SDIO/MMC transfer protocol utilizes the following definitions:

- **Command:** A command is a 6-byte token that starts an operation. The command set includes card initialization, card register reads and writes, and data transfers. The MMC/SD/SDIO controller sends the command serially on the SD_CMD signal pin.
- **Response:** A response is a token that is an answer to a command token. Each command has either a specific response type or no response type. The format for a response varies according to the command sent and the card mode. Response formats are detailed in the *MultiMediaCard System Specification Version 4.0*.
- **Data:** Data is transferred serially between the SDIO/MMC controller and the card in 8-bit blocks and at rates up to 48 MB/s. The format for the data depends on the card mode.

Depending on the status of certain enable bits, a particular response type can be selected. Table 42 summarizes these Response Type dependencies.

Table 42. Determining the Response Type

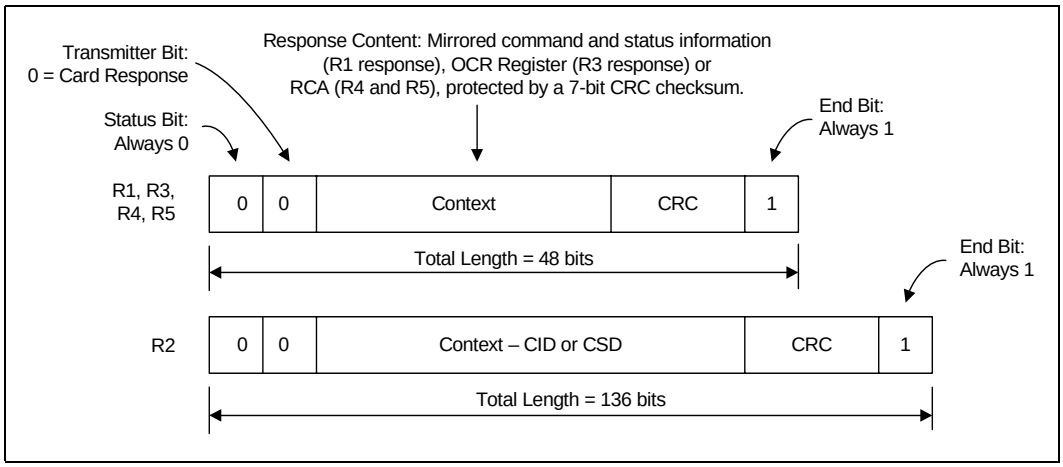
Response Type Select	Index Check Enable	CRC Check Enable	Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R5, R6
11	1	1	R1b, R5b

Once known, the Response Type will be transmitted by occupying a certain bit field within the 48-bit or 136-bit response. Table 43 summarizes the Response Register mapping.

Table 43. Response Register Mapping

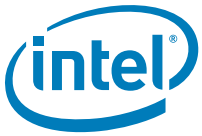
Kind of Response	Meaning of Response	Length of Response	Response Mapping	RESP Register Mapping
R1, R1b Normal Response	Card Status	48	39:8	REP[31:0]
R1b Auto CMD12 Response	Card Status for AutoCMD12	48	39:8	REP[127:96]
R2 CID, CSD Register Response	CID or CSD register incl	136	127:1	REP[126:0]
R3 OCR Register	OCR Register	48	39:8	REP[31:0]
R4 OCR Register	OCR Register in I/O mode	48	39:8	REP[31:0]
R5, R5b	SDIO Response	48	39:8	REP[31:0]
R6 Published RCA Response	New published RCA[31:16] etc.	48	39:8	REP[31:0]

Figure 7. Response Token Formats



15.1.2 Integrated Pull-Up Resistors

The Intel® SCH SDIO/MMC controller contains on-die pull-up resistors on each data bus pin. The value of these internal resistors is nominally 75 kΩ and meets the pull-up requirement for both SD/SDIO 1.1 and MMC 4.1 specifications.



15.2 PCI Configuration Registers

Table 44. SDIO/MMC PCI Register Address Map

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	See description.	RO
04–05h	PCICMD	PCI Command	0000h	R/W, RO
06–07h	PCISTS	PCI Status	0280h	R/WC, RO
08h	RID	Revision Identification	See description	RO
09h–0Bh	CC	Class Codes	080501h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10–13h	MEM_BASE	Base Address Register	00000000h	R/W,R0
2Ch	SSID	Subsystem Identifiers	0000h	RO
34h	CAP_PTR	Capabilities Pointer	00h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See description	RO
40h	SLOTINF	Slot Information	02h	RO
84h–87h	BC	Buffer Control	00000000h	RO, R/W
90h–93h	SDIOID	SDIO Identification	00000000h	RO, R/W
F4h-F7h	CAPCNTL	Capabilities Control	0000000xh	RO, R/W
F8h-FBh	MANID	Manufacturers ID	00000F86h	RO
FC–FFh	FD	Function Disable	00000000h	RO, R/W

NOTE: Address locations that are not shown should be treated as Reserved.

15.2.1 VID—Vendor Identification Register

Address Offset: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Default and Access	Description
15:0	8086 RO	**Vendor ID (VID):** This is a 16-bit value assigned to Intel.

15.2.2 DID—Device Identification Register

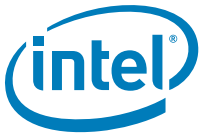
Address Offset: 02h–03h Attribute: RO
Default Value: See bit description Size: 16 bits

Bit	Default and Access	Description
15:0	See description RO	**Device ID (DID):** This is a 16-bit value assigned to the SDIO controller. 811Ch SDIO Controller #1 (D30:F0) 811Dh SDIO Controller #2 (D30:F1) 811Eh SDIO Controller #3 (D30:F2)

15.2.3 PCICMD—PCI Command Register

Address Offset: 04h–05h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:3	0s RO	Reserved
2	0 R/W	**Bus Master Enable (BME):** Allows the SDIO controller to act as a bus master. 0 = Disable bus mastering 1 = Enable bus mastering
1	0 R/W	**Memory Space Enable (MSE)**. Allows access to the SDIO controller memory space 0 = Disable access to memory space 1 = Enable access to memory space
0	0 RO	Reserved



15.2.4 PCISTS—PCI Status Register

Address Offset: 06h–07h Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:0	0000h RO	Reserved

15.2.5 CC—Class Codes Register

Address Offset: 08h–0Bh Attribute: RO
Default Value: 08050100h Size: 32 bits

Bit	Default and Access	Description
31:24	02h RO	**Base Class Code (BCC)** 02h = Indicates that this device is a generic peripheral. **Note:** Network device mode is not supported.
23:16	00h RO	**Sub Class Code (SCC)** 00 = this field indicates that this device is an SDIO host controller **Note:** Network device mode is not supported.
15:8	01h RO	**Programming Interface (PI)** 01h = Indicates the DMA is supported with this controller **Note:** Network device mode is not supported.
7:0	00h RO	**Revision ID (RID):** Matches the value of the RID register in the LPC bridge.

15.2.6 HEADTYP—Header Type Register

Address Offset: 0Eh Attribute: RO
Default Value: See description Size: 8 bits

Bit	Default and Access	Description
7	1 or 0 RO	**Multi-Function Device (MFD)** 0 = Single function device (Functions 1 and 2) 1 = Multi function device (Function 0)
6:0	00h RO	**Configuration Layout:** Hardwired to 00h, which indicates the standard PCI configuration layout.

15.2.7 MEM_BASE—Base Address Register

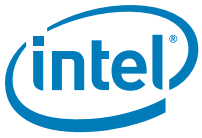
Address Offset: 10h–13h Attribute:R/W, RO
Default Value: 00000000h Size:32 bits

Bit	Default and Access	Description
31:8	000000h R/W	**Memory Base Address:** Provides the 256 byte t memory space for slot 1's address space.
7:1	00h RO	Reserved**.**
0	0 RO	**Space Indicator:** This bit reads 0, indicating that the BAR is memory mapped.

15.2.8 SS—Subsystem Identifier Register

Offset: 2Ch Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Default and Access	Description
7:0	description RO	**Revision ID (RID):** Matches the value of the RID register in the LPC bridge. Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the RID for each stepping.



15.2.9 INT_LN—Interrupt Line Register

Address Offset: 3Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Interrupt Line (INT_LN):** This data is not used by the Intel® SCH. It is to communicate to software the interrupt line that the interrupt pin is connected to.

15.2.10 INT_PN—Interrupt Pin Register

Address Offset: 3Dh Attribute: RO
Default Value: See Description Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Interrupt Line (INT_LN):** This value tells the software which interrupt pin each SDIO/MMC host controller uses. The upper 4 bits are hardwired to 0000b; the lower 4 bits are determine by the Interrupt Pin default values that are programmed in the memory-mapped configuration space as follows: SDIO #1 — D30IP.SD0IP (Chipset Config Registers:Offset 3104:bits 3:0) SDIO #2 — D30IP.SD1IP (Chipset Config Registers:Offset 3104:bits 7:4) SDIO #3 — D30IP.SD2IP (Chipset Config Registers:Offset 3104:bits 11:8) **NOTE:** This does not determine the mapping to the PIRQ pins.

15.2.11 SLOTINF—Slot Information Register

Address Offset: 40h Attribute: RO
Default Value: 02h Size: 8 bits

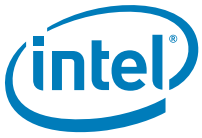
Bit	Default and Access	Description
7	0 RO	Reserved
6:4	000b RO	**Number of Slots (NS):** 000b indicates 1 slot supported on this controller.
3	0 RO	Reserved
2:0	010b RO	**First Base Address Register Number (FBAR):** Indicates the offset containing the MEM_BASE (10h).

15.2.12 BC—Buffer Control Register

Address Offset:	84h–87h	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

BIOS/Firmware must correctly program the Buffer Strength bits based on the length of signal traces used in the design.

Bit	Default and Access	Description
31:6	00000h RO	Reserved
5:4	00	**Core Clock Delay (CCD):** Connects to clock buffer. The length value to program is: 00 = 0 to 4 inches 01 = 4 to 5 inches 10 = Reserved 11 = Reserved
3:2	00	**Data Buffer Output Delay (DBOD):** Connects to all data buffers. The length value to program is: 00 = 0 to 4 inches 01 = 4 to 5 inches 10 = Reserved 11 = Reserved
1:0	00	**Data Buffer Input Delay (DBID):** Connects to all data buffers. The length value to program is: 00 = 0 to 4 inches 01 = 4 to 5 inches 10 = Reserved 11 = Reserved



15.2.13 SDIOID—SDIO Identification Register

Address Offset: 90h–93h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:1	0 RO	Reserved
0	0 R/W	**Host Controller ID as Network Device (HCND):** 1 = The base class, bus class, and programming interface for this SDIO controller changes to a network controller. | **NOTE:** Network device mode the is not supported.

15.2.14 CAPCNTL—SDIO Capability Control Register

Address Offset: F4h–F7h Attribute: RO, R/W
Default Value: 0000000xh Size: 32 bits

Bit	Default and Access	Description
31:8	000h RO	Reserved
2	1b RW	**Bit 2 Control:** Bit2 control bit for register offset 40h bit 21;
1	see des RW	**Bit 1 Control:** Bit1 control bit for register offset 40h bit 17 . this bit will default to a 1 for SDIO Slot 0, and 0 for SDIO Slot 1 and 2
0	0b RW	**Bit 0 Control:** Bit0 control bit for register offset 40h bit 16

Note: Bit 2:0 Notes: The default value of these register bits matches the default value of the bits in register offset 40h. Writing these bits to a different value allows validation to test the hardware in other configurations without changing the register bits in offset 40h.

15.2.15 MANID—Manufacturer ID

Address Offset: F8h–FBh Attribute: RO
Default Value: 00000F86h Size: 32 bits

Bit	Default and Access	Description
31:24	00h RO	Reserved
23:16	xh RO	**Stepping ID:** Refer to the Spec Update
15:8	0Fh RO	**Manufacturer:** 0Fh = Intel
7:0	86h RO	**Process/Dot:** 86h = process 861.6

15.2.16 FD—Function Disable Register

Address Offset: FCh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:1	0 RO	Reserved
0	0 R/W	**Disable (D):** 0 = This function is enabled 1 = This function is disabled and configuration space is disabled

15.3 SDIO/MMC Memory-Mapped Registers

For the following memory mapped registers, the base address is that pointed to by the contents of the MEM_BASE (offset 10h) register described above.

Here is a list of the SDIO transfer restrictions:

- the Intel® SCH does not support zero block size transfer
- For DMA mode, the Intel® SCH does not support the following mode:
  - offset 0Ch, bit 5 = 1, Multiple Transfer
  - offset 0Ch, bit 1 = 1, Block Count Enabled
  - offset 06h = 0000h, Block Count = 0 (aka Stop Multiple Transfer)
- For PIO mode, the Intel® SCH does not support the following modes:
  - (Stop Multiple Transfer)
    offset 0Ch, bit 5 = 1, Multiple Transfer
    offset 0Ch, bit 1 = 1, Block Count Enabled
    offset 06h = 0000h, Block Count = 0
  - Infinite Transfer
    offset 0Ch, bit 5 = 1, Multiple Transfer
    offset 0Ch, bit 1 = 0, Block Count Disabled
    offset 06h = 0000h, Block Count = 0 or 1

Table 45. SDIO/MMC Memory-Mapped Register Address Map (Sheet 1 of 2)

MEM_BASE + Offset	Mnemonic	Register Name	Default	Type
00h–03h	DMAADR	DMA Address	00000000h	R/W
04h–05h	BLKSZ	Block Size	0000h	RO, R/W
06h–07h	BLKCNT	Block Count	0000h	R/W
08h–0Bh	CMDARG	Command Argument	00000000h	R/W
0Ch–0Dh	XFRMODE	Transfer Mode	0000h	RO, R/W
0Eh–0Fh	SDCMD	SDIO Command	0000h	RO, R/W
10h–1Fh	RESP	Response	0s	R/W
20h–23h	BUFDATA	Buffer Data Port	00000000h	R/W
24h–27h	PSTATE	Present State	00000000h	RO, R/W, ROC
28h	HOSTCTL	Host Control	00h	RO, R/W
29h	PWRCTL	Power Control	00h	RO, R/W
2Ah	BLKGAPCTL	Block Gap Control	00h	RO, R/W
2Bh	WAKECTL	Wakeup Control	00h	RO, R/W
2Ch–2Dh	CLKCTL	Clock Control	0000h	RO, R/W
2Eh	TOCTL	Timeout Control	00h	RO, R/W
2Fh	SWRST	Software Reset	00h	RO, R/W, R/WC
30h–31h	NINTSTS	Normal Interrupt Status	0000h	RO, R/WC
32h–33h	ERINTSTS	Error Interrupt Status	0000h	RO, R/WC
34h–35h	NINTEN	Normal Interrupt Enable	0000h	RO, R/W

Table 45. SDIO/MMC Memory-Mapped Register Address Map (Sheet 2 of 2)

MEM_BASE + Offset	Mnemonic	Register Name	Default	Type
36h–37h	ERINTEN	Error Interrupt Enable	0000h	RO, R/WC
38h–39h	NINTSIGEN	Normal Interrupt Signal Enable	0000h	RO, R/W
3Ah–3Bh	ERINTSIGEN	Error Interrupt Signal Enable	0000h	RO, R/WC
3Ch–3Dh	AC12ERRSTS	Auto CMD12 Error Status	0000h	RO
40h–43h	CAP	Capabilities	00000000h	RO
48h–4Bh	MCCAP	Maximum Current Capabilities	00000000h	RO
FCh–FDh	SLTINTSTS	Slot Interrupt Status	0000h	RO
FEh–FFh	CTRLRVER	Host Controller Version	0000h	RO

15.3.1 DMAADR—DMA Address Register

I/O Offset: Base + (00h–03h) Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0 R/W	**System Address (SA):** This field contains the system memory address for a DMA transfer. During data transfers, reads of these bits will return invalid data and writes will be ignored. When the Intel® SCH stops a DMA transfer, this points to the system address of the next data position. The DMA transfer stops at every boundary specified by BS.BB. Intel® SCH generates DMA Interrupt to request software to update this register. Software must then write the address of the next data position to this register. When the upper byte of this register (offset 003h) is written, the Intel® SCH restarts the transfer. When restarting a DMA transfer through the Resume command or by setting the Continue Request bit in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the System Address register. If the DMA transfer crosses DMA buffer boundary, the DMA system address must be chosen such that it is any multiple of the programmed blk_size below the DMA buffer boundary. This equates to: DMA Sys Addr = DMA buffer boundary – (n * blk_size) where n is any number that will equate the DMA Sys Addr below the DMA buffer boundary.

15.3.2 BLKSZ—Block Size Register

I/O Offset: Base + (04h-05h) Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>15</td><td>0
RO</td><td>Reserved</td></tr>
<tr><td>14:12</td><td>000b
R/W</td><td>Buffer Boundary (BB): These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the boundary specified by this field and Intel® SCH generates the DMA Interrupt to request software to update DSA.
If 000b (buffer size = 4 KB), the lower 12 address bits points to data in the contiguous buffer while the upper 20 address bits point to the location of the buffer in system memory. The DMA transfer stops when the Host Controller detects “carry out” of the address from bit 11 to 12. The address “carry out bit” changes depending on the size of the buffer. This function is active when the DMA Enable in the Transfer Mode register is set to 1.
<table>
<tr><th>Bits</th><th>Buffer Size</th><th>Carry Out Bit</th></tr>
<tr><td>004</td><td>4 KB</td><td>A11</td></tr>
<tr><td>001</td><td>8 KB</td><td>A12</td></tr>
<tr><td>---</td><td>---</td><td>---</td></tr>
<tr><td>110</td><td>256 KB</td><td>A17</td></tr>
<tr><td>111</td><td>512 KB</td><td>A18</td></tr>
</table></td></tr>
<tr><td>11:0</td><td>000h
R/W</td><td>Transfer Block Size (TBS): Specifies the size of each block, in Bytes, for data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. During data transfers, reads of these bits will return invalid data and writes will be ignored.
<table>
<tr><th>Bits</th><th>Size</th></tr>
<tr><td>0000h</td><td>No Data Transfer
(Not supported)</td></tr>
<tr><td>0001h</td><td>1 Byte</td></tr>
<tr><td>0002h</td><td>2 Bytes</td></tr>
<tr><td>0003h</td><td>3 Bytes</td></tr>
<tr><td>---</td><td>---</td></tr>
<tr><td>01FFh</td><td>511 Bytes</td></tr>
<tr><td>0200h</td><td>512 Bytes</td></tr>
<tr><td>0400h</td><td>1024 Bytes</td></tr>
<tr><td>0800h</td><td>2048 Bytes</td></tr>
<tr><td>(0FFFh</td><td>4095 Bytes</td></tr>
</table></td></tr>
</table>

15.3.3 BLKCNT—Block Count Register

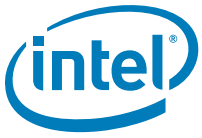
I/O Offset: Base + (06h-07h) Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:0	0000h R/W	**Count (C):** Contains the number of blocks to be transferred. During a transfer operation, read operations to this register will return invalid data and writes will be ignored. When a suspend command is received by the controller, this register will reflect the number of blocks yet to be transferred.

15.3.4 CMDARG—Command Argument Register

I/O Offset: Base + (08h-0Bh) Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	00000000h R/W	**Argument (A):** Contains the command to be transmitted. Maps to bits 39:8 of the command format in the SD/MMC card specifications.



15.3.5 XFRMODE—Transfer Mode Register

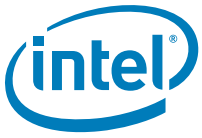
I/O Offset: Base + (0Ch-0Dh) Attribute: R/O, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:7	00h RO	Reserved
6	0 RW	**CMC COMP ATA:** Command Completion Signal Enable for CE-ATA Device 0 = Device will not send command completion signal 1 = Device will send command completion signal
5	0 R/W	**Multiple Block Select (MBS):** Enables multiple block data transfers on the data bus. 0 = Single block transfers only 1 = Multi-block transfers allowed
4	0 R/W	**Data Direction (DATDIR):** Defines the direction of data transfers. 0 = Write (Host to Client) 1 = Read (Client to Host)
3	0 RO	Reserved
2	0 R/W	**Auto CMD12 Enable (AC12EN):** Multiple block transfers for memory require CMD12 be issued to stop the transaction. 0 = Do not automatically issue the CMD12 command after the last block transfer. 1 = Automatically issue the CMD12 command when the last block transfer is completed.
1	0 R/W	**Block Count Enable (BCE):** This bit is only relevant for multi-block transfers. 0 = Disables the block counter 1 = Enables the block counter
0	0 R/W	**DMA Enable (DMAEN):** DMA transfers may only be enabled if the DMA Support bit in the capabilities register is set. A DMA transfer begins with software writes to the upper bute of the DMA Address register 0 = Disable DMA transfers 1 = Enable DMA transfers

15.3.6 XFRMODE—Transfer Mode Register

I/O Offset: Base + (0Ch-0Dh) Attribute: R/O, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:6	00h RO	Reserved
5	0 R/W	**Multiple Block Select (MBS):** Enables multiple block data transfers on the data bus. 0 = Single block transfers only 1 = Multi-block transfers allowed
4	0 R/W	**Data Direction (DATDIR):** Defines the direction of data transfers. 0 = Write (Host to Client) 1 = Read (Client to Host)
3	0 RO	Reserved
2	0 R/W	**Auto CMD12 Enable (AC12EN):** Multiple block transfers for memory require CMD12 be issued to stop the transaction. 0 = Do not automatically issue the CMD12 command after the last block transfer. 1 = Automatically issue the CMD12 command when the last block transfer is completed.
1	0 R/W	**Block Count Enable (BCE):** This bit is only relevant for multi-block transfers. 0 = Disables the block counter 1 = Enables the block counter
0	0 R/W	**DMA Enable (DMAEN):** DMA transfers may only be enabled if the DMA Support bit in the capabilities register is set. A DMA transfer begins with software writes to the upper bute of the DMA Address register 0 = Disable DMA transfers 1 = Enable DMA transfers



15.3.7 CMD—Command Register

I/O Offset: Base + (0Eh-0Fh) Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:14	00b RO	Reserved
13:8	00h R/W	**Command Index (CMDIDX):** Contain the command number (ex: CMD16, ACMD51, etc.) that is specified in bits 45:40 of the Command-Format in the SD Memory Card Physical Layer and SDIO Card Specifications.
7:6	00b R/W	**Command Type (CT):** 00b = Normal 01b = Suspend (CMD52 for writing “Bus Suspend” in CCCR) 10b = Resume 11b = Abort
5	0 R/W	**Data Present Select (DPS):** This bit is set to indicate that data is present and shall be transferred using SD_DAT. It is cleared for the following: • Commands using only CMD line (ex. CMD52). • Commands with no data transfer but using busy signal on DAT[0] (ex. CMD38) • Resume command
4	0 R/W	**Command Index Check Enable (CICE):** This bit determines if the command and response index fields should be compared. 0 = Do not check the index field 1 = Compare the index fields of the command and response. If the indices do not match a Command Index Error is reported.
3	0 R/W	**Command CRC Check Enable (CCCE):** Checks for errors in the CRC field in the response. 0 = Disable CRC field checking 1 = Check the CRC field for errors. If an error is detected, a Command CRC Error is reported.
2	0 R/W	Reserved
1:0	00b R/W	**Response Length Select (RSPLENSEL)** 00b = No Response 01b = Response length 136 10b = Response length 48 11b = Response length 48 (check busy after response)

15.3.8 RESP—Response Register

I/O Offset: Base + (10h-1Fh) Attribute: R/W
Default Value: all zeros Size: 128 bits

The Response Register holds the data content that was transmitted by the SDIO/MMC device to the host controller as part of its response to a command. Only specific portions of this 128-bit register are used at any one time depending on the type of response send from the client device.

Bit	Default and Access	Description
127:0	0s R/W	**Command Response (RESP):** Contains the content portion of a card's response to commands issued from the SDIO/MMC host controller.

15.3.9 BUFDATA—Buffer Data Register

I/O Offset: Base + (20h-23h) Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	00000000h R/W	**Buffer Data (BD):** The Intel® SCH buffer data is accessed by this register.

15.3.10 PSTATE—Present State Register

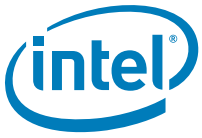
I/O Offset: Base + (24h–27h) Attribute: RO, R/W, ROC
Default Value: 00000000h Size: 32 bits

The PSTATE register indicates what SD_DAT[7:0] signal(s) are in use.

Bit	Default and Access	Description
31:25	00h RO	Reserved
24	0 RO	**Command Level (CMDLVL):** This bit reflects the state of the SDn_CMD signal.
23:20	0h RO	**SD_DAT[3:0] Signal Level (D30LVL):** The levels on these 4 bits mirror the levels of the corresponding SD_DAT bus signals: **Bit Signal** 23 SD_DAT[3] 22 SD_DAT[2] 21 SD_DAT[1] 20 SD_DAT[0]
19	0 RO	**Write Protect (WP):** This bit reflects the status of the SDn_WP signal used for memory cards. 0 = Write Enabled (SDn_WP = 0) 1 = Write Protected (SDn_WP = 1)

Bit	Default and Access	Description
18	0 RO	**Card Detect (CD):** This bit reflects the **inverted** status of the SD_CD# signal. 0 = Card not detected (SD_ CD# = 1) 1 = Card detected (SD_CD# = 0)
17	0 RO	**Card State Stable (CSS):** This bit reflects the stability of the SD_CD# signal and can be used for testing. This state of this bit is not altered by the Software Reset register. 0 = SD_CD# is not stable 1 = SD_CD# is stable (either high or low)
16	0 RO	**Card Inserted (CI):** This bit indicates if a card has been inserted. A 0-to-1 transition of this bit triggers a Card Insertion interrupt. Conversely, a 1-to-0 transition will trigger a Card Removal interrupt. This state of this bit is not altered by the Software Reset register. If a Card is removed while its power is on and its clock is oscillating, the host controller shall turn off the bus by clearing PWRCTL.BUSPWR and CLKCTL.CLKEN. The host controller should then clear SWRST.SRFA. The card detect is active regardless of the SD Bus Power. 0 = Reset/Debouncing/No Card 1 = Card Inserted
15:12	0h RO	Reserved
11	0 ROC	**Buffer Read Enable (BRE):** The status of this bit should be used for non-DMA reads. A 1-to-0 transition of this bit occurs when all the block data is read from the buffer. A 0-to-1 transition occurs when all the block data is ready in the buffer and generates a Buffer Read Ready interrupt. 0 = Read Disable. All blcok data has been read. 1 = Read Enable. Valid data exists in the host's buffer.
10	0 ROC	**Buffer Write Enable (BUFWREN):** The status of this bit should be used for non-DMA writes. This read-only flag indicates if space is available for write data. A 1-to-0 transition indicates all the block data has been written to the buffer. A 0-to-1 transition occurs when the top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. 0 = Write Disable 1 = Write Enable. Data may be written to the data buffer.
9	0 ROC	**Read Transfer Active (RTA)** 0 = No data to transfer. The last data block has been received, or When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. 1 = Transferring data. The end bit of a read command has been received, or the Continue Request bit of the BLKGAPCTL register was set. A 1-to-0 transition will cause a Transfer Complete interrupt to be generated.

Bit	Default and Access	Description
8	0 ROC	**Write Transfer Active (WTA)** 0 = No valid write data exists in the host controller. This bit is cleared in either of the following cases: – After getting the CRC status of the last data block as specified by the transfer count – After getting a CRC status of any block where data transmission was stopped by a Stop At Block Gap 1 = Transferring data This bit is set in either of the following cases: – After the end bit of the write command. – When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer.
7:3	0h	Reserved
2	0 ROC	**DAT Line Active (DLA):** Indicates if one of the SD_DAT lines is currently in use. 0 = SD_DATx is inactive 1 = SD_DATx is active
1	0 ROC	**DAT-Command Inhibit (DCI):** This bit is set if either the DLA or RTA bits are set to 1. Clearing this bit sets NIS.TC. 0 = A command using the SD_DAT bus cannot be issued. 1 = A command using the SD_DAT bus can be issued.
0	0 ROC	**Command Inhibit (CI)**. 0 = Indicates SD_CMD is not in use and that the host controller may issue a command using the SD_CMD signal. 1 = The controller cannot issue a commend because of a command conflict error or because of a Command Not Issued By AutoCMD12 Error.



15.3.11 HOSTCTL—Host Control Register

I/O Offset: Base + 28h Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:4	0000b RO	Reserved
3	0 R/W	**8-bit MMC Support (MMC8):** If set, (and bit 1 = 0) the Intel® SCH supports 8-bit MMC. When cleared the Intel® SCH does not support this feature
2	0 R/W	**High Speed Enabled (HSEN):** High-speed mode will cause to the controller to drive SD_CMD and SD_DAT[7:0] at the rising edge of SD_CLK. Default mode is to output at the falling edge of SD_CLK for normal speed operation. 0 = Normal Speed Mode 1 = High Speed Mode
1	0 R/W	**Data Transfer Width (DTW):** If SD8M is 0, this bit will determine the final width of the data transfers on SD_DAT[7:0]. 0 = 1-bit mode 1 = 4-bit mode
0	0 R/W	**LED Control (LEDCTL):** This bit turns the external LED on or off. 0 = LED is off 1 = LED is on

15.3.12 PWRCTL—Power Control Register

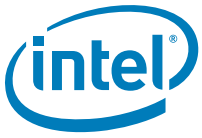
I/O Offset: Base + (29h) Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:4	0h RO	Reserved
3:1	000b R/W	**SD Bus Voltage Select (VSEL):** Only 111b (3.3 V) may be written to these bits. Other values will be ignored.
0	0 R/W	**SD Bus Power Enable (PWREN)** 0 = The SD Bus is not powered 1 = The SD Bus is powered

15.3.13 BLKGAPCTL—Block Gap Control Register

I/O Offset: Base + (2Ah) Attribute: RO, R/W
Default Value: 00 Size: 8 bits

Bit	Default and Access	Description
7:4	0h RO	Reserved
3	0 R/W	**Interrupt At Block Gap:** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card.
2	0 R/W	**Read Wait Control (RWC):** If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the DAT[2] line. Otherwise the Intel® SCH stops SD Clock to hold read data. When software detects an card insertion, if the card does not support read wait, this bit shall never be set. If this bit is cleared, Suspend/Resume cannot be supported.
1	0 R/W	**Continue Request (CR):** This bit is used to restart a transaction which was stopped using the SBC bit. To cancel stop at the block gap, clear SBC to 0 and set this bit to restart the transfer. Intel® SCH automatically clears this bit in either of the following cases: • Read transaction: PS.DLA changes from 0 to 1 as a read transaction restarts. • Write transaction: PS.WTA changes from 0 to 1 as the write transaction restarts. It is not necessary for software to clear this bit. If SR is set, any write to this bit is ignored.
0	0 R/W	**Stop Request (SR):** This is used to stop executing a transaction at the next block gap for both DMA and non-DMA transfers. Until the Transfer Complete is set to 1, indicating a transfer completion software shall leave this bit set to 1. Clearing both this bit and CR shall not cause the transaction to restart. RWC is used to stop the read transaction at the block gap. Intel® SCH shall honor this bit for write transfers, but for read transfers it requires that the card support Read Wait. Software shall not set this bit during read transfers unless the card supports Read Wait and has set RWC. In the case of write transfers in which software writes data to the Buffer Data Port register, software shall set this bit after all block data is written. If set, software shall not write data to Buffer Data Port register. This bit affects PS.RTA, PS.WTA, PS.DLA and Command Inhibit (DAT) in the Present State register.



15.3.14 WAKECTL—Wake Control Register

I/O Offset: Base + 2Bh Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:3	00h RO	Reserved
2	0 R/W	**Card Removal Enable (CRME):** FN_WUS (Wake Up Support) in CIS does not effect this bit. 0 = Wakeup events will not be triggered due to a card removal interrupt. 1 = Enables wakeup event when a Card Removed interrupt is detected (NINTSTS.CR).
1	0 R/W	**Card Insertion Enable (CINE):** FN_WUS (Wake Up Support) in CIS does not effect this bit. 0 = Wakeup events will not be triggered due to a card insertion interrupt. 1 = Enables wakeup event when a Card Insertion interrupt is detected (NINTSTS.CIN).
0	0 R/W	**Card Interrupt Enable (CIE):** When set, enables wakeup event by Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. 0 = Wakeup events will not be triggered due to a card interrupt. 1 = Enables wakeup event with a Card Interrupt is detected (NINTSTS.CI).

15.3.15 CLKCTL—Clock Control Register

I/O Offset: Base + (2Ch-2Dh) Attribute: RO, R/W
Default Value: 00h Size: 16 bits

Bit	Default and Access	Description
15:8	00h R/W	**Frequency Divisor (FD):** This register is used to select the final frequency of SDCLK pin. The value of these bits determines a divisor to be applied to the Base Clock Frequency (found in the Capabilities register). Only the following settings are allowed: 80h divide by 256 40h divide by 128 20h divide by 64 10h divide by 32 08h divide by 16 04h divide by 8 02h divide by 4 01h divide by 2 00h Base clock (10 MHz – 63 MHz) When setting multiple bits, the most significant bit is used as the divisor. The two default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register. At the initialization of the controller, these bits will be set according to the Capabilities register.
7:3	0h RO	Reserved
2	0 R/W	**Clock Enable (CLKEN)** 0 = SD_CLK is disabled. The controller clears this bit if no card is detected. 1 = SD_CLK is enabled. The FD bits may not be changed.
1	0 RO	**Internal Clock Stable (ICS):** This bit is set to 1 when SD Clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. This is useful when using PLL for a clock oscillator that requires setup time.
0	0 R/W	**Internal Clock Enable (ICE):** This bit is set to 0 when the Host Driver is not using the Host Controller or the Host Controller awaits a wakeup interrupt. The Host Controller should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the Host Controller shall set in this register to 1. This bit shall not effect card detection.

15.3.16 TOCTL—Timeout Control Register

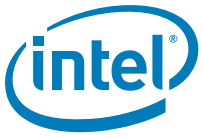
I/O Offset: Base + (2Eh) Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:4	0h RO	Reserved
3:0	0h R/W	**Data Timeout Counter Value (DTCV):** This value determines the interval by which SD_DAT line timeouts are detected. Refer to the Data Timeout Error in the Error Interrupt Status register for information on factors that dictate timeout generation. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). **Bit Code** / **Description** 1111b: Reserved 1110b: TMCLK × 2^{27} ---: --- 0001b: TMCLK × 2^{14} 0000b: TMCLK × 2^{13} At the initialization of the controller, these bits will be set according to the Capabilities register.

15.3.17 SWRST—Software Reset Register

I/O Offset: Base + (2F) Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:3	0h RO	Reserved
2	0 RWAC	**Software Reset for SD_DAT:** The following registers and bits are cleared by this bit: Register: Buffer Data (BUFDATA) — Bits: All Register: Present State (PSTATE) — Bits: Buffer Read Enable; Buffer Write Enable; Read Transfer Active; Write Transfer Active DAT Line Active; Command Inhibit (DAT) Register: Block Gap Control (BLKGAPCTL) — Bits: Continue Request; Stop At Block Gap Request Register: Normal Interrupt Status (NINTSTS) — Bits: Buffer Read Ready; Buffer Write Ready; DMA Interrupt; Block Gap Event
1	0 R/W	**Reset CMD (RC)**. When set, the following bits are cleared: PSTATE.CI, NINTSTS.CC
0	0 R/W	**Reset All (ALL)**. This bit resets the entire host controller except the card detection circuit. Which includes the DMA system address and Buffer Data Port. 1 = The SD controller shall reset itself.



15.3.18 NINTSTS—Normal Interrupt Status Register

I/O Offset: Base + (30h-31h) Attribute: RO, R/WC
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15	0 RO	**Error Interrupt (EI):** This bit allows the software to efficiently test for an error by checking this bit before scanning all bits in the Error Interrupt Status (ERINTSTS) register. 0 = No bits in ERINTSTS are set 0 = At least one bit in ERINTSTS has been set
14:9	00h RO	Reserved
8	0 RO	**Card Interrupt (CI):** This bit is cleared by resetting the SD card interrupt factor. In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. It is necessary to define how to handle this delay. When this status has been set and the Host Driver needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status Enable register shall be set to 0 in order to clear the card interrupt statuses latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (it should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again.
7	0 R/WC	**Card Removed (CRM):** This bit is cleared by writing a 1 to it. 0 = Card state stable or debouncing. 1 = Card Removed. Set when PSTATE.CI is cleared. When software clears this bit (by writing a 1 to it), the status of the PSTATE.CI bit should be confirmed to ensure no card detect interrupts are missed.
6	0 R/WC	**Card Insertion (CIN):** This bit is cleared by writing a 1 to it. 0 = Card state stable or debouncing 1 = Card Inserted. Set when PSTATE.CI is set. When software clears this bit (by writing a 1 to it), the status of the PSTATE.CI bit should be confirmed to ensure no card detect interrupts are missed.
5	0 R/WC	**Buffer Read Ready (BRR):** Set when PSTATE.BRE is set.
4	0 R/WC	**Buffer Write Ready (BWR):** Set when PSTATE.BWE is set.
3	0 R/WC	**DMA Interrupt:** This status is set if the Host Controller detects the Host DMA Buffer boundary during transfer. Refer to the Host DMA Buffer Boundary in the Block Size register. Other DMA interrupt factors may be added in the future. This interrupt shall not be generated after the Transfer Complete.

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>2</td><td>0
R/WC</td><td>Block Gap Event (BGE): Operation of this bit is enabled if BLKGAPCTL.SR is set.
• Read: This bit is set at the falling edge of the DAT Line Active Status, when the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function.
• Write: Set at the falling edge of Write Transfer Active Status (After getting CRC status at SD Bus timing.</td></tr>
<tr><td>1</td><td>0
R/WC</td><td>Transfer Complete (TC): This bit is set when a read/write transfer is completed.
• Read: This bit is set at the falling edge of Read Transfer Active Status. There are two cases in which this interrupt is generated. The first is when a data transfer is completed as specified by data length (After the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the Stop At Block Gap Request in the Block Gap Control register (After valid data has been read to the Host System). Refer to Section 3.10.3 for more details on the sequence of events.
• Write: This bit is set at the falling edge of the DAT Line Active Status. There are two cases in which this interrupt is generated. The first is when the last data is written to the SD card as specified by data length and the busy signal released. The second is when data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control register and data transfers completed. (After valid data is written to the SD card and the busy signal released). Refer to Section 3.10.4 for more details on the sequence of events.
The table below shows that Transfer Complete has higher priority than Data Timeout Error. If both bits are set to 1, the data transfer can be considered complete.
TC | Timeout Error | Meaning of the status
0 | 0 | Interrupted by another factor
0 | 1 | Timeout occur during transfer
1 | Don't Care | Data transfer complete</td></tr>
<tr><td>0</td><td>0
R/WC</td><td>Command Complete (CC): This bit is set when get the end bit of the command response. (Except Auto CMD12) Refer to PSTATE.CI. The table below shows that ERINTSTS.CTE has higher priority than this bit. If both bits are set, the response was not received correctly.
CC | CMD Timeout Error | Meaning of the status
0 | 0 | Interrupted by another factor
1 | 0 | Response received
X | 1 | Response not received within 64 SDCLK cycles.</td></tr>
</table>

15.3.19 ERINTSTS—Error Interrupt Status Register

I/O Offset: Base + (32h-33h) Attribute: RO, R/WC
Default Value: 0000h Size: 16 bits

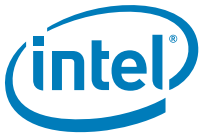
Bit	Default and Access	Description
15:9	00h RO	Reserved
8	0 R/WC	**Auto CMD12 Error (AC12):** Occurs when detecting that one of the bits in AC12ES has been set. This bit is set not only on errors on Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error.
7	0 R/WC	**Current Limit Error (CL):** By setting PC.BP, Intel® SCH is requested to supply power to the SD Bus. If Intel® SCH supports the Current Limit function, it can be protected from an invalid card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the Host Controller is not supplying power to SD card due to some failure. Reading 0 means that the Host Controller is supplying power and no error has occurred. The Host Controller may require some sampling time to detect the current limit. If the Host Controller does not support this function, this bit shall always be set to 0.
6	0 R/WC	**Data End Bit Error:** Occurs either when detecting 0 at the end bit position of read data which uses the DAT line or at the end bit position of the CRC Status.
5	0 R/WC	**Data CRC Error:** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC status having a value of other than 010.
4	0 R/WC	**Data Timeout Error (DTE):** Occurs when detecting one of following timeout conditions: • Busy timeout for R1b,R5b type • Busy timeout after Write CRC status • Write CRC Status timeout • Read Data timeout.
3	0 R/WC	**Command Index Error (CIE):** Occurs if a command index error occurs in the command response.
2	0 R/WC	**Command End Bit Error (CEBE):** Occurs when the end bit of a command response is 0.
1	0 R/WC	**Command CRC Error (CCE):** Command CRC Error is generated in two cases. • If a response is returned and CTE is cleared, this bit is set when detecting a CRC error in the command response. • If Intel® SCH drives SD_CMD to 1, but detects 0 on the next SD_CLK edge, Intel® SCH aborts the command (stops driving CMD line) and sets this bit. CTE shall also be set.
0	0 R/WC	**Command Timeout Error (CTE):** Occurs only if no response is returned within 64 SDCLKs from the end bit of the command. If Intel® SCH detects a CMD line conflict, in which case Command CRC Error shall also be set, this bit shall be set and the command will be aborted.

15.3.20 NINTEN—Normal Interrupt Enable Register

I/O Offset:	Base + (34h-35h)	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

These bits enable or mask the different normal interrupts.

Bit	Default and Access	Description
15	0 RO	Reserved: Hardcoded to 0.
14:9	00h RO	Reserved
8	0 R/W	**Card Interrupt Status Enable (CISE):** This bit should be cleared before servicing a Card Interrupt, and then enabled after all interrupt requests from the card are serviced and cleared. 0 = Card Interrupt reporting is masked 1 = Card Interrupt reporting is enabled
7	0 R/W	**Card Removal Status Enable (CRSE)**
6	0 R/W	**Card Insertion Status Enable (CISE)**
5	0 R/W	**Buffer Read Ready Status Enable (BRSE)**
4	0 R/W	**Buffer Write Ready Status Enable (BWSE)**
3	0 R/W	**DMA Interrupt Status Enable (DISE)**
2	0 R/W	**Block Gap Event Status Enable (BGSE)**
1	0 R/W	**Transfer Complete Status Enable (TCSE)**
0	0 R/W	**Command Complete Status Enable (CCSE)**



15.3.21 ERINTEN—Error Interrupt Enable Register

I/O Offset: Base + (36h-37h) Attribute: RO, R/WC
Default Value: 0000h Size: 16 bits

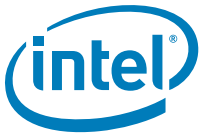
Bit	Default and Access	Description
15:9	00h RO	Reserved
8	0 R/WC	**Auto CMD12 Error Enable**
7	0 R/WC	**Current Limit Error Enable**
6	0 R/WC	**Data End Bit Error Enable**
5	0 R/WC	**Data CRC Error Enable**
4	0 R/WC	**Data Timeout Error Enable**
3	0 R/WC	**Command Index Error Enable**
2	0 R/WC	**Command End Bit Error Enable**
1	0 R/WC	**Command CRC Error Enable**
0	0 R/WC	**Command Timeout Error Enable**

15.3.22 NINTSIGEN—Normal Interrupt Signal Enable Register

I/O Offset:	Base + (38h-39h)	Attribute:	RO, R/WC
Default Value:	0000h	Size:	16 bits

This register is used to select which normal interrupt status is indicated to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables Interrupt generation.

Bit	Default and Access	Description
15:9	00h RO	Reserved
8	0 R/W	**Card Interrupt Signal Enable**
7	0 R/W	**Card Removal Signal Enable**
6	0 R/W	**Card Insertion Signal Enable**
5	0 R/W	**Buffer Read Ready Signal Enable**
4	0 R/W	**Buffer Write Ready Signal Enable**
3	0 R/W	**DMA Interrupt Signal Enable**
2	0 R/W	**Block Gap Event Signal Enable**
1	0 R/W	**Transfer Complete Signal Enable**
0	0 R/W	**Command Complete Signal Enable**



15.3.23 ERINTSIGEN—Error Interrupt Signal Enable Register

I/O Offset:	Base + (3Ah-3Bh)	Attribute:	RO, R/WC
Default Value:	0000h	Size:	16 bits

This register is used to select which interrupt status is notified to the Host System as the Interrupt. These status bits all share the same 1-bit interrupt line. Setting any of these bits to 1 enables interrupt generation. Non-reserved bits in this register are cleared by writing a 1 to them.

Bit	Default and Access	Description
15:9	0h RO	Reserved
8	0 R/WC	**Auto CMD12 Error Signal Enable**
7	0 R/WC	**Current Limit Error Signal Enable**
6	0 R/WC	**Data End Bit Error Signal Enable**
5	0 R/WC	**Data CRC Error Signal Enable**
4	0 R/WC	**Data Timeout Error Signal Enable**
3	0 R/WC	**Command Index Error Signal Enable**
2	0 R/WC	**Command End Bit Error Signal Enable**
1	0 R/WC	**Command CRC Error Signal Enable**
0	0 R/WC	**Command Timeout Error Signal Enable**

15.3.24 AC12ERRSTS—Automatic CMD12 Error Status Register

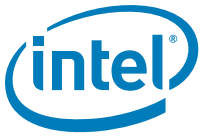
I/O Offset: Base + (3Ch-3Dh) Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:8	00h RO	Reserved
7	0 RO	**Command Not Issued Error (NCIE):** When set, indicates than a command (without SD_DAT being used) was not executed due to an Index Error, End Bit Error, CRC Error, or Timeout Error.
6:5	00b RO	Reserved
4	0 RO	**Index Error (IE):** Occurs if the Command Index Error occurs in response to a command.
3	0 RO	**End Bit Error (EBE):** Occurs when the end bit if a command response is 0.
2	0 RO	**CRC Error (CRCE):** Occurs in a CRC error is detected in the command response.
1	0 RO	**Timeout Error (TE):** If no response is returned within 64 SD_CLK's from the command end bit, this will be set. If set, IE, EBE, and CRCE have no meaning.
0	0 RO	**Not Executed (NE):** Indicates that an error has prevented the Intel® SCH from issuing the AutoCMD12 to stop a multiple-block transfer. If set, TE, IE, EBE, and CRCE have no meaning.

15.3.25 CAP—Capabilities Register

I/O Offset: Base + (40h-43h) Attribute: RO
Default Value: 00000060h Size: 32 bits

Bit	Default and Access	Description
63:27	00h RO	Reserved
26	0 RO	**Support for 1.8 V (S18)** 0 = indicates 1.8 V is not supported.
25	0 RO	**Support for 3.0 V (S30)** 0 = indicates 3.0 V is not supported.
24	1 RO	**Support for 3.3 V (S33)** 1 = indicates that 3.3 V is supported.
23	0 RO	**Suspend/Resume Support (SRS)** 1 = Suspend and Resume are not supported 0 = Suspend and Resume are supported
22	1 RO	**DMA Support (DMA)** 1 = indicates that DMA transfers are supported.



<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>21</td><td>1
RO</td><td>High-Speed Support (HS)
1 = indicates that high-speed operation is supported.</td></tr>
<tr><td>20:18</td><td>000b
RO</td><td>Reserved</td></tr>
<tr><td>17:16</td><td>desc
RO</td><td>Max Block Length (MBL): The maximum block length is fixed by these bits.

<table>
<tr><th>Function</th><th>Bits</th><th>Max Block Size</th></tr>
<tr><td>D30:F0</td><td>10</td><td>2048 bytes</td></tr>
<tr><td>D30:F1</td><td>00</td><td>512 bytes</td></tr>
<tr><td>D30:F2</td><td>00</td><td>512 bytes</td></tr>
</table>
</td></tr>
<tr><td>15:14</td><td>00b
RO</td><td>Reserved</td></tr>
<tr><td>13:8</td><td>30h
RO</td><td>Base Clock Frequency for SD_CLK (BCF): This value indicates the base (maximum) clock frequency for the SD Clock. Unit values are 1 MHz.
If the real frequency is 16.5MHz, the lager value shall be set 01 0001b (17 MHz) because the Host Driver use this value to calculate the clock divider value (Refer to the SDCLK Frequency Select in the Clock Control register.) and it shall not exceed upper limit of the SD Clock frequency.
The supported clock range is 10 MHz to 63 MHz.
If these bits are all 0, the Host System has to get information using another method.</td></tr>
<tr><td>7</td><td>1
RO</td><td>Timeout Clock Unit (TCU): This bit shows the unit of base clock frequency used to detect Data Timeout Error.
0 = kHz,
1 = MHz</td></tr>
<tr><td>6</td><td>0
RO</td><td>Reserved</td></tr>
<tr><td>5:0</td><td>30h
RO</td><td>Timeout Clock Frequency (TCF): This bit shows the base clock frequency used to detect Data Timeout Error. The Timeout Clock Unit defines the unit of this fields value.
Timeout Clock Unit =0 [kHz] unit: 1 kHz to 63 kHz
Timeout Clock Unit =1 [MHz] unit: 1 MHz to 63 MHz
Not 0 1 kHz to 63 kHz or 1 MHz to 63 MHz</td></tr>
</table>

15.3.26 MCCAP—Maximum Current Capabilities Register

I/O Offset: Base + (48h-4Bh) Attribute: RO
Default Value: 00000000 00000000h Size: 32 bits

Bit	Default and Access	Description
63:24	00h RO	Reserved
23:16	00h RO	**Maximum Current for 1.8 V** 000 - Get Information from other sources
15:8	00h RO	**Maximum Current for 3.0 V** 000 - Get Information from other sources
7:0	01h RO	**Maximum Current for 3.3 V** This field reports the max current that the power supply can deliver to the SDIO card. 01 = 4 mA is the max current that the controller can deliver. However, The Intel® SCH does not report the actual max current, software should ignore the max current value reported in this field.

15.3.27 SLTINTSTS—Slot Interrupt Status Register

I/O Offset: Base + (FCh-FDh) Attribute: RO
Default Value: 0000h Size: 16 bits

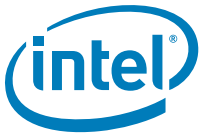
Bit	Default and Access	Description
15:1	0000h RO	Reserved
0	0 RO	**Slot 0 Interrupt:** Logical OR of the Interrupt Signal and Wakeup Signal.

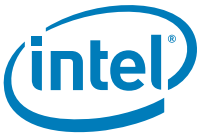
15.3.28 HCVER—Host Controller Version Register

I/O Offset: Base + (FEh–FFh) Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:8	00h RO	**Vendor Version Number (VVN):** 00h indicates the first version.
7:0	00h RO	**Specification Version Number (SVN):** 00h indicates support for specification version 1.0.

§ §





16 Parallel ATA (D31:F1)

16.1 Functional Overview

The Intel® SCH PATA interface supports only the primary channel, with one master and one slave device. Any writes to the secondary channel are ignored, and reads will return all ones, except for bit 7, which returns a 0.

The Parallel ATA (PATA) controller in the Intel® SCH supports three types of data transfers:

1. Programmed I/O (PIO): A protocol used to transfer data between the processor as the ATA device. PIO allows transfer rates up to 16 MB/s.
2. Multi-word DMA: DMA protocol that resembles the DMA on the ISA bus. Allows transfer rates of up to 16 MB/s.
3. Ultra-DMA: Source synchronous DMA protocol that allows transfer rates of up to 100 MB/s.

Table 46. Supported PATA Standards and Modes

PATA Standard	Transfer Modes Supported	Transfer Rate (MB/s)
ATA-1 (ATA, IDE)	PIO Modes 0, 1, 2	3.3, 5.2, 8.3
	Single-word DMA Modes 0, 1, 2	2.1, 4.2, 8.3
	Multi-word DMA Mode 0	4.2
ATA-2, ATA-3 (EIDE, Fast ATA)	PIO Modes 3,4	11.1, 16.6
	Multi-word DMA Modes 1,2	13.3, 16.6
ATA/ATAPI-4 (Ultra DMA, Ultra ATA)	Ultra DMA Modes 0,1, 2 (a.k.a. Ultra DMA/33)	16.7, 25.0, 33.3
ATA/ATAPI-5 (Ultra-DMA, Ultra ATA)	Ultra DMA Modes 3, 4 (a.k.a. Ultra DMA/66)	44.4, 66.7
ATA/ATAPI-6 (Ultra-DMA, Ultra ATA)	Ultra-DMA Mode 5 (a.k.a. Ultra DMA/100)	100 (reads) 89 (writes)

16.1.1 Programmed I/O Transfers

The Programmed I/O (PIO) transfer method uses the processor to move data between an I/O port and main memory through individual operations. A typical sequence follows:

- The processor programs the I/O device with a command.
- Data is transferred (either as a series of PIO operations to the data port or as a DMA operation)
- The I/O device asserts an interrupt when all data has been transferred.
- The processor reads status information from the device.

16.1.1.1 ATA Port Decode

Table 47 specifies the registers that effect the Intel® SCH hardware definition. The Data Register must be accessed using 16-bit or 32-bit I/O instructions. All other registers must be accessed using 8-bit I/O instructions. These following registers are implemented in the device.

Table 47. ATA Command Block Registers (PATA_DCS1#)

I/O Offset	Function (Read)	Function (Write)
00h	Data	Data
01h	Error	Features
02h	Sector Count	Sector Count
03h	Sector Number	Sector Number
04h	Cylinder Low	Cylinder Low
05h	Cylinder High	Cylinder High
06h	Drive	Head
07h	Status	Command

Table 48. ATA Control Block Registers (PATA_DCS3#)

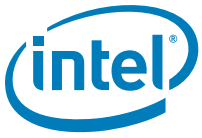
I/O Offset	Function (Read)	Function (Write)
00h	Reserved	
01h	Reserved	
02h	Alt Status	Device control
03h	Forward to LPC - Not claimed by IDE	

The command and control blocks are accessible at fixed I/O addresses. These blocks are decoded when CMD.IOSE is set. An access to these addresses results in the assertion of the appropriate chip select (PATA_DCS1# / PATA_DCS3#) and the command strobes (PATA_DIOR#, PATA_DIOW#).

There are two I/O ranges: the Command Block, which corresponds to the PATA_DCS1# chip select, and the Control Block, which corresponds to the PATA_DCS3# chip select. The Command Block is an 8-byte range, while the control block is a 4-byte range.

- **Command Block Offset:** 01F0h for Primary, 0170h for Secondary
- **Control Block Offset:** 03F4h for Primary, 0374h for Secondary

The secondary range, while active, does not result in cycles on the interface.



16.1.1.2 PIO Cycle Timings

16.1.1.2.1 PIO Timing Modes

An ATA transaction consists of startup latency, cycle latency, and shutdown latency.

- Startup latency provides the setup time for chip select and address pins with respect to the read and write strobes.
- Cycle latency consists of the I/O strobe assertion length and recovery time. Recovery time is provided so that transactions may occur back to back on the interface without incurring additional startup and shutdown latency.
- Shutdown latency is incurred after an outstanding transaction has completed and before another transaction can proceed (such as one to a different address). It provides hold time on the chip select and address pins with respect to the read and write strobes.

Accesses to the data port are the only accesses where multiple cycle latency cycles may run under a single startup and shutdown latency. For non-data port and non-enhanced mode data port transactions, startup and shutdown latency are always incurred. The chip selects are assured to be deasserted for at least two ATA clocks after the deassertion of the I/O strobe for the last transaction and before the Startup latency of the next.

16.1.1.2.2 Waitstates with PATA_IORDY

If PATA_IORDY is deasserted when the initial sample point is reached, additional waitstates are added. Since the rising edge of PATA_IORDY must be synchronized, at least two additional core clocks are added.

16.1.1.2.3 Write Posting

The Intel® SCH absorbs I/O writes to the data port into a buffer when D0TIM.PPE is set. When the buffer is full, subsequent writes are held in wait-states. The buffer can accept writes of 16 bits, and will not accept data until it is completely empty.

16.1.1.2.4 Read Prefetch

Read prefetch is enabled by setting bits in the PCI configuration register 40h: bit 2 for device 0 and bit 6 for device 1. A 32-bit buffer is provided per cable to pre-fetch from each data port. If pre-fetching is enabled, and the command is a “safe” read command, the sector will be pre-fetched. Pre-fetch is not initiated until the first data port read. Pre-fetches from the data port are scheduled as two back-to-back 16-bit reads on the interface.

Words 255 and 256 of the sector are not pre-fetched to avoid fetching across a sector boundary. After the 256th word is read, pre-fetching resumes if a subsequent data port read occurs. If a write to byte 7 of the ATA command block occurs, the buffer is invalidated and pre-fetching is disabled.

16.1.1.3 Cycle Snooping

16.1.1.3.1 Device Active Status

The task file is shared between two devices on a single cable. Ownership is transferred between devices through a write to bit 4 of the Device/Head register (address 1F6h for primary, 176h for secondary). The Intel® SCH snoops this write so that it can run with the proper timings for that device. When cleared, the master or “device 0” owns the cable. When set, the slave or “device 1” owns the cable.

The Intel® SCH only allows pre-fetching of 512-byte sectors, and certain devices. The Intel® SCH snoops writes to the command register. “Safe” read commands are defined in the table below.

- 20h: Read Sector with Retry
- 21h: Read Sector without Retry
- C4h: Read Multiple Sectors

16.1.2 Multi-Word DMA Transfers

In the multi-word DMA and Ultra DMA protocols, the Intel® SCH acts as a bus master to communicate with main memory, and transfers data to the device. The following terms are used for DMA transfers:

- **Read State:** Data transfers from main memory to a device
- **Write State**: Data transfers from a device to main memory.

DMA transfers are performed as scatter-gather. Software builds a table of Physical Region Descriptors (PRDs) in memory that contains base memory addresses for the source or destination of data, and byte counts off that base address. Table 49 and Table 50 show the structure of PRD base address and descriptor information. The Intel® SCH fetches from this table and moves data between the device and memory location pointed to by the table. Each entry in the table is called a Physical Region Descriptor (PRD).

Table 49. PRD Base Address

Bit	Description
31:0	**Data Base Address (DBA):** Indicates the 32-bit offset of the data block.

NOTE: The memory region specified by the descriptor cannot cross a 64 KB boundary.

Table 50. PRD Descriptor Information

Bit	Description
31	**End of List (E):** When set, indicates this is the last entry in the list. Intel® SCH stops processing entries at this point.
30:16	Reserved
15:0	**Byte Count (BC):** Indicates the length, in bytes, of the data block. Bit 0 of this structure must always be 0 to indicate an even number of bytes.

Table 51 describes how to interpret the PATA Status Register bits after a DMA transfer has started.

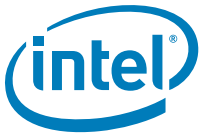


Table 51. Interrupt/Active Bit Interaction

Int	Active	Description
0	1	DMA transfer is in progress.
1	0	The device generated an interrupt. The controller exhausted the PRD. Indicates the size of the PRD was equal to the device transfer size.
1	1	The device generated an interrupt. The controller has not reached the end of the PRD. Indicates the size of the PRD was larger than the device transfer size.
0	0	This is an error condition. The PRD's specified a smaller size than the device's transfer size.

16.1.2.1 DMA Protocol

To initiate a bus master transfer between memory and a PATA device, the following steps are required:

1. Software prepares a PRD table in system memory. The PRD table must be dword-aligned and must not cross a 64 KB boundary.
2. Software provides the starting address of the PRD Table by loading the PRD Table Pointer Register. The direction of the data transfer is specified by setting the Read/Write Control bit. The interrupt bit and Error bit in the Status register are cleared.
3. Software issues the appropriate DMA transfer command to the disk device.
4. The bus master function is engaged by software writing a 1 to the Start bit in the Command Register. The first entry in the PRD table is fetched and loaded into two registers which are not visible by software, the Current Base and Current Count registers. These registers hold the current value of the address and byte count loaded from the PRD table. The value in these registers is only valid when there is an active command to an IDE device.
5. Once the PRD is loaded internally, the PATA device will receive a DMA acknowledge.
6. The controller transfers data to/from memory responding to DMA requests from the PATA device. The PATA device and the host controller may or may not throttle the transfer several times. When the last data transfer for a region has been completed on the IDE interface, the next descriptor is fetched from the table. The descriptor contents are loaded into the Current Base and Current Count registers.
7. At the end of the transfer, the PATA device signals an interrupt.
8. In response to the interrupt, software resets the Start/Stop bit in the command register. It then reads the controller status followed by the drive status to determine if the transfer completed successfully.

The last PRD in a table has the End of List (EOL) bit set. The PCI bus master data transfers terminate when the physical region described by the last PRD in the table has been completely transferred. The active bit in the Status Register is reset and the DDRQ signal is masked.

The buffer is flushed (when in the write state) or invalidated (when in the read state) when a terminal count condition exists; that is, the current region descriptor has the EOL bit set and that region has been exhausted. The buffer is also flushed (write state) or invalidated (read state) when the Interrupt bit in the Bus Master PATA Status register is set. Software that reads the status register and finds the Error bit reset, and either the Active bit reset or the Interrupt bit set, can be assured that all data destined for system memory has been transferred and that data is valid in system memory. Table 51 describes how to interpret the Interrupt and Active bits in the Status Register after a DMA transfer has started.

16.1.3 Synchronous (Ultra) DMA Transfers

The Intel® SCH supports Ultra DMA/100/66/33 bus mastering protocol, providing support for a variety of transfer speeds with PATA devices. Ultra DMA mode 3 provides transfers up to 33 MB/s, Ultra DMA mode 4 provides transfers at up to 44 MB/s or 66 MB/s, and Ultra DMA mode 5 can achieve read transfer rates up to 100 MB/s and write transfer rates up to 88.9 MB/s.

The Ultra DMA definition also incorporates a Cyclic Redundancy Checking (CRC-16) error checking protocol.

16.1.3.1 Operation

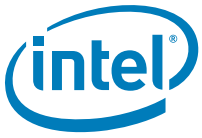
Initial setup programming consists of enabling and performing the proper configuration of the Intel® SCH and the PATA device for Ultra DMA operation. For the Intel® SCH, this consists of enabling synchronous DMA mode and setting up appropriate Synchronous DMA timings.

When ready to transfer data to or from an PATA device, the Bus Master PATA programming model is followed. Once programmed, the PATA device and the Intel® SCH controls the transfer of data by Ultra DMA protocol. The actual data transfer consists of three phases, a start-up phase, a data transfer phase, and a burst termination phase.

The PATA device begins the start-up phase by asserting DMARQ signal. When ready to begin the transfer, the Intel® SCH asserts PATA_DMACK# signal. When PATA_DMACK# signal is asserted, the host controller drives CS0# and CS1# inactive, PATA_DA[2:0] low. For write cycles, the Intel® SCH deasserts STOP, waits for the PATA device to assert PATA_IORDY#, and then drives the first data word and STROBE signal. For read cycles, the Intel® SCH tri-states the PATA_DD lines, deasserts STOP, and asserts PATA_IORDY#. The PATA device then sends the first data word and STROBE.

The data transfer phase continues the burst transfers with the data transmitter (Intel® SCH – writes, PATA device – reads) providing data and toggling STROBE. Data is transferred (latched by receiver) on each rising and falling edge of STROBE. The transmitter can pause the burst by holding STROBE high or low, resuming the burst by again toggling STROBE. The receiver can pause the burst by deasserting DMARDY# and resumes the burst by asserting DMARDY#. The Intel® SCH pauses a burst transaction to prevent an internal line buffer overflow or underflow condition, resuming once the condition has cleared. It may also pause a transaction if the current PRD byte count has expired, resuming once it has fetched the next PRD.

The current burst can be terminated by either the transmitter or receiver. A burst termination consists of a Stop Request, Stop Acknowledge and transfer of CRC data. The Intel® SCH can stop a burst by asserting STOP, with the PATA device acknowledging by deasserting DMARQ. The PATA device stops a burst by deasserting DMARQ and the Intel® SCH acknowledges by asserting STOP. The transmitter then drives the STROBE signal to a high level. The Intel® SCH then drives the CRC value onto the DD lines and deassert DMACK#. The PATA device latches the CRC value on rising edge of DMACK#. The Intel® SCH terminates a burst transfer if it needs to service the opposite PATA channel, if a Programmed I/O (PIO) cycle is executed to the PATA channel currently running the burst, or upon transferring the last data from the final PRD.



16.1.3.2 Ultra DMA Timing

The Cycle Time and Ready to Pause time for Ultra DMA modes are programmed by the D0TIM register. The Cycle Time represents the minimum pulse width of the data strobe (STROBE) signal. The Ready to Pause time represents the number of Base Clock periods that the Intel® SCH waits from deassertion of DMARDY# to the assertion of STOP when it desires to stop a burst read transaction.

The internal Base Clock for Ultra DMA/100 (Mode 5) runs at 133 MHz, and the Cycle Time (CT) must be set for three Base Clocks. The Intel® SCH thus toggles the write strobe signal every 22.5 ns, transferring two bytes of data on each strobe edge. This means that the Intel® SCH performs Mode 5 write transfers at a maximum rate of 88.9 MB/s. For read transfers, the read strobe is driven by the PATA device, and the Intel® SCH supports reads at the maximum rate of 100 MB/s.

16.2 PCI Configuration Registers

All of the PATA registers are in the core power well, and none of the registers can be locked. Any undefined registers in the PATA Register Address Map should be treated as Reserved.

Table 52. PATA Register Address Map

Offset	Mnemonic	Register Name	Default	Type
00h–03h	ID	Identifiers	811A8086	RO
04h–05h	PCICMD	Command Register	0000h	RO, R/W
06h–07h	PCISTS	Device Status	0000h	RO
08h	RID	Revision ID	See Description	RO
09h–0Bh	CC	Class Codes	010180h	RO
0Ch	CLS	Cache Line Size	0000h	RO
0Dh	MLT	Master Latency Timer	0000h	RO
20h–23h	BMBAR	Bus Master Base Address	00000001h	RO, R/W
2Ch–2Fh	SS	Subsystem Identifiers	00000000h	RO, R/W
3Ch–3Dh	INTR	Interrupt Information	See Description	RO, R/W
60h–63h	MC	Miscellaneous Configuration	00000000h	RO, R/W
80h–81h	D0TIM	Device 0 Timing	00000000h	RO, R/W
80h–83h	D1TIM	Device 1 Timing	00000000h	RO, R/W

NOTE: Address locations that are not shown should be treated as Reserved.

16.2.1 ID—Identifiers Register

Offset: 00–03h Attribute: RO
Default Value: 811A8086h Size: 32 bits

Bit	Default and Access	Description
31:16	811Ah RO	**Device ID (DID):** 811Ah indicates this is a PATA controller.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates the company vendor.

16.2.2 PCICMD—Command Register

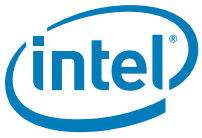
Offset: 04h–05h Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:11	00h RO	Reserved
10	0 R/W	**Interrupt Disable (ID)** 0 = When cleared, IRQ14 may be asserted 1 = When set, IRQ14 is deasserted
9:3	00h RO	Reserved
2	0 R/W	**Bus Master Enable (BME):** This bit controls the host controller's ability to act as a master.
1	0	Reserved
0	0 R/W	**I/O Space Enable (IOSE)** 0 = Disable 1 = Enable. Access to the ATA ports and the DMA registers is enabled

16.2.3 PCISTS—Device Status Register

Offset: 06h–07h Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:4	00h RO	Reserved
3	0 RO	**Interrupt Status (IS):** Reflects the state of interrupt at the input of the enable/disable circuit. This bit is a 1 when the interrupt is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register).
2:0	000b RO	Reserved



16.2.4 RID—Revision ID Register

Offset: 08h Attribute: RO, R/W
Default Value: see description Size: 8 bits

The value reported in this register comes from the RID register in the LPC bridge.

Bit	Default and Access	Description
7:0	see description RO	**Revision ID**: Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the value of the Revision ID Register.

16.2.5 CC—Class Code Register

Offset: 09h–0Bh Attribute: RO
Default Value: 010180h Size: 24 bits

Bit	Default and Access	Description
23:16	01h RO	**Base Class Code (BCC):** This field indicates that this is a mass storage device.
15:8	01h RO	**Sub Class Code (SCC):** This field indicates that this is a device.
7:0	80h RO	**Programming Interface (PIP):** 80h indicates this is a bus master.

16.2.6 CLS—Cache Line Size Register

Offset: 0Ch Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:0	0000h RO	Reserved

16.2.7 MLT—Master Latency Timer Register

Offset: 0Dh Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Default and Access	Description
15:0	0000h RO	Reserved

16.2.8 BMBAR—Bus Master Base Address Register

Offset:	20h–23h	Attribute:	RO, R/W
Default Value:	00000001h	Size:	32 bits

This BAR is used to allocate I/O space for the SFF-8038i mode of operation (DMA).

Bit	Default and Access	Description
31:16	0000h RO	Reserved
15:4	00h R/W	**Base Address (BA):** This field is the base address of the I/O space (16, consecutive I/O locations).
3:1	000b RO	Reserved
0	1 RO	**Resource Type Indicator (RTE):** This bit indicates a request for I/O space.

16.2.9 SS—Sub System Identifiers Register

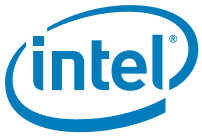
Offset:	2Ch–2Fh	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

The value reported in this register comes from the value of the SS register in the LPC bridge.

16.2.10 INTR—Interrupt Information Register

Offset:	3Ch–3Dh	Attribute:	RO, R/W
Default Value:	see description	Size:	16 bits

Bit	Default and Access	Description
15:8	00h RO	**Interrupt Pin (IPIN):** Reserved
7:0	00h R/W	**Interrupt Line (ILINE):** This field is a software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.



16.2.11 MC—Miscellaneous Configuration Register

Offset:	60h–63h	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

This register provides global configuration parameters for the controller.

Bit	Default and Access	Description
31:3	0s RO	Reserved
2	0 R/W	**Drive Bus to Ground (DBC)** 0 = Pins are in their normal mode 1 = All PATA interface pins are driven to ground
1	0 R/W	**Tristate Bus (TB)** 0 = Pins are in their normal mode 1 = All PATA interface pins are tri-stated.
0	0 RW	**Base Clock Lower Half (BCLH):** This bit determines the base clock to use when building counts. 0 = 100 MHz 1 = 133 MHz

16.2.12 D0TIM/D1TIM—Device 0/1 Timing Register

Offset:	D0TIM: 80h–83h D1TIM: 84h–87h	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

Bit	Default and Access	Description
31	0 R/W	**Use Synchronous DMA (USD)** 0 = Multi-word DMA modes are used for DMA transfers 1 = Synchronous DMA modes are used for DMA transfers
30	0 R/W	**Prefetch/Post Enable (PPE):** When using PIO, this bit enables the prefetch/post buffer.
29:19	0s RO	Reserved

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>18:16</td><td>000b
R/W</td><td>Ultra DMA Mode (UDM): This field indicates which timings to use when running synchronous DMA cycles to the device. 100 MHz timing:
<table>
<tr><th rowspan="2">Bits</th><th rowspan="2">Mode</th><th colspan="2">Intel® SCH Receiving</th><th>Intel® SCH Driving</th></tr>
<tr><th>tcyc</th><th>trp</th><th>tcyc</th></tr>
<tr><td>000</td><td>Mode 0</td><td>7</td><td>16</td><td>12</td></tr>
<tr><td>001</td><td>Mode 1</td><td>5</td><td>13</td><td>8</td></tr>
<tr><td>010</td><td>Mode 2</td><td>4</td><td>10</td><td>6</td></tr>
<tr><td>011</td><td>Mode 3</td><td>2</td><td>10</td><td>4</td></tr>
<tr><td>100</td><td>Mode 4</td><td>1</td><td>10</td><td>3</td></tr>
<tr><td>101</td><td>Mode 5</td><td>1</td><td>9</td><td>2</td></tr>
<tr><td>110–111</td><td colspan="4">Reserved</td></tr>
</table>
There are also fixed clock counts, regardless of DMA mode, that are used when starting and stopping transactions:
<table>
<tr><th>MC.BC</th><th>tENV</th><th>tLI</th><th>tMLI</th><th>tSS</th></tr>
<tr><td>00</td><td>3</td><td>0</td><td>3</td><td>6</td></tr>
<tr><td>01</td><td>4</td><td>0</td><td>4</td><td>7</td></tr>
<tr><td>10</td><td>4</td><td>0</td><td>4</td><td>8</td></tr>
<tr><td>11</td><td>4</td><td>0</td><td>4</td><td>9</td></tr>
</table></td></tr>
<tr><td>15:10</td><td>000000b
RO</td><td>Reserved</td></tr>
<tr><td>9:8</td><td>00b
R/W</td><td>Mutli-word DMA Mode (MDM): This field indicates which timings to use when running multi-word DMA cycles to the device.
<table>
<tr><th rowspan="2">Bits</th><th rowspan="2">Mode</th><th colspan="2">100 MHz Clock</th></tr>
<tr><th>stb</th><th>Rec</th></tr>
<tr><td>00</td><td>Mode 0</td><td>22</td><td>26</td></tr>
<tr><td>01</td><td>Mode 1</td><td>8</td><td>7</td></tr>
<tr><td>10</td><td>Mode 2</td><td>7</td><td>5</td></tr>
<tr><td>11</td><td colspan="3">Reserved</td></tr>
</table></td></tr>
<tr><td>7:3</td><td>00000b</td><td>Reserved</td></tr>
<tr><td>2:0</td><td>000b
R/W</td><td>PIO Mode (PM): This filled indicates which timings to use when running PIO cycles to the dataport.
<table>
<tr><th>Bits</th><th>Mode</th><th>Startup</th><th>Strobe</th><th>Recovery</th></tr>
<tr><td colspan="5">100 MHz Timings</td></tr>
<tr><td>-</td><td>Register</td><td>7</td><td>29</td><td>24</td></tr>
<tr><td>000</td><td>Mode 0</td><td>7</td><td>17</td><td>37</td></tr>
<tr><td>001</td><td>Mode 1</td><td>5</td><td>13</td><td>21</td></tr>
<tr><td>010</td><td>Mode 2</td><td>3</td><td>10</td><td>11</td></tr>
<tr><td>011</td><td>Mode 3</td><td>3</td><td>8</td><td>7</td></tr>
<tr><td>100</td><td>Mode 4</td><td>3</td><td>7</td><td>3</td></tr>
<tr><td>111</td><td>Reserved</td><td></td><td></td><td></td></tr>
</table></td></tr>
</table>

16.3 I/O Registers

Intel® SCH uses 16 bytes of I/O space, allocated by BMBAR. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no effect.

Table 53. PATA Memory-Mapped I/O Register Address Map

Offset	Mnemonic	Register Name	Default	Access
00h	PCMD	Primary Command	00h	RO, R/W
02h	PSTS	Primary Status	00h	RO, R/W, R/WC
04h	PDTP	Primary Data Table Pointer	See description	RO, R/W
10h	SCMD	Secondary Command	See **Note**	
12h	SSTS	Secondary Status		
14h	SDTP	Secondary Data Table Pointer		

NOTE: The secondary registers are available, but provide no functionality.

16.3.1 PCMD—Primary Command Register

Offset: 00h Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:4	0000b RO	Reserved
3	0 R/W	**Read/Write (RWC):** This bit sets the direction of the bus master transfer: This bit must not be changed when the bus master function is active. 0 = Memory to device 1 = Device to memory
2:1	00b RO	Reserved
0	0 R/W	**Start/Stop Bus Master (START):** This bit, when set, enables bus master operation of the controller. All state information is lost when this bit is cleared. Master mode operation cannot be paused. If this bit is reset while bus master operation is still active and the device has not yet finished its data transfer, the bus master command is said to be aborted.

16.3.2 PSTS—Primary Status Register

Offset: 02h Attribute: RO, R/W, R/WC
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7	0 RO	Reserved
6	0 R/W	**Device 1 DMA Capable (D1DC):** A scratchpad bit set by device dependent code to indicate that device 1 of this channel is capable of DMA transfers. This bit has no effect on hardware.
5	0 R/W	**Device 0 DMA Capable (D0DC):** A scratchpad bit set by device dependent code to indicate that device 0 of this channel is capable of DMA transfers. This bit has no effect on hardware.
4:3	00b RO	Reserved
2	0 R/WC	**Interrupt (I):** This bit is set when IDEIRQ goes active. When set, all data transferred from the device is valid at its destination. If cleared while the interrupt is still active, this bit remains cleared until another assertion edge is detected on the interrupt line.
1	0 RO	**Error (ERR):** Intel® SCH will never set this bit.
0	0 RO	**Active (ACT):** This bit is set by the host when PCMD.START is set, and cleared by the host when the last transfer for a region is performed, where EOT for that region is set in the region descriptor, and when PCMD.START is cleared and the controller has returned to an idle condition.

16.3.3 PDTP—Primary Descriptor Table Pointer Register

Offset: 04h Attribute: RO, R/W
Default Value: see description Size: 32 bits

Bit	Default and Access	Description
31:2	See description R/W	**Descriptor Base Address (DBA):** This field corresponds to A[31:2]. This table must not cross a 64 KB boundary in memory. When read, the current value of the pointer is returned.
1:0	00b RO	Reserved

§ §

17 LPC Interface (D31:F0)

17.1 Functional Overview

The LPC controller implements a low pin count interface that supports the LPC 1.1 specification:

- LSMI# can be connected to any of the SMI capable GPIO signals.
- The EC's PME# should connect it to GPE#.
- The LPC controller's SUS_STAT# signal is connected directly to the LPCPD# signal.

The LPC controller does not implement DMA or bus mastering cycles.

The LPC bridge function of the Intel® SCH resides in PCI Device 31:Function 0. This function contains many other functional units, such as Interrupt controllers, Timers, Power Management, System Management, GPIO, RTC, and LPC Configuration Registers. This section contains the PCI configuration registers for the primary LPC interface. Power Management details are found in a separate chapter, and other ACPI functions (RTC, SMBus, GPIO, Interrupt controllers, Timers, etc.) can be found in the ACPI chapter.

17.1.1 Memory Cycle Notes

For cycles below 16M, the LPC Controller will perform standard LPC memory cycles. For cycles targeting firmware, firmware memory cycles are used. Only 8-bit transfers are performed. If a larger transfer appears, the LPC controller will break it into multiple 8-bit transfers until the request is satisfied.

If the cycle is not claimed by any peripheral (and subsequently aborted), the LPC Controller will return a value of all 1s to the processor.

17.1.2 TPM 1.2 Support

The LPC interface supports accessing TPM 1.2 devices by LPC TPM START encoding. Memory addresses within the range FED40000h to FED4BFFFh will be accepted by the LPC bridge and sent on LPC as TPM special cycles. No additional checking of the memory cycle is performed.

17.1.3 FWH Cycle Notes

The Intel® SCH has been designed to accommodate both LPC and FWH interfaces which allows the FWH interface signals to be communicated over the same set of pins as LPC. The FWH interface is designed to use an LPC-compatible start cycle, with a reserved cycle type code. This ensures that all LPC devices present on the shared interface will ignore cycles destined for the FWH, without becoming “confused” by the different protocol.

If a flash device connects to LPC interface, it must be compliant with FWH specification 1.0e. The first BIOS commands issued to the LPC bus use the FWH instruction set and will not execute properly unless a FWH-compatible flash device is used.

If the LPC controller receives any SYNC returned from the device other than short (0101), long wait (0110), or ready (0000) when running a FWH cycle, indeterminate results may occur. A FWH device is not allowed to assert an Error SYNC.

17.1.4 LPC Output Clocks

The Intel® SCH provides three output clocks to drive external LPC devices that may require a PCI-like clock (25 MHz or 33 MHz). The LPC output clocks operate at 1/4th the frequency of H_CLKIN[P/N].

LPC_CLKOUT0 should be used to provide clocking to the FWH boot device. Because LPC_CLKOUT0 is the first clock to be used in the system, configuring its drive strength is done by a strapping option on the RESERVED1 pin. (Refer to Table 3.) The buffer strengths of LPC_CLKOUT1 and LPC_CLKOUT2 default to 2-loads per clock and can be reprogrammed by the CMC by using the SoftStrap utility.

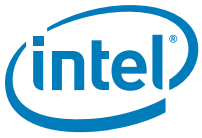
Note: By default, the LPC clocks are only active when LPC bus transfers occur. Because of this behavior, LPC clocks must be routed directly to the bus devices; they cannot go through a clock buffer or other circuit that could delay the signal going to the end device.

17.2 PCI Configuration Registers

Note: Address locations that are not shown should be treated as Reserved.

Table 54. LPC Interface PCI Register Address Map

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	8119h	RO
04h–05h	PCICMD	PCI Command	0003h	RO
06h–07h	PCISTS	PCI Status	0000h	RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Codes	060100h	RO
0Eh	HEADTYP	Header Type	80h	RO
2Ch–2Fh	SS	Sub System Identifiers	00000000h	R/WO
40h–43h	SMBASE	SMBus Base Address	00000000h	RO. R/W
44h–47h	GPIOBASE	GPIO Base Address	00000000h	R/W, RO
48h–4Bh	PM1BASE	PM1_BLK Base Address	00000000h	RO/ R/W
4Ch–4Fh	GPEBASE	GPE1_BLK Base Address	00000000h	RO, R/W
54h–57h	LPCS	LPC Clock Control	00000000h	RO, R/W
58h–5Bh	ACPI_CTL	ACPI Control	00000000h	RO, R/W
5Ch–5Fh	MC	Miscellaneous Control	00000000h	RO, R/W
60h–67h	PIRQ[x]_RT	PIRQ[A–H] Routing Control	80h	RO, R/W
68h	SIRQ_CTL	Serial IRQ Control	00h	R/W, RO
D4h–D7h	BDE	BIOS Decode Enable	FF000000h	RO, R/W
D8h–DBh	BIOS_CTL	BIOS Control	00000100h	RO, R/W
F0h–F3h	RCBA	Root Complex Base Address	00000000h	RO, R/W



17.2.1 VID—Vendor Identification Register

Offset: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bit

Bit	Default and Access	Description
15:0	8086h RO	**Vendor ID:** This is a 16-bit value assigned to Intel.

17.2.2 DID—Device Identification Register

Offset: 02h–03h Attribute: RO
Default Value: See bit description Size: 16 bit

Bit	Default and Access	Description
15:0	8119h RO	**Device ID:** This is a 16-bit value assigned to the Intel® SCH LPC bridge.

17.2.3 PCICMD—PCI COMMAND Register

Offset: 04h–05h Attribute: RO
Default Value: 0003h Size: 16 bit

Bit	Default and Access	Description
15:3	0 RO	Reserved
1	1 RO	**Memory Space Enable (MSE):** Memory space cannot be disabled on LPC.
0	1 RO	**I/O Space Enable (IOSE):** I/O space cannot be disabled on LPC.

17.2.4 PCISTS—PCI Status Register

Offset: 06–07h Attribute: RO
Default Value: 0000h Size: 16 bit

Bit	Default and Access	Description
15:0	0000h RO	Reserved

17.2.5 RID—Revision Identification Register

Offset: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Revision ID:** Refer to the *Intel® System Controller Hub (Intel® SCH) Specification Update* for the value of the Revision ID Register.

17.2.6 CC—Class Codes Register

Offset: 09h–0Bh Attribute: RO
Default Value: 060100h Size: 24 bits

Bit	Default and Access	Description
23:16	06h RO	**Base Class Code (BCC):** This field indicates the device is a bridge device.
15:8	01h RO	**Sub-Class Code (SCC):** This field indicates the device is a PCI to ISA bridge.
7:0	00h RO	**Programming Interface (PI):** The LPC bridge has no programming interface.

17.2.7 HEADTYP—Header Type Register

Offset: 0Eh Attribute: RO
Default Value: 80h Size: 8 bits

Bit	Default and Access	Description
7	1 RO	**Multi-Function Device (MFD):** This bit is 1 to indicate a multi-function device.
6:0	00h RO	**Header Type (HTYPE):** Identifies the header layout is a generic device.

17.2.8 SS—Sub System Identifiers Register

Offset:	2Ch–2Fh	Attribute:	R/WO
Default Value:	00000000h	Size:	32 bits

This register is initialized to logic 0 by the assertion of RESET#. This register can be written only once after RESET# deassertion.

Bit	Default and Access	Description
31:16	0000h R/WO	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken.
15:00	0000h R/WO	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action is taken.

17.3 ACPI Device Configuration

17.3.1 SMBASE—SMBus Base Address Register

Offset:	40h–43h	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

Bit	Default and Access	Description
31	0b R/W	**Enable (EN)** 1 = Decode of the I/O range pointed to by the SMBASE.BA field is enabled.
30:16	0s RO	Reserved
15:6	0s R/W	**Base Address (BA):** This field provides the 64 bytes of I/O space for SMBus
5:0	0s RO	Reserved

17.3.2 GPIOBASE—GPIO Base Address Register

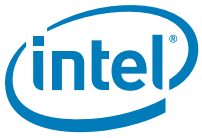
Offset: 44h–47h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31	0 R/W	**Enable (EN)** 1 = Decode of the I/O range pointed to by the GPIOBASE.BA is enabled.
30:16	0s RO	Reserved
15:6	0s R/W	**Base Address (BA):** This field provides the 64 bytes of I/O space for GPIO.
5:0	0s RO	Reserved

17.3.3 PM1BASE—PM1_BLK Base Address Register

Offset: 48–4Bh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31	0 R/W	**Enable (EN)** 1 = Decode of the I/O range pointed to by the PM1BASE.BA is enabled.
30:16	0s RO	Reserved
15:4	0s R/W	**Base Address (BA):** This field provides the 16 bytes of I/O space for PM1_BLK.
3:0	0s RO	Reserved



17.3.4 GPE0BASE—GPE0_BLK Base Address Register

Offset:	4Ch–4Fh	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

For processor C-state microcode to function correctly, GPE0BASE must be located 16 bytes after PM1BASE. System BIOS has the responsibility to ensure these address are placed correctly.

Bit	Default and Access	Description
31	0 R/W	**Enable (EN)** 1 = Decode of the IO range pointed to by the GPE0BASE.BA is enabled.
30:16	0s RO	Reserved
15:6	0s R/W	**Base Address (BA):** This field provides the 64 bytes of I/O space for PM1_BLK
5:0	0s RO	Reserved

17.3.5 LPCS—LPC Clock Control Register

Offset:	54h–57h	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

The LPC Clock 2 and 1 are controlled using the SoftStrap software.

Bit	Default and Access	Description
31:19	0s RO	Reserved
18	1 R/W	**Clock 2 Enable (EN)** 1 = Enabled. 0 = Disabled.
17	1 R/W	**Clock 1 Enable (EN)** 1 = Enabled. 0 = Disabled.
16:0	0s RO	Reserved

17.3.6 ACPI_CTL—ACPI Control Register

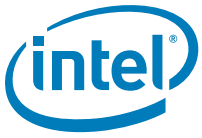
Offset: 58h–5Bh Attribute: RO, R/W
Default Value: 00000001h Size: 32 bits

Bit	Default and Access	Description
31:3	0s RO	Reserved
2:0	001b R/W	**SCI IRQ Select (SCIS):** This field specifies on which IRQ SCI will rout to. If not using APIC, SCI must be routed to IRQ9–11, and that interrupt is not sharable with SERIRQ, but is shareable with other interrupts. If using APIC, SCI can be mapped to IRQ20–23, and can be shared with other interrupts. Bits / SCI Map / Bits / SCI Map 000 IRQ9 100 IRQ20 001 IRQ10 101 IRQ21 010 IRQ11 110 IRQ22 011 SCI Disabled 111 IRQ23 When the interrupt is mapped to APIC interrupts 9, 10 or 11, APIC must be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, APIC must be programmed for active-low reception.

17.3.7 MC - Miscellaneous Control Register

Offset: 5Ch–5Fh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:0	0s RO	Reserved



17.4 Interrupt Control

17.4.1 PIRQ[n]_ROUT—PIRQ[A,B,C,D] Routing Control Register

Offset:	PIRQA – 60h, PIRQB – 61h PIRQC – 62h, PIRQD – 63h PIRQE – 64h, PIRQF – 65h PIRQG – 66h, PIRQH – 67h	Attribute:	RO, R/W
Default Value:	80h	Size:	8 bits

Bit	Default and Access	Description
7	1 R/W	**Interrupt Routing Enable (IRQEN)** 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. **NOTE:** BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.
6:4	000b RO	Reserved

17.4.2 SIRQ_CTL—Serial IRQ Control Register

Offset:	68h	Attribute:	RO, R/W
Default Value:	00h	Size:	8 bits

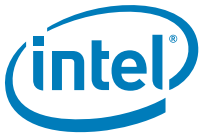
Bit	Default and Access	Description
7	0 R/W	**Mode (MD):** This bit must be set to ensure that the first action of Intel® SCH is a start frame. 0 = Intel® SCH is in quiet mode 1 = Intel® SCH is in continuous mode
6:0	0s RO	Reserved

17.5 FWH Configuration Registers

17.5.1 FWH_IDSEL—FWH ID Select Register

Offset: D0h–D3h Attribute: RO, R/W
Default Value: 00112233h Size: 32 bits

Bit	Default and Access	Description
31:28	0h RO	**F8-FF IDSEL (IF8):** IDSEL to use in FWH cycle for range enabled by BDE.EF8. The Address ranges are: FFF80000h – FFFFFFFFh, FFB80000h – FFBFFFFFh and 000E0000h – 000FFFFFh
27:24	0h R/W	**F0-F7 IDSEL (IF0):** IDSEL to use in FWH cycle for range enabled by BDE.EF0. The Address ranges are: FFF00000h – FFF7FFFFh, FFB00000h – FFB7FFFFh
23:20	1h R/W	**E8-EF IDSEL (IE8):** IDSEL to use in FWH cycle for range enabled by BDE.EE8. The Address ranges are: FFE80000h – FFEFFFFFh, FFA80000h – FFAFFFFFh
19:16	1h R/W	**E0-E7 IDSEL (IE0):** IDSEL to use in FWH cycle for range enabled by BDE.EE0. The Address ranges are: FFE00000h – FFE7FFFFh, FFA00000h – FFA7FFFFh
15:12	2h R/W	**D8-DF IDSEL (ID8):** IDSEL to use in FWH cycle for range enabled by BDE.ED8. The Address ranges are: FFD80000h – FFDFFFFFh, FF980000h – FF9FFFFFh
11:8	2h R/W	**D0-D7 IDSEL (ID0):** IDSEL to use in FWH cycle for range enabled by BDE.ED0. The Address ranges are: FFD00000h – FFD7FFFFh, FF900000h – FF97FFFFh
7:4	3h R/W	**C8-CF IDSEL (IC8):** IDSEL to use in FWH cycle for range enabled by BDE.EC8. The Address ranges are: FFC80000h – FFCFFFFFh, FF880000h – FF8FFFFFh
3:0	3h R/W	**C0-C7 IDSEL (IC0):** IDSEL to use in FWH cycle for range enabled by BDE.EC0. The Address ranges are: FFC00000h – FFC7FFFFh, FF800000h – FF87FFFFh



17.5.2 BDE—BIOS Decode Enable

Offset: D4h–D7h Attribute: RO, R/W
Default Value: 7F000000h Size: 32 bits

Bit	Default and Access	Description
31	0b RO	**F8–FF Enable (EF8):** Enables decoding of BIOS range FFF80000h – FFFFFFFFh and FFB80000h – FFBFFFFFh. 0 = Disable 1 = Enable
30	1b R/W	**F0–F8 Enable (EF0):** Enables decoding of BIOS range FFF00000h – FFF7FFFFh and FFB00000h – FFB7FFFFh. 0 = Disable 1 = Enable
29	1b R/W	**E8–EF Enable (EE8):** Enables decoding of BIOS range FFE80000h – FFEFFFFFh and FFA80000h – FFAFFFFFh. 0 = Disable 1 = Enable
28	1b R/W	**E0–E8 Enable (EE0):** Enables decoding of BIOS range FFE00000h – FFE7FFFFh and FFA00000h – FFA7FFFFh. 0 = Disable 1 = Enable
27	1b R/W	**D8–DF Enable (ED8):** Enables decoding of BIOS range FFD80000h – FFDFFFFFh and FF980000h – FF9FFFFFh. 0 = Disable, 1 = Enable
26	1b R/W	**D0–D7 Enable (ED0):** Enables decoding of BIOS range FFD00000h – FFD7FFFFh and FF900000h – FF97FFFFh. 0 = Disable 1 = Enable
25	1b R/W	**C8–CF Enable (EC8):** Enables decoding of BIOS range FFC80000h – FFCFFFFFh and FF880000h – FF8FFFFFh. 0 = Disable 1 = Enable
24	1b R/W	**C0–C7 Enable (EC0):** Enables decoding of BIOS range FFC00000h – FFC7FFFFh and FF800000h – FF87FFFFh. 0 = Disable 1 = Enable
23:00	000000h RO	Reserved

17.5.3 BIOS_CTL—BIOS Control Register

Offset: D8h–DBh Attribute: RO, R/W
Default Value: 00000100h Size: 32 bits

Bit	Default and Access	Description
31:9	0 RO	Reserved
8	1 R/W	**Prefetch Enable (PFE)** 0 = Disable. 1 = Enable BIOS prefetching. An access to BIOS causes a 64-byte fetch of the line starting at that region. Subsequent accesses within that region result in data being returned from the prefetch buffer. **NOTE:** The prefetch buffer is invalidated when this bit is cleared, or a BIOS access occurs to a different line than what is currently in the buffer.
7:2	000000b RO	Reserved
1	0 R/WLO	**Lock Enable (LE):** When set, setting the WP bit will cause SMIs. When cleared, setting the WP bit will not cause SMIs. Once set, this bit can only be cleared by a RESET#. 0 = Setting the BIOSWE will not cause SMIs. 1 = Enables setting the BIOSWE bit to cause SMIs. Once set, this bit can only be cleared by a RESET#
0	0 R/W	**Write Protect (WP):** When set, access to BIOS is enabled for both read and write cycles. When cleared, only read cycles are permitted to BIOS. When written from a 0 to a 1 and LE is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

17.6 Root Complex Register Block Configuration

17.6.1 RCBA—Root Complex Base Address Register

Offset: F0h–F3h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:14	0 R/W	**Base Address (BA):** Base Address for the root complex register block decode range. This address is aligned on a 16 kB boundary.
13:1	0 RO	Reserved
0	0 R/W	**Enable (EN)** 1 = Enables the range specified in RCBA.BA to be claimed as the RCRB.

§ §

18 ACPI Functions (D30:F0)

ACPI (Advanced Configuration and Power Interface) is an open industry specification co-developed by Compaq*, Intel, Microsoft*, Phoenix*, and Toshiba*. It establishes industry-standard interfaces for OS-directed configuration and power management on laptops, desktops, and servers.

The Intel® SCH includes several internal ACPI devices:

- Two Timers
  - An 8254 Timer
  - Precision Event Timer
- Real Time Clock
- Various Interrupt Controllers
  - Two, 8259 Programmable Interrupt Controllers
  - An Advanced Programmable Interrupt Controller (IOxAPIC)
  - A Serial Interrupt Controller
- SMBus Controller

18.1 8254 Timer

18.1.1 Overview

The 8254 Timer is clocked by a 14.31818-MHz clock and contains three counters which have fixed uses.

- Counter 0: System Timer
- Counter 1: Refresh Request
- Counter 2: Speaker Tone

18.1.1.1 Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

18.1.1.2 Counter 1, Refresh Request Signal

This counter is typically programmed for Mode 2 operation and impacts the period of the REF_TOGGLE bit in Port 61. Programming the counter to anything other than Mode 2 will result in undefined behavior for the REF_TOGGLE bit.

18.1.1.3 Counter 2, Speaker Tone

This counter typically programmed for Mode 3 operation.

18.1.2 Timer Programming

The counter/timers are programmed in the following fashion:

1. Write a control word to select a counter
2. Write an initial count for that counter.
3. Load the least and/or most significant bytes (as required by Control Word bits 5, 4) of the 16-bit counter.
4. Repeat with other counters

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting will be affected as described in the mode definitions. The new count must follow the programmed count format.

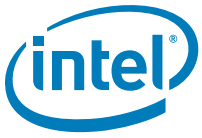
If a counter is programmed to read/write 2-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- **Control Word Command:** Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- **Counter Latch Command:** Latches the current count so that it can be read by the system. The countdown process continues.
- **Read Back Command:** Reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 55. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware retriggerable one-shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, etc.
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.



18.1.3 Reading From the Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, counter Latch Command, and the Read-Back Command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for 2-byte counts, two bytes must be read. The two bytes do not have to be read in sequence (one right after the other). Read, write, or programming operations for other counters can be inserted between them.

18.1.3.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through port 40h (counter 0), 41h (counter 1), or 42h (counter 2).

Note: Performing a direct read from the counter will not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of counter 2, the count can be stopped by writing to NSC.TC2E.

18.1.3.2 Counter Latch Command

The Counter Latch Command, written to port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a 2-byte count. The count value is then read from each counter's Count Register as was programmed by the Control Register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch Commands do not effect the programmed mode of the counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

18.1.3.3 Read Back Command

The Read Back Command, written to port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back Command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back Commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back Command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back Commands. If multiple count and/or status Read Back Commands are issued to the same counters without any intervening reads, all but the first are ignored.

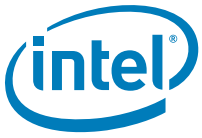
If both count and status of a counter are latched, the first read operation from that counter will return the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two type counts, return the latched count. Subsequent reads return unlatched count.

18.1.4 I/O Registers

All registers are powered by the core power well.

Table 56. I/O Register Map

Port	N	Register Name/Function	Default Value	Type
40h		Counter 0 Interval Time Status Byte Format	0UUUUUUUb	RO
41h		Counter 1 Interval Time Status Byte Format	0UUUUUUUb	RO
42h		Counter 2 Interval Time Status Byte Format	0UUUUUUUb	RO
43h		Timer Control Word Register	UUh	WO
50h		Counter 0 Counter Access Port Register	UUh	R/W
51h		Counter 1 Counter Access Port Register	UUh	R/W
52h		Counter 2 Counter Access Port Register	UUh	R/W



18.1.4.1 Counter [0..2] Interval Timer Status Byte Format Register

Offset/Port:	40h, 41h, 42h	Attribute:	RO
Default Value:	0UUUUUUUb	Size:	8 bits

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2) returns the status byte.

Bit	Default and Access	Description
7	0 RO	**Counter OUT Pin State:** 0 = OUT pin of the counter is 0 1 = OUT pin of the counter is 1
6	U RO	**Count Register Status:** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 = Count has been transferred from CR to CE and is available for reading 1 = Null Count. Count has not been transferred from CR to CE and is not yet available for reading
5:4	UU RO	**Read/Write Selection Status:** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	UUU RO	**Mode Selection Status:** These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 = Out signal on end of count (=0) 001 = Hardware retriggerable one-shot x10 = Rate generator (divide by n counter) x11 = Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	U RO	**Countdown Type Status:** This bit reflects the current countdown type. 0 = Binary countdown 1 = Binary coded decimal (BCD) countdown

18.1.4.2 TCW—Timer Control Word Register

Offset/Port:	43h	Attribute:	WO
Default Value:	UUh	Size:	8 bits

This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Bit	Default and Access	Description
7:6	UU WO	**Counter Select (CS):** The Counter Selection bits select the counter that the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1. 00 = Counter 0 select 01 = Counter 1 select 10 = Counter 2 select 11 = Read Back Command
5:4	UU WO	**Read/Write Select RWS):** These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2). 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	UUU WO	**Counter Mode Selection (CMS):** These bits select one of six possible modes of operation for the selected counter. 000 = Out signal on end of count (=0) 001 = Hardware retriggerable one-shot x10 = Rate generator (divide by n counter) x11 = Square wave output 100 = Software triggered strobe 101 = Hardware triggered strobe
0	U WO	**Binary/BCD Countdown Select (BCS):** 0 = Binary countdown is used. The largest possible binary count is 216 1 = Binary coded decimal (BCD) count is used. The largest possible BCD count is 104

There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined. These register formats are described in the following sections.

18.1.4.3 TCW—Timer Control Word Register (Read Back Command)

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read.

Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, (depending on whether the counter is programmed for 1- or 2-byte counts) return a latched count. Subsequent reads return an unlatched count.

Bit	Default and Access	New Description
7:6		**Read Back Command:** Must be “11” to select the Read Back Command
5		**Latch Count of Selected Counters:** 0 = Current count value of the selected counters will be latched 1 = Current count will not be latched
4		**Latch Status of Selected Counters:** 0 = Status of the selected counters will be latched 1 = Status will not be latched
3		**Counter 2 Select (C2S):** When set to 1, Counter 2 count and/or status will be latched.
2		**Counter 1 Select (C1S):** When set to 1, Counter 1 count and/or status will be latched.
1		**Counter 0 Select (C0S):** When set to 1, Counter 0 count and/or status will be latched.
0		Reserved

18.1.4.4 TCW—Timer Control Word Register (Counter Latch Command)

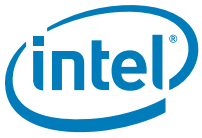
This latches the current count value and is used to ensure the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for Counter 0, 41h for Counter 1, and 42h for Counter 2). The count must be read according to the programmed format, i.e., if the counter is programmed for 2-byte counts, two bytes must be read. It is not necessary to read the two bytes in sequence. That is, the two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Bit	Default and Access	Description
7:6		**Counter Selection:** These bits select the counter for latching. If “11” is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Counter 1 10 = Counter 2
5:4		**Counter Latch Command:** Write “00” to select the Counter Latch Command.
3:0		Reserved. Must be 0.

18.1.4.5 Counter Access Ports Register

Offset/Port:	50h, 51h, 52h	Attribute:	R/W
Default Value:	UUh	Size:	8 bits

Bit	Default and Access	Description
7:0	Undefined R/W	**Counter Port:** Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.



18.2 High Precision Event Timer

The High Precision Event Timer (HPET) function provides a set of timers that to be used by the operating system for timing events. One timer block is implemented, containing one counter and three timers.

18.2.1 Functional Overview

18.2.1.1 Non-Periodic Mode—All timers

This mode can be thought of as creating a one-shot. When a timer is set up for non-periodic mode, it generates an interrupt when the value in the main counter matches the value in the timer's comparator register. As timers 1 and 2 are 32-bit, they will generate another interrupt when the main counter wraps.

T0CV cannot be programmed reliably by a single 64-bit write in a 32-bit environment, unless only the periodic rate is being changed. If T0CV needs to be reinitialized, the following algorithm is performed:

1. Set T0CC.TVS
2. Set the lower 32 bits of T0CV
3. Set T0CC.TVS
4. Set the upper 32 bits of T0CV

Every timer is required to support the non-periodic mode of operation.

18.2.1.2 Periodic Mode—Timer 0 only

When set up for periodic mode, when the main counter value matches the value in T0CV, an interrupt is generated (if enabled). Hardware then increases T0CV by the last value written to T0CV. During run-time, T0CV can be read to find out when the next periodic interrupt will be generated. Software is expected to remember the last value written to T0CV.

Example: If the value written to T0CV is 00000123h, then

- An interrupt will be generated when the main counter reaches 00000123h
- T0CV will then be adjusted to 00000246h
- Another interrupt will be generated when the main counter reaches 00000246h
- T0CV will then be adjusted to 00000369h
- When the incremented value is greater than the maximum value possible for TnCV, the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h.

If software wants to change the periodic rate, it writes a new value to T0CV. When the timer's comparator matches, the new value is added to derive the next matching point. If software resets the main counter, the value in the comparator's value register must also be reset by setting T0CC.TVS. To avoid race conditions, this should be done with the main counter halted. The following usage model is expected:

1. Software clears GC.EN to prevent any interrupts
2. Software clears the main counter by writing a value of 00h to it
3. Software sets T0CC.TVS
4. Software writes the new value in T0CV
5. Software sets GC.EN to enable interrupts.

18.2.1.3 Interrupts

If each timer has a unique interrupt and the timer has been configured for edge-triggered mode, then there are no specific steps required. If configured to level-triggered mode, then its interrupt must be cleared by software by writing a 1 back to the bit position for the interrupt to be cleared.

Interrupts associated with the various timers have several interrupt mapping options. Software should mask GC.LRE when reprogramming HPET interrupt routing to avoid spurious interrupts.

18.2.1.3.1 Mapping Option #1: Legacy Option (GC.LRE set)

Setting the GC.LRE bit high forces the following mapping:

Table 57. Legacy Timer Interrupt Mapping

Timer	8259 Mapping	APIC Mapping	Comment
0	IRQ0	IRQ2	The 8254 timer will not cause any interrupts.
1	IRQ8	IRQ8	RTC will not cause any interrupts.
2	T2C.IRQ	T2C.IRC	

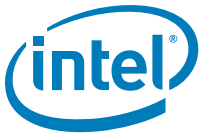
18.2.1.3.2 Mapping Option #2: Standard Option (GC.LRE cleared)

Each timer has its own routing control. The interrupts can be routed to various interrupts in the I/O APIC. TnC.IRC indicates which interrupts are valid options for routing. If a timer is set for edge-triggered mode, the timers should not be shared with any other interrupts.

18.2.2 Registers

The HPET register space is memory mapped to a 1 KB block starting at address FED00000h. All registers are in the core well and reset by RESET#. Accesses that cross register boundaries result in undefined behavior.

Offset / Port	Mnemonic	Register	Default	Access
000h–007h	GCID	General Capabilities and ID	0429B17F_8086A201h	RO
010h–017h	GCFG	General Configuration	0000000000000000h	RO, R/W
020h–027h	GIS	General Interrupt Status	0000000000000000h	RO, R/WC
0F0h–0F7h	MCV	Main Counter Value	0000000000000000h	R/W
100h–107h	T0C	Timer 0 Configuration and Capabilities	See Description	RO, R/W
108h–10Fh	T0CV	Timer 0 Comparator Value	0000000000000000h	RO, R/W
120h–127h	T1C	Timer 1 Configuration and Capabilities	See Description	RO, R/W
128h–12Fh	T1CV	Timer 1 Comparator Value	0000000000000000h	RO, R/W
140h–147h	T2C	Timer 2 Configuration and Capabilities	See Description	RO, R/W
148h–14Fh	T2CV	Timer 2 Comparator Value	0000000000000000h	RO, R/W



18.2.2.1 GCID—General Capabilities and ID Register

Offset/Port: 000–007h Attribute: RO
Default Value: 0429B17F_8086A201h Size: 64 bits

Bit	Default and Access	Description
63:32	0429B17Fh RO	**Counter Tick Period (CTP):** This field indicates a period of 69.841279 ns, (14.31818-MHz clock period).
31:16	8086h RO	**Vendor ID (VID):** Value of 8086h indicates Intel Corporation.
15	1 RO	**Legacy Rout Capable (LRC):** This bit indicates support for Legacy Interrupt Rout.
14	0 RO	Reserved
13	1 RO	**Counter Size (CS):** This bit is set to indicate that the main counter is 64 bits wide.
12:8	02h RO	**Number of Timers (NT)**: Indicates that 3 timers are supported.
7:0	01h RO	**Revision ID (RID)**: Indicates that revision 1.0 of the specification is implemented.

18.2.2.2 GC—General Configuration Register

Offset/Port: 010–017h Attribute: RO, R/W
Default Value: 00000000h Size: 64 bits

Bit	Default and Access	Description
63:02	0 RO	Reserved
1	0 R/W	**Legacy Rout Enable (LRE):** When set, interrupts will be routed as follows: • Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC • Timer 1 will be routed to IRQ8 in 8259 and I/O APIC • Timer 2 will be routed as per the routing in T2C When set, the TNC.IR will have no impact for timers 0 and 1.
0	0 R/W	**Overall Enable (EN):** When set, the timers can generate interrupts. When cleared, the main counter will halt and no interrupts will be caused by any timer. For level-triggered interrupts, if an interrupt is pending when this bit is cleared, the GIS.Tx will not be cleared.

18.2.2.3 GIS—General Interrupt Status Register

Offset/Port: 020–027h Attribute: RO, R/WC
Default Value: 0s Size: 64 bits

Bit	Default and Access	Description
63:03	0 RO	Reserved
2	0 R/WC	**Timer 2 Status (T2):** Same functionality as T0, for timer 2.
1	0 R/WC	**Timer 1 Status (T1):** Same functionality as T0, for timer 1.
0	0 R/WC	**Timer 0 Status (T0):** In edge triggered mode, this bit always reads as 0. In level triggered mode, this bit is set when an interrupt is active.

18.2.2.4 MCV—Main Counter Value Register

Offset/Port: 0F0–0F7h Attribute: R/W
Default Value: 0s Size: 64 bits

Bit	Default and Access	Description
63:0	0 R/W	**Counter Value (CV):** Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

18.2.2.5 T[0:2]CC—Timer N Configuration and Capabilities Register

Offset/Port: 100h, 120h, 140h Attribute: RO, R/W
Default Value: see description Size: 64 bits

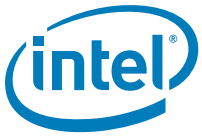
Bit	Default and Access	Description
63:32	see description RO	**Interrupt Rout Capability (IRC):** This field indicates I/OxAPIC interrupts the timer can use: • Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 • Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0 RO	Reserved
15	RO	**FSB Interrupt Delivery (FID):** Not supported
14	0 RO	**FSB Enable (FE):** Not supported, since FID is not supported.
13:9	0 R/W	**Interrupt Rout (IR):** This field indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this particular timer, the value read back will not match what is written. If GC.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0 RO/R/W	**Timer 32-bit Mode (T32M):** When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only 0.
7	0 RO	Reserved
6	0 RO/R/W	**Timer Value Set (TVS):** This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0/1 RO	**Timer Size (TS):** 1 = 64-bit, 0 = 32-bit. Set for timer 0. Cleared for timers 1 and 2.
4	0/1 RO	**Periodic Interrupt Capable (PIC):** When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0 RO/R/W	**Timer Type (TYP):** If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is R/W for timer 0, and RO for timers 1 and 2.
2	0 R/W	**Interrupt Enable (IE):** When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0 R/W	**Timer Interrupt Type (IT):** When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0 RO	Reserved

18.2.2.6 T[0:2]CV—Timer N Comparator Value Register

Offset/Port:	108h, 128h, 148h	Attribute:	RO, R/W
Default Value:	1s	Size:	64 bits

Reads to this register return the current value of the comparator. The default value for each timer is all 1s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide.

Bit	Description
63:0	**Timer Compare Value** — R/W. Reads to this register return the current value of the comparator Timers 0, 1, or 2 are configured to non-periodic mode: Writes to this register load the value against which the main counter should be compared for this timer. • When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). • The value in this register does not change based on the interrupt being generated. Timer 0 is configured to periodic mode: • When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). • After the main counter equals the value in this register, the value in this register is increased by the value last written to the register. As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h Default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer has a default value of 00000000FFFFFFFFh. A 64-bit timer has a default value of FFFFFFFFFFFFFFFFh.



18.3 8259 Interrupt Controller

18.3.1 Overview

The ISA-compatible interrupt controller (8259) incorporates the functionality of two 8259 interrupt controllers: a master and a slave. The following table shows how the cores are connected:

Table 58. Master 8259 Input Mapping

8259 Input	Connected Pin/Function
0	Internal Timer/Counter 0 output or Multimedia Timer #0
1	IRQ1 through SERIRQ
2	Slave Controller INTR output
3	IRQ3 through SERIRQ, PIRQx
4	IRQ4 through SERIRQ, PIRQx
5	IRQ5 through SERIRQ, PIRQx
6	IRQ6 through SERIRQ, PIRQx
7	IRQ7 through SERIRQ, PIRQx

Table 59. Slave 8259 Input Mapping

8259 Input	Connected Pin/Function
0	Inverted IRQ8# from internal RTC or HPET
1	IRQ9 through SERIRQ, SCI, or PIRQx
2	IRQ10 through SERIRQ, SCI, or PIRQx
3	IRQ11 through SERIRQ, SCI, or PIRQx
4	IRQ12 through SERIRQ, SCI, or PIRQx
5	PIRQx
6	IDEIRQ, SERIRQ, PIRQx
7	PIRQx

The slave controller is cascaded onto the master controller through master controller interrupt input 2. Interrupts can individually be programmed to be edge or level, except for IRQ0, IRQ2, IRQ8#. Active-low interrupt sources, such as the PIRQ#s, are internally inverted before being sent to the 8259. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term “high” indicates “active”, which means “low” on an originating PIRQ#.

18.3.2 Interrupt Handling

18.3.2.1 Generating

The 8259 interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. These bits are defined as follows:

- **Interrupt Request Register (IRR):** Set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode.
- **Interrupt Service Register (ISR):** Set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
- **Interrupt Mask Register (IMR):** Determines whether an interrupt is masked. Masked interrupts will not generate INTR.

18.3.2.2 Acknowledging

The CPU generates an interrupt acknowledge cycle which is translated into an Interrupt Acknowledge Special Cycle to the Intel® SCH. The 8259 translates this cycle into two internal INTA# pulses expected by the 8259 cores. The 8259 uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave will sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon bits [7:3] of the corresponding ICW2 register, combined with three bits representing the interrupt within that controller.

Table 60. Content of Interrupt Vector Byte

Master,Slave Interrupt	Bits [7:3]	Bits [2:0]
IRQ7,15	ICW2[7:3]	111
IRQ6,14		110
IRQ5,13		101
IRQ4,12		100
IRQ3,11		011
IRQ2,10		010
IRQ1,9		001
IRQ0,8		000

18.3.2.3 Hardware/Software Interrupt Sequence

1. One or more of the Interrupt Request lines (IRQs) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
2. The 8259 sends INTR active (high) to the CPU if an asserted interrupt is not masked.
3. The CPU acknowledges the INTR and responds with an interrupt acknowledge cycle.
4. Upon observing the special cycle the Intel® SCH converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast internally by the master 8259 to the slave 8259. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
6. Upon receiving the second internally generated INTA# pulse, the 8259 returns the interrupt vector. If no interrupt request is present, the 8259 will return vector 7 from the master controller.
7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

18.3.3 Initialization Command Words (ICW)

Before operation can begin, each 8259 must be initialized. In the Intel® SCH this is a four byte sequence to ICW1, ICW2, ICW3, and ICW4. The address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the master controller, and A0h for the slave controller.

18.3.3.1 ICW1

A write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, Intel® SCH 8259 expects three more byte writes to 21h for the master controller, or A1h for the slave controller to complete the ICW sequence.

1. A write to ICW1 starts the initialization sequence during which the following automatically occur:
   a. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt
   b. The Interrupt Mask Register is cleared
   c. IRQ7 input is assigned priority 7
   d. The slave mode address is set to 7
   e. Special Mask Mode is cleared and Status Read is set to IRR.

18.3.3.2 ICW2

The second write in the sequence, ICW2, is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

18.3.3.3 ICW3

The third write in the sequence, ICW3, has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the Intel® SCH, IRQ2 is used. Therefore, bit 2 of ICW3 on the master controller is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the master controller broadcasts a code to the slave controller if the cascaded interrupt won arbitration on the master controller. The slave controller compares this identification code to the value stored in its ICW3, and if it matches, the slave controller assumes responsibility for broadcasting the interrupt vector.

18.3.3.4 ICW4

The final write in the sequence, ICW4, must be programmed both controllers. At the very least, bit 0 must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

18.3.4 Operation Command Words (OCW)

These command words reprogram the Interrupt Controller to operate in various interrupt modes.

- OCW1 masks and unmasks interrupt lines
- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function
- OCW3 is sets up ISR/IRR reads, enables/disables the Special Mask Mode SMM, and enables/ disables polled interrupt mode.

18.3.5 Modes of Operation

18.3.5.1 Fully Nested Mode

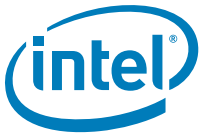
In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the CPU issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate another interrupt.

Interrupt priorities can be changed in the rotating priority mode.

18.3.5.2 Special Fully Nested Mode

This mode will be used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully nested mode is programmed to the master controller. This mode is similar to the fully nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority interrupts within the slave will be recognized by the master and will initiate interrupts to the processor. In the normal nested mode, a slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-Specific EOI command to the slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the master.



18.3.5.3 Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt will have to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2; the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the Rotate in Automatic EOI Mode which is set by (R=1, SL=0, EOI=0).

18.3.5.4 Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 will be the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: R=1, SL=1, and LO-L2 is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (R=1, SL=1, EOI=1 and LO-L2=IRQ level to receive bottom priority.

18.3.5.5 Poll Mode

Poll Mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine—do not need separate vectors if the service routine uses the poll command. Polled Mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll Command.

The Poll command is issued by setting P=1 in OCW3. The 8259 treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read will contain a 1 in bit 7 if there is an interrupt, and the binary code of the highest priority level in bits 2:0.

18.3.5.6 Edge and Level Triggered Mode

In ISA systems this mode is programmed using bit 3 in ICW1, which sets level or edge for the entire controller. In the Intel® SCH, this bit is disabled and a new register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control Registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low to high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector will be returned.

18.3.6 End of Interrupt (EOI)

18.3.6.1 Normal EOI

In Normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non- Specific. When a Non-Specific EOI command is issued, the 8259 will clear the highest ISR bit of those that are set to 1. A non-specific EOI is the normal mode of operation of the 8259 within the Intel® SCH, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the 8259 is operated in modes which preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI.

An ISR bit that is masked will not be cleared by a Non-Specific EOI if the 8259 is in the Special Mask Mode. An EOI command must be issued for both the master and slave controller.

18.3.6.2 Automatic EOI

In this mode, the 8259 will automatically perform a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single 8259. The AEOI mode can only be used in the master controller.

18.3.7 Masking Interrupts

18.3.7.1 Masking on an Individual Interrupt Request

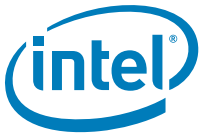
Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller will mask all requests for service from the slave controller.

18.3.7.2 Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The Special Mask Mode enables all interrupts not masked by a bit set in the Mask Register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the Special Mask Mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern.

The special Mask Mode is set by OCW3.SSMM and OCW3.SMM set, and cleared when OCW3.SSMM and OCW3.SMM are cleared.



18.3.8 Steering of PCI Interrupts

The Intel® SCH can be programmed to allow PIRQ[A:H]# to be internally routed to interrupts 3-7, 9-12, 14 or 15, through the PARC, PBRC, PCRC, PDRC, PERC, PFRC, PGRC, and PHRC registers in the chipset configuration section. One or more PIRQx# lines can be routed to the same IRQx input.

The PIRQx# lines are defined as active low, level sensitive. When PIRQx# is routed to specified IRQ line, software must change the corresponding ELCR1 or ELCR2 register to level sensitive mode. The Intel® SCH will internally invert the PIRQx# line to send an active high level to the 8259. When a PCI interrupt is routed onto the 8259, the selected IRQ can no longer be used by an ISA device.

18.3.9 I/O Registers

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ0–7), and at A0h and A1h for the slave controller (IRQ8–13). These registers have multiple functions, depending upon the data written to them. Table 61 provides a description of the different register possibilities for each address.

Table 61. 8259 I/O Register Mapping

Port		Register Name/Function	Aliases
20h	MICW1	Master Init. Cmd Word 1	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch
	MOCW2	Master Op Ctrl Word 2	
	MOCW3	Master Op Ctrl Word 3	
21h	MICW2	Master Init. Cmd Word 2	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh
	MICW3	Master Init. Cmd Word 3	
	MICW4	Master Init. Cmd Word 4	
	MOCW1	Master Op Ctrl Word 1	
A0h	SICW1	Slave Init. Cmd Word 1	A4h, A8h, ACh, B0h, B4h, B8h, BCh
	SOCW2	Slave Op Ctrl Word 2	
	SOCW3	Slave Op Ctrl Word 3	
A1h	SICW2	Slave Init. Cmd Word 2	A5h, A9h, ADh, B1h, B5h, B9h, BDh
	SICW3	Slave Init. Cmd Word 3	
	SICW4	Slave Init. Cmd Word 4	
	SOCW1	Slave Op Ctrl Word 1	
4D0h	ELCR1	Master Edge/Level Triggered	-
4D1h	E:CR2	Slave Edge/Level Triggered	-

18.3.9.1 MICW1/SICW1—Master/Slave Initialization Command Word 1 Register

Offset/Port:	Master: 20h Slave: A0h	Attribute:	WO
Default Value:	UUh	Size:	8 bits

Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

- The Interrupt Mask register is cleared
- IRQ7 input is assigned priority 7
- The slave mode address is set to 7
- Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Bit	Default and Access	Description
7:5	Undefined WO	These bits are MCS-85 specific, and not needed. Should be programmed to “000”.
4	Undefined WO	**ICW/OCW Select:** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	Undefined WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by ELCR1 and ELCR2.
2	Undefined WO	**ADI:** Ignored for the Intel® SCH. Should be programmed to 0.
1	Undefined WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	Undefined WO	**wICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

18.3.9.2 MICW2/SICW2—Master/Slave Initialization Command Word 2 Register

Offset/Port:	Master: 21h Slave: A1h	Attribute:	WO
Default Value:	UUh	Size:	8 bits

MICW2 and SICW2 are used to initialize the master or slave interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA values are 08h for the MICW2 and 70h for the SICW2.

<table>
<tr><th>Bit</th><th>Default and Access</th><th>Description</th></tr>
<tr><td>7:3</td><td>Undefined
WO</td><td>Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.</td></tr>
<tr><td>2:0</td><td>Undefined
WO</td><td>Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits 7:3 to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a 3-bit binary code:
<table>
<tr><th>Code</th><th>Master Interrupt</th><th>Slave Interrupt</th></tr>
<tr><td>000</td><td>IRQ0</td><td>IRQ8</td></tr>
<tr><td>001</td><td>IRQ1</td><td>IRQ9</td></tr>
<tr><td>010</td><td>IRQ2</td><td>IRQ10</td></tr>
<tr><td>011</td><td>IRQ3</td><td>IRQ11</td></tr>
<tr><td>100</td><td>IRQ4</td><td>IRQ12</td></tr>
<tr><td>101</td><td>IRQ5</td><td>IRQ13</td></tr>
<tr><td>110</td><td>IRQ6</td><td>IRQ14</td></tr>
<tr><td>111</td><td>IRQ7</td><td>IRQ15</td></tr>
</table>
</td></tr>
</table>

18.3.9.3 MICW3—Master Initialization Command Word 3 Register

Offset/Port: 21h Attribute: WO
Default Value: UUh Size: 8 bits

Bit	Default and Access	Description
7:3	Undefined WO	These bits must be programmed to 0.
2	Undefined WO	**Cascaded Controller Connection (CCC):** This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8-15 is cascaded on IRQ2.
1:0	Undefined WO	These bits must be programmed to 0.

18.3.9.4 SICW3—Slave Initialization Command Word 3 Register

Offset/Port: A1h Attribute: WO
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7:3	X WO	Reserved. Must be 0.
2:0	0 WO	**Slave Identification Code:** This field must be programmed to 02h to match the code broadcast by the master controller during the INTA# sequence.

18.3.9.5 MICW4/SICW4—Master/Slave Initialization Command Word 4 Register

Offset/Port:	Master: 21h Slave: A1h	Attribute:	WO
Default Value:	00h	Size:	8 bits

Bit	Default and Access	Description
7:5	0 WO	Reserved. Must be 0.
4	0 WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0 WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0 WO	**Master/Slave in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.
1	0 WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed. AEOI is discussed in Section 18.3.6.2.
0	0 WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

18.3.9.6 MOCW1/SOCW1—Master/Slave Operational Control Word 1 (Interrupt Mask) Register

Offset/Port:	Master: 21h Slave: A1h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Default and Access	Description
7:0	00h R/W	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

18.3.9.7 MOCW2/MOCW2—Master/Slave Operational Control Word 2 Register

Offset/Port:	Master: 20h Slave: A0h	Attribute:	WO
Default Value:	001UUUUUb	Size:	8 bits

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Default and Access	Description
7:5	001 WO	**Rotate and EOI Codes:** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 = Rotate in Auto EOI Mode (Clear) 001 = Non-specific EOI command 010 = No Operation 011 = *Specific EOI Command 100 = Rotate in Auto EOI Mode (Set) 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 – L2 Are Used
4:3	Undefined WO	**OCW2 Select:** When selecting OCW2, bits 4:3 = “00”
2:0	Undefined WO	**Interrupt Level Select (L2, L1, L0):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case.

Code	Interrupt Level
000	IRQ0/8
001	IRQ1/9
010	IRQ2/10
011	IRQ3/11
100	IRQ4/12
101	IRQ5/13
110	IRQ6/14
111	IRQ7/15

18.3.9.8 MOCW3/SOCW3—Master/Slave Operational Control Word 3 Register

Offset/Port:	Master: 20h Slave: A0h	Attribute:	RO, WO
Default Value:	001XXX10b	Size:	8 bits

Bit	Default and Access	Description
7	0 RO	Reserved. Must be 0.
6	0 WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	1 WO	**Enable Special Mask Mode (ESMM)** 0 = SMM bit becomes a “don't care” 1 = SMM bit is enabled to set or reset the Special Mask Mode
4:3	X WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = “01”.
2	X WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	10 WO	**Register Read Command (RRC):** These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not effect the register read selection. Following ICW initialization, the default OCW3 port address read will be “read IRR”. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 = No Action 01 = No Action 10 = Read IRQ Register 11 = Read IS Register

18.3.9.9 ELCR1—Master Edge/Level Control Register

Offset/Port:	4D0h	Attribute:	RO, R/W
Default Value:	00h	Size:	8 bits

Bit	Default and Access	Description
7:3	0 R/W	**Edge Level Control (ECL[7:3])**: In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0 RO	Reserved. The cascade channel, IRQ2, heart beat timer (IRQ0), and keyboard controller (IRQ1), cannot be put into level mode.

18.3.9.10 ELCR2—Slave Edge/Level Control Register

Offset/Port: 4D1h Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7	0 R/W	**Edge Level Control (ECL[15:14]):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0 RO	Reserved
4	0 R/W	**Edge Level Control (ECL[12:9]:** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0 RO	Reserved

18.4 Advanced Peripheral Interrupt Controller (IOxAPIC)

18.4.1 Functional Overview

Delivery of interrupts with the IOxAPIC is done by writing to a fixed set of memory locations in CPU(s).

The following sequence is used:

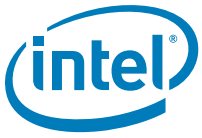
- When the Intel® SCH detects an interrupt event (active edge for edge-triggered mode or a change for level-triggered mode), it sets or resets the internal IRR bit associated with that interrupt.
- The Intel® SCH delivers the message by performing a write cycle to the appropriate address with the appropriate data.

When either an edge-triggered or level-triggered interrupt is detected, the “Assert Message” is sent by the IOxAPIC controller. In the case of a level-triggered interrupt, however, if the interrupt is still active after the EOI, then another “Assert Message” is sent to indicate that the interrupt is still active.

18.4.2 Unsupported Modes

These delivery modes are not supported for the following reasons:

- **NMI/INIT:** This cannot be delivered while the CPU is in the Stop Grant state. In addition, this is a break event for power management
- **SMI:** There is no way to block the delivery of the SMI#, except through BIOS
- **Virtual Wire Mode B:** The Intel® SCH does not support the INTR of the 8259 routed to the I/OxAPIC pin 0.



18.4.2.1 EOI (End Of Interrupt)

An EOI is performed as a PCI Express EOI message. The data of the EOI message is the vector. This value is compared with all the vectors inside the IOxAPIC, and any match causes RTE[x].RIRR to be cleared.

18.4.2.2 Interrupt Message Format

The Intel® SCH writes the message to the backbone as a 32-bit memory write cycle. It uses the following formats the Address and Data:

Table 62. Interrupt Delivery Address Value

Bit	Description
31:20	FEEh
19:12	**Destination ID:** RTE[x].DID
11:4	**Extended Destination ID:** RTE[x].EDID
3	**Redirection Hint:** If RTE[x].DLM = “Lowest Priority” (001), this bit will be set. Otherwise, this bit will be cleared.
2	**Destination Mode:** RTE[x].DSM
1:0	00

Table 63. Interrupt Delivery Data Value

Bit	Description
31:16	0000h
15	**Trigger Mode:** RTE[x].TM
14	**Delivery Status:** 1 = Assert, 0 = deassert. Only Assert messages are sent. This bit is always set to 1
13:12	00
11	**Destination Mode:** RTE[x].DSM
10:8	**Delivery Mode:** RTE[x].DLM
7:0	**Vector:** RTE[x].VCT

18.4.3 PCI Express Interrupts

When external devices through PCI Express generate an interrupt, they will send the message defined in the PCI Express specification for generating INTA# – INTD#. These will be translated internal assertions/deassertions of INTA# – INTD#.

18.4.4 Routing of Internal Device Interrupts

The internal devices on the Intel® SCH drive PCI interrupts. These interrupts can be routed internally to any of PIRQA# – PIRQH#. This is done utilizing the “Device X Interrupt Pin” and “Device X Interrupt Route” registers located in chipset configuration space. See Section 6.2.

For each device, the “Device X Interrupt Pin” register exists which tells the functions which interrupt to report in their PCI header space, in the “Interrupt Pin” register, for the operating system.

Additionally, the “Device X Interrupt Route” register tells the interrupt controller, in conjunction with the “Device X Interrupt Pin” register, which of the internal PIRQA# – PIRQH# to drive the devices interrupt onto. This requires the interrupt controller to know which function each device is connected to.

18.4.5 Memory Registers

The APIC is accessed through an indirect addressing scheme. These registers are mapped into memory space starting at address FEC00000h. The registers are shown below.

Table 64. APIC Memory-Mapped Register Locations

Address	Symbol	Register
FEC00000h	IDX	Index Register
FEC00010h	WDW	Window Register
FEC00040h	EOI	EOI Register

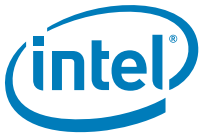
18.4.5.1 Address FEC00000h: IDX—Index Register

This 8-bit register selects which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired APIC internal register.

The registers listed below can be accessed through the IDX register. When accessing these registers, accesses must be done as DWs, otherwise unspecified behavior will result. Software should not attempt to write to reserved registers. Some reserved registers may return non-zero values when read.

Table 65. IDX Register Values

Offset	Symbol	Register	Default	Access
00h	ID	Identification	0000000h	RO, R/W
01h	VS	Version	0000000h	RO, R/W
10h–11h	RTE0	Redirection Table 0	0000000h	RO, R/W
12h–13h	RTE1	Redirection Table 1	0000000h	RO, R/W
3Eh–3Fh	RTE23	Redirection Table 23	0000000h	RO, R/W



18.4.5.2 ID—Identification Register

Offset: 00h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:28	0 RO	Reserved
27:24	0h R/W	**APIC Identification (AID):** Software must program this value prior to using the controller.
23:16	0 RO	Reserved
15	0 R/W	**Scratchpad**
14	0 R/W	Reserved. Writes to this bit have no effect.
13:0	0 RO	Reserved

18.4.5.3 VS—Version Register

Offset: 01h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

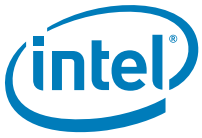
Bit	Default and Access	Description
31:24	00h RO	Reserved
23:16	17h RO	**Maximum Redirection Entries (MRE):** This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. In Intel® SCH this field is hardwired to 17h to indicate 24 interrupts.
15	0 RO	**Pin Assertion Register Supported (PRQ):** This bit Indicates that the IOxAPIC does not implement the Pin Assertion Register.
14:8	0 RO	Reserved
7:0	20h RO	**Version (VS):** This field identifies the implementation version as IOxAPIC.

18.4.5.4 RTE[0-23]—Redirection Table Entry Register

Offset: 10h–3Fh Attribute: RO, R/W
Default Value: see table below Size: 64 bits

There are a total of 24 Redirection Table Entry registers, each at a different 8-bit offset address, starting at 10h.

Bit	Default and Access	Description
63:56	X R/W	**Destination ID (DID):** Destination ID of the local APIC.
55:48	X R/W	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0 RO	Reserved
16	1 R/W	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	X R/W	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	X R/W	**Remote IRR (RIRR):** This is used for level triggered interrupts its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	X R/W	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	X RO	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	X R/W	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	X R/W	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are as follows: Value / Name/Notes 000 Fixed 001 Lowest Priority 010 SMI/not supported 011 Reserved 100 NMI/not supported 101 INIT/not supported 110 Reserved 111 ExtINT
10:0	X R/W	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 1-h and FEh.



18.4.5.5 Address FEC00010h: WDW—Window Register

This 32-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities.

18.4.5.6 Address FEC00040h: EOI—EOI Register

When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:8 are ignored.

18.5 Serial Interrupt

18.5.1 Overview

The interrupt controller supports a serial IRQ scheme. The signal used to transmit this information is shared between the interrupt controller and all peripherals that support serial interrupts. The signal line, SERIRQ, is synchronous to LPC clock, and follows the sustained tri-state protocol that is used by LPC signals. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S - Sample Phase:** Signal driven low
- **R - Recovery Phase:** Signal driven high
- **T - Turn-around Phase:** Signal released

The interrupt controller supports 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0- 1, 3-15), the four PCI interrupts, and the control signals SMI# and IOCHK#. Serial interrupt information is transferred using three types of frames:

- **Start Frame:** SERIRQ line driven low by the interrupt controller to indicate the start of IRQ transmission
- **Data Frames:** IRQ information transmitted by peripherals. The interrupt controller supports 21 data frames.
- **Stop Frame:** SERIRQ line driven low by the interrupt controller to indicate end of transmission and next mode of operation.

18.5.2 Start Frame

The serial IRQ protocol has two modes of operation which effect the start frame:

- **Continuous Mode:** The interrupt controller is solely responsible for generating the start frame
- **Quiet Mode:** Peripheral initiates the start frame, and the interrupt controller completes it.

These modes are entered through the length of the stop frame. See section 13.5.4 for information on how this is done.

Continuous mode must be entered first, to start the first frame. This start frame width is determined by the SCNT.SFPW field in D31:F0 configuration space. This is a polling mode.

In Quiet mode, the SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives SERIRQ low. The interrupt controller senses the line low and drives it low for the remainder of the Start Frame. Since the first LPC clock of the start frame was driven by the peripheral, the interrupt controller drives SERIRQ low for 1 LPC clock less than in continuous mode. This mode of operation allows for lower power operation.

18.5.3 Data Frames

Once the Start frame has been initiated, the SERIRQ peripherals start counting frames based on the rising edge of SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of one clock each:

- **Sample Phase:** During this phase, a device drives SERIRQ low if its corresponding interrupt signal is low. If its corresponding interrupt is high, then the SERIRQ devices tri-state SERIRQ. SERIRQ remains high due to pull-up resistors.
- **Recovery Phase:** During this phase, a device drives SERIRQ high if it was driven low during the Sample Phase. If it was not driven during the sample phase, it remains tri-stated in this phase.
- **Turn-around Phase:** The device tri-states SERIRQ.

18.5.4 Stop Frame

After the data frames, a Stop Frame will be driven by the interrupt controller. SERIRQ will be driven low for 2 or 3 LPC clocks. The number of clocks is determined by the SCNT.MD field in D31:F0 configuration space. The number of clocks determines the next mode:

Table 66. Serial Interrupt Mode Selection

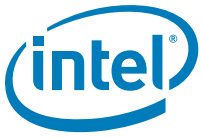
Stop Frame Width	Next Mode
2 LPC clocks	Quiet Mode: Any SERIRQ device initiates a Start Frame
3 LPC clocks	Continuous Mode: Only the interrupt controller initiates a Start Frame

18.5.5 Unsupported Serial Interrupts

There are four interrupts on the serial stream which are not supported by the serial interrupt controller of the Intel® SCH. These interrupts are generated internally, and are not sharable with other devices within the system. These interrupts are:

- IRQ0: Heartbeat interrupt generated off of the internal 8254, counter 0.
- IRQ8#: RTC interrupt can only be generated internally.
- IRQ13: This interrupt is not supported by the Intel® SCH.
- IRQ14: PATA interrupt can only be generated from the external P-Device.

The interrupt controller will ignore the state of these interrupts in the stream.



18.5.6 Data Frame Format

Table 67 shows the format of the data frames. The decoded INT[A:D]# values are ANDed with the corresponding PCI Express input signals (PIRQ[A:D]#). This way, the interrupt can be shared.

The other interrupts decoded through SERIRQ are also ANDed with the corresponding internal interrupts. For example, if IRQ10 is set to be used as the SCI, then it is ANDed with the decoded value for IRQ10 from the SERIRQ stream.

Table 67. Data Frame Format

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. IRQ0 can only be generated through the internal 8524
2	IRQ1	5	Before port 60h latch
3	SMI#	8	Causes SMI# if low. Will set bit 15 in the SMI_STS register
4	IRQ3	11	
5	IRQ4	14	
6	IRQ5	17	
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can only be generated internally
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	Before port 60h latch
14	IRQ13	41	Ignored
15	IRQ14	44	Ignored
16	IRQ15	47	
17	IOCHCK#	50	Same as ISA IOCHCK# going active.
18	PCI INTA#	53	
19	PCI INTB#	56	
20	PCI INTC#	59	
21	PCI INTD#	62	

18.6 Real Time Clock

18.6.1 Overview

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 ms to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768-kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block have very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions. A host-initiated write takes precedence over a hardware update in the event of a collision.

18.6.2 Update Cycles

An update cycle occurs once a second, if B.SET bit is not asserted and the divide chain is properly configured. During this procedure, the stored time and date will be incremented, overflow will be checked, a matching alarm condition will be checked, and the time and date will be rewritten to the RAM locations. The update cycle will start at least 488 μs after A.UIP is asserted, and the entire cycle will not take more than 1984 μs to complete. The time and date RAM locations (0-9) will be disconnected from the external bus during this time.

18.6.3 Interrupts

The RTC interrupt is internally routed within the Intel® SCH to interrupt vector 8. This interrupt is not it shared with any other interrupt. IRQ8# from the SERIRQ stream is ignored. The HPET can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

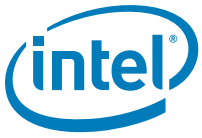
18.6.4 Lockable RAM Ranges

The RTC's battery-backed RAM supports two 8-byte ranges that can be locked through the PCI config space. If the locking bit is set, the corresponding range in the RAM will not be readable or writeable. A write cycle to those locations has no effect. A read cycle to those locations will not return the location's actual value (undefined).

Once a range is locked, the range can be unlocked only by a warm reset, which will invoke the BIOS and allow it to relock the RAM range.

18.6.5 Month and Year Alarms

Month and year alarms are not supported in the Intel® SCH.



18.6.6 I/O Registers

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A–D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM. All data movement between the host CPU and the RTC is done through registers mapped to the standard I/O space.

Table 68. RTC I/O Registers

I/O Locations	Function
70h and 74h	Real-Time Clock (Standard RAM) Index Register
71h and 75h	Real-Time Clock (Standard RAM) Target Register
72h and 76h	Extended RAM Index Register (if enabled)
73h and 77h	Extended RAM Target Register (if enabled)

NOTES:

1. I/O locations 70h and 71h are the standard ISA location for the real-time clock. Locations 72h and 73h are for accessing the extended RAM. The extended RAM bank is also accessed using an indexed scheme. I/O address 72h is used as the address pointer and I/O address 73h is used as the data register. Index addresses above 127h are not valid.
2. Software must preserve the value of bit 7 at I/O addresses 70h and 74h. When writing to this address, software must first read the value, and then write the same value for bit 7 during the sequential address write.

Note: Port 70h is not directly readable. The only way to read this register is through Alt Access mode. Although RTC Index bits 6:0 are readable from port 74h, bit 7 will always return 0. If the NMI# enable is not changed during normal operation, software can alternatively read this bit once and then retain the value for all subsequent writes to port 70h.

18.6.7 Indexed Registers

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70/71h or 72/73h), as shown in Table 69.

Table 69. RTC (Standard) RAM Bank

Index	Name
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Register A
0Bh	Register B
0Ch	Register C
0Dh	Register D
0Eh–7Fh	114 Bytes of User RAM

18.6.7.1 RTC_REGA—Register A

Offset: 0A Attribute: R/W
Default Value: UUh Size: 8 bit

This register is used for general configuration of the RTC functions. None of the bits are affected by RESET# or any other Intel® SCH reset signal.

Bit	Default and Access	Description
7	Undefined R/W	**Update In Progress (UIP):** This bit may be monitored as a status flag. 0 = The update cycle will not start for at least 488 µs. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:4	Undefined R/W	**Division Chain Select (DV[2:0]):** These three bits control the divider chain. The division chain itself is reset by RSMRST# to all 0s and it can also be cleared to 0s by firmware through programming of DV. The periodic event (setting of RTCIS.PF and the associated interrupt) can be based on the time as measured from RSMRST# deassertion until a divider reset (DV='11x' to '010') is performed by firmware. DV2 corresponds to bit 6. 010 = Normal Operation 11X = Divider Reset 101 = Bypass 15 stages (test mode only) 100 = Bypass 10 stages (test mode only) 011 = Bypass 5 stages (test mode only) 001 = Invalid 000 = Invalid
3:0	Undefined R/W	**Rate Select (RS[3:0]):** Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in Register B. Otherwise this tap will set the PF flag of Register C. If the periodic interrupt is not to be used, these bits should all be set to 0. RS3 corresponds to bit 3. 0000 = Interrupt never toggles 0001 = 3.90625 ms 0010 = 7.8125 ms 0011 = 122.070 µs 0100 = 244.141 µs 0101 = 488.281 µs 0110 = 976.5625 µs 0111 = 1.953125 ms 1000 = 3.90625 ms 1001 = 7.8125 ms 1010 = 15.625 ms 1011 = 31.25 ms 1100 = 62.5 ms 1101 = 125 ms 1110 = 250 ms 1111= 500 ms

18.6.7.2 RTC_REGB—Register B, General Configuration (LPC I/F—D31:F0)

Offset: 0Bh Attribute: R/W
Default Value: U0U00UUU Size: 8 bit

Bit	Default and Access	Description
7	Undefined R/W	**Update Cycle Inhibit (SET):** Enables/Inhibits the update cycles. This bit is not affected by RSMRST# nor any other reset signal. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to 0. When set is 1, the BIOS may initialize time and calendar bytes safely. **NOTE:** This bit should be set then cleared early in BIOS POST after each powerup.
6	0 R/W	**Periodic Interrupt Enable (PIE):** This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur with a time base set with the RS bits of register A.
5	Undefined R/W	**Alarm Interrupt Enable (AIE):** This bit is cleared by RTCRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the AF is set by an alarm match from the update cycle. An alarm can occur once a second, once an hour, once a day, or once a month.
4	0 R/W	**Update-Ended Interrupt Enable (UIE):** This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the update cycle ends.
3	0 R/W	**Square Wave Enable (SQWE):** This bit serves no function in the Intel® SCH. It is left in this register bank to provide compatibility with the Motorola 146818B. The Intel® SCH has no SQW pin. This bit is cleared by RSMRST#, but not on any other reset.
2	Undefined R/W	**Data Mode (DM).** This bit specifies either binary or BCD data representation. This bit is not affected by RSMRST# nor any other reset signal. 0 = BCD 1 = Binary
1	Undefined R/W	**Hour Format (HOURFORM):** This bit indicates the hour byte format. This bit is not affected by RSMRST# nor any other reset signal. 0 = 12-hour mode. In twelve-hour mode, the seventh bit represents a.m. as 0 and p.m. as 1. 1 = 24-hour mode.

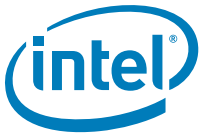
Bit	Default and Access	Description
0	Undefined R/W	**Daylight Savings Enable (DSE):** This bit triggers two special hour updates per year. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. This bit is not affected by RSMRST# nor any other reset signal. 0 = Daylight Savings Time updates do not occur. 1 = a) Update on the first Sunday in April, where time increments from 1:59:59 a.m. to 3:00:00 a.m. b) Update on the last Sunday in October when the time first reaches 1:59:59 a.m. it is changed to 1:00:00 a.m. The time must increment normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly.

18.6.7.3 RTC_REGC—Register C (Flag Register)

Offset: 0Ch Attribute: RO
Default Value: 00U00000 Size: 8 bit

Writes to Register C have no effect.

Bit	Default and Access	Description
7	0 RO	**Interrupt Request Flag (IRQF):** IRQF = (PF * PIE) + (AF * AIE) + (UF *UFE). This bit also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# or a read of Register C.
6	0 RO	**Periodic Interrupt Flag (PF):** This bit is cleared upon RSMRST# or a read of Register C. 0 = If no taps are specified through the RS bits in Register A, this flag will not be set. 1 = Periodic interrupt Flag will be 1 when the tap specified by the RS bits of register A is 1.
5	Undefined RO	**Alarm Flag (AF):** 0 = This bit is cleared upon RTCRST# or a read of Register C. 1 = Alarm Flag will be set after all Alarm values match the current time.
4	0 RO	**Update-Ended Flag (UF):** 0 = The bit is cleared upon RSMRST# or a read of Register C. 1 = Set immediately following an update cycle for each second.
3:0	0h RO	Reserved.



18.6.7.4 RTC_REGD—Register D (Flag Register)

Offset: 0Dh Attribute: R/W
Default Value: 10UUUUUU Size: 8 bit

Bit	Default and Access	Description
7	1 R/W	**Valid RAM and Time Bit (VRT):** 0 = This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles. 1 = This bit is hardwired to 1 in the RTC power well.
6	0 R/W	Reserved. This bit always returns a 0 and should be set to 0 for write cycles.
5:0	Undefined R/W	**Date Alarm:** These bits store the date of month alarm value. If set to 000000b, then a don't care state is assumed. The host must configure the date alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return 0s to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

18.7 General Purpose I/O

18.7.1 Functional Description

18.7.1.1 Power Wells

GPIO[6:0], GPIO[9:8], and SLPIOVR# are in the core well. GPIOSUS[3:0] are in the resume well.

18.7.1.2 SMI# and SCI Routing

If GPGPE.EN[n] is set, and the GPIO is configured as an input, the GPE bit GPE0S.GPIO will be set. If GPSMI.EN[n] is set, and the GPIO is configured as an input, the SMI bit SMIS.GPIO will be set.

18.7.1.3 Triggering

A GPIO (whether in the core well or resume well) can cause an wake event and SMI/SCI on either its rising edge, its falling edge, or both. These are controlled through the CGTPE and CGTNE registers for the core well GPIOs, and RGTPE and RGTNE for the resume well GPIOs. If the bit corresponding to the GPIO is set, the transition will cause a wake event/SMI/SCI, and the corresponding bit in the trigger status register (CGTS for core well GPIOs, RGTS for resume well GPIOs). The event can be cleared by writing a 1 to the status bit position.

18.7.2 I/O Registers

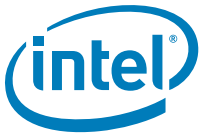
The control for the general purpose I/O signals is handled through an independent 64-byte I/O space. The base offset for this space is selected by the GPIOBASE register in D31:F0 config space.

Table 70. GPIO I/O Register Map

Offset	Mnemonic	Name	Default	Access
00h–03h	CGEN	Core Well GPIO Enable	000003FFh	RO, R/W
04h–07h	CGIO	Core Well GPIO Input/Output Select	000003FFh	RO, R/W
08h–0Bh	CGLV	Core Well GPIO Level for Input or Output	00000000h	RO, R/W
0Ch–0Fh	CGTPE	Core Well GPIO Trigger Positive Edge Enable	00000000h	RO, R/W
10h–13h	CGTNE	Core Well GPIO Trigger Negative Edge Enable	00000000h	RO, R/W
14h–17h	CGGPE	Core Well GPIO GPE Enable	00000000h	RO, R/W
18h–1Bh	CGSMI	Core Well GPIO SMI Enable	00000000h	RO, R/W
1Ch–1Fh	CGTS	Core Well GPIO Trigger Status	00000000h	RO, R/W
20h–23h	RGEN	Resume Well GPIO Enable	0000000Fh	RO, R/W
24h–27h	RGIO	Resume Well GPIO Input/Output Select	00000000h	RO, R/W
28h–2Bh	RGLV	Resume Well GPIO Level for Input or Output	00000000h	RO, R/W
2Ch–2Fh	RGTPE	Resume Well GPIO Trigger Positive Edge Enable	00000000h	RO, R/W
30h–33h	RGTNE	Resume Well GPIO Trigger Negative Edge Enable	00000000h	RO, R/W
34h–37h	RGGPE	Resume Well GPIO GPE Enable	00000000h	RO, R/W
38h–3Bh	RGSMI	Resume Well GPIO SMI Enable	00000000h	RO, R/W
3Ch–3Fh	RGTS	Resume Well GPIO Trigger Status	00000000h	RO, R/W

If a bit is allocated for a GPIO that doesn't exist, unless otherwise indicated, the bit will always read as 0 and values written to that bit will have no effect.

All core well bits are reset by the standard conditions that assert RESET#, and all suspend well bits are reset by the standard conditions that clear internal suspend registers.



18.7.2.1 CGEN—Core Well GPIO Enable Register

Offset: 00–03h Attribute: RO, R/W
Default Value: 000003FFh Size: 32 bits

Bit	Default and Access	Description
31:10	0s RO	Reserved
9	1 R/W	**GPIO 9 Enable (GP9EN)** 0 = Neither GPIO9 or EXTTS1# functionality is usable. 1 = GPIO9 will behave as a GPIO9 and allows EXTTS1# input to pass to the thermal management controller when CGIO[9] is set for input.
8	1 R/W	**GPIO 8 Enable (GP8EN)** 0 = GPIO8 will behave as PROCHOT# output 1 = GPIO8 will behave as a GPIO
7	1 RO	Reserved. GPIO7 is configured by the CMC as SLPIOVR#
6:0	7Fh RO	Reserved. All unmultiplexed GPIOs are enabled by default.

18.7.2.2 CGIO—Core Well GPIO Input/Output Select Register

Offset: 04–07h Attribute: RO, R/W
Default Value: 000003FFh Size: 32 bits

Bit	Default and Access	Description
31:10	0s RO	Reserved
9:0	3FFh R/W	**Input/Output (I/O)** 1 = the GPIO signal (if enabled) is programmed as an input. 0 = the GPIO signal is programmed as an output. If the pin is multiplexed, and not enabled, writes to these bits have no effect. **NOTE:** Do not write a “0” to bit 7, it may affect the SLPIOVR# configuration done by the CMC. **NOTE:** Bit 9 must be set in order for GPIO[9] to function as EXTTS1# input.

18.7.2.3 CGLVL—Core Well GPIO Level for Input or Output Register

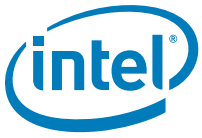
Offset: 08–0Bh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:10	0s RO	Reserved
9:0	0s R/W	**Level (LVL):** If the GPIO is programmed to be an output (CGIO.IO[n] = 0), then this bit is used by software to drive a value on the pin. 1 = high, 0 = low. If the GPIO is programmed as an input, then this bit reflects the state of the input signal (1 = high, 0 = low.) and writes will have no effect. The value of this bit has no meaning if the GPIO is disabled (CGEN.EN[n] = 0).

18.7.2.4 CGTPE—Core Well GPIO Trigger Positive Edge Enable Register

Offset: 0C–0Fh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:10	0s RO	Reserved
9:0	0s R/W	**Trigger Enable (TE)** 1 = corresponding GPIO, if enabled as input using GIO.IO[n], will case an SMI#/SCI when a 0-to-1 transition occurs. 0 = GPIO is not enabled to trigger an SMI#/SCI on a 0-to-1 transition. This bit has no meaning if CGIO.IO[n] is cleared (i.e., programmed for output)



18.7.2.5 CGTNE—Core Well GPIO Trigger Negative Edge Enable Register

Offset: 10–13h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:10	0s RO	Reserved
9:0	0s R/W	**Trigger Enable (TE)** 1 = corresponding GPIO, if enabled as input using CGIO.IO[n], will case an SMI#/SCI when a 1-to-0 transition occurs. 0 = GPIO is not enabled to trigger an SMI#/SCI on a 1-to-0 transition. This bit has no meaning if CGIO.IO[n] is cleared (i.e., programmed for output)

18.7.2.6 CGGPE—Core Well GPIO GPE Enable Register

Offset: 14–17h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:10	0s RO	Reserved
9:0	0s R/W	**Enable (EN):** When set, when CGTS.TS[n] is set, the ACPI GPE0E.GPIO bit will be set.

18.7.2.7 CGSMI—Core Well GPIO SMI Enable Register

Offset: 18–1Bh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:10	0s RO	Reserved
9:0	0s R/W	**Enable (EN):** When set, when CGTS.TS[n] is set, the ACPI SMIE.GPIO bit will be set.

18.7.2.8 CGTS—Core Well GPIO Trigger Status Register

Offset: 1C–1Fh Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Default and Access	Description
31:10	0s RO	Reserved
9:0	0s R/WC	**Trigger Status (TS)** 1 = the corresponding CGPIO, if enabled as input using CGIO.IO[n], triggered an SMI#/SCI. This will be set if a 0-to-1 transition occurred and CGTPE.TE[n] was set, or a 1-to-0 transition occurred and CGTNE.TE[n] was set. If both CGTPE.TE[n] and CGTNE.TE[n] are set, then this bit will be set on both a 0-to-1 and a 1-to-0 transition. This bit will not be set if the Core well GPIO[n] is configured as an output.

18.7.3 Resume Well GPIO I/O Registers

The resume-well I/O registers starting at offsets 20h through 3Ch follow the same format as their core-well counter parts detailed above. The only difference is that these registers live in the resume well and are not reset during removal of the core power supply.

Notable differences between the core well registers and the resume well versions are described below:

18.7.3.1 RGEN—Resume Well GPIO Enable Register

Offset: 20–23h Attribute: RO, R/W
Default Value: 00000FFh Size: 32 bits

Bit	Default and Access	Description
31:4	0s RO	Reserved
3	1 R/W	**Resume Well GPIO 3 Enable (RGP3EN)** 0 = GPIO3 will behave as USBCC input 1 = GPIO3 will behave as a GPIO
2:0	111b RO	Reserved. All unmultiplexed resume well GPIOs are enabled by default.

18.8 SMBus Controller

18.8.1 Overview

The Intel® SCH provides an SMBus 1.0-compliant host controller. The host controller provides a mechanism for the CPU to initiate communications with SMB peripherals (slaves).

The host controller is used to send commands to other SMB devices. It runs off of the backbone clock, with a minimum SMBCLK frequency the backbone clock divided by 4 (i.e., SMBCLK, at a minimum, is 4 backbone clocks). The frequency to use for SMBCLK is chosen by programming HCLK.DIV. To ensure proper data capture, the minimum value to be programmed into this register is 9h (for 33-MHz backbone), or 7h (for 25-MHz clock), resulting in a frequency roughly equivalent to 1 MHz. Software then sets up the host controller with an address, command, and for writes, data, and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it will generate an SMI# or interrupt, if enabled.

The host controller supports eight command protocols of the SMB interface (see the SMBus Specification): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process call, Block Read, Block Write and Block write-block read process call.

The host controller requires the various data and command fields be setup for the type of command to be sent. When software sets HCTL.ST, the host controller will perform the requested transaction and generate an interrupt or SMI# (if enabled) when finished. Once started, the values of the HCTL, HCMD, TSA, HD0, and HD1 should not be changed or read until HSTS.INTR has been set. The host controller will update all registers while completing the new command.

18.8.2 Bus Arbitration

Several masters may attempt to get on the bus at the same time by driving SMBDATA low to signal a start condition. When the Intel® SCH releases SMBDATA, and samples it low, then some other master is driving the bus and Intel® SCH must stop transferring data. If the Intel® SCH loses arbitration, it sets HSTS.BE, and if enabled, generates an interrupt or SMI#. The CPU is responsible for restarting the transaction.

18.8.3 Bus Timings

The SMBus runs at between 10–100 kHz. The Intel® SCH SMBus will run off of the backbone clock.

Table 71. SMBus Timings

Timing	Min AC	Spec Name
t_{LOW}	4.7 µs	Clock low period
t_{HIGH}	4.0 µs	Clock high period
$t_{SU:DAT}$	250 ns	Data setup to rising SMBCLK
$t_{HD:DAT}$	0 ns	Data hold from falling SMBCLK
$t_{HD:STA}$	4.0 µs	Repeat Start Condition generated from rising SMBCLK
$t_{SU:STA}$	4.7 µs	First clock fall from start condition
$t_{SU:STO}$	4.0 µs	Last clock rising edge to last data rising edge (stop condition)
t_{BUF}	4.7 µs	Time between consecutive transactions

The Min AC column indicates the minimum times required by the SMBus specification. The Intel® SCH tolerates these timings. When the Intel® SCH is sending address, command, or data bytes, it will drive data relative to the clock it is also driving. It will not start toggling the clock until the start or stop condition meets proper setup and hold. The Intel® SCH will also ensure minimum time between SMBus transactions as a master.

18.8.3.1 Clock Stretching

Devices may stretch the low time of the clock. When the Intel® SCH attempts to release the clock (allowing the clock to go high), the clock will remain low for an extended period of time. The Intel® SCH monitors SMBCLK after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. The low period of the clock can be stretched by an SMBus master if it is not ready to send or receive data.

18.8.3.2 Bus Time Out

If there is an error in the transaction, such that a device does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction will time out. The Intel® SCH will discard the cycle, and set HSTS.DE. The time out minimum is 25 ms. The time-out counter inside the Intel® SCH will start when the first bit of data is transferred by Intel® SCH.

18.8.4 SMI#

The system can be set up to generate SMI# by setting HCTL.SE.

18.8.5 I/O Registers

Table 72. SMBus I/O Register Map

Address	Mnemonic	Register Name	Default	Access
00h	HCTL	Host Control	00h	RO, R/W
01h	HSTS	Host Status	00h	R/W
02h–03h	HCLK	Host Clock Divider	0000h	R/W
04h	TSA	Transmit Slave Address	00h	R/W
05h	HCMD	Host Command	00h	R/W
06h	HD0	Host Data 0	00h	R/W
07h	HD1	Host Data 1	00h	R/W
20h–3Fh	HBD	Host Block Data	00h	R/W

18.8.5.1 HCTL—Host Control Register

Offset: 00h Attribute: RO, R/W
Default Value: 00h Size: 8 bits

Bit	Default and Access	Description
7	0 R/W	**SMI Enable (SE):** Enable generation of an SMI# upon completion of the command.
6	0 RO	Reserved
5	0 R/W	**Alert Enable (AE):** Software sets this bit to enable an interrupt/SMI# due to SMBALERT#.
4	0 R/W	**Start/Stop (ST):** Initiates the command described in the CMD field. This bit always reads zero. HSTS.BSY identifies when the Intel® SCH has finished the command. If this bit is cleared prior to the command completing, the transaction will be stopped, and HSTS.CS will be cleared.
3	0 RO	Reserved
2:0	R/W	**Command (CMD):** Indicates the command that the Intel® SCH is to perform. If enabled, the Intel® SCH will generate an interrupt or SMI# when the command has completed. If a reserved command is issued, the Intel® SCH will set HSTS.DE and perform no command, and will not operate until HSTS.DE is cleared.

Bits	Command Description
000	**Quick**: Uses TSA.
001	**Byte**: Uses TSA and CMD registers. TSA.R determines the direction.
010	**Byte Data**: Uses TSA, CMD, and HD0 registers. TSA.R determines the direction. If a read, HD0 will contain the read data.
011	**Word Data**: Uses TSA, CMD, HD0, and HD1 registers. TSA.R determines the direction. If a read, HD0 and HD1 contain the read data.
100	**Process Call:** Uses TSA, HCMD, HD0, and HD1 registers. TSA.R determines the direction. Upon completion, HD0 and HD1 contain the read data.
101	**Block**: Uses TSA, CMD, HD0, and HBD registers. For writes, the count is stored in HD0 and indicates how many bytes of data will be transferred. For reads, the count is received and stored in HD0. TSA.R determines the direction. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of HBD. For reads, the data is stored in HBD.
110 - 111	Reserved

18.8.5.2 HSTS—Host Status Register

Offset: 01h Attribute: RO, R/W
Default Value: 00h Size: 8 bits

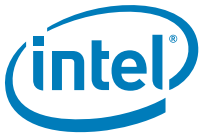
Bit	Default and Access	Description
7:4	0h RO	Reserved
3	0 RO	**Busy (BSY):** When set, indicates that the Intel® SCH is running a command. No SMB registers should be accessed while this bit is set.
2	0 R/WC	**Bus Error (BE):** When set, indicates a transaction collision.
1	0 R/WC	**Device Error (DE):** When set, this indicates one of the following errors: Invalid Command Field, an unclaimed cycle, or a time-out error.
0	0 R/WC	**Completion Status (CS):** When BSY is cleared, if this bit is set, the command completed successfully. If cleared, the command did not complete successfully.

18.8.5.3 HCLK—Host Clock Divider Register

Offset: 02h Attribute: R/W
Default Value: 0000h Size: 8 bits

Bit	Default and Access	Description
15:0	00h R/W	**Divider (DIV):** This controls how many backbone clocks should be counted for the generation of SMBCLK. Recommended values are listed below:

SM Bus Frequency	Backbone Frequency	
	33 MHz	25 MHz
1 kHz	208Eh	186Ah
10 kHz	0342h	0271h
50 kHz	00A7h	007Dh
100 kHz	0054h	003Fh
400 kHz	0015h	0010h
1 MHz	0009h	0007h



18.8.5.4 TSA—Transmit Slave Address Register

Offset:	04h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Default and Access	Description
7:1	0 R/W	**Address (AD):** 7-bit address of the targeted slave.
0	0 R/W	**Read (R):** Direction of the host transfer. 0 = write 1 = read

18.8.5.5 HCMD—Host Command Register

Offset:	05h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This field is transmitted in the command field of the SMB protocol during the execution of any command.

Bit	Default and Access	Description
7:0	00h R/W	**Command (CMD)**

18.8.5.6 HD0—Host Data 0 Register

Offset:	06h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This field is transmitted in the DATA0 field of an SMBus cycle. For block writes, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1h (1 bytes) and 20h (32 bytes) for block counts. A count of 00h or above 20h will result in no transfer and will set HSTS.F.

Bit	Default and Access	Description
7:0	00h R/W	**DATA 0**

18.8.5.7 HD1—Host Data 1 Register

Offset:	07h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This field is transmitted in the DATA1 field of an SMBus cycle.

Bit	Default and Access	Description
7:0	00h R/W	**DATA 1**

18.8.5.8 HBD—Host Data Block Register

Offset:	20h–3Fh	Attribute:	4R/W
Default Value:	00h	Size:	256 bits

Bit	Default and Access	Description
255:0	0 R/W	**Data (D):** This contains block data to be sent on a block write command, or received block data, on a block read command. Any data received over 32-bytes will be lost.

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19 Absolute Maximums and Operating Conditions

19.1 Absolute Maximums

Table 73 lists the Intel® SCH maximum environmental stress ratings. Functional operating parameters at the absolute maximum and minimum is neither implied nor ensured.

The voltage on a specific pin shall be denoted as "V" followed by the subscripted name of that pin. For example:

- V_{TT} refers to the voltage applied to the V_{TT} signal (In the case of power supply signal names, the second V is not repeated in the subscripted portion.)
- V_{H_SWING} would refer to the voltage level of the H_SWING signal.

Caution: At conditions outside functional operation limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits. If the component is exposed to conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded. Although the device contains protective circuitry to resist damage from electro-static discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 73. Intel® SCH Absolute Maximum Ratings (Sheet 1 of 2)

Parameter	Description / Signal Names	Min	Max	Unit
T_{die}	Die Temperature under bias[1]	0	90	ºC
$T_{storage\ (short\text{-}term)}$ $T_{storage\ (sustained\ exposure)}$	Storage Temperature[2, 3,5] Storage Temperature[2, 3,5]	-45 -10	75 45	ºC
Voltage on any 3.3-V Pin with respect to Ground		-0.5	V_{CC33} + 0.5	V
Voltage on any 5-V Tolerant Pin with respect to Ground (V_{CC5REF} = 5 V)		-0.5	V_{CC5REF} + 0.5	V
1.05-V Supply Voltage with respect to V_{SS}	VCC, VTT, VCCSUSBYP, VCCSUSUSBBYP	-0.5	2.1	V
1.5 V Supply Voltage with respect to V_{SS}	VCCAHPLL, VCCDHPLL, VCCLVDS, VCCSDVO, VCCPCIE, VCCAPCIEPLL, VCCADPLLA, VCCADPLLB, VCC15, VCC15, VCC15USB, VCC15USBSUSBYP, VCCAUSBPLL, VCC15SUS, VCCRTCBYP, VCCHDA[4]	-0.5	2.1	V

Table 73. Intel® SCH Absolute Maximum Ratings (Sheet 2 of 2)

Parameter	Description / Signal Names	Min	Max	Unit
1.8 V Supply Voltage with respect to V_{SS}	VCCSM	-0.3	2.3	V
3.3 V Supply Voltage with respect to V_{SS}	VCCAPCIEBG, VCC33, VCC33, VCCP33USBSUS, VCCAUSBBGSUS, VCC33SUS, VCC33RTC, VCCHDA	-0.5	4.6	V
5.0 V Supply Voltage with respect to V_{SS}	VCC5REF, VCC5REFSUS	-0.5	5.5	V

NOTES:
1. Functionality is not ensured for parts that exceed T_{die} temperature above 90ºC. T_{die} is measured at top center of the package. Full performance may be affected if the on-die thermal sensor is enabled.
2. Possible damage to the Intel® SCH may occur if the Intel® SCH storage temperature exceeds 75ºC. Intel does not ensure functionality for parts that have exceeded temperatures above 75ºC due to specification violation.
3. Storage temperature is applicable to storage conditions only. In this scenario, the device must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not effect the long-term reliability of the device. This rating applies to the silicon and does not include any tray or packaging.
4. VCCHDA is configurable for 1.5-V or 3.3-V operation. Use the appropriate Maximum Limits for the selected configuration.
5. In addition to this storage temperature specification, compliance to the latest IPC/JEDEC J-STD-033B.1 joint industry standard is required for all Surface Mount Devices (SMDs). This document governs handling, packing, shipping and use of moisture/reflow sensitive SMDs.

Table 74. Intel® SCH Maximum Power Consumption

Power Plane	Maximum Power Consumption			Unit	Notes
Symbol	S0	S3	S4/S5		
	See Table 77	50m	100u	W	1, 2

NOTES:
1. This specification applies for worst case scenario per rail. In this context, a cumulative use of these values will represent a non realistic application.
2. These power numbers should not be used for average battery shelf life projections since these are absolute worst case numbers.

20 DC Characteristics

20.1 Signal Groups

The signal description includes the type of buffer used for the particular signal.

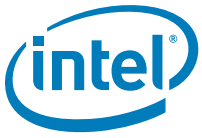
Table 75. Intel® SCH Buffer Types

Buffer Type	Description
AGTL+	Assisted Gunning Transceiver Logic Plus. Open Drain interface signals that require termination. Refer to the AGTL+ I/O Specification for complete details.
CMOS, CMOS Open Drain	1.05-V CMOS buffer
CMOS_HDA	CMOS buffers for Intel HD Audio interface that can be configured for either 1.5-V or 3.3-V operation.
CMOS1.8	1.8-V CMOS buffer. These buffers can be configured as Stub Series Termination Logic (SSTL1.8)
CMOS3.3, CMOS3.3 Open Drain	3.3-V CMOS buffer
CMOS3.3-5	3.3-V CMOS buffer, 5-V tolerant
USB	Compliant with USB1.1 and USB2.0 specifications.
PCIE	PCI Express interface signals. These signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 V_{max}. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V.
SDVO	Serial-DVO differential output buffers. These signals are AC coupled.
LVDS	Low Voltage Differential Signal buffers. These signals should drive across a 100-Ohm resistor at the receiver when driving.
Analog	Analog reference or output. Can be used as a threshold voltage or for buffer compensation.

Table 76. Intel® SCH Signal Group Definitions

Signal Group	Signals	Notes
AGTL+	H_ADS#, H_ADSTB[1:0]#, H_DBSY#, H_DEFER#, H_DRDY#, H_DSTBN[3:0]#, H_DSTBP[3:0]#, H_BPRI#, H_CPURST#, H_TRDY#, H_RS[2:0]#, H_DPWR#	
CMOS	H_A[31:3]#, H_BNR#, H_BREQ0#, H_D[63:0]#, H_DINV[3:0]#, H_HIT#, H_HITM#, H_REQ[4:0]#, H_LOCK#, H_THRMTRIP#, H_CPUSLP#, H_PBE#, H_INTR, H_NMI, H_SMI#, TDI, TMS, TRST#, H_STPCLK#, H_DPSLP#, H_DPRSTP#, H_CPUPWRGD, BSEL2, CFG[1:0], TCK	1
CMOS Open Drain	H_INIT#	
CMOS_HDA	HDA_RST#, HDA_SYNC, HDA_SDO, HDA_SDI[1:0], HDA_DOCKEN#, HDA_DOCKRST#	2
CMOS1.8	SM_DQ[63:0], SM_DQS[7:0], SM_MA[14:0], SM_BS[2:0], SM_RAS#, SM_CAS#, SM_WE#, SM_RCVENIN#, SM_RCVENOUT#, SM_CS[1:0]#, SM_CKE[1:0]	
CMOS3.3	LPC_AD[3:0], LPC_FRAME#, LPC_SERIRQ, LPC_CLKRUN# SD2_DATA[7:0], SD[0:2]_CMD, SD[0:2]_WP, SD[0:2]_CD#, SD[0:2]_LED, INTVRMEN, SPKR, SMI#, EXTTS, THRM#, RESET#, PWROK, RSMRST#, RTCRST#, SUSCLK, WAKE#, STPCPU#, DPRSLPVR, SLPMODE, RSTWARN, SLPRDY#, RSTRDY#, L_VDDEN, L_BKLTEN, L_BKLTCTL, USB_OC[7:0]#, GPIO[9:8], SLPIOVR#, GPIO[6:0], GPIOSUS[3:0]	
CMOSS3.3 Open Drain	CLKREQ#, GPE#, TDO, L_DDC_CLK, L_DDC_DATA, L_CTLA_CLK, L_CTLB_CLK, SDVO_CTRLCLK, SDVO_CTRLDATA, SMB_DATA, SMB_ALERT#	
CMOS3.3-5	PATA_DD[15:0], PATA_DA[2:0], PATA_DIOR#, PATA_DIOW#, PATA_DDACK#, PATA_DCS3#, PATA_DCS1#, PATA_DDREQ, PATA_IORDY, PATA_IDEIRQ	
PCIE	PCIE_PETp[2:1], PCIE_PETn[2:1], PCIE_PERp[2:1], PCIE_PERn[2:1]	
SDVO	SDVOB_RED+, SDVOB_RED-, SDVOB_GREEN+, SDVOB_GREEN-, SDVOB_BLUE+, SDVOB_BLUE-, SDVOB_CLK+, SDVOB_CLK- SDVOB_INT+, SDVOB_INT-, SDVO_TVCLKIN+, SDVO_TVCLKIN-, SDVO_STALL+, SDVO_STALL-	
LVDS	LA_DATAP[3:0], LA_DATAN[3:0], LA_CLKP, LA_CLKN	
USB	USB_DP[7:0], USB_DN[7:0]	
Analog, Reference	H_RCOMPO, H_SWING, H_GVREF, H_CGVREF, PCIE_ICOMPO, SM_VREF, SM_RCOMPO, PCIE_ICOMPI, RTC_X1, RTC_X2, USB_RBIASP, USB_RBIASN	
Clocks	H_CLKINP, H_CLKINN, PCIE_CLKINP, PCIE_CLKINN, USB_CLK48, SMB_CLK, LPC_CLKOUT[1:0], DA_REFCLKINP, DA_REFCLKINN, DB_REFCLKINPSCC, DB_REFCLKINNSCC, HDA_CLK, SUSCLK, SD[2:0]_CLK, SM_CK[1:0], SM_CK[1:0]#, CLK14, RTC_X1, RTC_X2	

NOTES:
1. These are 1.05-V buffers powered by VTT (except BSEL and TCK which are powered by VCC).
2. The Intel HD Audio interface signals can operate in either 1.5-V or 3.3-V ranges. 3.3 V operation is the default. The HDA interface can be configured to use the low voltage range by setting the Low Voltage Mode Enable bit of the HDCTL PCI configuration register (D27:F0, offset 40h, bit 0).



20.2 Power and Current Characteristics

Table 77. Thermal Design Power

Symbol	Parameter	Range	Unit	Notes
TDP	Thermal Design Power (under nominal voltages)	1.6 – 2.3	W	1

NOTES:

1. This specification is the Thermal Design Power and is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component. It does not represent the expected power generated by a power virus. Studies by Intel indicate that no application will cause thermally significant power dissipation exceeding this specification, although it is possible to concoct higher power synthetic workloads that write but never read. Under realistic read/write conditions, this higher power workload can only be transient and is accounted in the AC (max) specification.

Table 78. DC Current Characteristics (Sheet 1 of 2)

Symbol	Parameter	Signal Names	Max[1,2]	Unit	Notes
I_{VTT}	1.05-V V_{TT} Supply Current	VTT	739	mA	3
I_{VCC_105}	1.05-V Core Supply Current	VCC	1800	mA	4,5
I_{VCC_15}	1.5-V Core Supply Current	VCC15	10	mA	
$I_{VCCPCIE}$	1.5-V PCI Express Supply Current	VCCPCIE, VCCPCIEPLL	250	mA	6,7
$I_{VCCLVDS}$	1.5-V LVDS Supply Current	VCCLVDS	62	mA	
$I_{VCCSDVO}$	1.5-V SDVO Supply Current	VCCSDVO	73	mA	
$I_{VCCPCIEBG}$	3.3-V PCI Express Band Gap	VCCPCIEBG	5	mA	
I_{VCC33}	3.3-V HV CMOS Supply Current	VCC33	100	mA	
$I_{VCCHPLL}$	1.5-V Host PLL Supply Current	VCCAHPLL, VCCDHPLL	15 42	mA mA	
$I_{VCCADPLLA,B}$	1.5-V Display PLLA and PLLB Supply Current	VCCADPLLA, VCCADPLLB	48 48	mA mA	
$I_{VCCUSB15}$	1.5-V USB Core Current	VCCUSBCORE	322	mA	
$I_{VCCUSBSUS}$	3.3-V USB Suspend Current	VCC33USBSUS	32	mA	
$I_{VCCUSBSUSBG}$	3.3-V USB Suspend Bandgap Current	VCC33USBBGSUS	5	mA	
$I_{VCCUSBPLL}$	1.5-V USB PLL Current	VCCAUSBPLL	11	mA	
$I_{VCCSUS33}$	3.3-V Suspend Current	VCC33SUS	5	mA	
$I_{VCC33RTC}$	3.3-V Real Time Clock	VCC33RTC	6	µA	
$I_{VCC5REF}$	5-V Reference Current	VCC5REF	3	mA	
$I_{VCC5REFSUS}$	5-V Suspend Current	VCC5REFSUS	1	mA	

Table 78. DC Current Characteristics (Sheet 2 of 2)

Symbol	Parameter	Signal Names	Max[1,2]	Unit	Notes
DDR2 Interface[8,9]					
I_{VCCSM}	DDR2 System Memory: (1.8-V, 533 MTs) (1.5-V, 533 MTs)	VCCSM	 568 473	mA	
I_{SUS_VCCSM}	DDR2 System Memory Interface (1.8-V) Standby Supply Current	VCCSM	~5	mA	10
I_{SMVREF}	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current		10	µA	
I_{SUS_SMVREF}	DDR2 System Memory Interface Reference Voltage (0.90 V) Standby Supply Current		10	µA	10
I_{TTRC}	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current	VCCSM	20	mA	
I_{SUS_TTRC}	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Standby Supply Current	VCCSM	15	µA	10

NOTES:
1. This note has been removed.
2. I_{CCMAX} is determined on a per-interface basis, and all cannot happen simultaneously.
3. Can vary from CPU. This estimate does not include sense Amps, as they are on a separate rail, or processor-specific signals.
4. Estimate is only for max current coming through the chipset's supply balls.
5. Includes maximum leakage.
6. Rail includes PLL current.
7. I_{CCMAX} number includes max current for all signal names listed in the table.
8. Determined with 2x Intel® SCH DDR2 buffer strength settings into a 50 Ohms to ½ VCCSM (DDR/DDR2) test load.
9. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express specification and measured over any 250 consecutive TX UI's. Specified at the measurement point and measured over any 250 consecutive ULS. The test load shown in receiver compliance eye diagram of PCI Express specification. Should be used as the RX device when taking measurements
10. Standby refers to system memory in Self Refresh during S3 (STR).

20.3 General DC Characteristics

The voltage on a specific pin shall be denoted as “V” followed by the subscripted name of that pin. For example:

- V_{TT} refers to the voltage applied to the VTT signal. (In the case of power supply signal names, the second V is not repeated in the subscripted portion.)
- V_{H_SWING} would refer to the voltage level of the H_SWING signal

Table 79. Operating Condition Power Supply and Reference DC Characteristics (Sheet 1 of 2)

Signal Name	Parameter	Min	Nom	Max	Unit	Notes
Power Supply Voltages						
VCC	1.05 V Intel® SCH Core Supply Voltage	0.9975	1.05	1.1025	V	
VTT	1.05 V Host AGTL+ Termination Voltage	0.9975	1.05	1.1025	V	
VCC15 VCCPCIE VCCSDVO VCCLVDS VCC15USB	1.5 V Supply Voltage	1.425	1.50	1.575	V	
VCCAHPLL VCCDHPLL VCCAPCIEPLL VCCADPLLA VCCADPLLB VCCAUSBPLL	Various 1.5 V PLL Supply Voltages	1.425	1.5	1.575	V	1
VCCSM	1.8 V DDR2 I/O Supply Voltage 1.5 V DDR2 I/O Supply Voltage	1.7 1.425	1.8 1.5	1.9 1.575	V	
VCC33 VCCPCIEBG	3.3 V Power Supply Voltage	3.135	3.3	3.465	V	
VCCHDA	1.5/3.3 V Supply for Intel High Definition Audio	1.425 3.135	1.5 3.3	1.575 3.465	V	
VCC33SUS VCCP33USBSUS VCCAUSBBGSUS	3.3 V Suspend-Well Power Supplies	3.135	3.3	3.465	V	
VCC5REF VCC5REFSUS	5 V Reference Voltages	4.75	5.0	5.25	V	
VCC33RTC	Real Time Clock Voltage	2.0	3.3	3.6	V	
Reference Signals						
H_SWING	Host Compensation Reference Voltage	0.3125 x V_{TT} – 1%	0.3125 x V_{TT}	0.3125 x V_{TT} + 1%	V	
H_GVREF	Host AGTL+ Reference Voltage	2/3 x V_{TT} – 1%	2/3 x V_{TT}	2/3 x V_{TT} + 1%	V	

Table 79. Operating Condition Power Supply and Reference DC Characteristics (Sheet 2 of 2)

Signal Name	Parameter	Min	Nom	Max	Unit	Notes
H_CGVREF	Host CMOS Reference Voltage	0.49 x V_{TT}	0.50 x V_{TT}	0.51 x V_{TT}	V	
SM_VREF	DDR2 Reference Voltage	0.49 x V_{CCSM}	0.50 x V_{CCSM}	0.51 x V_{CCSM}		
H_RCOMPO SM_RCOMPO PCIE_ICOMPO PCIE_ICOMPI USB_RBIASP USB_RBIASN						

Table 80. Active Signal DC Characteristics (Sheet 1 of 3)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
AGTL+						
V_{IL}	Input Low Voltage	–0.1	0.0	$^2/_3$ V_{TT} – 0.1	V	
V_{IH}	Input High Voltage	$^2/_3$ V_{TT} + 0.1	V_{TT}	V_{TT} + 0.1	V	
V_{OL}	Output Low Voltage	—	—	$^1/_3$ V_{TT} + 0.1	V	
V_{OH}	Output High Voltage	V_{TT} – 0.1	—	VTT	V	
I_{OL}	Output Low Current	—	—	V_{TTMAX} ÷ (1.5 R_{ttmin})	mA	1
I_{LEAK}	Input Leakage Current	—	—	20	µA	2
C_{IN}	Input Capacitance	2	—	3.5	pF	
CMOS, CMOS Open Drain						
V_{IL}	Input Low Voltage	–0.1	0.0	½ V_{TT} – 0.7	V	4
V_{IH}	Input High Voltage	½ V_{TT} + 0.7	V_{TT}	V_{TT} + 0.1	V	4
V_{OL}	Output Low Voltage	—	—	0.1 x VTT	V	4
V_{OH}	Output High Voltage	0.9 x V_{TT}	—	VTT	V	4
I_{LEAK}	Input Leakage Current	—	—	20	µA	2, 3
C_{IN}	Input Capacitance	1	—	3.5	pF	
CMOS_HDA						
V_{IL}	Input Low Voltage	–0.1	0.0	½ V_{CCHDA} – 0.7	V	
V_{IH}	Input High Voltage	½ V_{CCHDA} + 0.7	V_{CCHDA}	V_{CCHDA} + 0.1	V	
V_{OL}	Output Low Voltage	—	—	0.1 V_{CCHDA}	V	
V_{OH}	Output High Voltage	0.9 V_{CCHDA}	—	—	V	
I_{LEAK}	Input Leakage Current	—	—	20	µA	
C_{IN}	Input Capacitance	2	—	3.5	pF	
CMOS1.8						
V_{IL}	Input Low Voltage	—	—	V_{SM_VREF} – 0.250	V	
V_{IH}	Input High Voltage	V_{SM_VREF} + 0.250	—	—	V	

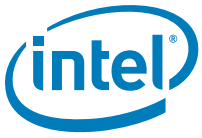


Table 80. Active Signal DC Characteristics (Sheet 2 of 3)

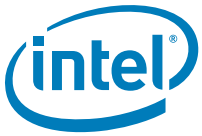
Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{OL}	Output Low Voltage	—	—	V_{SM_VREF} – 0.250	V	
V_{OH}	Output High Voltage	V_{SM_VREF} + 0.250	—	—	V	
I_{OL}	Output Low Current	—	—	0.3	mA	
I_{LEAK}	Input Leakage Current	—	—	1.4	µA	5
C_{IN}	Input Capacitance	2.0	—	3.4	pF	
CMOS3.3, CMOS3.3 Open Drain						
V_{IL}	Input Low Voltage	–0.1	0.0	½ V_{CC33} – 0.7	V	
V_{IH}	Input High Voltage	½ V_{CC33} + 0.7	V_{CC33}	V_{CC33} + 0.1	V	
V_{OL}	Output Low Voltage	—	—	0.1 V_{CC33}	V	3
V_{OH}	Output High Voltage	0.9 V_{CC33}	—	—	V	3
I_{OL}	Output Low Current	—	—	1.5	mA	
I_{OH}	Output High Current	—	—	-0.5mA	mA	
I_{LEAK}	Input Leakage Current	—	—	20	µA	3
C_{IN}	Input Capacitance	1	—	3.5	pF	
CMOS3.3–5						
V_{IL}	Input Low Voltage	–0.1	0.0	½ V_{CC33} – 0.7	V	
V_{IH}	Input High Voltage	½ V_{CC33} + 0.7	V_{CC33}	V_{CC33} + 0.1	V	
V_{OL}	Output Low Voltage	—	—	0.1 V_{CC33}	V	
V_{OH}	Output High Voltage	0.9 V_{CC33}	—	—	V	
I_{LEAK}	Input Leakage Current	—	—	20	µA	
C_{IN}	Input Capacitance	1	—	3.5	pF	
USB						
Refer to the *Universal Serial Bus (USB) Base Specification, Rev. 2.0*.						
PCIE						
$V_{TX\text{-}DIFF\ P\text{-}P}$	Differential Peak to Peak Output Voltage	0.4	—	0.6	V	6
$V_{TX\_CM\text{-}ACp}$	AC Peak Common Mode Output Voltage	—	—	20	mV	6
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX\text{-}DIFF\ p\text{-}p}$	Differential Input Peak to Peak Voltage	0.175	—	1.2	V	6
$V_{RX\_CM\text{-}ACp}$	AC peak Common Mode Input Voltage	—	—	150	mV	
SDVO						
$V_{TX\text{-}DIFF\ P\text{-}P}$	Differential Peak to Peak Output Voltage	0.4	—	0.6	V	6
$V_{TX\_CM\text{-}ACp}$	AC Peak Common Mode Output Voltage	—	—	20	mV	6

Table 80. Active Signal DC Characteristics (Sheet 3 of 3)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX-DIFF\ p-p}$	Differential Input Peak to Peak Voltage	0.175	—	1.2	V	6
V_{RX_CM-ACp}	AC peak Common Mode Input Voltage	—	—	150	mV	
LVDS						
V_{OD}	Differential Output Voltage	250	350	450	mV	
ΔV_{OD}	Change in V_{OD} between Complementary Output States	0.8	—	50	mV	
V_{OS}	Offset Voltage	—	1.25	1.375	V	
ΔV_{OS}	Change in V_{OS} between Complementary Output States	—	—	50		
I_{Os}	Output Short Circuit Current	—	-3.5	-10		
I_{OZ}	Output Tristate Current	—	±1	±10		
Differential Clocks						
V_{SWING}	Input swing	300	—	—	mV	7, 8
V_{CROSS}	Crossing point	300	—	550	mV	7, 9, 10, 11
V_{CROSS_VAR}	V_{CROSS} Variance	—	—	140	mV	7, 9, 10, 12
V_{IH}	Maximum input voltage	—	—	1.15	V	7, 9, 13
V_{IL}	Minimum input voltage	-0.3	—	—	V	7, 9, 14
RTC_X1, RTC_X2						
V_{IL}	Input Low Voltage	-0.5	—	0.1	V	
V_{IH}	Input High Voltage	0.4	—	1.2	V	
C_{IN}	Input Capacitance		3.5		pF	

NOTES:

1. R_{ttmin} = 50 Ohm
2. $V_{OL} < V_{PAD} < V_{TT}$
3. For CMOS Open Drain signals defined in Table 80, V_{OH}, V_{OL}, and I_{LEAK} DC specifications are not applicable due to the pull-up/pull-down resister that is required on the board.
4. BSEL2, CFG[1:0] and TCK signals reference V_{CC}, not V_{TT}.
5. At VCCSM = 1.7 V.
6. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express specification and measured over any 250 consecutive TX UIs. Specified at the measurement point and measured over any 250 consecutive ULS. The test load shown in receiver compliance eye diagram of PCI Express specification. Should be used as the RX device when taking measurements.
7. Applicable to the following signals: H_CLKINN/P, PCIE_CLKINN/P, DB_DREFCLKIN[N,P]SCC, DA_DREFCLKINN/P
8. Measurement taken from differential waveform.
9. Measurement taken from single ended waveform.
10. V_{CROSS} is defined as the voltage where Clock = Clock#.



11. Only applies to the differential rising edge (that is, Clock rising and Clock# falling)
12. The total variation of all V_{CROSS} measurements in any particular system. This is a subset of V_{CROSS}MIN /V_{CROSS}max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting V_{CROSS_VAR} to be smaller than V_{CROSS} absolute.
13. The max voltage including overshoot.
14. The min voltage including undershoot.

Table 81. PLL Noise Rejection Specifications

PLL	Noise Rejection Specification	Notes
VCCAHPLL	34 dB(A) attenuation of power supply noise in 1-MHz (f1) to 66-MHz (f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 120 mV	
VCCDHPLL	peak to peak noise should be limited to < 120 mV	
VCCAPCIE	< 0 dB(A) in 0 to 1MHz, 20 dB(A) attenuation of power supply noise in 1 MHz(f1) to 1.25 GHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 40 mV	
VCCADPLLA	20 dB(A) attenuation of power supply noise in 10-kHz(f1) to 2.5-MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 100 mV	
VCCADPLLB	20 dB(A) attenuation of power supply noise in 10-kHz(f1) to 2.5-MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 100 mV	
VCCAUSBPLL	USB PLL	

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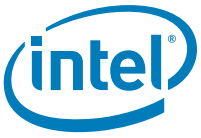


21 Ballout and Package Information

The Intel® SCH comes in an Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 1249 solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out zone, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994. The dimensions are in millimeters. Key package attributes are listed below:

Dimensions:

- Package parameters: 22 mm x 22 mm
- Ball Count: 1249
- Land metal diameter: 375 microns
- Solder resist opening: 321 microns

Tolerances:

- .X - ± 0.1
- .XX - ± 0.05
- Angles - ± 1.0 degrees

21.1 Package Diagrams

Figure 8. Package Dimensions (Top View)

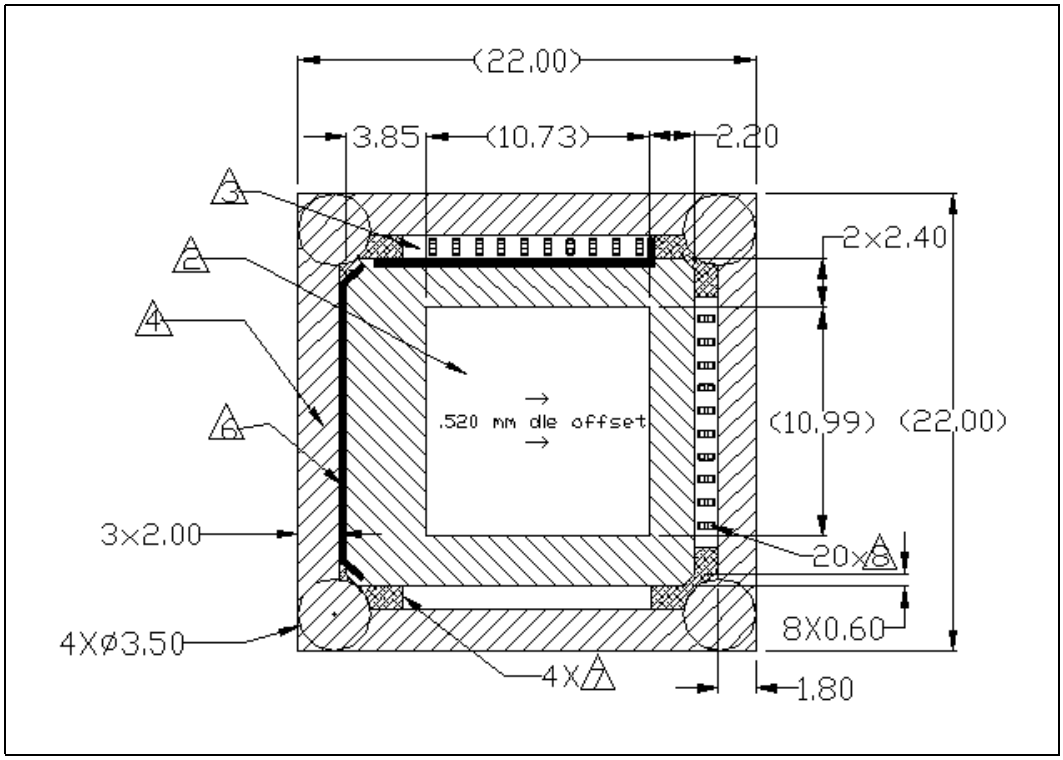


Figure 9. Package Dimensions (Bottom View)

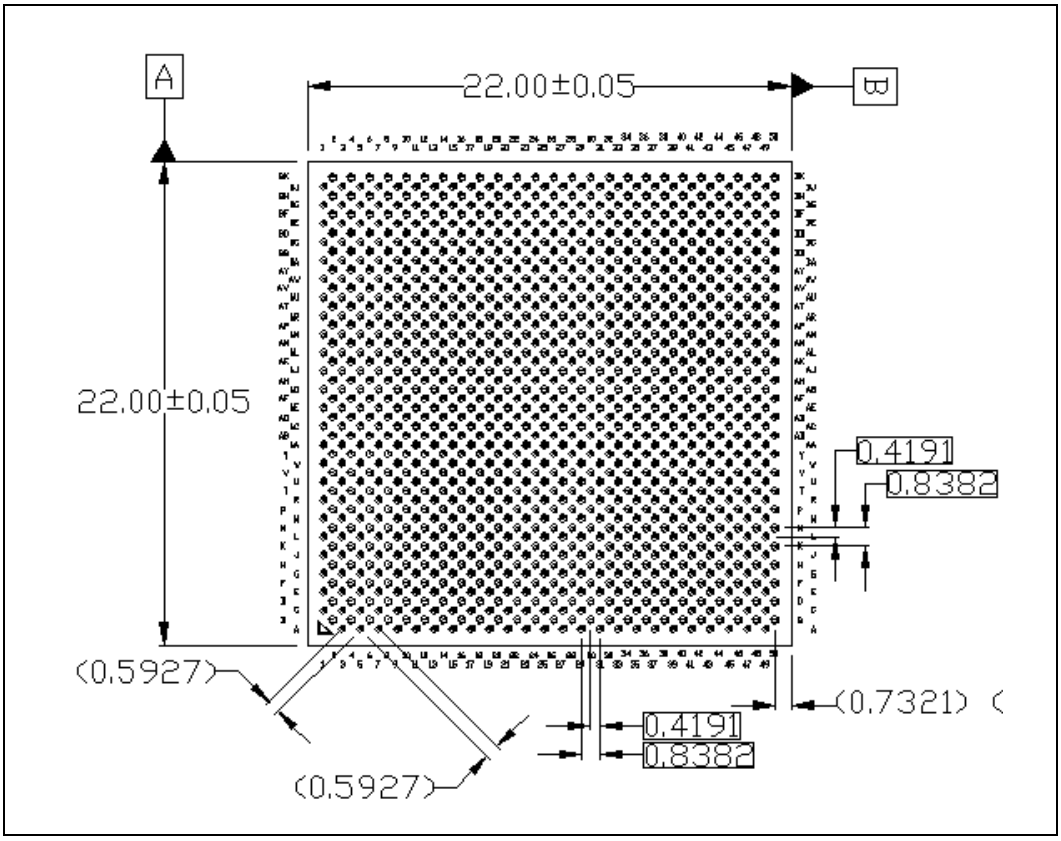
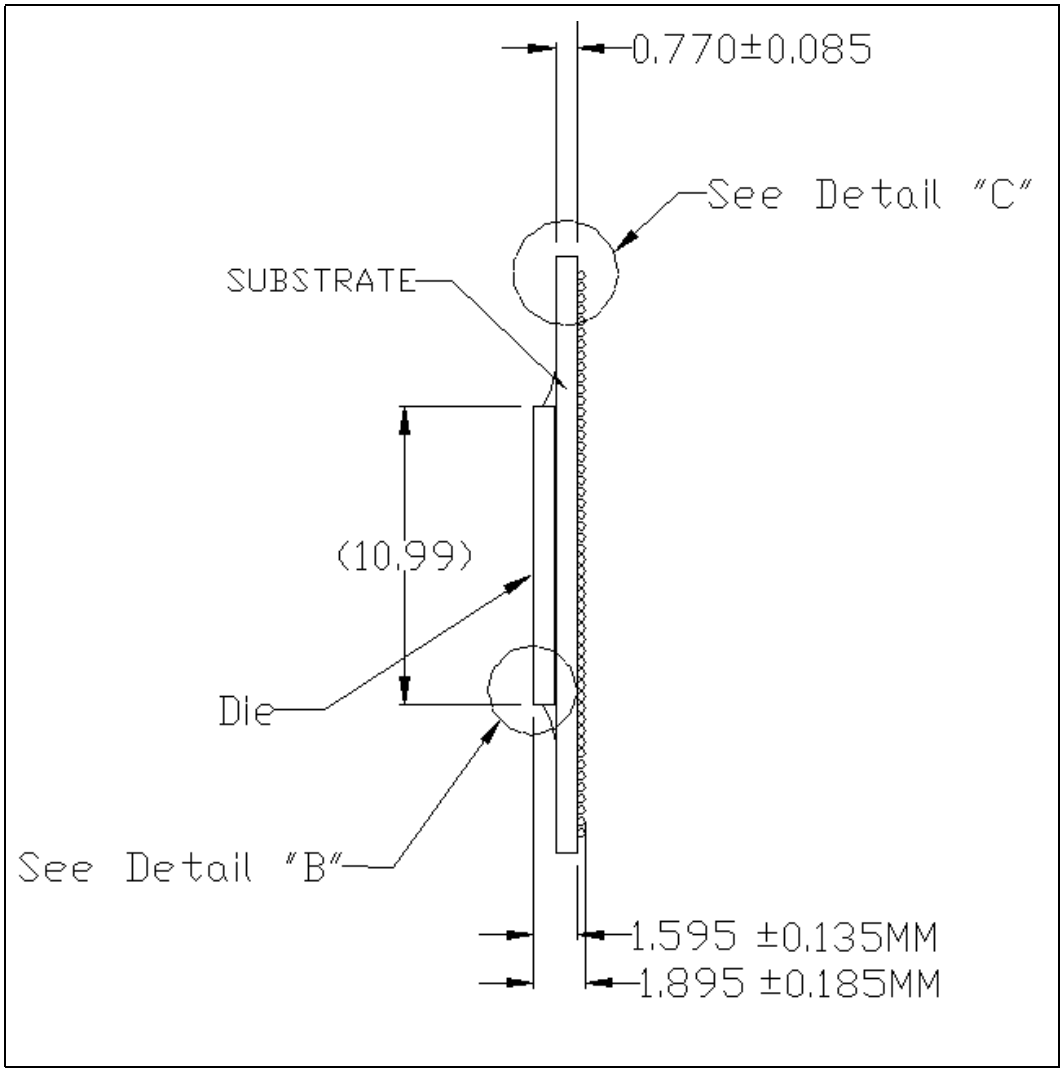


Figure 10. Package Dimensions (Side View, Unmounted)



NOTE: Maximum outgoing package coplanarity not to exceed 8 mils.

Figure 11. Package Dimensions (Solder Ball Detail “C”)

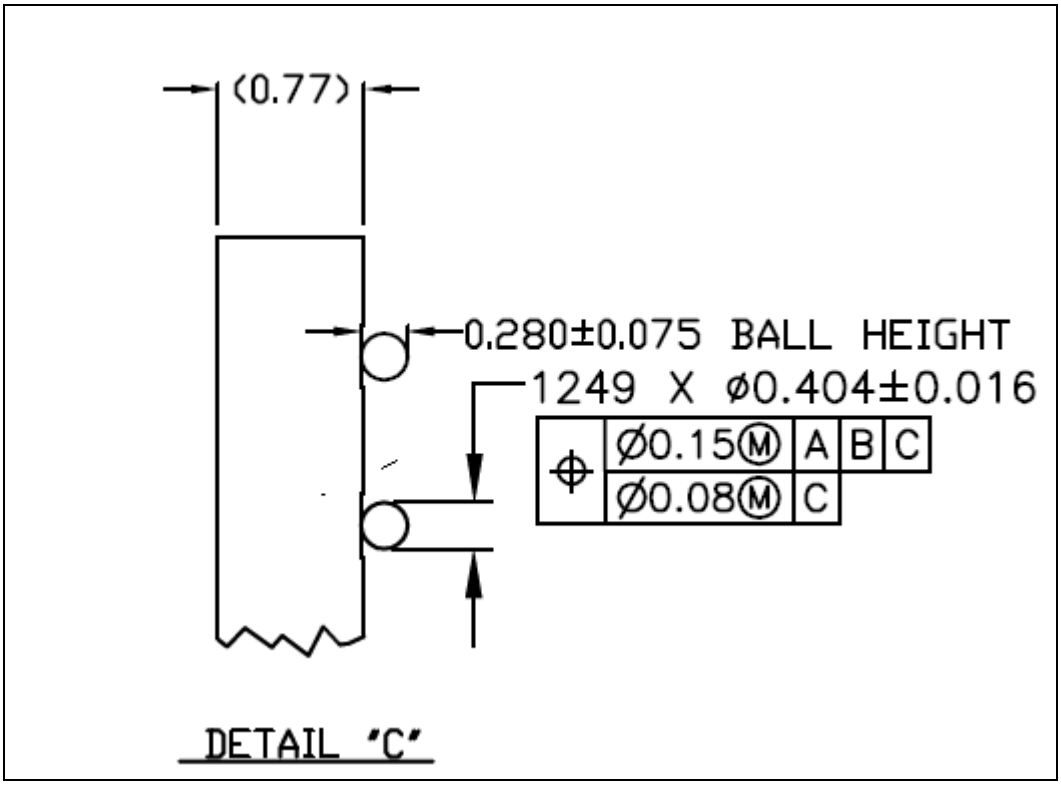


Figure 12. Package Dimensions (Underfill Detail “B”)

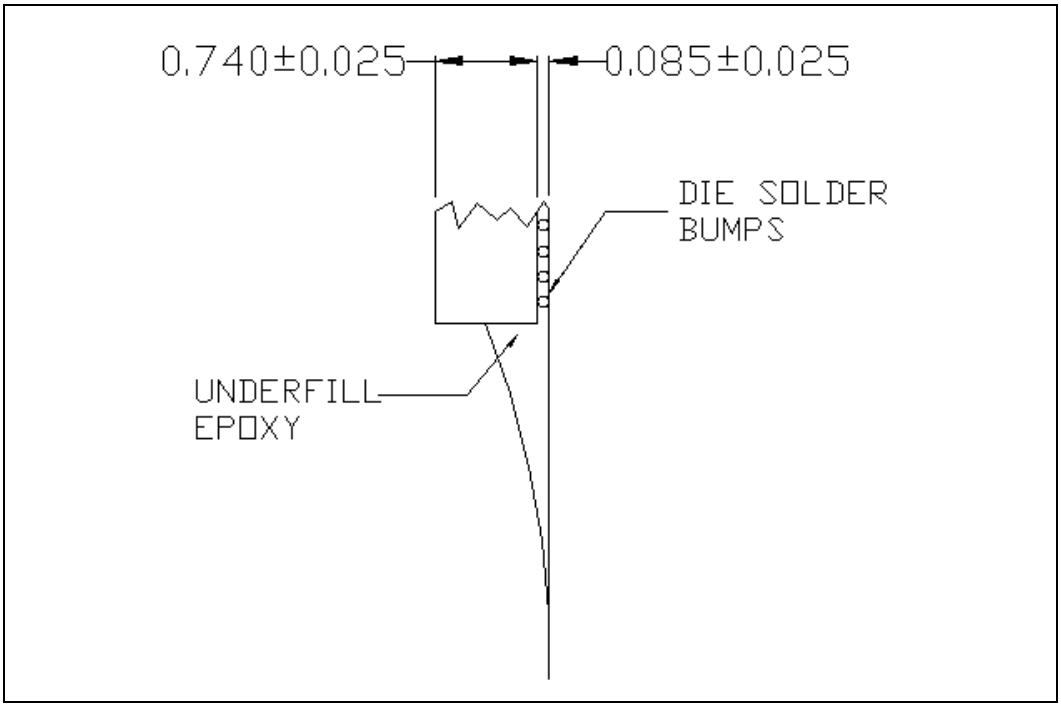
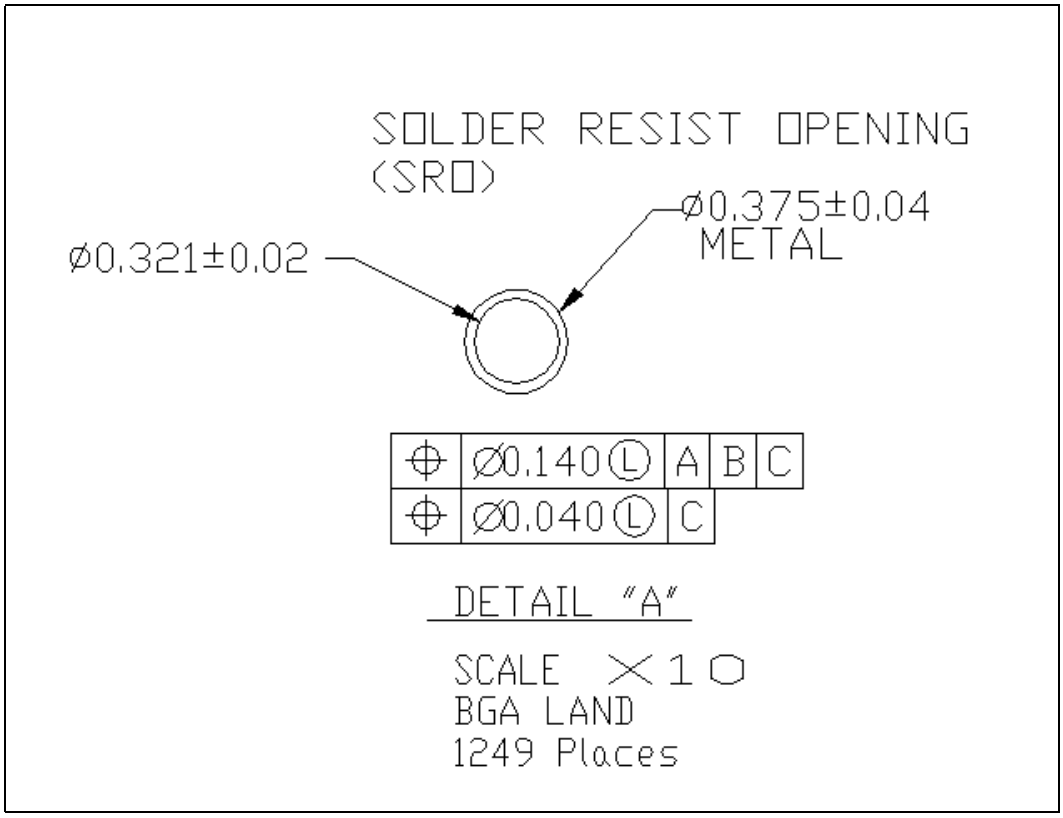
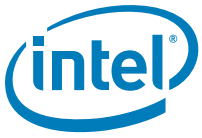


Figure 13. Package Dimensions (Solder Resist Opening)





21.2 Ballout Definition and Signal Locations

Figure 14, Figure 15, and Figure 16 provide the ballout as viewed from the top of the package. Table 82 lists the ballout alphabetically by signal name.

Figure 14. Intel® SCH Ball Map (Top View, Columns 1–17)

#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	#
A			VSS_NCTF		VSS_NCTF		H_A20#		H_A21#		H_A22#		HDA_RST#		VSS		SD0_DATA1	A
B		VSS_NCTF		H_A30#		H_A23#		H_ADSTB1#		H_A26#		H_A29#		HDA_SDI1		RESERVED19		B
C	VSS_NCTF		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	C
D		H_A12#		H_A16#		H_A27#		H_A31#		H_A28#		H_A17#		HDA_SDO		XOR_TEST		D
E	VSS_NCTF		VSS		VSS		VSS		VSS		VSS		HDA_SYNC		HDA_DOCKEN#		VSS	E
F		H_A15#		H_A7#		H_A10#		H_DPSLP#		H_A25#		H_TRDY#		HDA_SDI0		SD0_DATA3		F
G	H_A8#		VSS		VSS		VSS		VSS		H_A19#		VSS		VSS		VSS	G
H		H_A13#		H_ADSTB0#		H_A11#		H_A24#		H_DBSY#		H_A18#		HDA_DOCKRST#		SD0_DATA0		H
J	H_A14#		VSS		VSS		VSS		H_DRDY#		VCCHDA		VSS		SD0_CMD		VSS	J
K		H_REQ4#		H_A5#		H_ADS#		H_REQ2#		H_CLKINN		VCCHDA		HDA_CLK		RESERVED20		K
L	H_BREQ0#		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	L
M		H_A3#		H_A9#		H_CPURST#		H_A4#		H_CLKINP		VTT		VTT		VCC33		M
N	H_REQ1#		VSS		VSS		VSS		VSS		VSS		VTT		VCC33		VCC33	N
P		H_A6#		H_REQ0#		H_DPWR#		H_REQ3#		H_BPRI#		VTT		VSS		VSS		P
R	H_BNR#		VSS		VSS		VSS		VSS		VSS		VTT		VCC15		VCC15	R
T		H_RS1#		H_RS0#		H_HITM#		H_RS2#		H_RCOMPO		VTT		VSS		VCC		T
U	H_D8#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	U
V		H_D2#		H_D6#		H_SWING		H_D0#		H_HIT#		VTT		VSS		VCC		V
W	H_DSTBP0#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	W
Y		H_D7#		H_DSTBN0#		H_LOCK#		H_D9#		H_GVREF		VTT		VSS		VCC		Y
AA	H_D3#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AA
AB		H_D10#		H_D12#		H_SMI#		H_D15#		H_NMI		VTT		VSS		VCC		AB
AC	H_D4#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AC
AD		H_D5#		H_CGVREF		H_DEFER#		H_DINV0#		H_STPCLK#		VTT		VSS		VCC		AD
AE	H_D14#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AE
AF		H_D11#		H_D1#		H_INTR		H_D13#		H_INIT#		VTT		VSS		VCC		AF
AG	H_D21#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AG
AH		H_D17#		H_D29#		H_PBE#		H_D22#		H_CPUSLP#		VTT		VSS		VCC		AH
AJ	H_D16#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AJ
AK		H_D25#		H_D20#		H_TESTIN#		H_D23#		H_DPRSTP#		VTT		VSS		VCC		AK
AL	H_DSTBN1#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AL
AM		H_DINV1#		H_DSTBP1#		H_THRMTRIP#		H_D18#		VSS		VTT		VSS		VCC		AM
AN	H_D19#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AN
AP		H_D31#		H_D30#		H_CPUPWRGD		H_D24#		RESERVED4		VTT		VSS		VCCSM		AP
AR	H_D26#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AR
AT		H_D28#		H_D41#		H_D38#		H_D27#		RESERVED5		VTT		VSS		VCCSM		AT
AU	H_D37#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VSS	AU
AV		H_D44#		H_D32#		H_D34#		H_D39#		H_D43#		VTT		VSS		VCCSM		AV
AW	H_DSTBN2#		VSS		VSS		VSS		VSS		VSS		VTT		VSS		VCCSM	AW
AY		H_D47#		H_DSTBP2#		H_D42#		H_D35#		H_DINV2#		VSS		VSS		VSS		AY
BA	H_D36#		VSS		VSS		VSS		VSS		VCCAHPLL		SM_CAS#		SM_CS1#		SM_WE#	BA
BB		H_D46#		H_D40#		H_D33#		H_D60#		VCCDHPLL		VSS		VSS		VSS		BB
BC	H_D45#		VSS		VSS		VSS		VSS		SM_DQ63		SM_DQ62		SM_DQ57		SM_DQ54	BC
BD		H_D48#		H_D53#		H_D52#		H_D56#		H_D50#		VSS		VSS		VSS		BD
BE	H_D55#		VSS		VSS		VSS		VSS		SM_CK1		SM_RCOMPO		RESERVED2		SM_MA10	BE
BF		H_D54#		H_D57#		H_D61#		H_DSTBP3#		H_D62#		VSS		VSS		VSS		BF
BG	VSS_NCTF		VSS		VSS		VSS		VSS		SM_CK1#		SM_DQS7		SM_DQ56		SM_DQ50	BG
BH		VSS_NCTF		H_D49#		H_D63#		H_DSTBN3#		H_D58#		VSS		VSS		VSS		BH
BJ	VSS_NCTF		VSS_NCTF		VSS		VSS		VSS		VSS		SM_DQ58		SM_DQ61		SM_DQ51	BJ
BK		VSS_NCTF		VSS_NCTF		H_D59#		H_DINV3#		H_D51#		SM_DQ59		SM_DQ60		SM_DQ55		BK
#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	#

Figure 15. Intel® SCH Ball Map (Top View, Columns 18–33)

#	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	#
A		SD2_PWR#		SD1_LED		SD2_DATA3		SD2_DATA1		L_DDCCLK		SDVO_CTRLDATA		L_BKLTEN		L_BKLTCTL	A
B	SD0_CD#		SD1_WP		SD1_CD#		SD2_CMD		SD2_WP		CLKREQ#		SMI#		RESERVED1		B
C		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	C
D	SD0_CLK		SD1_PWR#		SD1_DATA3		SD2_LED		SD2_CLK		L_CTLA_CLK		L_VDDEN		EXTTS		D
E		VSS		VSS		VSS		SD2_DATA7		VSS		VSS		VSS		VSS	E
F	SD0_WP		SD1_CMD		SD1_DATA0		SD2_DATA4		SD2_DATA2		BSEL2		SDVO_CTRLCLK		THRM#		F
G		VSS		RESERVED18		VSS		VSS		VSS		GPIO0		VSS		GPIO3	G
H	SD0_LED		SD0_PWR#		SD1_CLK		SD2_DATA5		SD2_DATA6		L_DDCDATA		STPCPU#		CLK14		H
J		SD1_DATA1		VSS		SD2_DATA0		VSS		CFG0		VSS		GPIO7		VSS	J
K	SD0_DATA2		RESERVED21		SD1_DATA2		SD2_CD#		L_CTLB_DATA		GPIO9		GPIO1		SMB_ALERT#		K
L		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	L
M	VCC33		VCC33		VCC33		VCC33		VCC33		VCC33		VCC33		VCC15		M
N		VCC33		VCC33		VCC33		VCC33		VCC33		VCC33		VCC15		VCC15	N
P	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VCC15		P
R		VCC15		VCC15		VCC15		VCC15		VCC15		VCC15		VCC15		VCC15	R
T	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		T
U		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	U
V	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		V
W		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	W
Y	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC15USB		Y
AA		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AA
AB	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC15USB		AB
AC		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AC
AD	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC15USB		AD
AE		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AE
AF	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		AF
AG		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AG
AH	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		AH
AJ		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AJ
AK	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		AK
AL		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AL
AM	VCC		VCC		VCC		VCC		VCC		VCC		VCC		VCC		AM
AN		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AN
AP	VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		AP
AR		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AR
AT	VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCPCIE		AT
AU		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	AU
AV	VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		AV
AW		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM		VCCSM	AW
AY	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		AY
BA		SM_MA1		RESERVED3		SM_CS0#		SM_MA3		SM_MA2		SM_MA9		SM_MA7		SM_MA8	BA
BB	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		BB
BC		SM_DQ53		SM_DQ47		SM_MA5		SM_DQ40		SM_BS0		SM_DQ35		SM_DQ31		SM_DQ28	BC
BD	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		BD
BE		SM_MA13		SM_RAS#		SM_DQS5		SM_BS1		SM_DQ36		SM_MA4		SM_MA6		SM_MA12	BE
BF	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		BF
BG		SM_DQ52		SM_DQ46		SM_DQ41		SM_DQ38		SM_DQS4		SM_DQ33		SM_DQ25		SM_DQ26	BG
BH	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		BH
BJ		SM_DQ49		SM_DQ43		SM_DQ45		SM_DQ39		SM_MA0		SM_DQ32		SM_DQ30		SM_DQ29	BJ
BK	SM_DQS6		SM_DQ48		SM_DQ42		SM_DQ44		SM_DQ37		SM_DQ34		SM_DQ27		SM_DQS3		BK
#	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	#

Figure 16. Intel® SCH Ball Map (Top View, Columns 34–50)

#	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	#
A		LPC_AD2		PATA_DIOW#		PATA_DD7		PATA_DD9		PATA_DD10		VCC33RTC		VSS_NCTF		VSS_NCTF		A
B	CFG1		LPC_CLKOUT1		LPC_SERIRQ		PATA_DD15		PATA_DD6		PATA_DD2		PATA_DDACK#		VSS_NCTF		VSS_NCTF	B
C		VSS		VSS		VSS		VSS		VSS		VSS		PATA_DCS3#		PWROK		C
D	DPRSLPVR		LPC_CLKRUN#		LPC_CLKOUT2		PATA_DD0		PATA_DD12		PATA_DD4		PATA_IORDY		VSS		VSS_NCTF	D
E		VSS		VSS		VSS		VSS		PATA_DD14		VSS		PATA_DCS1#		RESERVED0		E
F	GPIO2		GPIO6		LPC_CLKOUT0		PATA_DD11		PATA_DD5		PATA_DIOR#		INTVRMEN		RTC_X1		RTC_X2	F
G		VSS		SMB_DATA		VSS		VSS		PATA_DD1		PATA_IDERQ		VSS		VSS		G
H	GPIO8		GPIO5		SMB_CLK		PATA_DA0		PATA_DD13		VSS		VSS		RTCRST#		RSTRDY#	H
J		SPKR		VSS		LPC_AD1		PATA_DD8		PATA_DDREQ		PATA_DA1		SUSCLK		SLPRDY#		J
K	VCC5REF		GPIO4		LPC_AD0		LPC_FRAME#		PATA_DA2		VSS		VSS		TDI		RSTWARN	K
L		VSS		VSS		LPC_AD3		PATA_DD3		RSMRST#		SLPMODE		VSS		VSS		L
M	VCC15		VCC15		VCC15		VSS		VSS		VSS		VSS		TDO		TMS	M
N		RESERVED15		RESERVED14		VSS		WAKE#		GPIOSUS1		GPIOSUS2		TCK		TRST#		N
P	VCC15		RESERVED9		RESERVED10		VSS		VSS		VSS		VSS		VSS		GPE#	P
R		VSS		VSS		VCC33SUS		GPIOSUS3		USB_OC0#		USB_OC2#		VSS		VSS		R
T	VCC		VSS		VCC33SUS		VSS		VSS		VSS		VSS		USB_DP7		USB_DN7	T
U		VSS		VCC33SUS		VSS		GPIOSUS0		USB_OC3#		USB_OC7#		USB_DN6		USB_DP6		U
V	VCC		VSS		VSS		VSS		VSS		VSS		VSS		USB_DP5		USB_DN5	V
W		VSS		RESERVED13		VCCP33USBSUS		USB_CLK48		USB_OC6#		USB_OC1#		VSS		VSS		W
Y	VCC15USB		VSS		VCCP33USBSUS		VSS		VSS		VSS		VSS		USB_DN4		USB_DP4	Y
AA		VSS		RESERVED11		VCCP33USBSUS		VCC5REFSUS		USB_OC5#		USB_OC4#		USB_DP3		USB_DN3		AA
AB	VCC15USB		RESERVED17		RESERVED12		VSS		VSS		VSS		VSS		USB_DP2		USB_DN2	AB
AC		VSS		RESERVED16		VCCAUSBPLL		VSSAUSBBGSUS		USB_RBIASP		USB_RBIASN		VSS		VSS		AC
AD	VCC15USB		VCCLVDS		VSS		VSS		VSS		VSS		VSS		USB_DN1		USB_DP1	AD
AE		VSS		VCCLVDS		VCCADPLLA		VCCAUSBBGSUS		DB_REFCLKINPSSC		DB_REFCLKINNSSC		USB_DN0		USB_DP0		AE
AF	VCC		VCCLVDS		VCCLVDS		VSS		VSS		VSS		VSS		LA_CLKP		LA_CLKN	AF
AG		VSS		VCCLVDS		VCCADPLLB		VSS		LA_DATAP3		LA_DATAN3		VSS		VSS		AG
AH	VCC		VCCSDVO		VCCSDVO		VSS		VSS		VSS		VSS		LA_DATAN2		LA_DATAP2	AH
AJ		VSS		VCCSDVO		VSS		VSS		LA_DATAN0		LA_DATAP0		VSS		VSS		AJ
AK	VCC		VCCSDVO		VCCSDVO		VSS		VSS		VSS		VSS		LA_DATAN1		LA_DATAP1	AK
AL		VSS		VCCSDVO		VSS		VSS		DA_REFCLKINP		DA_REFCLKINN		VSS		VSS		AL
AM	VCC		VCCPCIE		VSS		VSS		VSS		VSS		VSS		SDVOB_RED#		SDVOB_RED	AM
AN		VSS		VCCPCIE		VSS		VSS		SDVOB_STALL#		SDVOB_STALL		VSS		VCCAPCIEPLL		AN
AP	VCCSM		VCCPCIE		VCCPCIE		VSS		VSS		VSS		VSS		SDVOB_TVCLKIN		SDVOB_TVCLKIN#	AP
AR		VSS		VCCPCIE		VSS		VSS		SDVOB_BLUE#		SDVOB_BLUE		VSS		VSS		AR
AT	VCCPCIE		VCCPCIE		VCCPCIE		VSS		VSS		VSS		VSS		SDVOB_GREEN#		SDVOB_GREEN	AT
AU		VSS		VCCPCIE		VSS		VSS		RESERVED6		RESERVED7		SDVOB_INT		SDVOB_INT#		AU
AV	VCCSM		VCCSM		VCCPCIE		VSS		VSS		VSS		VSS		SDVOB_CLK		SDVOB_CLK#	AV
AW		VCCSM		VCCSM		VSS		VCCAPCIEBG		PCIE_PERp1		PCIE_PERn1		VSS		VSS		AW
AY	VSS		VSS		VSS		VSS		VSSAPCIEBG		VSS		VSS		PCIE_CLKINN		PCIE_CLKINP	AY
BA		SM_BS2		SM_MA14		SM_RCVENIN		RESET#		PCIE_PERn2		PCIE_PERp2		PCIE_ICOMPI		PCIE_ICOMPO		BA
BB	VSS		VSS		VSS		VSS		VSS		VSS		VSS		PCIE_PETn1		PCIE_PETp1	BB
BC		SM_DQ23		SM_DQS2		SM_DQ16		SM_DQ11		SM_DQ3		SM_DQ6		SM_DQ5		VSS		BC
BD	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		PCIE_PETp2	BD
BE		SM_MA11		SM_CKE1		SM_CKE0		SM_RCVENOUT		SM_VREF		SM_DQ2		SM_DQ4		PCIE_PETn2		BE
BF	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS_NCTF	BF
BG		SM_DQ21		SM_DQ18		SM_DQ15		SM_DQ9		SM_DQ12		SM_CK0		SM_DQ1		SM_DQ0		BG
BH	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS_NCTF	BH
BJ		SM_DQ22		SM_DQ20		SM_DQ14		SM_DQS1		SM_DQ13		SM_CK0#		SM_DQS0		VSS_NCTF		BJ
BK	SM_DQ24		SM_DQ19		SM_DQ17		SM_DQ10		SM_DQ8		SM_DQ7		VSS_NCTF		VSS_NCTF		RESERVED8 (NCTF)	BK
#	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	#

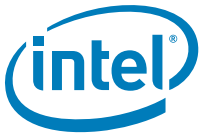


Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
BSEL2	F28
CFG0	J27
CFG1	B34
CLK14	H32
CLKREQ#	B28
DA_REFCLKINN	AL45
DA_REFCLKINP	AL43
DB_REFCLKINNSSC	AE45
DB_REFCLKINPSSC	AE43
DPRSLPVR	D34
EXTTS	D32
GPE#	P50
GPIO0	G29
GPIO1	K30
GPIO2	F34
GPIO3	G33
GPIO4	K36
GPIO5	H36
GPIO6	F36
GPIO7	J31
GPIO8	H34
GPIO9	K28
GPIOSUS0	U41
GPIOSUS1	N43
GPIOSUS2	N45
GPIOSUS3	R41
H_A3#	M2
H_A4#	M8
H_A5#	K4
H_A6#	P2
H_A7#	F4
H_A8#	G1
H_A9#	M4
H_A10#	F6
H_A11#	H6
H_A12#	D2

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
H_A13#	H2
H_A14#	J1
H_A15#	F2
H_A16#	D4
H_A17#	D12
H_A18#	H12
H_A19#	G11
H_A20#	A7
H_A21#	A9
H_A22#	A11
H_A23#	B6
H_A24#	H8
H_A25#	F10
H_A26#	B10
H_A27#	D6
H_A28#	D10
H_A29#	B12
H_A30#	B4
H_A31#	D8
H_ADS#	K6
H_ADSTB0#	H4
H_ADSTB1#	B8
H_BNR#	R1
H_BPRI#	P10
H_BREQ0#	L1
H_CGVREF	AD4
H_CLKINN	K10
H_CLKINP	M10
H_CPUPWRGD	AP6
H_CPURST#	M6
H_CPUSLP#	AH10
H_D0#	V8
H_D1#	AF4
H_D2#	V2
H_D3#	AA1
H_D4#	AC1

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
H_D5#	AD2
H_D6#	V4
H_D7#	Y2
H_D8#	U1
H_D9#	Y8
H_D10#	AB2
H_D11#	AF2
H_D12#	AB4
H_D13#	AF8
H_D14#	AE1
H_D15#	AB8
H_D16#	AJ1
H_D17#	AH2
H_D18#	AM8
H_D19#	AN1
H_D20#	AK4
H_D21#	AG1
H_D22#	AH8
H_D23#	AK8
H_D24#	AP8
H_D25#	AK2
H_D26#	AR1
H_D27#	AT8
H_D28#	AT2
H_D29#	AH4
H_D30#	AP4
H_D31#	AP2
H_D32#	AV4
H_D33#	BB6
H_D34#	AV6
H_D35#	AY8
H_D36#	BA1
H_D37#	AU1
H_D38#	AT6
H_D39#	AV8
H_D40#	BB4

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
H_D41#	AT4
H_D42#	AY6
H_D43#	AV10
H_D44#	AV2
H_D45#	BC1
H_D46#	BB2
H_D47#	AY2
H_D48#	BD2
H_D49#	BH4
H_D50#	BD10
H_D51#	BK10
H_D52#	BD6
H_D53#	BD4
H_D54#	BF2
H_D55#	BE1
H_D56#	BD8
H_D57#	BF4
H_D58#	BH10
H_D59#	BK6
H_D60#	BB8
H_D61#	BF6
H_D62#	BF10
H_D63#	BH6
H_DBSY#	H10
H_DEFER#	AD6
H_DINV0#	AD8
H_DINV1#	AM2
H_DINV2#	AY10
H_DINV3#	BK8
H_DPRSTP#	AK10
H_DPSLP#	F8
H_DPWR#	P6
H_DRDY#	J9
H_DSTBN0#	Y4
H_DSTBN1#	AL1
H_DSTBN2#	AW1

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
H_DSTBN3#	BH8
H_DSTBP0#	W1
H_DSTBP1#	AM4
H_DSTBP2#	AY4
H_DSTBP3#	BF8
H_GVREF	Y10
H_HIT#	V10
H_HITM#	T6
H_INIT#	AF10
H_INTR	AF6
H_LOCK#	Y6
H_NMI	AB10
H_PBE#	AH6
H_RCOMPO	T10
H_REQ0#	P4
H_REQ1#	N1
H_REQ2#	K8
H_REQ3#	P8
H_REQ4#	K2
H_RS0#	T4
H_RS1#	T2
H_RS2#	T8
H_SMI#	AB6
H_STPCLK#	AD10
H_SWING	V6
H_TESTIN#	AK6
H_THRMTRIP#	AM6
H_TRDY#	F12
HDA_CLK	K14
HDA_DOCKEN#	E15
HDA_DOCKRST#	H14
HDA_RST#	A13
HDA_SDI0	F14
HDA_SDI1	B14
HDA_SDO	D14
HDA_SYNC	E13

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
INTVRMEN	F46
L_BKLTCTL	A33
L_BKLTEN	A31
L_CTLA_CLK	D28
L_CTLB_DATA	K26
L_DDCCLK	A27
L_DDCDATA	H28
L_VDDEN	D30
LA_CLKN	AF50
LA_CLKP	AF48
LA_DATAN0	AJ43
LA_DATAN1	AK48
LA_DATAN2	AH48
LA_DATAN3	AG45
LA_DATAP0	AJ45
LA_DATAP1	AK50
LA_DATAP2	AH50
LA_DATAP3	AG43
LPC_AD0	K38
LPC_AD1	J39
LPC_AD2	A35
LPC_AD3	L39
LPC_CLKOUT0	F38
LPC_CLKOUT1	B36
LPC_CLKOUT2	D38
LPC_CLKRUN#	D36
LPC_FRAME#	K40
LPC_SERIRQ	B38
PATA_DA0	H40
PATA_DA1	J45
PATA_DA2	K42
PATA_DCS1#	E47
PATA_DCS3#	C47
PATA_DD0	D40
PATA_DD1	G43
PATA_DD2	B44

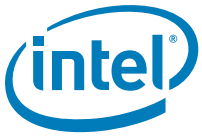


Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
PATA_DD3	L41
PATA_DD4	D44
PATA_DD5	F42
PATA_DD6	B42
PATA_DD7	A39
PATA_DD8	J41
PATA_DD9	A41
PATA_DD10	A43
PATA_DD11	F40
PATA_DD12	D42
PATA_DD13	H42
PATA_DD14	E43
PATA_DD15	B40
PATA_DDACK#	B46
PATA_DDREQ	J43
PATA_DIOR#	F44
PATA_DIOW#	A37
PATA_IDEIRQ	G45
PATA_IORDY	D46
PCIE_CLKINN	AY48
PCIE_CLKINP	AY50
PCIE_ICOMPI	BA47
PCIE_ICOMPO	BA49
PCIE_PERn1	AW45
PCIE_PERn2	BA43
PCIE_PERp1	AW43
PCIE_PERp2	BA45
PCIE_PETn1	BB48
PCIE_PETn2	BE49
PCIE_PETp1	BB50
PCIE_PETp2	BD50
PWROK	C49
RESERVED0	E49
RESERVED1	B32
RESERVED10	P38
RESERVED11	AA37

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
RESERVED12	AB38
RESERVED13	W37
RESERVED14	N37
RESERVED15	N35
RESERVED16	AC37
RESERVED17	AB36
RESERVED18	G21
RESERVED2	BE15
RESERVED3	BA21
RESERVED4	AP10
RESERVED5	AT10
RESERVED6	AU43
RESERVED7	AU45
RESERVED9	P36
RESET#	BA41
RSMRST#	L43
RSTRDY#	H50
RSTWARN	K50
RTC_X1	F48
RTC_X2	F50
RTCRST#	H48
SD0_CD#	B18
SD0_CLK	D18
SD0_CMD	J15
SD0_DATA0	H16
SD0_DATA1	A17
SD0_DATA2	K18
SD0_DATA3	F16
RESERVED20	K16
RESERVED19	B16
XOR_TEST	D16
RESERVED21	K20
SD0_LED	H18
SD0_PWR#	H20
SD0_WP	F18
SD1_CD#	B22

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
SD1_CLK	H22
SD1_CMD	F20
SD1_DATA0	F22
SD1_DATA1	J19
SD1_DATA2	K22
SD1_DATA3	D22
SD1_LED	A21
SD1_PWR#	D20
SD1_WP	B20
SD2_CD#	K24
SD2_CLK	D26
SD2_CMD	B24
SD2_DATA0	J23
SD2_DATA1	A25
SD2_DATA2	F26
SD2_DATA3	A23
SD2_DATA4	F24
SD2_DATA5	H24
SD2_DATA6	H26
SD2_DATA7	E25
SD2_LED	D24
SD2_PWR#	A19
SD2_WP	B26
SDVO_CTRLCLK	F30
SDVO_CTRLDATA	A29
SDVOB_BLUE	AR45
SDVOB_BLUE#	AR43
SDVOB_CLK	AV48
SDVOB_CLK#	AV50
SDVOB_GREEN	AT50
SDVOB_GREEN#	AT48
SDVOB_INT	AU47
SDVOB_INT#	AU49
SDVOB_RED	AM50
SDVOB_RED#	AM48
SDVOB_STALL	AN45

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
SDVOB_STALL#	AN43
SDVOB_TVCLKIN	AP48
SDVOB_TVCLKIN#	AP50
SLPMODE	L45
SLPRDY#	J49
SM_BS0	BC27
SM_BS1	BE25
SM_BS2	BA35
SM_CAS#	BA13
SM_CK0	BG45
SM_CK0#	BJ45
SM_CK1	BE11
SM_CK1#	BG11
SM_CKE0	BE39
SM_CKE1	BE37
SM_CS0#	BA23
SM_CS1#	BA15
SM_DQ0	BG49
SM_DQ1	BG47
SM_DQ2	BE45
SM_DQ3	BC43
SM_DQ4	BE47
SM_DQ5	BC47
SM_DQ6	BC45
SM_DQ7	BK44
SM_DQ8	BK42
SM_DQ9	BG41
SM_DQ10	BK40
SM_DQ11	BC41
SM_DQ12	BG43
SM_DQ13	BJ43
SM_DQ14	BJ39
SM_DQ15	BG39
SM_DQ16	BC39
SM_DQ17	BK38
SM_DQ18	BG37

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
SM_DQ19	BK36
SM_DQ20	BJ37
SM_DQ21	BG35
SM_DQ22	BJ35
SM_DQ23	BC35
SM_DQ24	BK34
SM_DQ25	BG31
SM_DQ26	BG33
SM_DQ27	BK30
SM_DQ28	BC33
SM_DQ29	BJ33
SM_DQ30	BJ31
SM_DQ31	BC31
SM_DQ32	BJ29
SM_DQ33	BG29
SM_DQ34	BK28
SM_DQ35	BC29
SM_DQ36	BE27
SM_DQ37	BK26
SM_DQ38	BG25
SM_DQ39	BJ25
SM_DQ40	BC25
SM_DQ41	BG23
SM_DQ42	BK22
SM_DQ43	BJ21
SM_DQ44	BK24
SM_DQ45	BJ23
SM_DQ46	BG21
SM_DQ47	BC21
SM_DQ48	BK20
SM_DQ49	BJ19
SM_DQ50	BG17
SM_DQ51	BJ17
SM_DQ52	BG19
SM_DQ53	BC19
SM_DQ54	BC17

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
SM_DQ55	BK16
SM_DQ56	BG15
SM_DQ57	BC15
SM_DQ58	BJ13
SM_DQ59	BK12
SM_DQ60	BK14
SM_DQ61	BJ15
SM_DQ62	BC13
SM_DQ63	BC11
SM_DQS0	BJ47
SM_DQS1	BJ41
SM_DQS2	BC37
SM_DQS3	BK32
SM_DQS4	BG27
SM_DQS5	BE23
SM_DQS6	BK18
SM_DQS7	BG13
SM_MA0	BJ27
SM_MA1	BA19
SM_MA2	BA27
SM_MA3	BA25
SM_MA4	BE29
SM_MA5	BC23
SM_MA6	BE31
SM_MA7	BA31
SM_MA8	BA33
SM_MA9	BA29
SM_MA10	BE17
SM_MA11	BE35
SM_MA12	BE33
SM_MA13	BE19
SM_MA14	BA37
SM_RAS#	BE21
SM_RCOMPO	BE13
SM_RCVENIN#	BA39
SM_RCVENOUT#	BE41

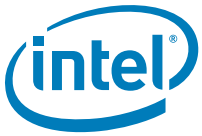


Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
SM_VREF	BE43
SM_WE#	BA17
SMB_ALERT#	K32
SMB_CLK	H38
SMB_DATA	G37
SMI#	B30
SPKR	J35
STPCPU#	H30
SUSCLK	J47
TCK	N47
TDI	K48
TDO	M48
THRM#	F32
TMS	M50
TRST#	N49
USB_CLK48	W41
USB_DN0	AE47
USB_DN1	AD48
USB_DN2	AB50
USB_DN3	AA49
USB_DN4	Y48
USB_DN5	V50
USB_DN6	U47
USB_DN7	T50
USB_DP0	AE49
USB_DP1	AD50
USB_DP2	AB48
USB_DP3	AA47
USB_DP4	Y50
USB_DP5	V48
USB_DP6	U49
USB_DP7	T48
USB_OC0#	R43
USB_OC1#	W45
USB_OC2#	R45
USB_OC3#	U43

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
USB_OC4#	AA45
USB_OC5#	AA43
USB_OC6#	W43
USB_OC7#	U45
USB_RBIASN	AC45
USB_RBIASP	AC43
VCC	AB16
VCC	AD16
VCC	AF16
VCC	AH16
VCC	AK16
VCC	AM16
VCC	T16
VCC	V16
VCC	Y16
VCC	AB18
VCC	AD18
VCC	AF18
VCC	AH18
VCC	AK18
VCC	AM18
VCC	T18
VCC	V18
VCC	Y18
VCC	AB20
VCC	AD20
VCC	AF20
VCC	AH20
VCC	AK20
VCC	AM20
VCC	T20
VCC	V20
VCC	Y20
VCC	AB22
VCC	AD22
VCC	AF22

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VCC	AH22
VCC	AK22
VCC	AM22
VCC	T22
VCC	V22
VCC	Y22
VCC	AB24
VCC	AD24
VCC	AF24
VCC	AH24
VCC	AK24
VCC	AM24
VCC	T24
VCC	V24
VCC	Y24
VCC	AB26
VCC	AD26
VCC	AF26
VCC	AH26
VCC	AK26
VCC	AM26
VCC	T26
VCC	V26
VCC	Y26
VCC	AB28
VCC	AD28
VCC	AF28
VCC	AH28
VCC	AK28
VCC	AM28
VCC	T28
VCC	V28
VCC	Y28
VCC	AB30
VCC	AD30
VCC	AF30

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VCC	AH30
VCC	AK30
VCC	AM30
VCC	T30
VCC	V30
VCC	Y30
VCC	AF32
VCC	AH32
VCC	AK32
VCC	AM32
VCC	T32
VCC	V32
VCC	AF34
VCC	AH34
VCC	AK34
VCC	AM34
VCC	T34
VCC	V34
VCC15	R15
VCC15	R17
VCC15	R19
VCC15	R21
VCC15	R23
VCC15	R25
VCC15	R27
VCC15	R29
VCC15	N31
VCC15	R31
VCC15	M32
VCC15	P32
VCC15	N33
VCC15	R33
VCC15	M34
VCC15	P34
VCC15	M36
VCC15	M38

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VCC15USB	AB32
VCC15USB	AD32
VCC15USB	Y32
VCC15USB	AB34
VCC15USB	AD34
VCC15USB	Y34
VCC33	N15
VCC33	M16
VCC33	N17
VCC33	M18
VCC33	N19
VCC33	M20
VCC33	N21
VCC33	M22
VCC33	N23
VCC33	M24
VCC33	N25
VCC33	M26
VCC33	N27
VCC33	M28
VCC33	N29
VCC33	M30
VCC33RTC	A45
VCC33SUS	U37
VCC33SUS	T38
VCC33SUS	R39
VCC5REF	K34
VCC5REFSUS	AA41
VCCADPLLA	AE39
VCCADPLLB	AG39
VCCAHPLL	BA11
VCCAPCIEBG	AW41
VCCAPCIEPLL	AN49
VCCAUSBBGSUS	AE41
VCCAUSBPLL	AC39
VCCDHPLL	BB10

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VCCHDA	J11
VCCHDA	K12
VCCLVDS	AD36
VCCLVDS	AF36
VCCLVDS	AE37
VCCLVDS	AG37
VCCLVDS	AF38
VCCP33USBSUS	Y38
VCCP33USBSUS	AA39
VCCP33USBSUS	W39
VCCPCIE	AT32
VCCPCIE	AT34
VCCPCIE	AM36
VCCPCIE	AP36
VCCPCIE	AT36
VCCPCIE	AN37
VCCPCIE	AR37
VCCPCIE	AU37
VCCPCIE	AP38
VCCPCIE	AT38
VCCPCIE	AV38
VCCSDVO	AH36
VCCSDVO	AK36
VCCSDVO	AJ37
VCCSDVO	AL37
VCCSDVO	AH38
VCCSDVO	AK38
VCCSM	AP16
VCCSM	AT16
VCCSM	AV16
VCCSM	AW17
VCCSM	AP18
VCCSM	AT18
VCCSM	AV18
VCCSM	AW19
VCCSM	AP20

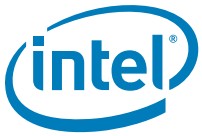


Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VCCSM	AT20
VCCSM	AV20
VCCSM	AW21
VCCSM	AP22
VCCSM	AT22
VCCSM	AV22
VCCSM	AW23
VCCSM	AP24
VCCSM	AT24
VCCSM	AV24
VCCSM	AW25
VCCSM	AP26
VCCSM	AT26
VCCSM	AV26
VCCSM	AW27
VCCSM	AP28
VCCSM	AT28
VCCSM	AV28
VCCSM	AW29
VCCSM	AP30
VCCSM	AT30
VCCSM	AV30
VCCSM	AW31
VCCSM	AP32
VCCSM	AV32
VCCSM	AW33
VCCSM	AP34
VCCSM	AV34
VCCSM	AW35
VCCSM	AV36
VCCSM	AW37
VSS	AA3
VSS	AC3
VSS	AE3
VSS	AG3
VSS	AJ3

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AL3
VSS	AN3
VSS	AR3
VSS	AU3
VSS	AW3
VSS	BA3
VSS	BC3
VSS	BE3
VSS	BG3
VSS	C3
VSS	E3
VSS	G3
VSS	J3
VSS	L3
VSS	N3
VSS	R3
VSS	U3
VSS	W3
VSS	AA5
VSS	AC5
VSS	AE5
VSS	AG5
VSS	AJ5
VSS	AL5
VSS	AN5
VSS	AR5
VSS	AU5
VSS	AW5
VSS	BA5
VSS	BC5
VSS	BE5
VSS	BG5
VSS	BJ5
VSS	C5
VSS	E5
VSS	G5

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	J5
VSS	L5
VSS	N5
VSS	R5
VSS	U5
VSS	W5
VSS	AA7
VSS	AC7
VSS	AE7
VSS	AG7
VSS	AJ7
VSS	AL7
VSS	AN7
VSS	AR7
VSS	AU7
VSS	AW7
VSS	BA7
VSS	BC7
VSS	BE7
VSS	BG7
VSS	BJ7
VSS	C7
VSS	E7
VSS	G7
VSS	J7
VSS	L7
VSS	N7
VSS	R7
VSS	U7
VSS	W7
VSS	AA9
VSS	AC9
VSS	AE9
VSS	AG9
VSS	AJ9
VSS	AL9

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AN9
VSS	AR9
VSS	AU9
VSS	AW9
VSS	BA9
VSS	BC9
VSS	BE9
VSS	BG9
VSS	BJ9
VSS	C9
VSS	E9
VSS	G9
VSS	L9
VSS	N9
VSS	R9
VSS	U9
VSS	W9
VSS	AM10
VSS	AA11
VSS	AC11
VSS	AE11
VSS	AG11
VSS	AJ11
VSS	AL11
VSS	AN11
VSS	AR11
VSS	AU11
VSS	AW11
VSS	BJ11
VSS	C11
VSS	E11
VSS	L11
VSS	N11
VSS	R11
VSS	U11
VSS	W11

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AY12
VSS	BB12
VSS	BD12
VSS	BF12
VSS	BH12
VSS	C13
VSS	G13
VSS	J13
VSS	L13
VSS	AB14
VSS	AD14
VSS	AF14
VSS	AH14
VSS	AK14
VSS	AM14
VSS	AP14
VSS	AT14
VSS	AV14
VSS	AY14
VSS	BB14
VSS	BD14
VSS	BF14
VSS	BH14
VSS	P14
VSS	T14
VSS	V14
VSS	Y14
VSS	A15
VSS	AA15
VSS	AC15
VSS	AE15
VSS	AG15
VSS	AJ15
VSS	AL15
VSS	AN15
VSS	AR15

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AU15
VSS	AW15
VSS	C15
VSS	G15
VSS	L15
VSS	U15
VSS	W15
VSS	AY16
VSS	BB16
VSS	BD16
VSS	BF16
VSS	BH16
VSS	P16
VSS	AA17
VSS	AC17
VSS	AE17
VSS	AG17
VSS	AJ17
VSS	AL17
VSS	AN17
VSS	AR17
VSS	AU17
VSS	C17
VSS	E17
VSS	G17
VSS	J17
VSS	L17
VSS	U17
VSS	W17
VSS	AY18
VSS	BB18
VSS	BD18
VSS	BF18
VSS	BH18
VSS	P18
VSS	AA19

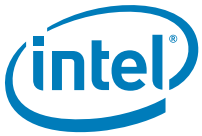


Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AC19
VSS	AE19
VSS	AG19
VSS	AJ19
VSS	AL19
VSS	AN19
VSS	AR19
VSS	AU19
VSS	C19
VSS	E19
VSS	G19
VSS	L19
VSS	U19
VSS	W19
VSS	AY20
VSS	BB20
VSS	BD20
VSS	BF20
VSS	BH20
VSS	P20
VSS	AA21
VSS	AC21
VSS	AE21
VSS	AG21
VSS	AJ21
VSS	AL21
VSS	AN21
VSS	AR21
VSS	AU21
VSS	C21
VSS	E21
VSS	J21
VSS	L21
VSS	U21
VSS	W21
VSS	AY22

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	BB22
VSS	BD22
VSS	BF22
VSS	BH22
VSS	P22
VSS	AA23
VSS	AC23
VSS	AE23
VSS	AG23
VSS	AJ23
VSS	AL23
VSS	AN23
VSS	AR23
VSS	AU23
VSS	C23
VSS	E23
VSS	G23
VSS	L23
VSS	U23
VSS	W23
VSS	AY24
VSS	BB24
VSS	BD24
VSS	BF24
VSS	BH24
VSS	P24
VSS	AA25
VSS	AC25
VSS	AE25
VSS	AG25
VSS	AJ25
VSS	AL25
VSS	AN25
VSS	AR25
VSS	AU25
VSS	C25

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	G25
VSS	J25
VSS	L25
VSS	U25
VSS	W25
VSS	AY26
VSS	BB26
VSS	BD26
VSS	BF26
VSS	BH26
VSS	P26
VSS	AA27
VSS	AC27
VSS	AE27
VSS	AG27
VSS	AJ27
VSS	AL27
VSS	AN27
VSS	AR27
VSS	AU27
VSS	C27
VSS	E27
VSS	G27
VSS	L27
VSS	U27
VSS	W27
VSS	AY28
VSS	BB28
VSS	BD28
VSS	BF28
VSS	BH28
VSS	P28
VSS	AA29
VSS	AC29
VSS	AE29
VSS	AG29

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AJ29
VSS	AL29
VSS	AN29
VSS	AR29
VSS	AU29
VSS	C29
VSS	E29
VSS	J29
VSS	L29
VSS	U29
VSS	W29
VSS	AY30
VSS	BB30
VSS	BD30
VSS	BF30
VSS	BH30
VSS	P30
VSS	AA31
VSS	AC31
VSS	AE31
VSS	AG31
VSS	AJ31
VSS	AL31
VSS	AN31
VSS	AR31
VSS	AU31
VSS	C31
VSS	E31
VSS	G31
VSS	L31
VSS	U31
VSS	W31
VSS	AY32
VSS	BB32
VSS	BD32
VSS	BF32

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	BH32
VSS	AA33
VSS	AC33
VSS	AE33
VSS	AG33
VSS	AJ33
VSS	AL33
VSS	AN33
VSS	AR33
VSS	AU33
VSS	C33
VSS	E33
VSS	J33
VSS	L33
VSS	U33
VSS	W33
VSS	AY34
VSS	BB34
VSS	BD34
VSS	BF34
VSS	BH34
VSS	AA35
VSS	AC35
VSS	AE35
VSS	AG35
VSS	AJ35
VSS	AL35
VSS	AN35
VSS	AR35
VSS	AU35
VSS	C35
VSS	E35
VSS	G35
VSS	L35
VSS	R35
VSS	U35

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	W35
VSS	AY36
VSS	BB36
VSS	BD36
VSS	BF36
VSS	BH36
VSS	T36
VSS	V36
VSS	Y36
VSS	C37
VSS	E37
VSS	J37
VSS	L37
VSS	R37
VSS	AD38
VSS	AM38
VSS	AY38
VSS	BB38
VSS	BD38
VSS	BF38
VSS	BH38
VSS	V38
VSS	AJ39
VSS	AL39
VSS	AN39
VSS	AR39
VSS	AU39
VSS	AW39
VSS	C39
VSS	E39
VSS	G39
VSS	N39
VSS	U39
VSS	AB40
VSS	AD40
VSS	AF40

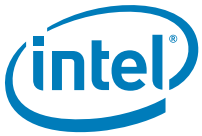


Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AH40
VSS	AK40
VSS	AM40
VSS	AP40
VSS	AT40
VSS	AV40
VSS	AY40
VSS	BB40
VSS	BD40
VSS	BF40
VSS	BH40
VSS	M40
VSS	P40
VSS	T40
VSS	V40
VSS	Y40
VSS	AG41
VSS	AJ41
VSS	AL41
VSS	AN41
VSS	AR41
VSS	AU41
VSS	C41
VSS	E41
VSS	G41
VSS	AB42
VSS	AD42
VSS	AF42
VSS	AH42
VSS	AK42
VSS	AM42
VSS	AP42
VSS	AT42
VSS	AV42
VSS	BB42
VSS	BD42

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	BF42
VSS	BH42
VSS	M42
VSS	P42
VSS	T42
VSS	V42
VSS	Y42
VSS	C43
VSS	AB44
VSS	AD44
VSS	AF44
VSS	AH44
VSS	AK44
VSS	AM44
VSS	AP44
VSS	AT44
VSS	AV44
VSS	AY44
VSS	BB44
VSS	BD44
VSS	BF44
VSS	BH44
VSS	H44
VSS	K44
VSS	M44
VSS	P44
VSS	T44
VSS	V44
VSS	Y44
VSS	C45
VSS	E45
VSS	AB46
VSS	AD46
VSS	AF46
VSS	AH46
VSS	AK46

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AM46
VSS	AP46
VSS	AT46
VSS	AV46
VSS	AY46
VSS	BB46
VSS	BD46
VSS	BF46
VSS	BH46
VSS	H46
VSS	K46
VSS	M46
VSS	P46
VSS	T46
VSS	V46
VSS	Y46
VSS	AC47
VSS	AG47
VSS	AJ47
VSS	AL47
VSS	AN47
VSS	AR47
VSS	AW47
VSS	G47
VSS	L47
VSS	R47
VSS	W47
VSS	BD48
VSS	BF48
VSS	BH48
VSS	D48
VSS	P48
VSS	AC49
VSS	AG49
VSS	AJ49
VSS	AL49

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VSS	AR49
VSS	AW49
VSS	BC49
VSS	G49
VSS	L49
VSS	R49
VSS	W49
VSS_NCTF	A3
VSS_NCTF	A5
VSS_NCTF	A47
VSS_NCTF	A49
VSS_NCTF	B2
VSS_NCTF	B48
VSS_NCTF	B50
VSS_NCTF	BF50
VSS_NCTF	BG1
VSS_NCTF	BH2
VSS_NCTF	BH50
VSS_NCTF	BJ1
VSS_NCTF	BJ3
VSS_NCTF	BJ49
VSS_NCTF	BK2
VSS_NCTF	BK4
VSS_NCTF	BK46
VSS_NCTF	BK48
VSS_NCTF	BK50
VSS_NCTF	C1
VSS_NCTF	D50
VSS_NCTF	E1
VSSAPCIEBG	AY42
VSSAUSBBGSUS	AC41
VTT	AB12
VTT	AD12
VTT	AF12
VTT	AH12
VTT	AK12

Table 82. Intel® SCH Pin List Arranged by Signal Name

Pin Name	Ball#
VTT	AM12
VTT	AP12
VTT	AT12
VTT	AV12
VTT	M12
VTT	P12
VTT	T12
VTT	V12
VTT	Y12
VTT	AA13
VTT	AC13
VTT	AE13
VTT	AG13
VTT	AJ13
VTT	AL13
VTT	AN13
VTT	AR13
VTT	AU13
VTT	AW13
VTT	N13
VTT	R13
VTT	U13
VTT	W13
VTT	M14
WAKE#	N41

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