

DRC3123J

Silicon NPN epitaxial planar type

For digital circuits

Complementary to DRA3123J

■ Features

- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

■ Packaging

Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

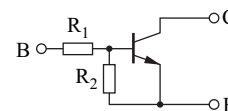
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	50	V
Collector-emitter voltage (Base open)	V_{CEO}	50	V
Collector current	I_{C}	100	mA
Total power dissipation	P_{T}	100	mW
Junction temperature	T_{J}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

■ Package

- Code
SSSMINI3-F2-B
- Pin Name
1: Base
2: Emitter
3: Collector

■ Marking Symbol: N4

■ Internal Connection

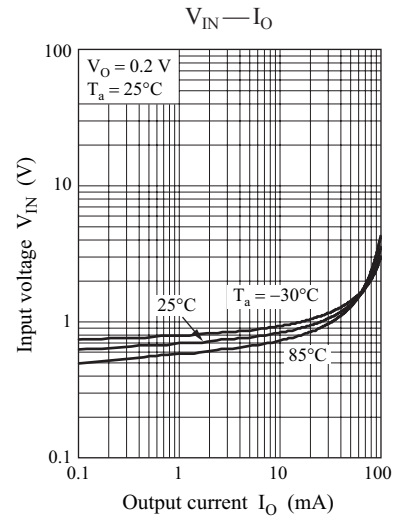
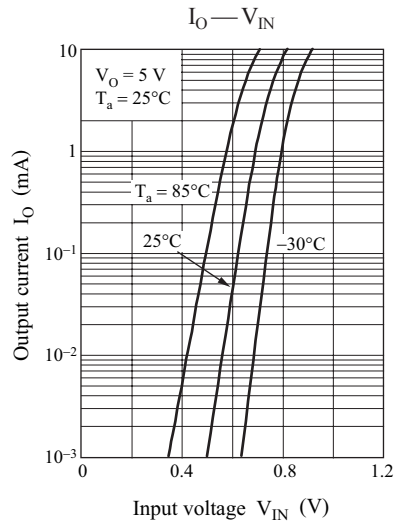
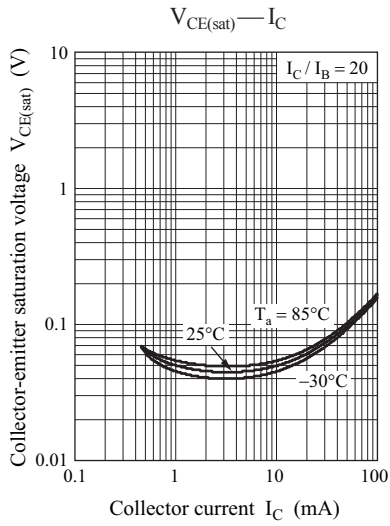
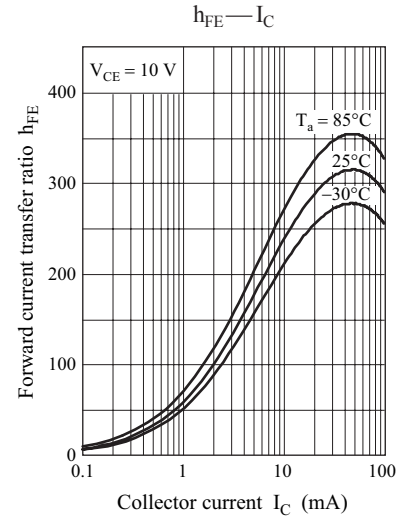
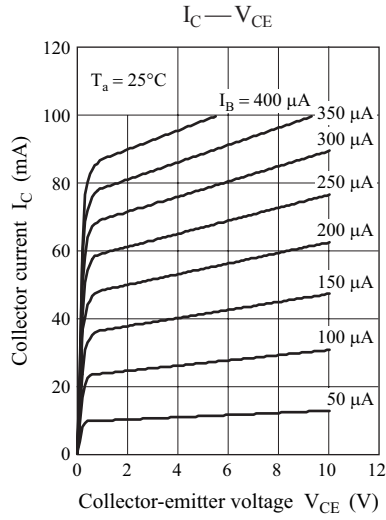
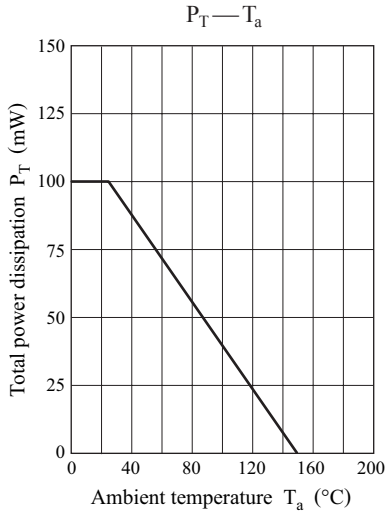


Resistance value	R_1	2.2	$\text{k}\Omega$
	R_2	47	$\text{k}\Omega$

■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

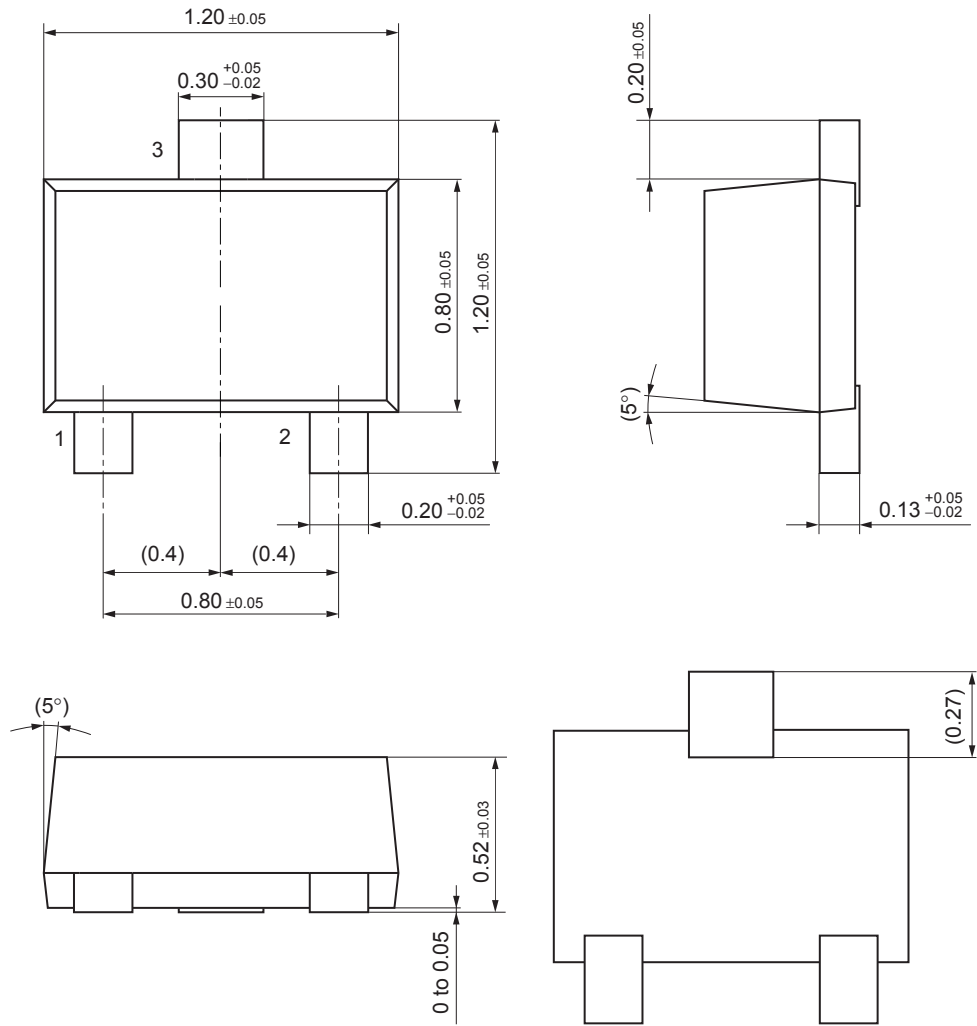
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_{\text{C}} = 10 \mu\text{A}, I_{\text{E}} = 0$	50			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_{\text{C}} = 2 \text{mA}, I_{\text{B}} = 0$	50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{\text{CB}} = 50 \text{V}, I_{\text{E}} = 0$			0.1	μA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{\text{CE}} = 50 \text{V}, I_{\text{B}} = 0$			0.5	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{\text{EB}} = 6 \text{V}, I_{\text{C}} = 0$			0.2	mA
Forward current transfer ratio	h_{FE}	$V_{\text{CE}} = 10 \text{V}, I_{\text{C}} = 5 \text{mA}$	80			—
Collector-emitter saturation voltage	$V_{\text{CE(sat)}}$	$I_{\text{C}} = 10 \text{mA}, I_{\text{B}} = 0.5 \text{mA}$			0.25	V
Input voltage (ON)	$V_{\text{I(on)}}$	$V_{\text{CE}} = 0.2 \text{V}, I_{\text{C}} = 5 \text{mA}$	1.2			V
Input voltage (OFF)	$V_{\text{I(off)}}$	$V_{\text{CE}} = 5 \text{V}, I_{\text{C}} = 100 \mu\text{A}$			0.4	V
Input resistance	R_1		-30%	2.2	+30%	$\text{k}\Omega$
Resistance ratio	R_1 / R_2		0.037	0.047	0.057	—

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.



SSSMini3-F2-B

Unit: mm



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