FNP600/850/1000 I²C Interface Programming Manual

1 Scope

This document describes in detail the I²C communication interface of the FNP600/850/1000 series. (FNP600-12/48, FNP850-12, FNP1000-48) This includes the physical layer and the SW protocol.

2 FNP600/850/1000 I²C Interface General Characteristic

FNP600/850/1000 I²C interface	**slave**
I²C Device Addressing Format	**7bit**
Device Address Range	**82_{Hex} ..BF_{Hex}**
Max. FNP600/850/1000 on one I²C Bus	**31**
Maximum I²C clock	**100kHz**
Maximum I²C clock without holding the SCL line down	**5kHz**
Pull-Up Voltage	**3.3…5V**
SDA/SCL internal series resistors	**0Ω**
Internal Pull-Up	**--**
Internal Pull-Up voltage	**--**
Internal capacitance	**70pF**
Internal Pull-Up Address lines	**>1.5kΩ**
Internal Pull-Up Address lines voltage	**5V**
Recommended external Pull-Up for SDA and SCL	**2.2kΩ …3.3kΩ**
Data Organization	**Serial EEPROM (256 x 8bit)**

Figure 2-1 Characteristic

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4 FNP600/850/1000 I²C features

4.1 Dynamic data

The FNP600/850/1000 series supports following monitoring features:
-Measured Output 1 voltage [V]
-Measured Output 1 current [A]
-Power Supply ok/false
-Output Voltage 1 in range/out of range
-Output Current 1 in range/out of range
-Input Voltage in range/out of range
-Temperature pre warning true/false
-Over Temperature true/false
-Fan OK/failure
-Fan Speed
-Time in Service

The FNP600/850/1000 series supports following control features:
-Set Output 1 voltage
-Output 1 enable/disable
-Fan speed full/internal controlled

4.2 Static data

In the EEPROM are following static data stored:
-Power Supply Model
-Serial Number
-Power-One Revision
-MFG Year
-MFG Month
-MFG Day
-MFG Name
-MFG Location Code
-Specified Output 1 Voltage
-Specified Output 2 Voltage
-Specified Output 1 Current
-Specified Output 2 Current
-Specified Output Power
-Minimum Specified Input Voltage
-Maximum Specified Input Voltage
-22 Bytes EEPROM for Customer use
-Checksum over static range

5 General I²C HW configuration

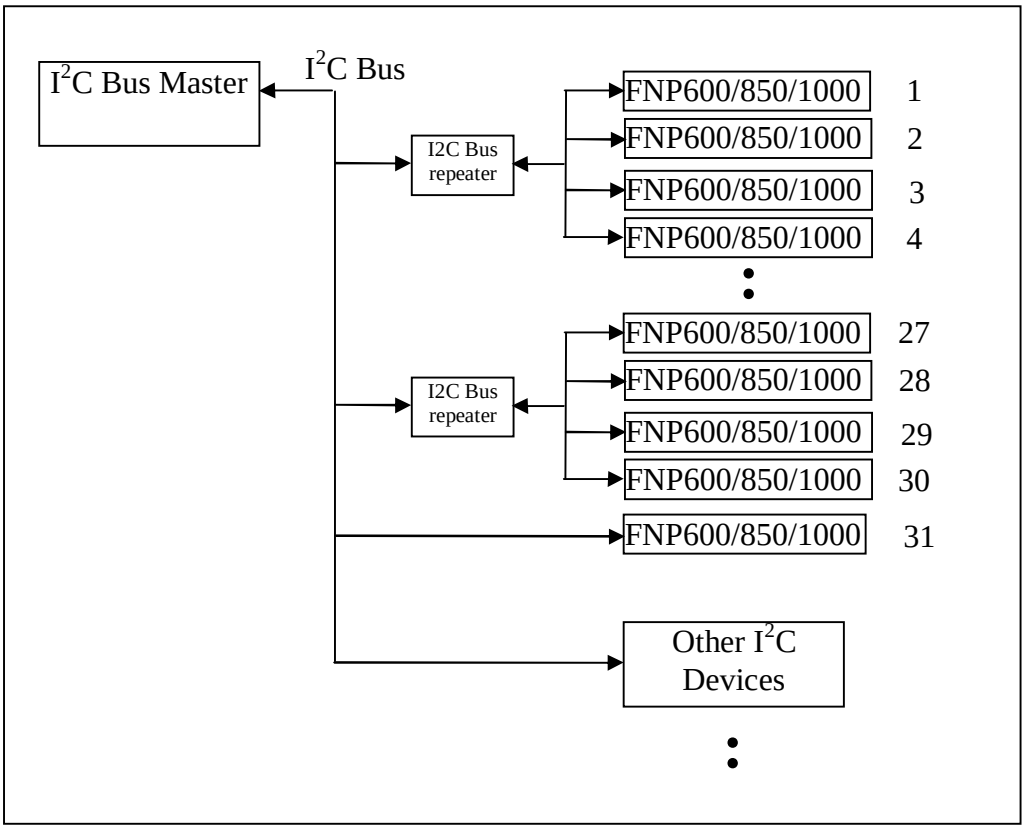


Figure 5-1 System Overview

To not exceed the I2C Bus limits of 400pF on the Bus, it needs for more than five FNP600/850/1000 one I2C Bus repeater. (Like PCA9515 from Philips or Texas Instruments)

5.1 Connecting the FNP600/850/1000 to the I²C Bus

The following diagram shows how the FNP600/850/1000 can be connected to the I²C Bus.

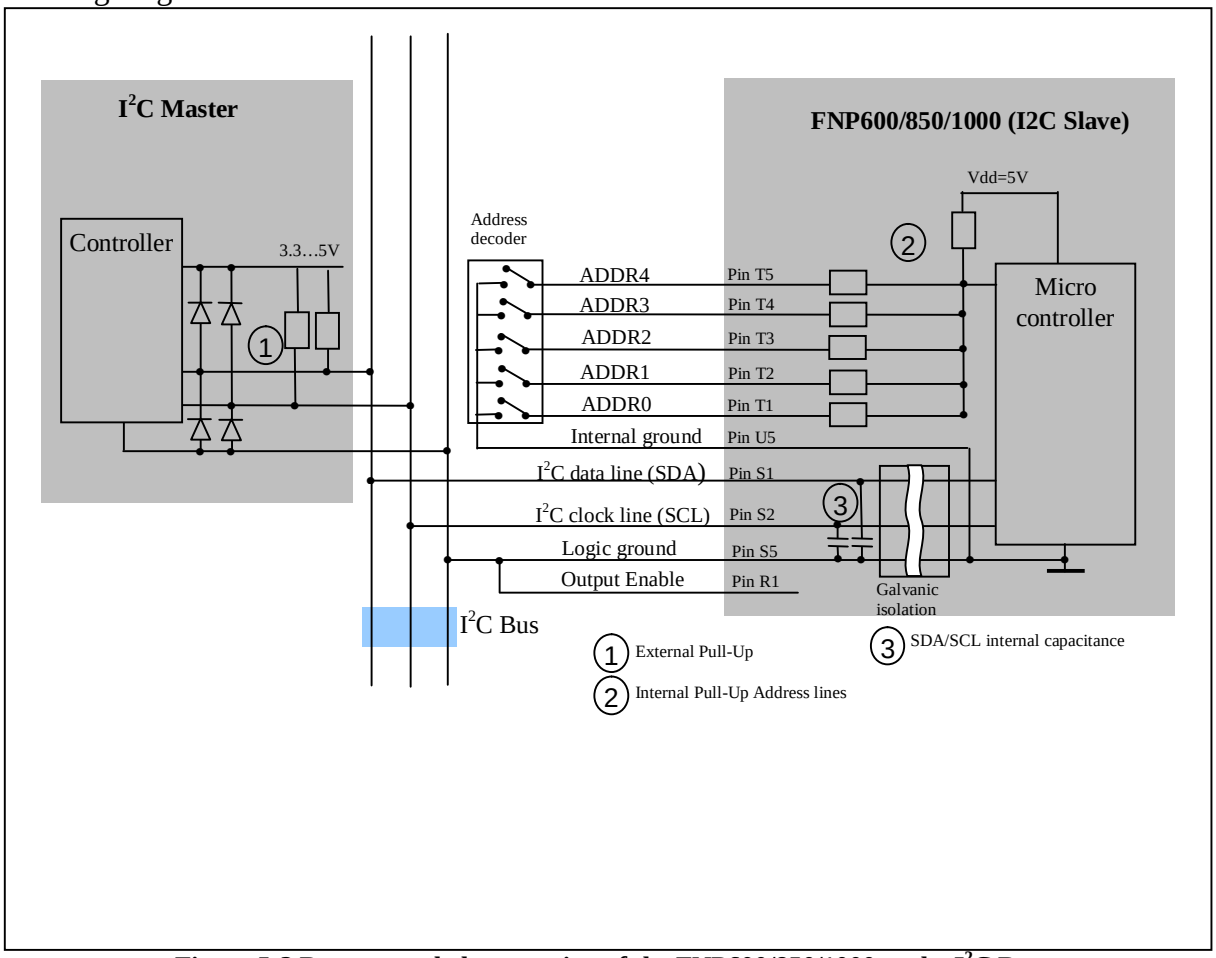


Figure 5-2 Recommended connecting of the FNP600/850/1000 to the I²C Bus

5.2 FNP600/850/1000 I²C Supply (Slave)

The FNP600/850/1000 Micro Controller is powered over the internal supply of the FNP600/850/1000. In case of AC failure or FNP600/850/1000 internal failure there is no power for the FNP600/850/1000 Micro Controller. This will have no influence on the I²C Bus, but the FNP600/850/1000 Micro Controller will not respond to the I2C Master. The FNP600/850/1000 Micro Controller will only replay to the I2C Master, if the Output Enable is connected to Logic Ground.

5.3 Device Address

The first byte after the START condition on the Bus is the device address sent out by the Bus Master to determine which device is being selected. The I²C Bus allows 7-bit or 10-bit addressing. The FNP600/850/1000 Interface uses a 7-bit address mode as defined in the Philips I²C specification. Each FNP600/850/1000 device has to be assigned to a unique address.

As shown below in Figure 5-3 Device Address the address byte is built up from three parts:
- Bit 6, 7: These bits are always the same independent of any address line.
- Bit 1...5: These bits depends how the Address line A0...A4 is connected on the backplane on the address decoder. These are logic 1 if open and logic 0 if wired to 0V (12V Standby RTN).

-Bit 0: This bit is the read/write bit (R=1/W=0) and determines the direction of the data from or to the Master.

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
FNP600/850/1000 Device Address	1	0	ADDR4 $*2^4$ + ADDR3$*2^3$+ ADDR2$*2^2$+ADDR1$*2^1$+ADDR0+1 (00001 … 11111)					direc.
	fix	fix						R/W

Figure 5-3 Device Address

	Address Line ADDR4	Address Line ADDR3	Address Line ADDR2	Address Line ADDR1	Address Line ADDR0	Read/ Write	Device Address [Bin]	Device Address [Hex]	Device Address [Dec]
FNP600/850/1000 Device address	0V	0V	0V	0V	0V	write	1000'0010	82	130
FNP600/850/1000 Device address	0V	0V	0V	0V	0V	read	1000'0011	83	131
FNP600/850/1000 Device address	0V	0V	0V	0V	open	write	1000'0100	84	132
FNP600/850/1000 Device address	0V	0V	0V	0V	open	read	1000'0101	85	133
FNP600/850/1000 Device address	0V	0V	0V	open	0V	write	1000'0110	86	134
FNP600/850/1000 Device address	0V	0V	0V	open	0V	read	1000'0111	87	135
FNP600/850/1000 Device address	0V	0V	0V	open	open	write	1000'1000	88	136
FNP600/850/1000 Device address	0V	0V	0V	open	open	read	1000'1001	89	137
FNP600/850/1000 Device address	0V	0V	open	0V	0V	write	1000'1010	8A	138
FNP600/850/1000 Device address	0V	0V	open	0V	0V	read	1000'1011	8B	139
FNP600/850/1000 Device address	0V	0V	open	0V	open	write	1000'1100	8C	140
FNP600/850/1000 Device address	0V	0V	open	0V	open	read	1000'1101	8D	141
FNP600/850/1000 Device address	0V	0V	open	open	0V	write	1000'1110	8E	142
FNP600/850/1000 Device address	0V	0V	open	open	0V	read	1000'1111	8F	143
FNP600/850/1000 Device address	0V	0V	open	open	open	write	1001'0000	90	144
FNP600/850/1000 Device address	0V	0V	open	open	open	read	1001'0001	91	145
FNP600/850/1000 Device address	0V	open	0V	0V	0V	write	1001'0010	92	146
FNP600/850/1000 Device address	0V	open	0V	0V	0V	read	1001'0011	93	147
FNP600/850/1000 Device address	0V	open	0V	0V	0V	write	1001'0100	94	148
FNP600/850/1000 Device address	open	open	open	0V	open	write	1011'1100	BC	188
FNP600/850/1000 Device address	open	open	open	0V	open	read	1011'1101	BD	189
FNP600/850/1000 Device address	open	open	open	open	0V	write	1011'1110	BE	190
FNP600/850/1000 Device address	open	open	open	open	0V	read	1011'1111	BF	191
FNP600/850/1000 Device address	open	open	open	open	open	write	1011'1111	BE	190
FNP600/850/1000 Device address	open	open	open	open	open	read	1011'1111	BF	191

Figure 5-4 Device Address Table

Example: On the backplane ADDR4, ADDR2 and ADDR0 are connected to 0V and ADDR3 and ADDR1 are left open, you will have the following device address to read a byte from the FNP:

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
			$0*2^4$	**$+1*2^3$**	**$+0*2^2$**	**$+1*2^1$**	**+ 0 + 1=**	
FNP600/850/1000 Device address	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**1**
	fix	fix	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	R

->$1001'0111_{Bin}=97_{Hex}=151_{Dec}$

5.4 I²C Bus Master and clock (SCL) speed

The I²C Bus Master controls communications between the Master and all I²C devices connected to the bus. If during an I²C communication cycle the FNP600/850/1000 is interrupted by an internal service interrupt, the FNP600/850/1000 will hold the SCL line low to force the master into a wait state. Data transfer will continue when the FNP600/850/1000 releases the SCL line.
Please note if the I²C bus is communicating with a clock frequency slower than 5 kHz, the SCL line will not be held low.

5.5 Maximum and minimum values for Pull-Up resisters

For I²C-bus systems, the values of the Pull-Up resistors depend on the following parameters:
- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current).

The supply voltage limits the minimum value of the Pull-Up resistor due to the specified minimum sink current of 3mA. On a 5V supply, this makes $\mathbf{R_{min}=5V/3mA=1.7k\Omega}$.
The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of the Pull-Up resister due to the specified rise time. For a System with 300pF capacitance (three FNP600/850/1000 at 60pF and a wire capacitance of 120pF) $\mathbf{R_{max}=3.5k\Omega}$.

For further information concerning the Pull-Up resister, refer to:
I²C Bus specification, 16.1 Maximum and minimum values of resistors Rp and Rs for Standard-mode I2C-bus devices.

6 SW Protocol

The data are organized like a serial I^2C EEPROM. Therefore each EEPROM address has defined data; this definition is documented in the I2C table for each model.

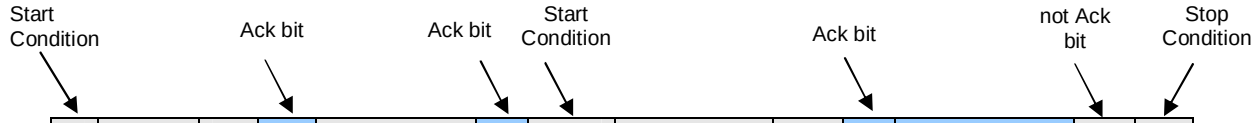
	Dez		Hex
Address	0	static data	0
	1	static data	1
	79	static data	4F
	80	static data	50
	81	open for customer use	51
	82	open for customer use	52
	102	open for customer use	66
	103	checksum over range above	67
	104	reserved	68
	105	reserved	69
	127	reserved	7F
	128	dynamic data	80
	129	dynamic data	81
	186	dynamic data	BA
	187	reserved	BB
	188	reserved	BC
	255	reserved	FF

Figure 6-1: Data Organization

There are three different message formats implemented in the FNP600/850/1000:
-Read a byte
-Read a block
-Write a byte

6.1 How to Read a byte

1) "Start condition" from Master
2) Master sends "Device address" with "write attribute"
3) "Acknowledge" from Slave device (FNP600/850/1000)
4) Master sends "EEPROM address"
5) "Acknowledge" from Slave device (FNP600/850/1000)
6) "Repeated start" from Master (Sr/S)
7) Master sends "Device address" with "read attribute"
8) "Acknowledge" from Slave device (FNP600/850/1000)
9) Slave sends "Data byte"
10) "Not Acknowledge" from Master (power management system)
11) "Stop condition" from Master



S	Slave Adr.	W	A	EEPROM Adr.	A	Sr/S	Slave Adr.	R	A	Data Byte	/A	P
	8bit			8 bit			8bit			8 bit		

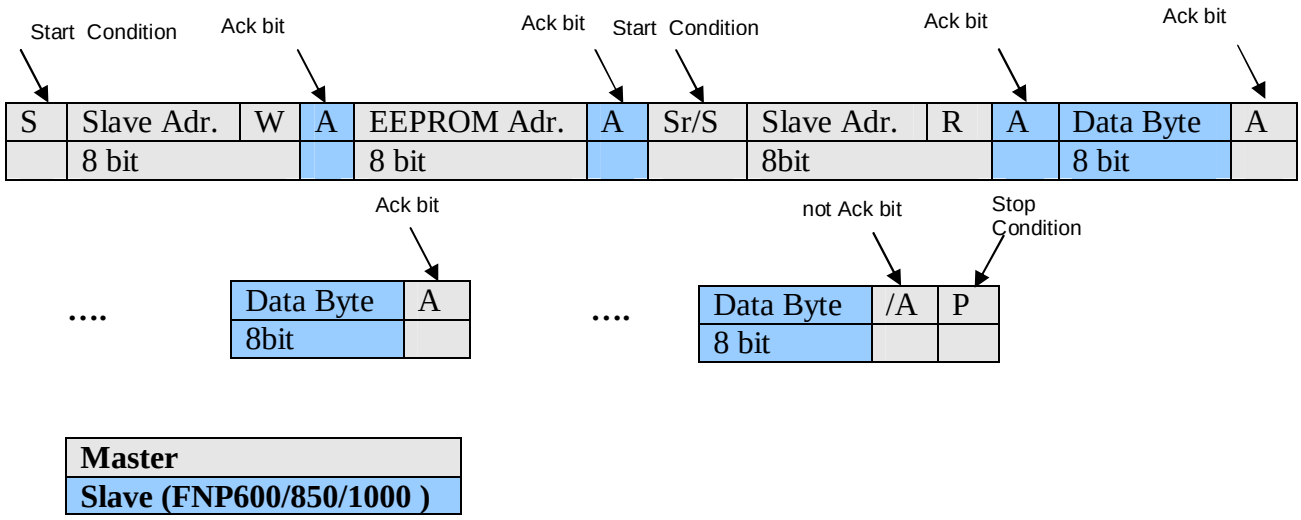
Master
Slave (FNP600/850/1000)

6.2 How to read a block

1) "Start condition" from Master
2) Master sends "Device address" with "write attribute"
3) "Acknowledge" from Slave device (FNP600/850/1000)
4) Master sends "EEPROM address"
5) "Acknowledge" from Slave device (FNP600/850/1000)
6) "Repeated start" from Master (Sr/S)
7) Master sends "Slave address" with "read attribute"
8) "Acknowledge" from Slave device (FNP600/850/1000)
9) Slave sends "Data byte"
10) "Acknowledge" from Master (power management system)

n-time repetition of step 9) and 10)

11) Slave sends "Data byte"
12) "Not Acknowledge" from Master (power management system)
13) "Stop condition" from Master



6.3 How to write a byte

1) "Start condition" from Master
2) Master sends "Slave address" with "write attribute"
3) "Acknowledge" from Slave device (FNP600/850/1000)
4) Master sends "EEPROM address"
5) "Acknowledge" from Slave device (FNP600/850/1000)
6) Master sends "Data byte"
7) "Acknowledge" from Slave device (FNP600/850/1000)
8) "Stop condition" from Master
9) Wait min. 8ms to write next byte (EEPROM write time)

S	Slave Adr.	W	A	EEPROM Adr.	A	Data Byte	A	P
	8 bit			8 bit		8bit		

Master
Slave (FNP600/850/1000)

7 Setting the Output Voltage

After writing the new Output Voltage value you have to disable and enable (SW or HW) the unit before the new Output Voltage will be set.

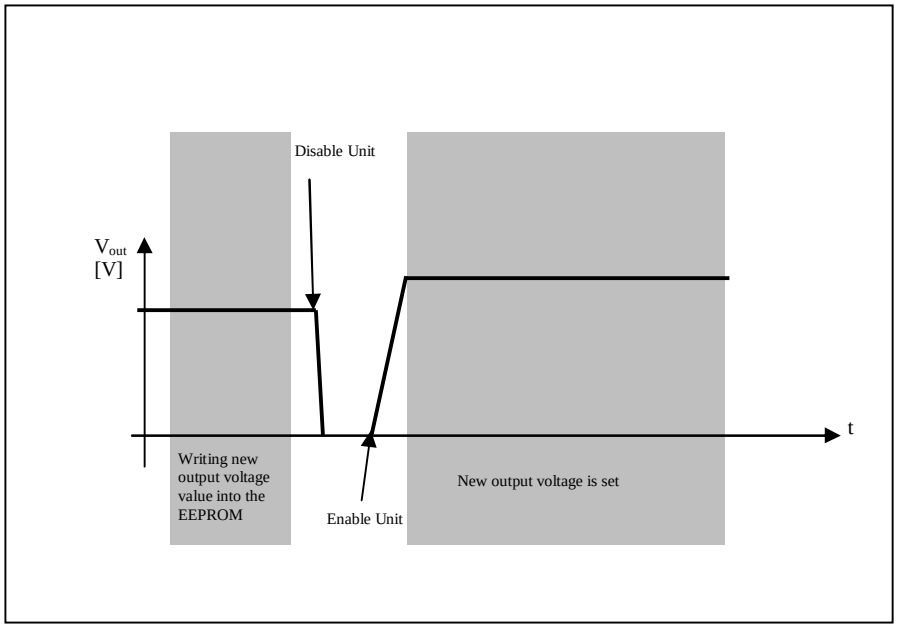


Figure 7-1 Setting the Output Voltage

8 Power-One I²C Interface tool

The Power-One I²C – Management Software (HZZ02002SW, www.power-one.com) demonstrates all the I²C interface features of the FNP600/850/1000.

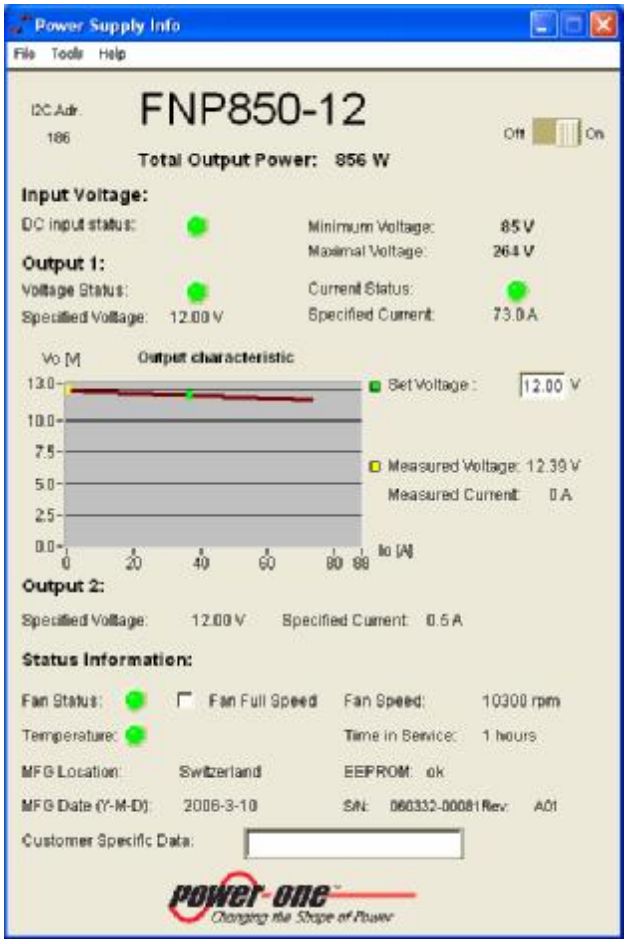


Figure 8-1 Screenshot FNP600/850/1000

Power-One I²C – Management Software supports two I²C converters:

iPort MIIC-201 (Micro Computer Control)	HZZ02002G from Power-One
	

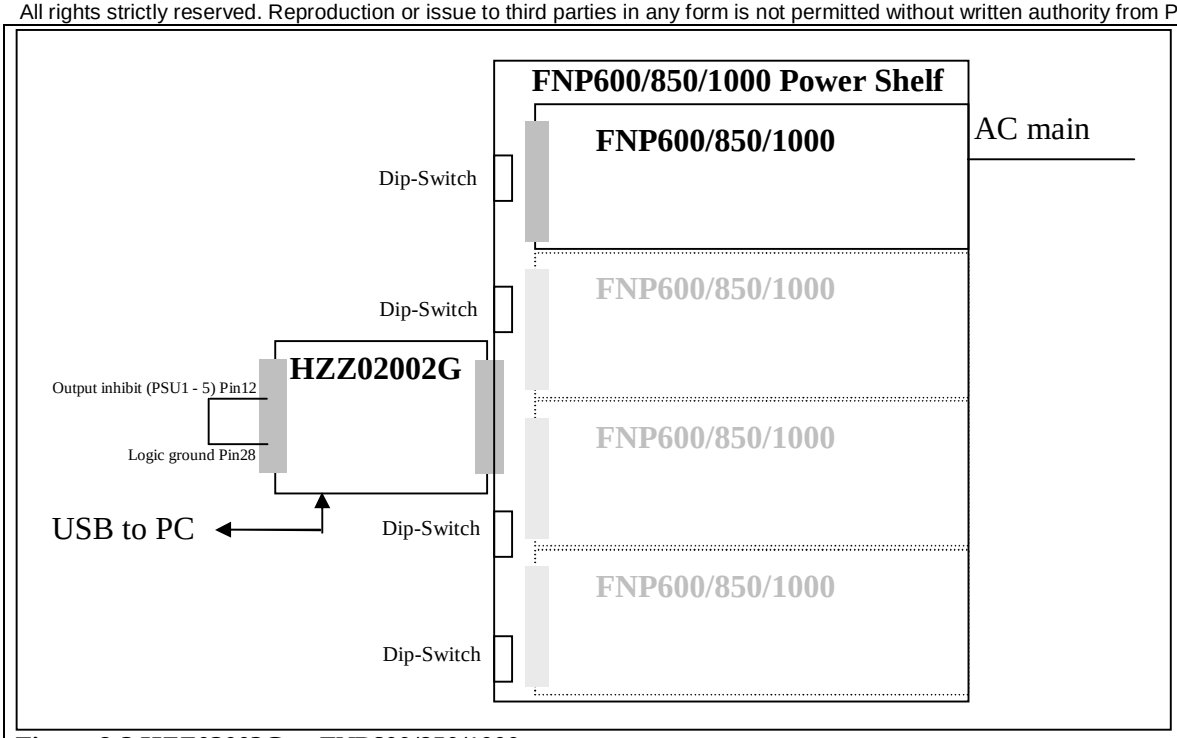


Figure 8-2 HZZ02002G to FNP600/850/1000 setup

Plug one or more FNP600/850/1000 into the power shelf, connect the HZZ02002G to the power shelf, connect on the other side of the HZZ02002G the “Output inhibit(PSU1-5)” Pin12 to “Logic Ground” Pin28 to enable the Unit and Power up the FNP60/850/1000.

Power Shelf Number to the according FNP60/850/1000 Model:

FNP600/850/1000 Model	Power Shelf Number
FNP600-12	FNR-5-12G
FNP850-12	FNR-5-12G
FNP600-48	FNR-5-48G
FNP1000-48	FNR-5-48G

Figure 8-3 Power Shelf Number to the according FNP600/850/1000 Model

The I^2C device address will be according the Dip-Switch on the Power Shelf, the I2C address will be found automatic by the Software. (HZZ02002SW).
In your final application the I^2C master will be a Micro Computer or an FPGA with an I^2C interface. That makes it easy and inexpensive to use the interface.

9 Bibliography

-Philips Semiconductors, The I 2C-BUS Specification, V.2.1, Document order number: 9398 393 40011
www.semiconductors.**philips**.com/ acrobat/literature/9398/39340011.pdf

-Philips SemiconductorsI2C Handbook
www.semiconductors.**philips**.com/ acrobat/various/**philips_i2c**_handbook.pdf

-Power-One, FNP600/850/1000 Data-Sheet
-Power-One, FNP600/850/1000 EEPROM Table

10 Figure Index

11 Glossary

µC	Micro Controller
Bin	Value in binary number system
Dec	Value in decimal number system
EEPROM	Electrically Erasable Programmable Read Only Memory
Hex	Value in hexadecimal number system
I^2C Bus	Inter-Integrated Circuit Bus
kHz	SI unit of frequency: Hertz(1/s) * 10^3
LSB	Least significant bit
MFG	Manufacturing
MSB	Most significant bit
pF	SI unit of Capacitance: farad($kg^{-1} \cdot m^{-2} \cdot A^2 \cdot s4$) * 10^{-12}
SCL	serial clock line
SDA	serial data line