

## OptiMOS® -T2 Power-Transistor



- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

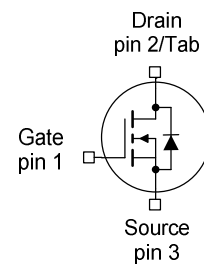
### Product Summary

|                  |     |    |
|------------------|-----|----|
| $V_{DS}$         | 30  | V  |
| $R_{DS(on),max}$ | 5.5 | mΩ |
| $I_D$            | 50  | A  |

### PG-TO252-3-11



| Type           | Package       | Marking |
|----------------|---------------|---------|
| IPD50N03S4L-06 | PG-TO252-3-11 | 4N03L06 |



**Maximum ratings**, at  $T_j=25\text{ °C}$ , unless otherwise specified

| Parameter                                    | Symbol         | Conditions                                               | Value        | Unit |
|----------------------------------------------|----------------|----------------------------------------------------------|--------------|------|
| Continuous drain current <sup>1)</sup>       | $I_D$          | $T_C=25\text{ °C}$ , $V_{GS}=10\text{ V}$                | 50           | A    |
|                                              |                | $T_C=100\text{ °C}$ , $V_{GS}=10\text{ V}$ <sup>2)</sup> | 50           |      |
| Pulsed drain current <sup>2)</sup>           | $I_{D,pulse}$  | $T_C=25\text{ °C}$                                       | 200          |      |
| Avalanche energy, single pulse <sup>2)</sup> | $E_{AS}$       | $I_D=50\text{ A}$                                        | 36           | mJ   |
| Avalanche current, single pulse              | $I_{AS}$       | -                                                        | 50           | A    |
| Gate source voltage                          | $V_{GS}$       | -                                                        | ±16          | V    |
| Power dissipation                            | $P_{tot}$      | $T_C=25\text{ °C}$                                       | 56           | W    |
| Operating and storage temperature            | $T_j, T_{stg}$ | -                                                        | -55 ... +175 | °C   |
| IEC climatic category; DIN IEC 68-1          | -              | -                                                        | 55/175/56    | -    |

| Parameter                           | Symbol     | Conditions                                   | Values |      |      | Unit |
|-------------------------------------|------------|----------------------------------------------|--------|------|------|------|
|                                     |            |                                              | min.   | typ. | max. |      |
| Thermal resistance, junction - case | $R_{thJC}$ | -                                            | -      | -    | 2.7  | K/W  |
| SMD version, device on PCB          | $R_{thJA}$ | minimal footprint                            | -      | -    | 62   |      |
|                                     |            | 6 cm <sup>2</sup> cooling area <sup>3)</sup> | -      | -    | 40   |      |

**Electrical characteristics**, at  $T_j=25\text{ }^{\circ}\text{C}$ , unless otherwise specified

#### Static characteristics

|                                  |               |                                                       |     |     |     |            |
|----------------------------------|---------------|-------------------------------------------------------|-----|-----|-----|------------|
| Drain-source breakdown voltage   | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=1mA$                                  | 30  | -   | -   | V          |
| Gate threshold voltage           | $V_{GS(th)}$  | $V_{DS}=V_{GS}, I_D=20\mu A$                          | 1.0 | 1.5 | 2.2 |            |
| Zero gate voltage drain current  | $I_{DSS}$     | $V_{DS}=30V, V_{GS}=0V, T_j=25^{\circ}\text{C}$       | -   | 0.1 | 1   | $\mu A$    |
|                                  |               | $V_{DS}=30V, V_{GS}=0V, T_j=125^{\circ}\text{C}^{2)}$ | -   | 10  | 100 |            |
| Gate-source leakage current      | $I_{GSS}$     | $V_{GS}=16V, V_{DS}=0V$                               | -   | -   | 100 | nA         |
| Drain-source on-state resistance | $R_{DS(on)}$  | $V_{GS}=4.5V, I_D=25A$                                | -   | 6.9 | 9.0 | m $\Omega$ |
|                                  |               | $V_{GS}=10V, I_D=50A$                                 | -   | 4.9 | 5.5 |            |

| Parameter                    | Symbol       | Conditions                                            | Values |      |      | Unit |
|------------------------------|--------------|-------------------------------------------------------|--------|------|------|------|
|                              |              |                                                       | min.   | typ. | max. |      |
| Input capacitance            | $C_{iss}$    | $V_{GS}=0V, V_{DS}=25V,$<br>$f=1MHz$                  | -      | 1790 | 2330 | pF   |
| Output capacitance           | $C_{oss}$    |                                                       | -      | 460  | 600  |      |
| Reverse transfer capacitance | $C_{rss}$    |                                                       | -      | 17   | 34   |      |
| Turn-on delay time           | $t_{d(on)}$  | $V_{DD}=15V, V_{GS}=10V,$<br>$I_D=30A, R_G=1.6\Omega$ | -      | 3    | -    | ns   |
| Rise time                    | $t_r$        |                                                       | -      | 1    | -    |      |
| Turn-off delay time          | $t_{d(off)}$ |                                                       | -      | 19   | -    |      |
| Fall time                    | $t_f$        |                                                       | -      | 7    | -    |      |

#### Gate Charge Characteristics<sup>2)</sup>

|                       |               |                                                      |   |     |    |    |
|-----------------------|---------------|------------------------------------------------------|---|-----|----|----|
| Gate to source charge | $Q_{gs}$      | $V_{DD}=24V, I_D=50A,$<br>$V_{GS}=0 \text{ to } 10V$ | - | 6   | 8  | nC |
| Gate to drain charge  | $Q_{gd}$      |                                                      | - | 3   | 6  |    |
| Gate charge total     | $Q_g$         |                                                      | - | 24  | 31 |    |
| Gate plateau voltage  | $V_{plateau}$ |                                                      | - | 3.2 | -  | V  |

#### Reverse Diode

|                                                |               |                                             |     |      |     |    |
|------------------------------------------------|---------------|---------------------------------------------|-----|------|-----|----|
| Diode continuous forward current <sup>2)</sup> | $I_S$         | $T_C=25^\circ C$                            | -   | -    | 50  | A  |
| Diode pulse current <sup>2)</sup>              | $I_{S,pulse}$ |                                             | -   | -    | 200 |    |
| Diode forward voltage                          | $V_{SD}$      | $V_{GS}=0V, I_F=50A,$<br>$T_J=25^\circ C$   | 0.6 | 0.95 | 1.3 | V  |
| Reverse recovery time <sup>2)</sup>            | $t_{rr}$      | $V_R=30V, I_F=I_S,$<br>$di_F/dt=100A/\mu s$ | -   | 17   | -   | ns |
| Reverse recovery charge <sup>2)</sup>          | $Q_{rr}$      |                                             | -   | 14   | -   | nC |

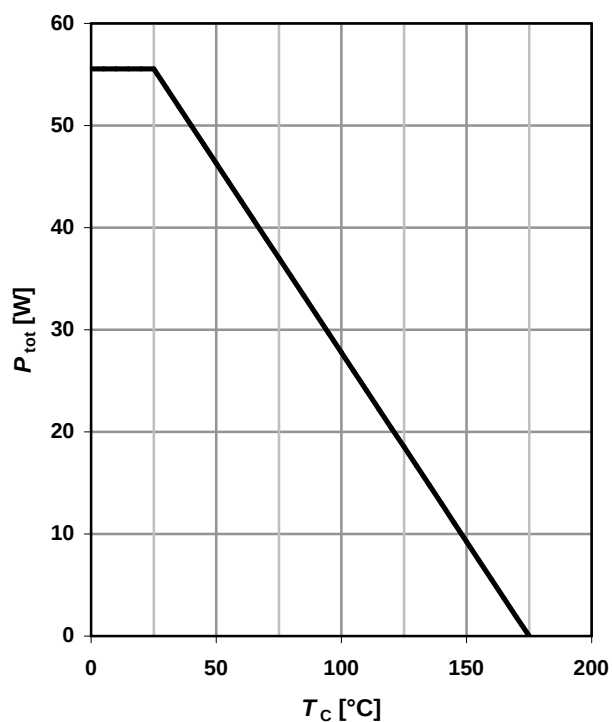
<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC} = 2.7K/W$  the chip is able to carry 77A at 25°C.

<sup>2)</sup> Defined by design. Not subject to production test.

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

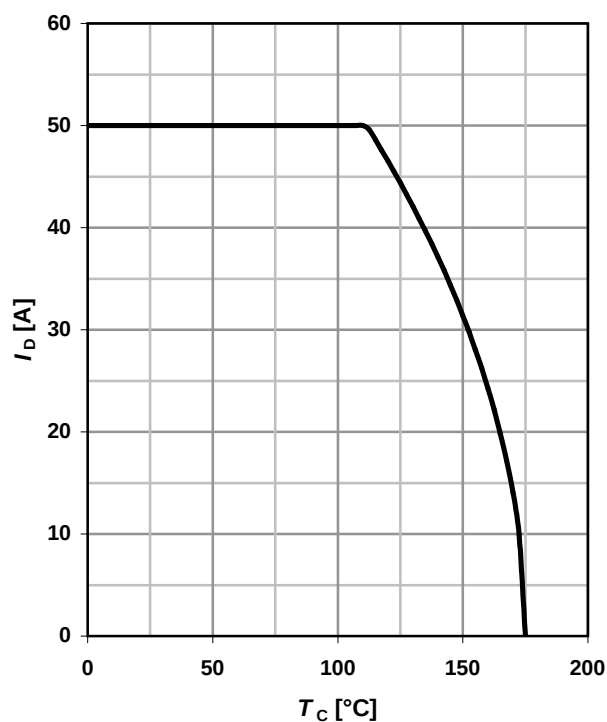
## 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



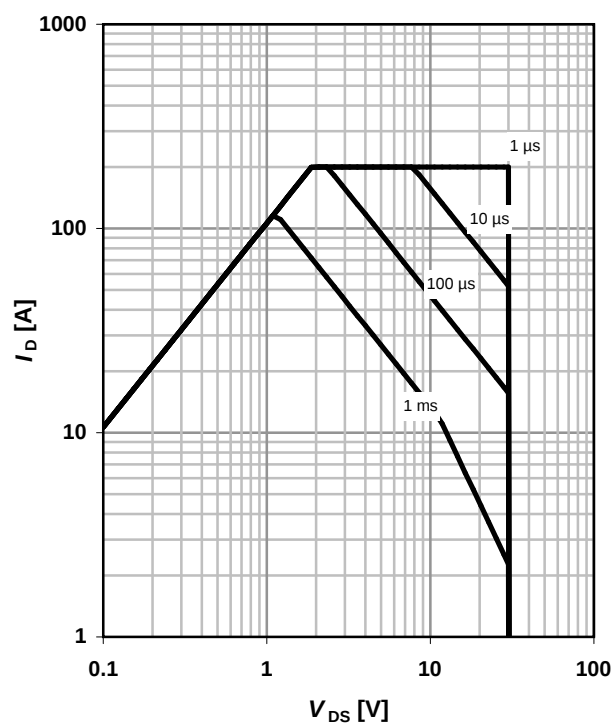
## 2 Drain current

$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



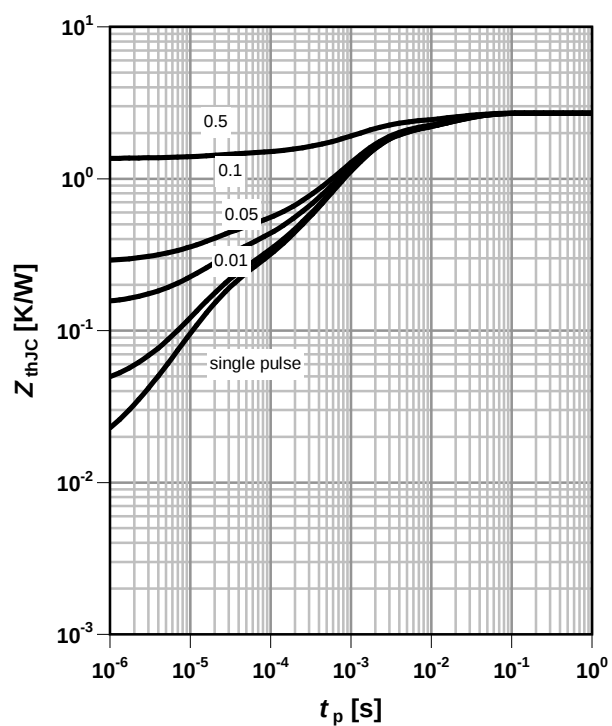
$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

parameter:  $t_p$



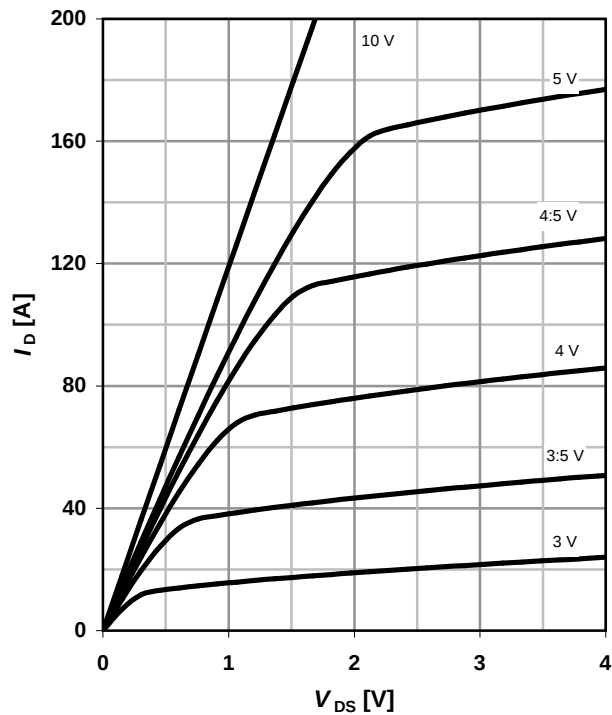
$$Z_{\text{thJC}} = f(t_p)$$

parameter:  $D = t_p/T$



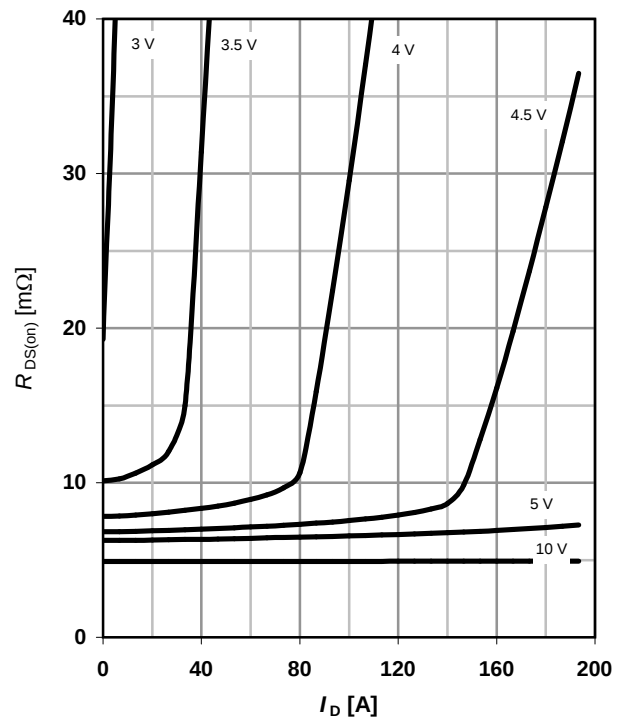
## 5 Typ. output characteristics

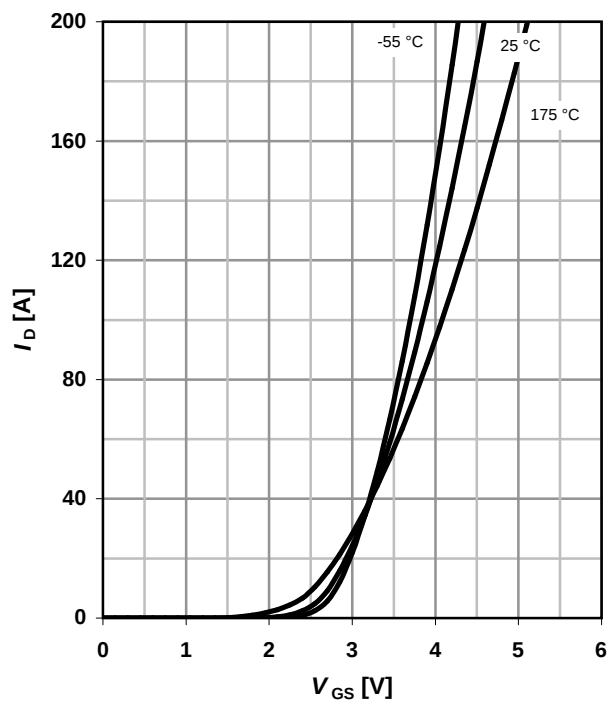
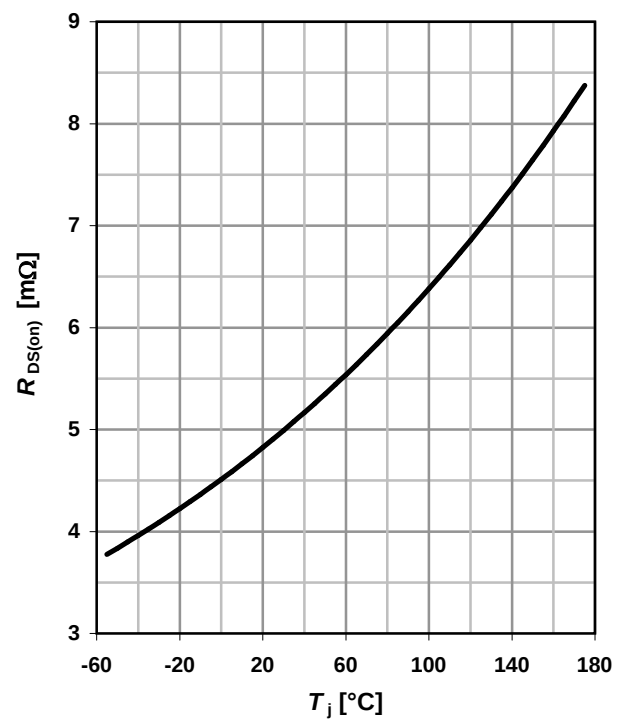
 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$ 

parameter:  $V_{GS}$ 


## 6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$ 

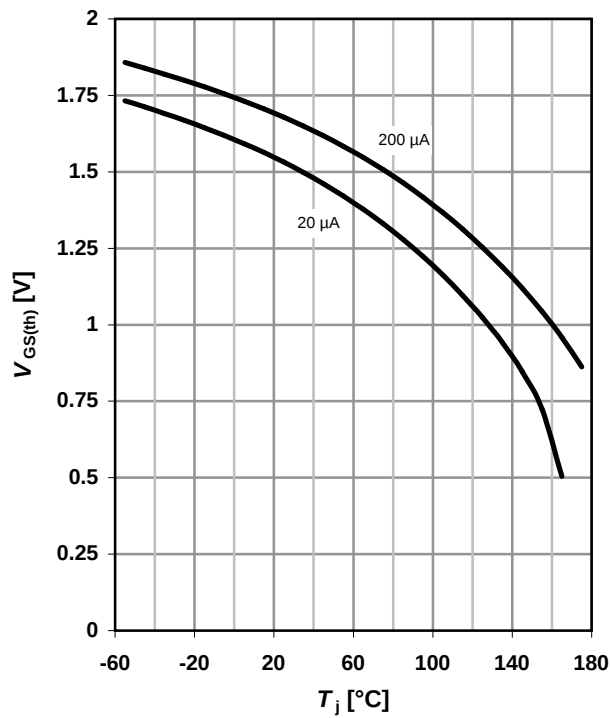
parameter:  $V_{GS}$ 

 $I_D = f(V_{GS}); V_{DS} = 6\text{V}$ 

parameter:  $T_j$ 

 $R_{DS(on)} = f(T_j); I_D = 50\text{ A}; V_{GS} = 10\text{ V}$ 


## 9 Typ. gate threshold voltage

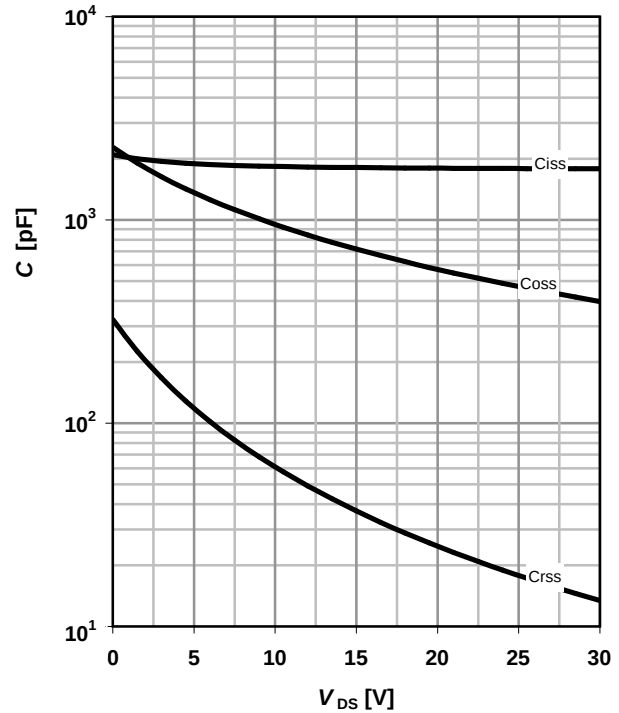
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter:  $I_D$



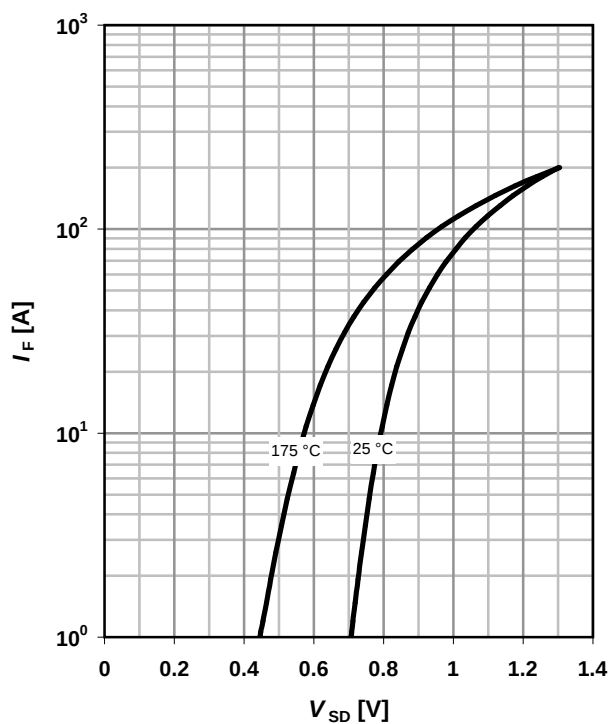
## 10 Typ. capacitances

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



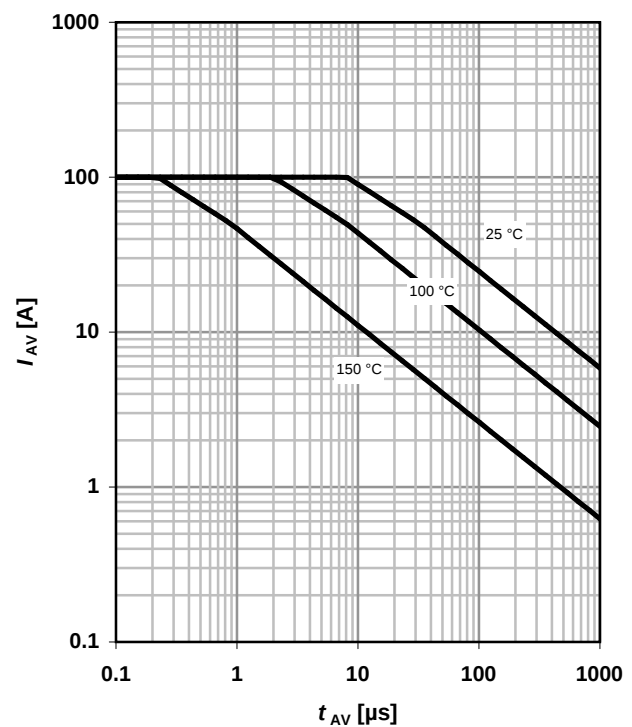
$$I_F = f(V_{SD})$$

parameter:  $T_j$



$$I_{AS} = f(t_{AV})$$

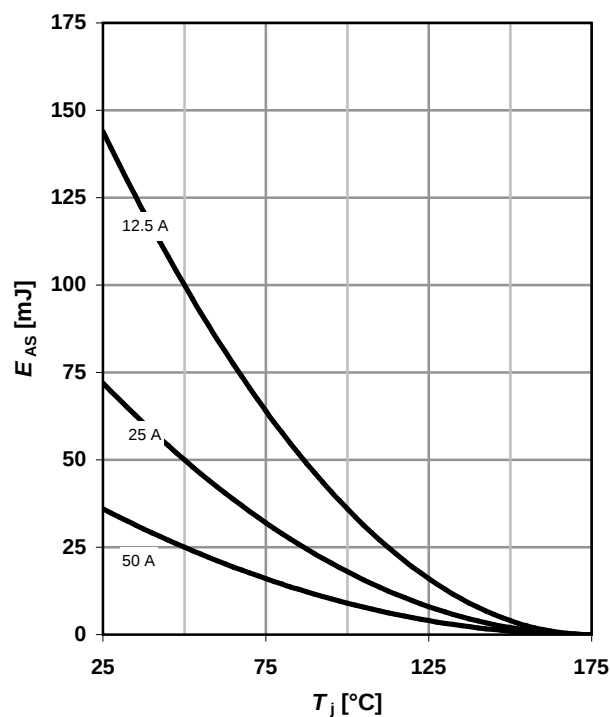
parameter:  $T_{j(start)}$



### 13 Avalanche energy

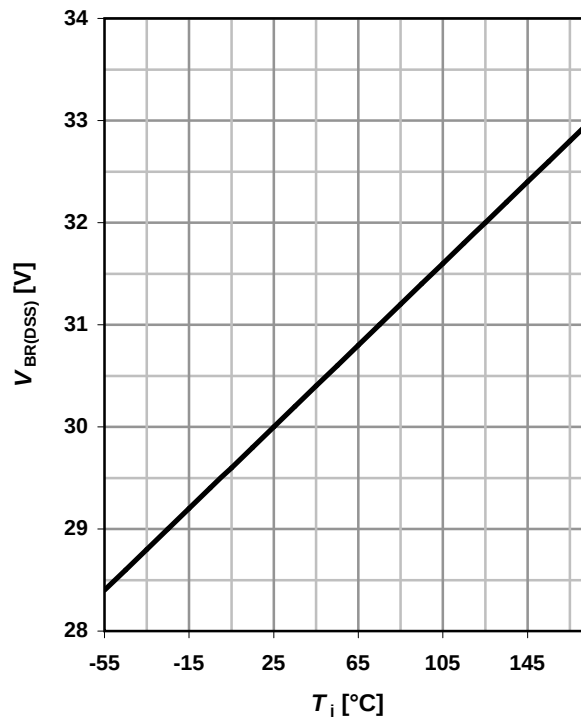
$$E_{AS} = f(T_j)$$

parameter:  $I_D$



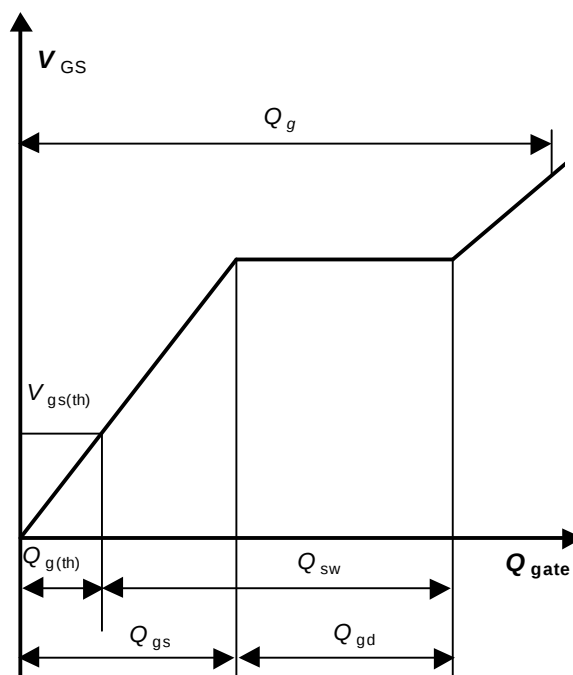
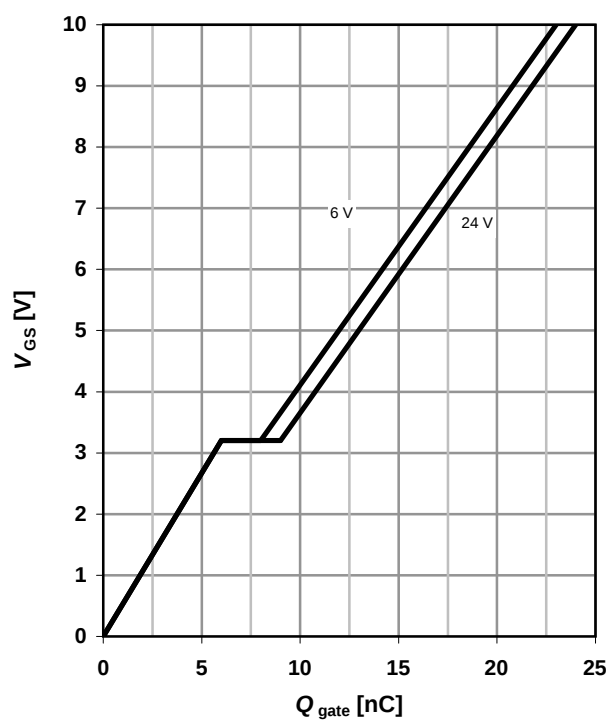
### 14 Drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



$$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$$

parameter:  $V_{DD}$



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Revision History

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| Version      | Date       | Changes                      |
|--------------|------------|------------------------------|
| Revision 1.1 | 05.10.2010 | Correction of pinout diagram |
|              |            |                              |
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