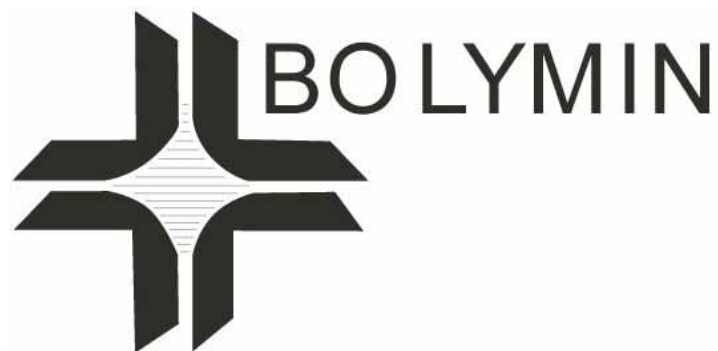




SPECIFICATIONS FOR LCD MODULE

MODEL NO.
BL12832BWRNH\$


COMPLIANT

FOR MESSRS:

ON DATE OF:

APPROVED BY:

BOLYMIN, INC.

13F-1, 20, TA-LONG RD., TAICHUNG CITY 403, TAIWAN, R.O.C.

WEB SITE: <http://www.bolymin.com.tw> TEL:+886-4-23293029 FAX:+886-4-23293055

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2008/09/16	SPEC.

CONTENTS

1. Numbering System
2. General Specification
3. Absolute Maximum Ratings
4. Electrical Characteristics
5. Optical Characteristics
6. Block Diagram
7. Interface Pin Function
8. Timing Characteristics
9. Graphic Display Data RAM Address MAP
10. Power ON / OFF Sequence & Application Circuit
11. Display Control Instruction
12. Reliability
13. Appendix

1. Numbering System

<u>B</u>	<u>L</u>	<u>12832</u>	<u>B</u>	<u>W</u>	<u>R</u>	<u>N</u>	<u>-</u>	<u>H</u>	<u>\$</u>
0	1	2	3	4	5	6	7	8	9

0	Brand	Bolymin	
1	Module Type	C= character type G= graphic type P= TAB/TCP type	O= COG type F= COF type L=PLED/OLED
2	Format	2002=20 characters, 2 lines 12232= 122 x 32 dots	
3	Version No.	A type	
4	LCD Color	G=STN/gray Y=STN/yellow-green PLED/yellow-green C=color STN,OLED/RGB E=OLED/yellow W=white	B=STN/blue,OLED/blue F=FSTN T=TN D=OLED/blue+yellow A=OLED/blue+yellow+green
5	LCD Type	R=positive/reflective P=positive/transflective	M=positive/transmissive N=negative/transmissive
6	Backlight type/color	L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green F=RGB array I=RGB edge Q=LED edge/red N=No backlight	D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white Y=LED Bottom/yellow O=LED array/orange K=LED edge/green A=LED edge/amber
7	CGRAM Font (applied only on character type)	J=English/Japanese Font E=English/European Font G=Chinese(simple) F=Chinese(traditional)	C=English/Cyrillic Font H=English/Hebrew Font A=English/Arabic Font
8	View Angle/ Operating Temperature	B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature	T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature E=Top/ultra wide temperature
9	Special Code	3=3 volt logic power supply n=negative voltage for LCD c=cable/connector xxx=to be assigned on datasheet	t=temperature compensation for LCD p=touch panel \$=RoHS

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128×32	dots
Module dimension (L*W*H)	30.4*14.5*1.61(MAX)	mm
View area	29.4*9.4	mm
Active area	25.58*6.38	mm
Dot size	0.18 (W)×0.18(H)	mm
Dot pitch	0.20(W)×0.20 (H)	mm
Color	white	

(2) Controller IC: SSD1305 Controller

(3) Temperature Range

Operating	-40 ~ +70
Storage	-40 ~ +85

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	-	+70	
Storage Temperature	TST	-40	-	+85	
Input Voltage (VDD)	VDD	-0.3	-	3.5	V
Supply Voltage (Vcc)	Vcc	8	-	16	V
Humidity	-	-	-	85	%
Operating lift time	-	-	30000(*)	-	Hrs

*:100cd/m² light on

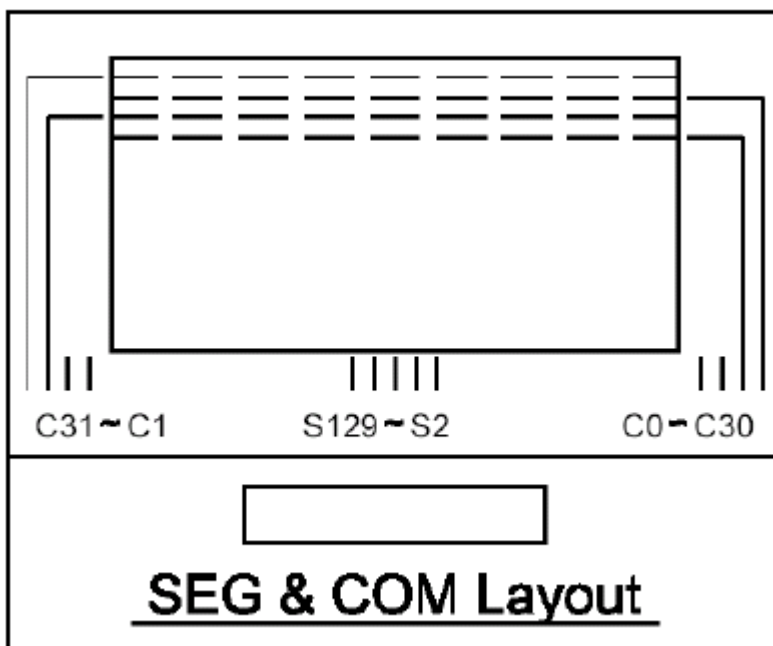
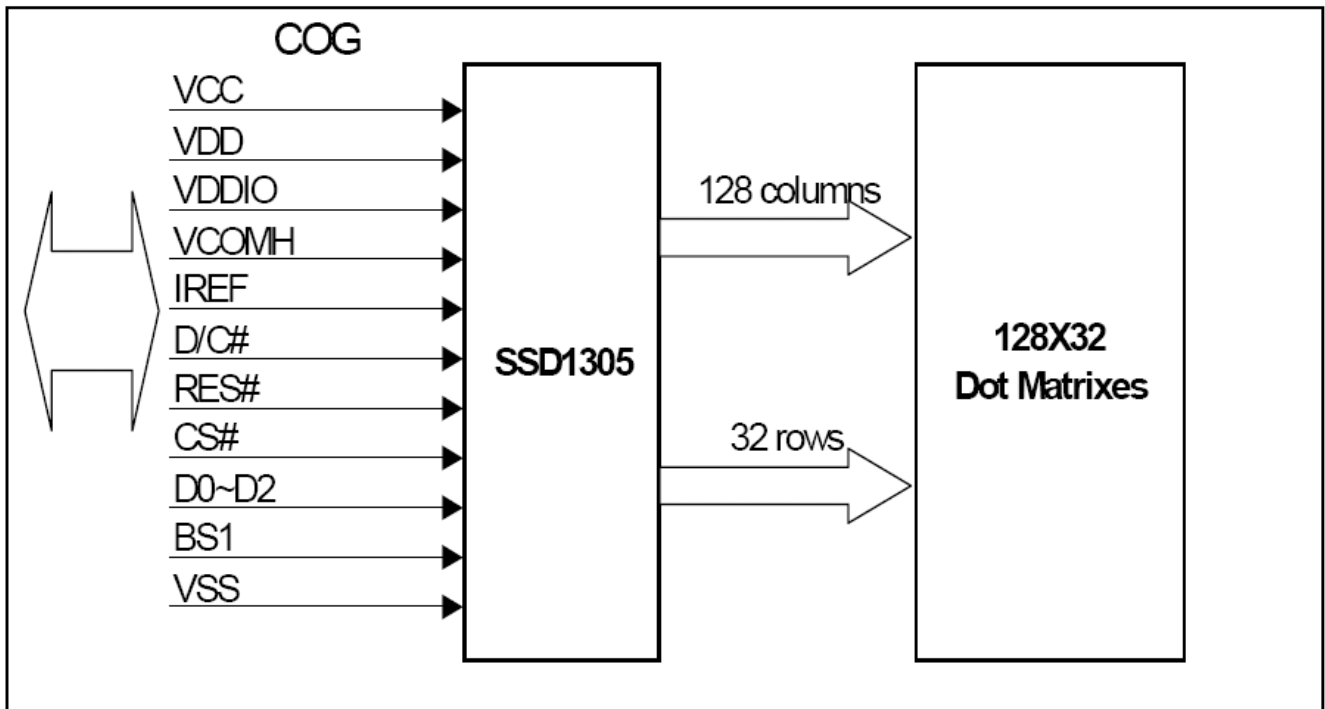
4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V _{DD} -V _{SS}	-	2.4	2.7	3.5	V
Supply Voltage For Panel	V _{CC} -V _{SS}	-	11.5	12	12.5	V
Input High Vol	V _{IH}	-	0.8V _{DD}	-	V _{DD}	V
Input Low Vol	V _{IL}	-	0	-	0.2V _{DD}	V
Output High Vol	V _{OH}	-	0.9V _{DD}	-	V _{DD}	V
Output Low Vol.	V _{OL}	-	0	-	0.1V _{DD}	V
Supply Current	I _{DD}	-	-	6	7	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	-	-	deg
Dark Room contrast	2000:1	-	-	-
Response Time	-	10	-	us

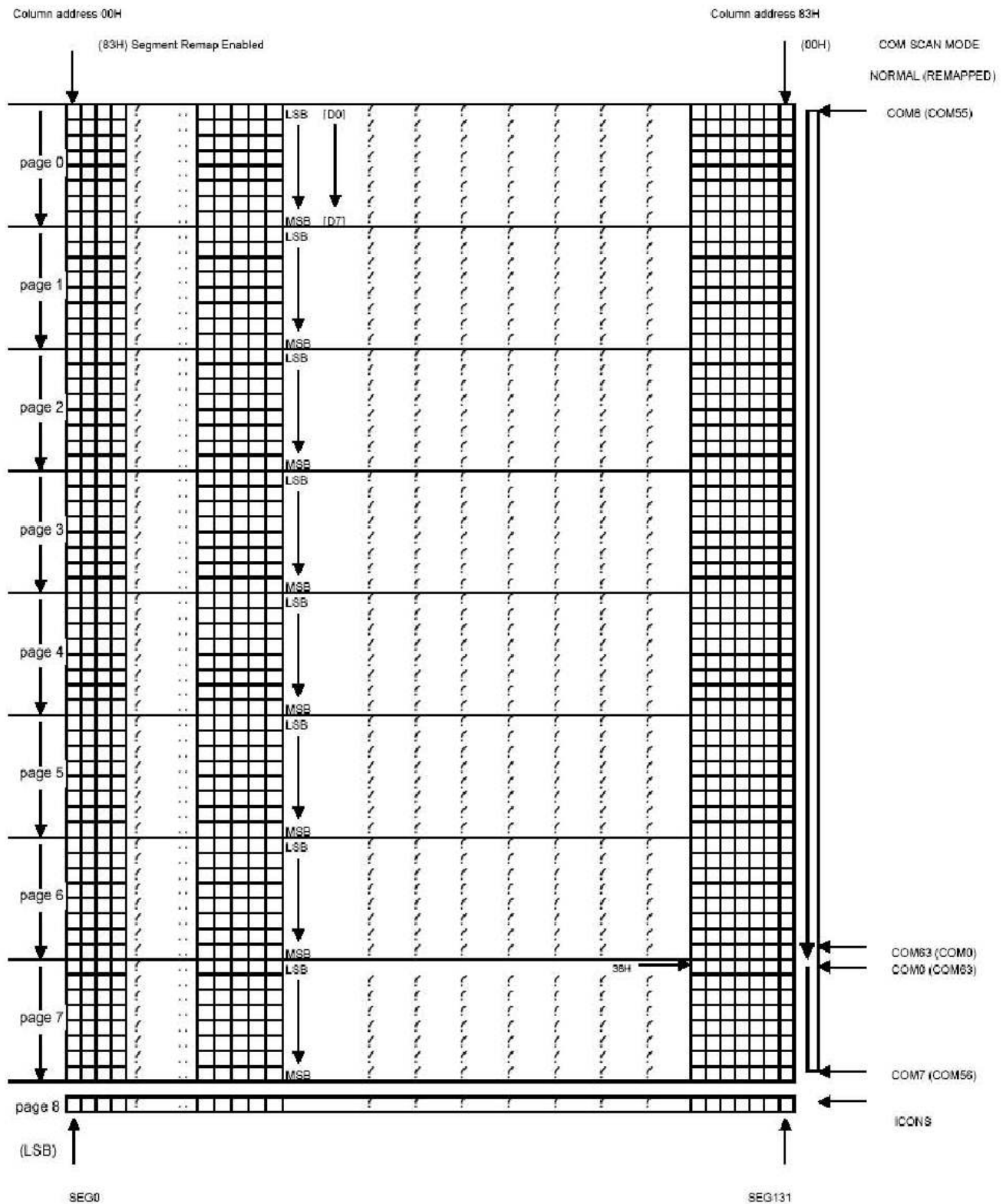
6. Block Diagram



7. Interface Pin Function

Pin No.	Symbol	Level	Description
1	NC	—	No connection
2	Vss	—	This is ground pin
3	Vcc	—	power supply for OLED panel
4	VCOMH	—	The COM voltage reference pin, this pin should be connected to ground through a capacitor
5	IREF	—	The current reference input pin, this pin should be connected to ground through a resistor.
6	D2	H/L	In SPI application, the pin should be floated
7	D1	H/L	Data bus line(SDIN)
8	D0	H/L	Data bus line(SCLK)
9	D/C#	H/L	This is data/command control pin, H: Data input ,L: Command input .
10	RES#	H/L	Hardware reset signal
11	CS#	H/L	Chip select pin.
12	BS1	H/L	Interface select pin, SPI: Active LOW
13	VDDIO	H/L	This pin is a power supply pin of I/O buffer
14	VDD	H/L	Voltage power supply for logic
15	Vss	—	This is ground pin
16	NC	—	No connection

8. Graphic Display Data RAM Address MAP

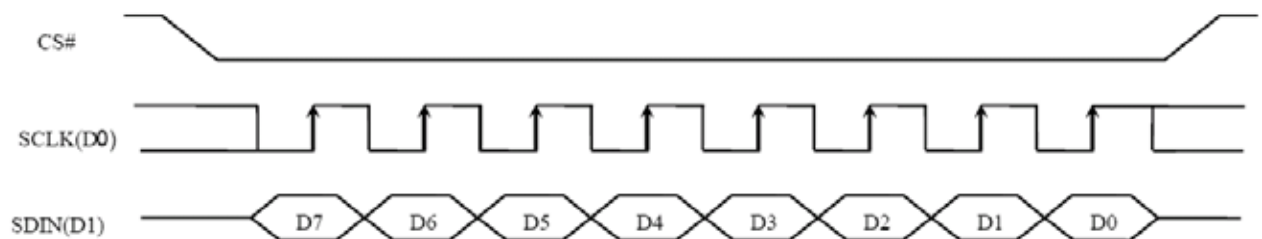
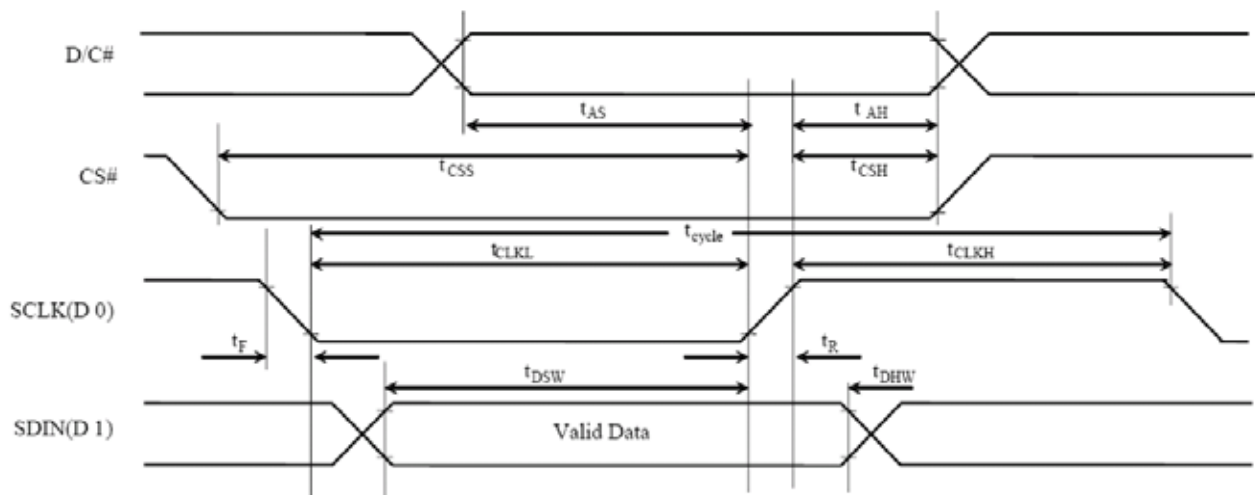


9. Timing Characteristics

9-1.8080 MPU Interface

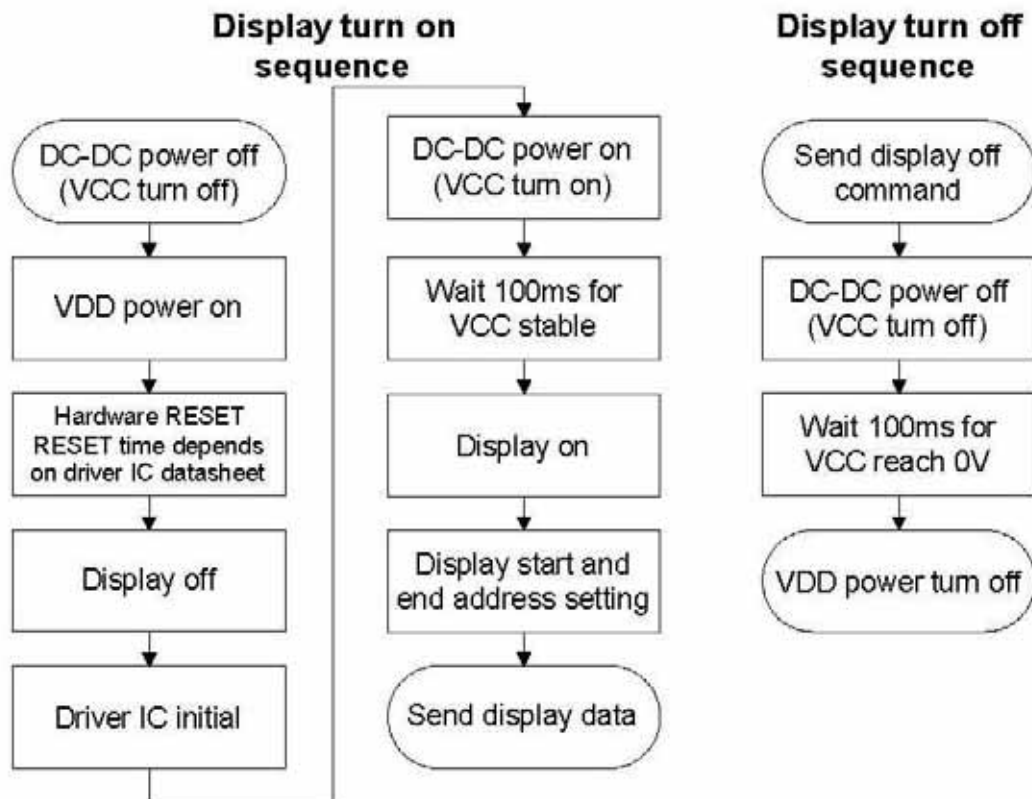
($V_{DD} - V_{SS} = 2.4V$ to $3.5V$, $V_{DDIO} = V_{DD}$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



10. Power ON / OFF Sequence & Application Circuit

10.1 POWER ON / OFF SEQUENCE



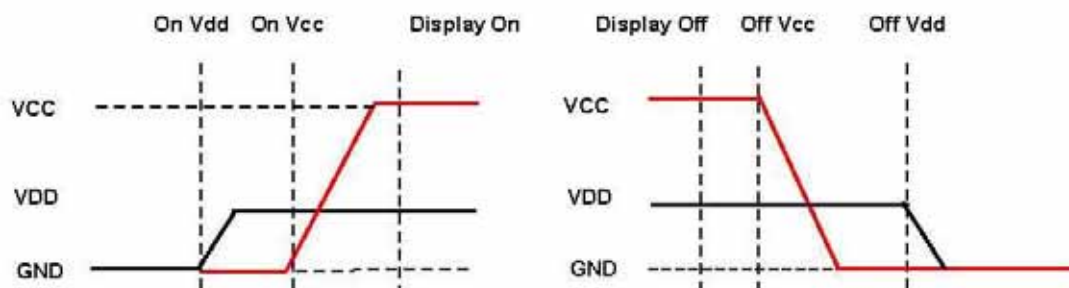
To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

Power up Sequence:

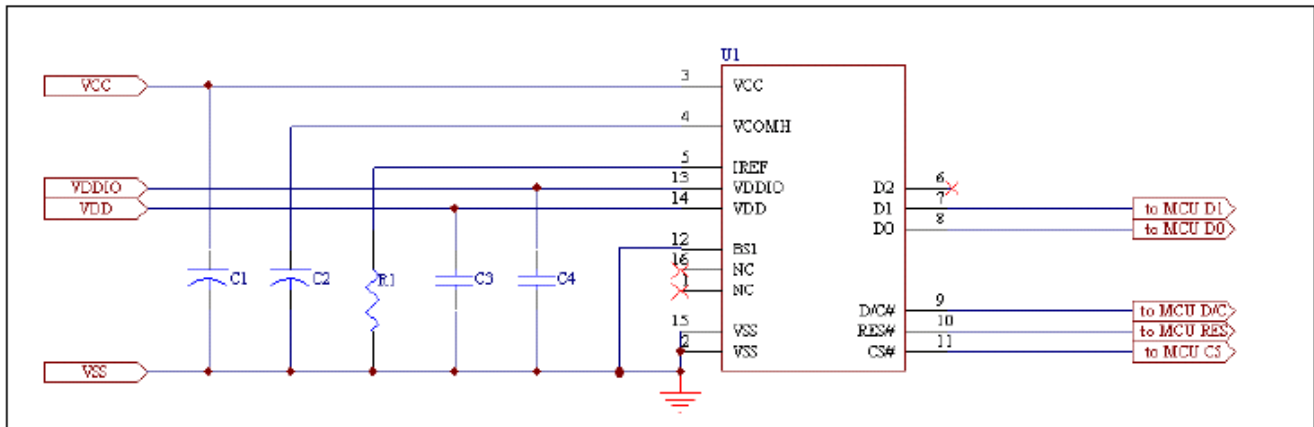
1. Power up Vdd
2. Hardware RESET
3. Send display off command
4. Power up Vcc
5. Delay 100ms (when Vcc is stable)
6. Send Display on command

Power down Sequence:

1. Send Display off command
2. Power down Vcc
3. Delay 100ms (When Vcc is reach 0 and panel is completely discharges)
4. Power down Vdd



10.2 Application circuit



VDDIO must always be equal or lower than VDD.

C1,C2: 4.7uF/25V (TANTALUM or Solid Tantalum 4.7uF/25V/A Case (Vishay 572D))

C3,C4: 4.7uF/25V

R1: 1M ohm/1% (0805)

11. Display Control Instruction

Command Table

(D/C#=0, R/W#(WR#)=0, E(RD#)=1) unless specific setting is stated)

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X ₃	X ₂	X ₁	X ₀	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A ₁	0 A ₀	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[7:0] B[7:0]	0 A ₇ B ₇	0 A ₆ B ₆	1 A ₅ B ₅	0 A ₄ B ₄	0 A ₃ B ₃	0 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-131d, (RESET=0d) B[7:0] : Column end address, range : 0-131d, (RESET=131d)
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A ₂ B ₂	1 A ₁ B ₁	0 A ₀ B ₀	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)
0	40~7F	0	1	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Set Display Start Line	Set display RAM display start line register from 0-63 using X ₅ X ₃ X ₂ X ₁ X ₀ . Display start line register is reset to 000000b during RESET.
0 0	81 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Contrast Control For BANK0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0 0	82 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Brightness For Area Color Banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0 0 0 0 0	91 X[5:0] A[5:0] B[5:0] C[5:0]	1 * * * *	0 * * * *	0 X ₅ A ₅ B ₅ C ₅	1 X ₄ A ₄ B ₄ C ₄	0 X ₃ A ₃ B ₃ C ₃	0 X ₂ A ₂ B ₂ C ₂	0 X ₁ A ₁ B ₁ C ₁	1 X ₀ A ₀ B ₀ C ₀	Set Look Up Table (LUT)	Set current drive pulse width of BANK0, Color A, B and C. BANK0: X[5:0] = 31... 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b) Color A: A[5:0] same as above (RESET = 111111b) Color B: B[5:0] same as above (RESET = 111111b) Color C: C[5:0] same as above (RESET = 111111b) Note (1) Color D pulse width is fixed at 64 clocks pulse.

Fundamental Command Table																	
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description						
0 0 0 0 0	92 A[7:0] B[7:0] C[7:0] D[7:0]	1 A ₇ B ₇ C ₇ D ₇	0 A ₆ B ₆ C ₆ D ₆	0 A ₅ B ₅ C ₅ D ₅	1 A ₄ B ₄ C ₄ D ₄	0 A ₃ B ₃ C ₃ D ₃	0 A ₂ B ₂ C ₂ D ₂	1 A ₁ B ₁ C ₁ D ₁	0 A ₀ B ₀ C ₀ D ₀	Set Bank Color of BANK1 to BANK16 (PAGE0)	Set the bank color of BANK1~BANK16 to any one of the 4 colors : A, B, C and D . A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK1 A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK2 : : D[5:4]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK15 D[7:6]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK16						
0 0 0 0 0	93 A[7:0] B[7:0] C[7:0] D[7:0]	1 A ₇ B ₇ C ₇ D ₇	0 A ₆ B ₆ C ₆ D ₆	0 A ₅ B ₅ C ₅ D ₅	1 A ₄ B ₄ C ₄ D ₄	0 A ₃ B ₃ C ₃ D ₃	0 A ₂ B ₂ C ₂ D ₂	1 A ₁ B ₁ C ₁ D ₁	1 A ₀ B ₀ C ₀ D ₀			Set Bank Color of BANK17~BANK32 (PAGE1)	Set the bank color of BANK17~BANK32 to any one of the 4 colors: A, B, C and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK17 A[3:2] : 00b, 01b, 10b, or 1b1 for Color = A, B, C or D of BANK18 : : D[5:4]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK31 D[7:6]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK32				
0 0 0 0 0	A0/A1	1	0	1	0	0	0	0	X ₀					Set Segment Re-map	X[0]=0b: column address 0 is mapped to SEG0 (RESET) X[0]=1b: column address 131 is mapped to SEG0		
0 0 0 0 0	A4/A5	1	0	1	0	0	1	0	X ₀							Entire Display ON	X ₀ =0b: Resume to RAM content display (RESET) Output follows RAM content X ₀ =1b: Entire display ON Output ignores RAM content
0 0 0 0 0	A6/A7	1	0	1	0	0	1	1	X ₀								
0 0 0 0 0	A8 A[5:0]	1 *	0 *	1 A ₅	0 A ₄	1 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 64MUX) A[5:0] from 0 to 14 are invalid entry.						
0 0 0 0 0	AA	1	0	1	0	1	0	1	0			Reserved	Reserved				
0 0 0 0 0	AB A[3:0] B[7:0] C[7:0]	1 * B ₇ C ₇	0 * B ₆ C ₆	1 * B ₅ C ₅	0 * B ₄ C ₄	1 A ₃ B ₃ C ₃	0 A ₂ B ₂ C ₂	1 A ₁ B ₁ C ₁	1 A ₀ B ₀ C ₀					Dim mode setting	A[3:0] : Reserved (set as 0000b) B [7:0] : Set contrast for BANK0, valid range 0-255d, please refer to command 81h C [7:0] : Set brightness for color bank, valid range 0-255d, please refer to command 82h		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	1 1	0 1	1 A ₀	Master Configuration	A[0]=0b, Select external V_{CC} supply (RESET) A[0]=1b, Select internal DC-DC voltage converter Note ⁽¹⁾ Refer to Section 8.11 for DC-DC converter details ⁽²⁾ The DC-DC converter must be enabled by the following command: ADh ; Master Configuration 8Fh ; Enable internal DC-DC AFh or ACh ; Display ON
0	AC AE AF	1	0	1	0	1	1	A ₁	A ₀	Set Display ON/OFF	ACh = Display ON in dim mode A Eh = Display OFF (sleep mode) (RESET) AFh = Display ON in normal mode
0	B0~B7	1	0	1	1	0	X ₂	X ₁	X ₀	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].
0	C0/C8	1	1	0	0	X ₃	0	0	0	Set COM Output Scan Direction	X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N-1] X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Display Offset	Set vertical shift by COM from 0~63. The value is reset to 00h after RESET.
0	D5 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b Range:0000b~1111b Frequency increases as setting value increases. Refer to section 10.1.23 for details.
0 0	D8	1 0	1 0	0 X ₅	1 X ₄	1 0	0 X ₂	0 0	0 X ₀	Set Area Color Mode ON/OFF & Low Power Display Mode	X[5:4]= 00b (RESET) : monochrome mode X[5:4]= 11b Area Color enable X[2]=0b and X[0]=0b: Normal power mode(RESET) X[2]=1b and X[0]=1b: Set low power display mode
0 0	D9 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	1 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry A[7:4] : Phase 2 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description												
00	DA	1	1	0	1	1	0	1	0	Set COM Pins Hardware Configuration	X[4]=0b, Sequential COM pin configuration X[4]=1b(RESET), Alternative COM pin configuration X[5]=0b(RESET), Disable COM Left/Right remap X[5]=1b, Enable COM Left/Right remap Please refer to Table 10-3 for details.												
00		0	0	X ₅	X ₄	0	0	1	0														
00	DB A[5:2]	1	1	0	1	1	0	1	1	Set V _{COMH} Deselect Level	<table><tr><th>A[5:2]</th><th>Hex code</th><th>V_{COMH} deselect level</th></tr><tr><td>000b</td><td>00h</td><td>~ 0.43 x V_{CC}</td></tr><tr><td>1101b</td><td>34h</td><td>~ 0.77 x V_{CC} (RESET)</td></tr><tr><td>1111b</td><td>3Ch</td><td>~ 0.83 x V_{CC}</td></tr></table>	A[5:2]	Hex code	V _{COMH} deselect level	000b	00h	~ 0.43 x V _{CC}	1101b	34h	~ 0.77 x V _{CC} (RESET)	1111b	3Ch	~ 0.83 x V _{CC}
A[5:2]	Hex code	V _{COMH} deselect level																					
000b	00h	~ 0.43 x V _{CC}																					
1101b	34h	~ 0.77 x V _{CC} (RESET)																					
1111b	3Ch	~ 0.83 x V _{CC}																					
00	E0	1	1	1	0	0	0	0	0	Enter Read Modify Write	Enter the Read Modify Write mode. Details please refer to section 10.1.28.												
00	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation												
00	EE	1	1	1	0	1	1	1	0	Exit Read Modify Write	Exit the Read Modify Write mode (Please refer to command E0h)												

Graphic Acceleration Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																										
0	26/27	0	0	1	0	0	1	1	X ₀	Horizontal Scroll Setup	X[0]=0, Right Horizontal Scroll X[0]=1, Left Horizontal Scroll A[2:0] : Set number of column scroll offset 000b No horizontal scroll 001b Horizontal scroll by 1 column 010b Horizontal scroll by 2 columns 011b Horizontal scroll by 3 columns 100b Horizontal scroll by 4 columns Other values are invalid. B[2:0] : Define start page address <table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table> C[2:0] : Set time interval between each scroll step in terms of frame frequency <table><tr><td>000b – 6 frames</td><td>100b – 3 frames</td></tr><tr><td>001b – 32 frames</td><td>101b – 4 frames</td></tr><tr><td>010b – 64 frames</td><td>110b – 2 frame</td></tr><tr><td>011b – 128 frames</td><td>111b – Invalid</td></tr></table> D[2:0] : Define end page address <table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table> The value of D[2:0] must be larger or equal to B[2:0]	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5		000b – 6 frames	100b – 3 frames	001b – 32 frames	101b – 4 frames	010b – 64 frames	110b – 2 frame	011b – 128 frames	111b – Invalid	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																																			
001b – PAGE1	100b – PAGE4	111b – PAGE7																																			
010b – PAGE2	101b – PAGE5																																				
000b – 6 frames	100b – 3 frames																																				
001b – 32 frames	101b – 4 frames																																				
010b – 64 frames	110b – 2 frame																																				
011b – 128 frames	111b – Invalid																																				
000b – PAGE0	011b – PAGE3	110b – PAGE6																																			
001b – PAGE1	100b – PAGE4	111b – PAGE7																																			
010b – PAGE2	101b – PAGE5																																				
0	A[2:0]	*	*	*	*	*	A ₂	A ₁	A ₀																												
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀																												
0	C[2:0]	*	*	*	*	*	C ₂	C ₁	C ₀																												
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀																												
0	29/2A	0	0	1	0	1	0	X ₁	X ₀	Continuous Vertical and Horizontal Scroll Setup	X ₁ X ₀ =01b : Vertical and Right Horizontal Scroll X ₁ X ₀ =10b : Vertical and Left Horizontal Scroll A[2:0] : Set number of column scroll offset 000b No horizontal scroll 001b Horizontal scroll by 1 column 010b Horizontal scroll by 2 columns 011b Horizontal scroll by 3 columns 100b Horizontal scroll by 4 columns Other values are invalid. B[2:0] : Define start page address <table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table> C[2:0] : Set time interval between each scroll step in terms of frame frequency <table><tr><td>000b – 6 frames</td><td>100b – 3 frames</td></tr><tr><td>001b – 32 frames</td><td>101b – 4 frames</td></tr><tr><td>010b – 64 frames</td><td>110b – 2 frame</td></tr><tr><td>011b – 128 frames</td><td>111b – Invalid</td></tr></table> D[2:0] : Define end page address <table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table> The value of D[2:0] must be larger or equal to B[2:0] E[5:0] : Vertical scrolling offset e.g. E[5:0]=01h refer to offset =1 row E[5:0]=3Fh refer to offset =63 rows	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5		000b – 6 frames	100b – 3 frames	001b – 32 frames	101b – 4 frames	010b – 64 frames	110b – 2 frame	011b – 128 frames	111b – Invalid	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																																			
001b – PAGE1	100b – PAGE4	111b – PAGE7																																			
010b – PAGE2	101b – PAGE5																																				
000b – 6 frames	100b – 3 frames																																				
001b – 32 frames	101b – 4 frames																																				
010b – 64 frames	110b – 2 frame																																				
011b – 128 frames	111b – Invalid																																				
000b – PAGE0	011b – PAGE3	110b – PAGE6																																			
001b – PAGE1	100b – PAGE4	111b – PAGE7																																			
010b – PAGE2	101b – PAGE5																																				
0	A[2:0]	*	*	*	*	*	A ₂	A ₁	A ₀																												
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀																												
0	C[2:0]	*	*	*	*	*	C ₂	C ₁	C ₀																												
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀																												
0	E[5:0]	*	*	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀																												

Graphic Acceleration Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. Note (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 * B ₆	1 A ₅ B ₅	0 A ₄ B ₄	0 A ₃ B ₃	0 A ₂ B ₂	1 A ₁ B ₁	1 A ₀ B ₀	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] Note (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line (X5X4X3X2X1X0 of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls Please refer to Figure 10-14 for details.

Read Command Table

Bit Pattern	Command	Description
D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Status Register Read	D[7] : Reserve D[6] : “1” for display OFF / “0” for display ON D[5] : Reserve D[4] : Reserve D[3] : Reserve D[2] : Reserve D[1] : Reserve D[0] : Reserve

Note

(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

12. Reliability

■ Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	—
2	High temp. (Operation)	70°C, 120hrs	—
3	Low temp. (Operation)	-40°C, 120hrs	—
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	—
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	—
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	—
7	Drop	Height: 120cm Sequence : 1 angle、 3 edges and faces Cycles: 1	—
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	—

