Evaluation Board for 16 Bit, 195kSPS Σ-Δ ADC

EVAL-AD7722CB

FEATURES

Full-Featured Evaluation Board for the AD7722
EVAL-CONTROL BOARD Compatible
Stand Alone Capability
Versatile Analog Signal Conditioning Circuit
Flexible Power & Grounding Configurations
On-Board 2.5V Reference
Crystal or CMOS Clock Oscillator Sampling Clock
Serial or Parallel Conversion Data Interface
PC Software for Control and Data Analysis when used with EVAL-CONTROL BOARD

INTRODUCTION

This Technical Note describes the evaluation board for the AD7722. The AD7722 is a complete low power, 16-bit, sigma-delta ADC. The part operates from a +5V supply and accepts a differential input voltage range of 0V to +2.5V or ±1.25V centered around a common mode bias. Full data on the AD7722 is available in the AD7722 data sheet available from Analog Devices. The data sheet should be consulted in conjunction with this Technical Note when using the Evaluation Board.

On-board components include an AD780 precision bandgap voltage reference, an opamp, OP184, used to buffer the reference voltage, a dual op-amp, OP275, used to condition the analog input and configure it to drive the AD7722 with single-ended or complimentary input signals. An on-board CMOS clock oscillator is also provided. The EVAL-AD7722CB can be configured for serial or parallel mode of operation. In parallel mode, a 16-bit register, 74FCT16374, latches the conversion results to a 40-pin IDC connector and to the 96-way DIN connector. In serial mode, the AD7722's serial interface signals are buffered with a 74FCT162244 and are available from a 20-pin header.

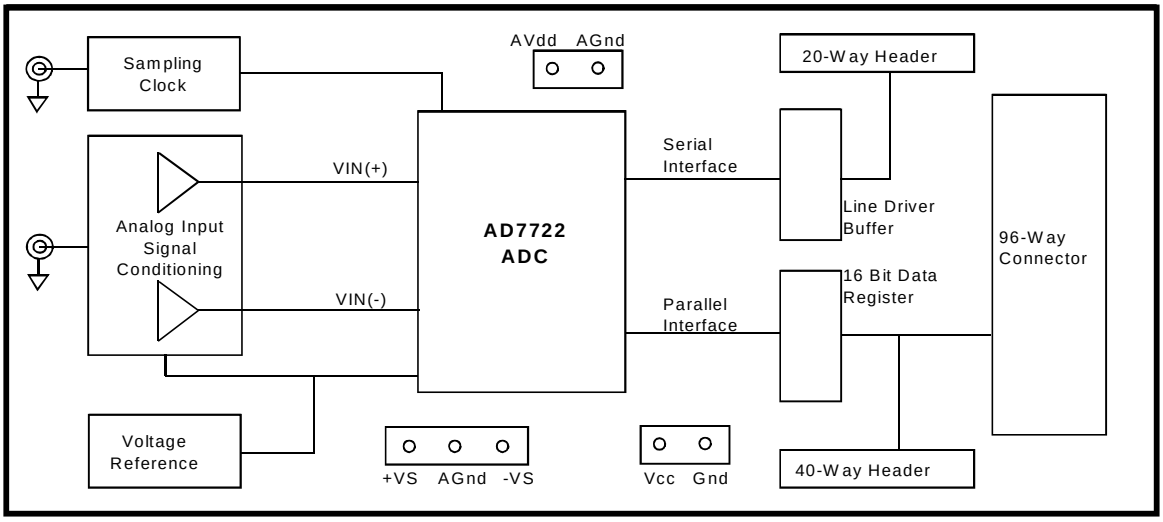
Power Supplies

When using this evaluation board with the Eval-Control Board all supplies are provided from the Eval-Control Board through the 96-way connector.

When using the board as a stand alone unit external supplies must be provided. This evaluation board has seven power supply inputs: AV_{DD}, A_{GND}, +VS, -VS, A_{GND}, V_{CC} and D_{GND}. +5V must be connected to the AVDD (P1) input to supply the AD7722 AV_{DD} pin and the AD7722 DV_{DD} pin (via a ferrite bead and 10Ω resistor), the AD780 voltage reference, the OP184 op-amp and the CMOS clock oscillator circuit. +5V and -5V are connected to the +VS and -VS inputs to supply the OP275 dual op-amp. 0V is connected to one or both of the A_{GND} inputs. The V_{CC} input is used to supply a separate +5V for the digital buffer circuitry and the D_{GND} input must be tied to 0V. The supplies are decoupled to the relevant ground plane with 22µF tantalum and 0.1µF multilayer ceramic capacitors at the point where they enter the board. The supply pins of the op-amps and voltage reference are also decoupled to A_{GND} with 10µF tantalum and a 0.1µF ceramic capacitor. The AD7722 AV_{DD} and DV_{DD} supply pins are decoupled to A_{GND} with 10µF tantalum and 0.1µF multilayer ceramic capacitors.

Extensive ground planes are used on this board to minimize the effect of high frequency noise interference. There are two ground planes, A_{GND} and D_{GND}. These are connected together using JP11.

Figure 1. FUNCTIONAL BLOCK DIAGRAM



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LINK AND SWITCH OPTIONS

There are 33 link options which must be set for the required operating setup before using the evaluation board. The functions of these options are outlined below.

Link No.	Function.
JP1	Selects between an external +VS connected to P3 or the +5V supply from the Eval-Control Board. When this link is in place, +VS is supplied by the Eval-Control Board. When this link is removed, +VS must be supplied from an external source via P3.
JP2	Selects the source of the AV_{DD} power plane When this link is in position "A", the AV_{DD} power plane is supplied from an external source via P1. When this link is in position "B", the AV_{DD} power plane is supplied from the Eval-Control Board.
JP3	Selects between an external -VS connected to P3 or the -5V supply from the Eval-Control Board. When this link is in place, -VS is supplied by the Eval-Control Board. When this link is removed, -VS must be supplied from an external source via P3.
JP4 JP7 JP9	These three jumpers allow the analog inputs of the AD7722 to be configured in bipolar mode for complementary or single ended drive. To create complementary signals, place these links in position "A" and leave the R6 position empty. In this mode a 1.25 Vp-p signal source, centered about ground, creates a ±1.25V full scale differential input. To select single ended drive configuration, place these links in position "B", remove R3 and place it in the open position for R6. In this mode, the IN(-) input is biased to 1.25V and a 2.5 Vp-p signal source, centered about ground, creates a ±1.25V full scale differential input.
JP5	This jumper allows a single power supply to power the analog signal conditioning amplifier, U8. When JP5 is inserted the V- supply pin of U8 is connected to A_{GND}. In this case ensure that JP3 is not inserted and that the V- input of P3 is open.
JP6 JP8 JP13 JP14	These link options allow operation with either the AD7722's internal reference or the external on-board AD780 reference. To select the AD7722 internal reference, remove JP13 & JP14 and place both JP6 & JP8 in position "A". To select the external AD780 reference, insert JP13 & JP14, place JP6 in position "B" and remove JP8.
JP10 JP12 JP15	These three jumpers select how an external clock source is applied to the CLKIN pin of the AD7722. See circuit diagram on page 9 for details.
JP11	This is used to connect the analog and digital ground planes. When using the Eval-Control Board to power the evaluation board, this jumper should be inserted. Otherwise it can be removed.
JP17	Place this jumper in position "B", so that the CAL pulse width is two CLKIN cycles wide.
JP19 - JP27	In serial mode these jumpers are inserted to connect the unused digital pins to ground. They must be removed in parallel mode operation.
JP28 JP29	These two jumpers are used in parallel mode operation to select how the conversion data is latched into the 16-bit data register, U9. When the shunt is installed in JP28, conversion results are latched on the falling edge of the $\overline{DRDY}$ output. When the shunt is installed in JP29, results are latched on the rising edge of the $\overline{DRDY}$ output. In serial mode this shunt should be removed.
JP30	This selects the digital power source for the board's digital interface circuitry. When using the Eval-Control Board this jumper is inserted thus supplying power from the Eval-Control Board. Remove the jumper to supply power from an external +5V source via the terminal block, P3.
JP31 - JP34	In serial mode these 4 jumpers set the logic level for the four control inputs SFMT, DOE, TSI and CFMT respectively. Place the relevant jumper in position "A" for a high logic level, and place it in position "B" for a low logic level. In parallel mode these jumpers have no effect on the operation of the board.
JP35	This jumper selects either serial or parallel mode of operation. Insert the jumper in position "A" for parallel mode and in position "B" for serial mode. If JP35 is set for parallel mode (position "A"), ensure that jumpers JP19-27 are unconnected.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. Table I shows the position in which all the links are set when the evaluation board is packaged.

Table I. Initial Link and Switch Positions

Link No.	Position	Function.
JP1	Inserted	+VS is supplied from the Eval-Control Board.
JP2	B	AV_{DD} power plane is supplied from the Eval-Control Board.
JP3	Inserted	-VS is supplied from the Eval-Control Board.
JP4 JP7 JP9	A	Analog input circuit configured to create complementary analog input signals.
JP5	Removed	The analog signal condition amplifier is set for dual power supply operation.
JP6 JP8 JP13 JP14	JP6-B JP8-Removed JP13-Inserted JP14-Inserted	Operation of the evaluation board with the external on-board AD780 voltage reference is selected.
JP10 JP12 JP15	JP10-A. JP12-B JP15-A	The on-board 25MHz CMOS clock oscillator provides the clock source. The 25MHz clock is divided by two to supply 12.5MHz to the AD7722.
JP11	Inserted	The analog and digital ground planes are connected at this point.
JP17	B	The pulse width of the CAL input signal is set to two CLKIN cycles in duration.
JP19 - JP27	Removed	As the board is set for parallel mode, these jumpers must be left unconnected.
JP28 JP29	JP28-Removed JP29-Inserted	Conversion results are latched on the rising edge of the $\overline{DRDY}$ output.
JP30	Inserted	The Eval-Control Board supplies the power for the board's digital interface circuitry.
JP31 - JP34	A	As the board is set for parallel operation, these jumper options have no effect on it's operation.
JP35	A	Board is set for parallel mode operation.

EVALUATION BOARD INTERFACING

Serial Interface

In serial mode operation, the AD7722 serial interface signals are buffered with a 74FCT162244 (U11) and are available at the 20-way header, P5. The pin functions of this header are listed in Table II.

Table II. Serial Header Interface(P5) Pin Functions

Pin Number	Function	Description
1,3,5,7,9,11	Ground	Tied to DGND
13,15,17,19	Ground	Tied to DGND
2	SCO	Serial Data Clock Output
4	SDO	Serial Data Output
6	FSO	Frame Sync. Output
8	FSI	Frame Sync. Logic Input
10	DVAL	Data Valid Logic Output
12	$\overline{CS}$	Chip Select
14	$\overline{UNI}$	Analog Input Range Select Input
16	P/$\overline{S}$	Parallel/Serial Interface Select input
18, 20	-	Unconnected

NB. Refer to the Data Sheet for more detailed information.

Parallel Interface

In parallel mode operation, a 16-bit 74FCT162374 register (U16) latches the conversion results to a 40-pin IDC connector and to a 96-pin DIN connector. The 40-pin IDC connector is used for external parallel interfacing to the board (see table III for pin functions). The 96-pin DIN connector is used to interface to the Eval-Control Board.

Table III. 40-Pin Parallel Interface(P4) Pin Functions

Pin Number	Function	Description
2,4,6, ... 40	Ground	Tied to DGND
1,3,5, ... 31	D15,D14,D13, ... D0	16-Bit Data Bus
33	$\overline{IRQ2}$	Data Ready Output
35,37,39	-	Unconnected

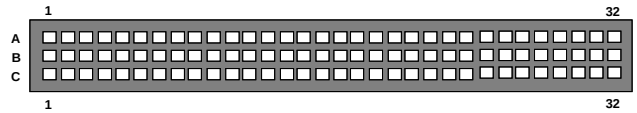

Figure 2. Pin Configuration for the 96-Way Connector, J1

Table IV. 96-Way Connector Pin Description

D0-D15 Data Bit 0 to Data Bit 15. 16-bit Data Bus.

$\overline{CS}$ Chip Select. A level sensitive logic input.

$\overline{IRQ2}$ Interupt Request 2. Connected to the AD7722 DRDY output pin via 2 inverting buffers.

+5V +5V supply. Used as power supply for digital interface circuitry.

DGND Digital Ground. Connected to the digital ground plane on the evaluation board.

AGND Analog Ground. These lines are connected to the analog ground plane on the evaluation board.

AVSS Analog -5V Supply. Used to supply the negative power pin of the analog input conditioning opamp.

AVDD Analog +5V Supply. Used to supply the AV_{DD} power plane and the positive power pin of the analog input conditioning opamp.

Table V. 96-Way Connector Pin Functions.

	RowA	RowB	RowC
1			
2		D0	
3		D1	
4	DGND	DGND	DGND
5		D2	
6		D3	
7		D4	
8	+5V	+5V	+5V
9		D5	
10		D6	$\overline{CS}$
11		D7	
12	DGND	DGND	DGND
13		D8	
14		D9	
15		D10	
16	DGND	DGND	DGND
17		D11	$\overline{IRQ2}$
18	D12	D13	D14
19			D15
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29	AGND	AGND	AGND
30		AGND	
31	AVSS	AVSS	AVSS
32	AVDD	AVDD	AVDD

SOCKETS

There are two input sockets relevant to the operation of the AD7722 on this evaluation board. The function of these sockets is outlined in Table VI.

Table VI. Socket Functions

Socket	Function
J1	BNC Socket for the analog input signal.
J2	BNC Socket for external CLKIN input.

CONNECTORS

There are six connectors on the AD7722 evaluation board as outlined in Table VII.

Table VII. Connector Functions

Connector	Function
P1	External AV_{DD} & A_{GND} power connector.
P2	External V_{CC} & D_{GND} power connector for digital interface circuitry.
P3	External -VS, A_{GND} & +VS power connector for analog input conditioning op-amp.
P4	40-pin IDC connector for Parallel Interface.
P5	20-pin header for Serial Interface.
P6	96-Way Connector for interface to Eval-Control Board.

Using a 50Ω Analog Signal Source.

If the user is using a 50Ω signal source to generate the analog input signal, a slight modification will be required in the analog front-end circuitry to avoid causing the analog input signal to become offset. If the analog input configuration op-amp, U8, is configured to create complementary signals then R3 must be changed from 499Ω to 449Ω. If the analog input configuration op-amp, U8, is configured to create single ended signals then R2 must be changed from 499Ω to 449Ω. Both of these modifications are required to create analog signals that span the full input range of the AD7722 ADC.

OPERATING WITH THE EVAL-CONTROL BOARD

The evaluation board can be operated in a stand-alone mode or operated in conjunction with the Eval-Control Board (in parallel mode only). This Eval-Control Board is available from Analog Devices under the order entry "EVAL-CONTROL BOARD". When operated with this control board, all supplies and control signals to operate the AD7722 are provided by theEval-Control Board when it is run under control of the AD7722 software which is provided with the AD7722 evaluation board package. This Eval-Control Board will also operate with all Analog Devices evaluation boards which end with the letters CB in their title.

The 96-way connector on the EVAL-AD7722CB plugs directly into the 96-way connector on the Eval-Control Board. No power supplies are required in the system. The Eval-Control Board generates all the required supplies for itself and the EVAL-AD7722CB. The Eval-Control Board is powered from a 12V ac transformer. This is a standard 12V ac transformer capable of supplying 1A current and is available as an accessory from Analog Devices under the following part numbers:

EVAL-110VAC-US:	For use in the U.S. or Japan
EVAL-220VAC-UK:	For use in the U.K.
EVAL-220VAC-EU:	For use in Europe

These transformers are also available for other suppliers including Digikey (U.S.) and Campbell Collins (U.K.).

Connection between the Eval-Control Board and the serial port of a PC is via a standard RS-232 cable which is provided as part of the Eval-Control Board package. Please refer to the manual which accompanies the Eval-Control Board for more details on the Eval-Control Board package.

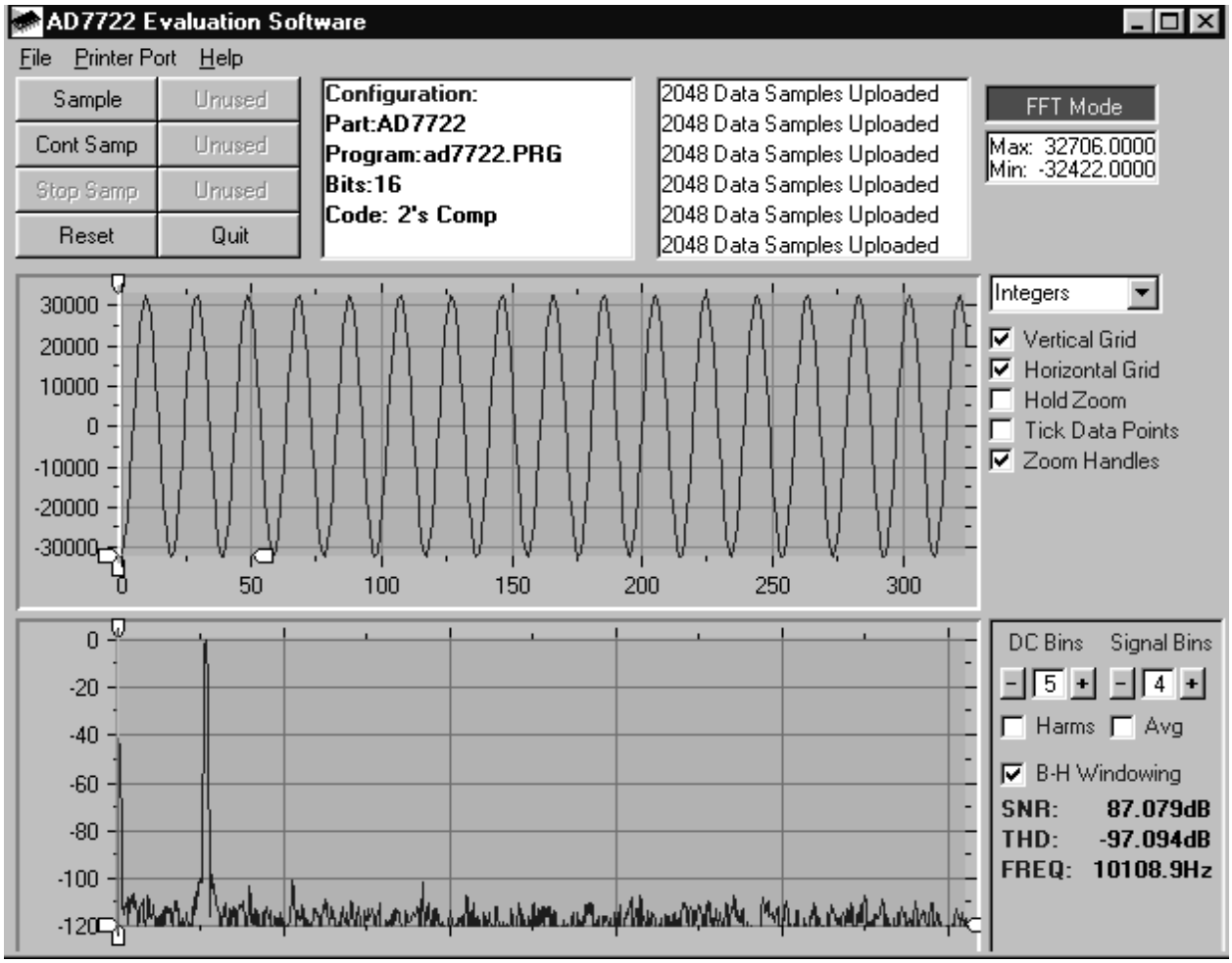

Figure 3. Main Screen - FFT Mode

SOFTWARE DESCRIPTION

The software which controls the Eval-Control Board and hence the AD7722 evaluation board has three main screens. The screen shown in Figure 3 is the screen which appears when the software is run. The main function of this screen is to allow the user to read a predetermined number of samples from the AD7722 evaluation board and display them in both the time and frequency domain. The screen can be divided into three sections. The upper third of the screen contains the control buttons, the menu bar and various status windows. The control buttons allow the user to take samples, reset the part and quit the program. The menu bar allows the user to enter the setup menu, select which printer port is being used to control the Eval-Control Board, load and save samples, get information about the software etc. The status windows indicate the setup of the AD7722 evaluation board/ device, number of samples taken, and any information/error messages that are generated.

The middle third of the screen is a Digital Storage Oscilloscope (DSO). When samples are uploaded from the Eval-Control Board, they are displayed here. The samples can be displayed as either integer values or as voltages. Once samples have been displayed, clicking at any point in the graph will display the sample number and the value of the point directly beneath the cursor. Along the axis of the graph are the **Zoom Handles**. These allow the user to zoom in and out to get a closer look at a particular sample if required. When another set of samples is taken, the graph will attempt to display all values collected unless the **Hold Zoom** check box is ticked. In this case, the graph will keep the same axis settings as for the previous set of data samples. Additional check boxes are provided to give the user control over the vertical and horizontal grids and data points.

The lower third of the screen will show either a Fast Fourier Transform (FFT) of the data or a Histogram which shows the number of occurrences of each particular code read back. The FFT (the default option) is typically used when the user is concerned with examining an ADC's performance in the frequency domain. When performing a Fourier Transform, the data can be windowed by a Blackman-Harris window before the transform by clicking the B-H box. When the B-H box is not clicked on, the data is not windowed. The Histogram will give an indication of the ADC's performance to DC signals. The option displayed can be toggled by clicking on the FFT Mode/Histogram Mode button in the top right of the screen. Figure 4 shows how the main screen looks when the Histogram option is selected.

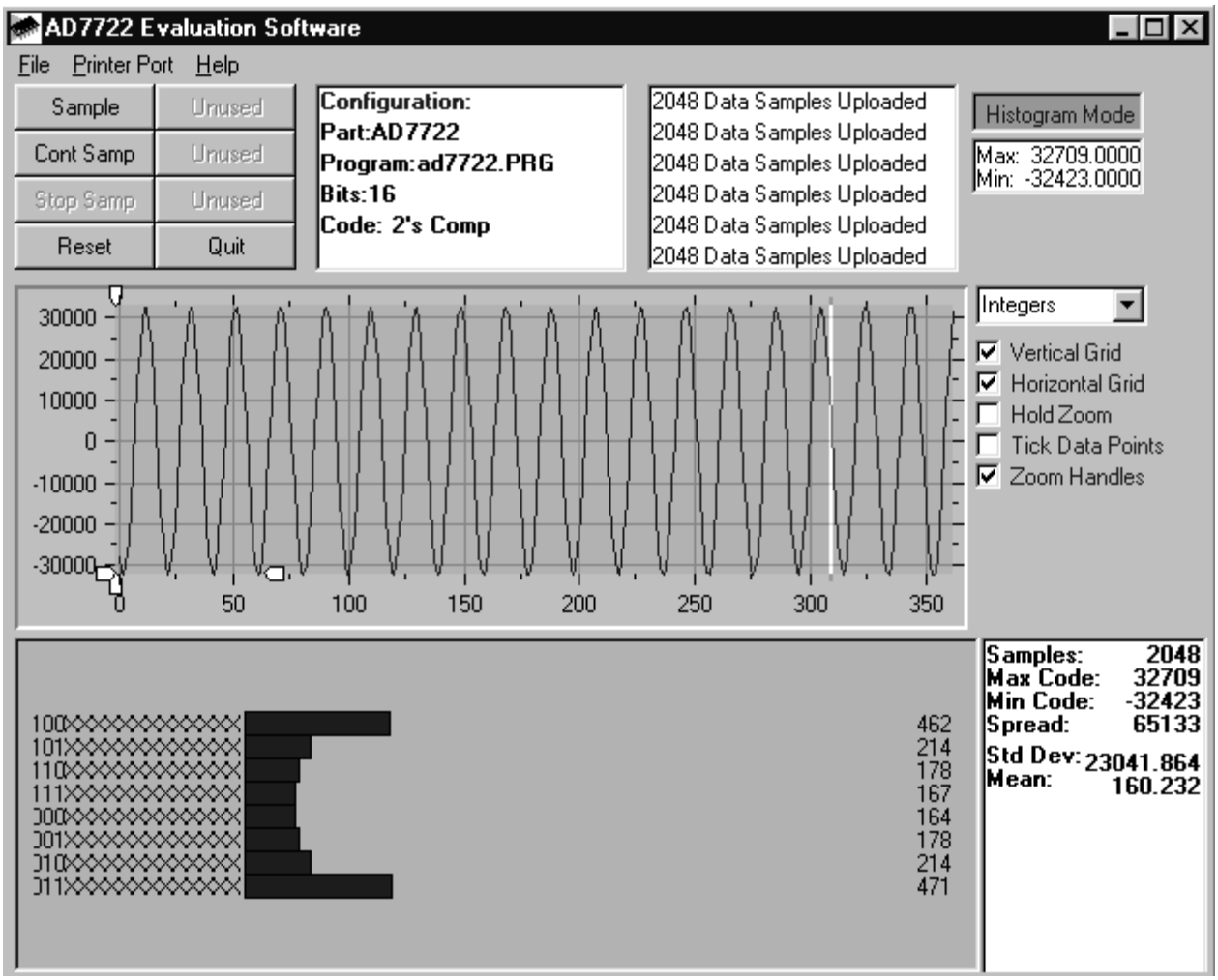

Figure 4. Main Screen - Histogram Mode

SETUP SCREEN

The Setup Screen is responsible for allowing the user to load a configuration file for the evaluation board. The configuration file will give the software detailed information about the evaluation board and the part connected to the Eval-Control Board such as number of bits, maximum sampling rate, power supply requirements, etc. The configuration file also tells the software the name of the DSP program file which it should download to the Eval-Control Board. These files are supplied by Analog Devices with the evaluation board. Figure 5 shows the setup screen. For the AD7722 evaluation board, the configuration file is called ad7722.cfg.

SETTING UP THE EVAL-CONTROL BOARD

The Eval-Control Board and AD7722 evaluation board should be connected together via the 96-way connector. The power should be applied to the Eval-Control Board. At this stage, the red LED should be flashing which indicates that the Eval-Control Board is functional and ready to receive instructions. The software which should have been installed should be loaded before the printer port cable is connected between the Eval-Control Board and the PC. This will ensure that the printer port has been initialized properly. The printer port cable can then be connected between the PC and the Eval-Control Board.

RUNNING THE SOFTWARE

With the hardware setup, the user is ready to use the AD7722 evaluation board with the Eval-Control Board. In the software, the user should select the **File** menu and click on **Setup**. This will display the setup form. A window on the left of the setup form lists all the available configuration files. The configuration file is a text based file which contains information about the AD7722 evaluation board such as part name, number of samples to be taken, default and maximum sampling frequency power supply settings, etc. The configuration file also contains the name of the DSP program file which is to be downloaded to the Eval-Control Board. The user should select the configuration file and click **Load**. The Eval-Control Board will be reset and the DSP program will be downloaded. During the download, the power supply settings indicated in the configuration file are set and the user may hear some relays clicking. The pulldown menu items such as 'number of samples' and 'sampling frequency' will have been set to the default values specified by the configuration file. The user is free to change these at will. Once the settings have been decided, the user can click **Close** to return to the main form.

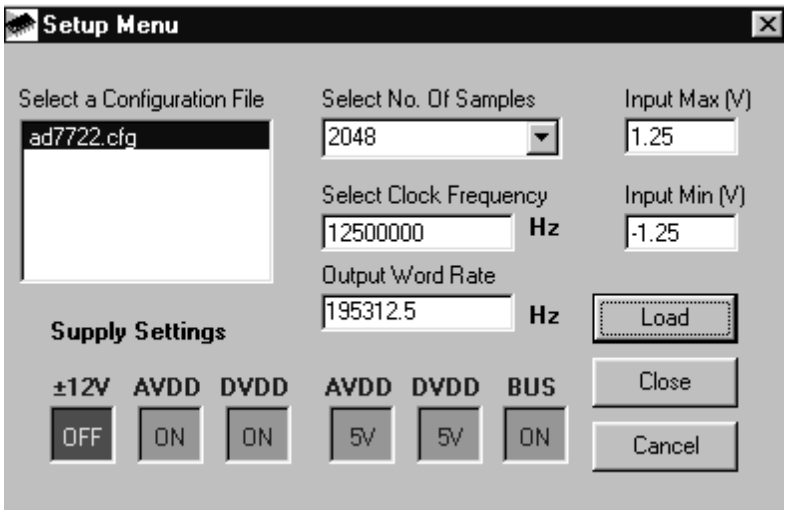

Figure 5. Setup Menu Screen

TAKING SAMPLES

When the user clicks **Sample**, the software will instruct the Eval-Control Board to take the required number of samples at the required frequency from the AD7722 evaluation board. These samples are then uploaded and displayed. An FFT and Histogram are also calculated and displayed. If the user clicks **Cont Samp**, the software will repeat the process indefinitely until the user clicks **Stop Samp**. While the software is continuously sampling data, the other control buttons are disabled.

OTHER BUTTONS

The **Reset** button will cause the Eval-Control Board to perform a reset function. When this occurs, the power supplies are turned off and the program in DSP memory is lost. The user should repeat the setup instructions to download another configuration file, if required.

The **Quit** button will exit the software. The program running on the Eval-Control Board is not terminated.

MENU BAR ITEMS

The main screen of the program contains a number of options available as pulldown menu items. The functions of these are listed below.

File Menu

Setup Menu: Selecting this option displays the Setup Screen as shown in Figure 5.

Load Raw Data: Selecting this option allows the user to load data which has been saved by the software during a previous session.

Save Raw Data: Selecting this option allows the user to save the current set of sample data points. The data can be reloaded to the Eval-Control Board software at a later date or can be used by other programs for further analysis.

Save Binary Data: Selecting this option allows the user to save the current set of sample data points. The data is saved in binary format as a text file. This method can be useful for examining code flicker, looking for stuck bits, etc.

Save FFT Data: Selecting this option allows the user to save the current set of FFT data points. FFT data cannot be reloaded into the Eval-Control Board software but can be loaded into other software packages for further analysis.

Exit: Quits the program.

Printer Port

This menu item allows the user to select which printer port should be used for communication with the Eval-Control Board.

LPT1: This option selects 0x378 as the printer port address. This is the default option.

LPT2: This option selects 0x278 as the printer port address.

PRN: This option selects 0x3BC as the printer port address.

Help:

This menu item gives information about the current revision of software for the AD7722 evaluation board being used.

SOFTWARE CONFIGURATION FILE

The software configuration file gives the Eval-Control Board software information on how the software and hardware should perform. It contains information such as the name of the DSP program to be downloaded, the default and maximum sample frequencies, the number of samples to take and the power supply settings to use. A typical Software Configuration file (*.cfg) is shown in Listing 1.

```
[EVAL-CONTROL BOARD]
partname:AD7722
programname:ad7722.PRG

clockfrequency:12500000
samples:2048


+/-15V:off
dvdd:5:on
avdd:5:on
bus:on
;options 2scomp, binary
dataformat:2scomp
numberofbits:16
inputVmax:1.25
inputVmin:-1.25
[endofcfg]
```

Listing 1. Software configuration File.

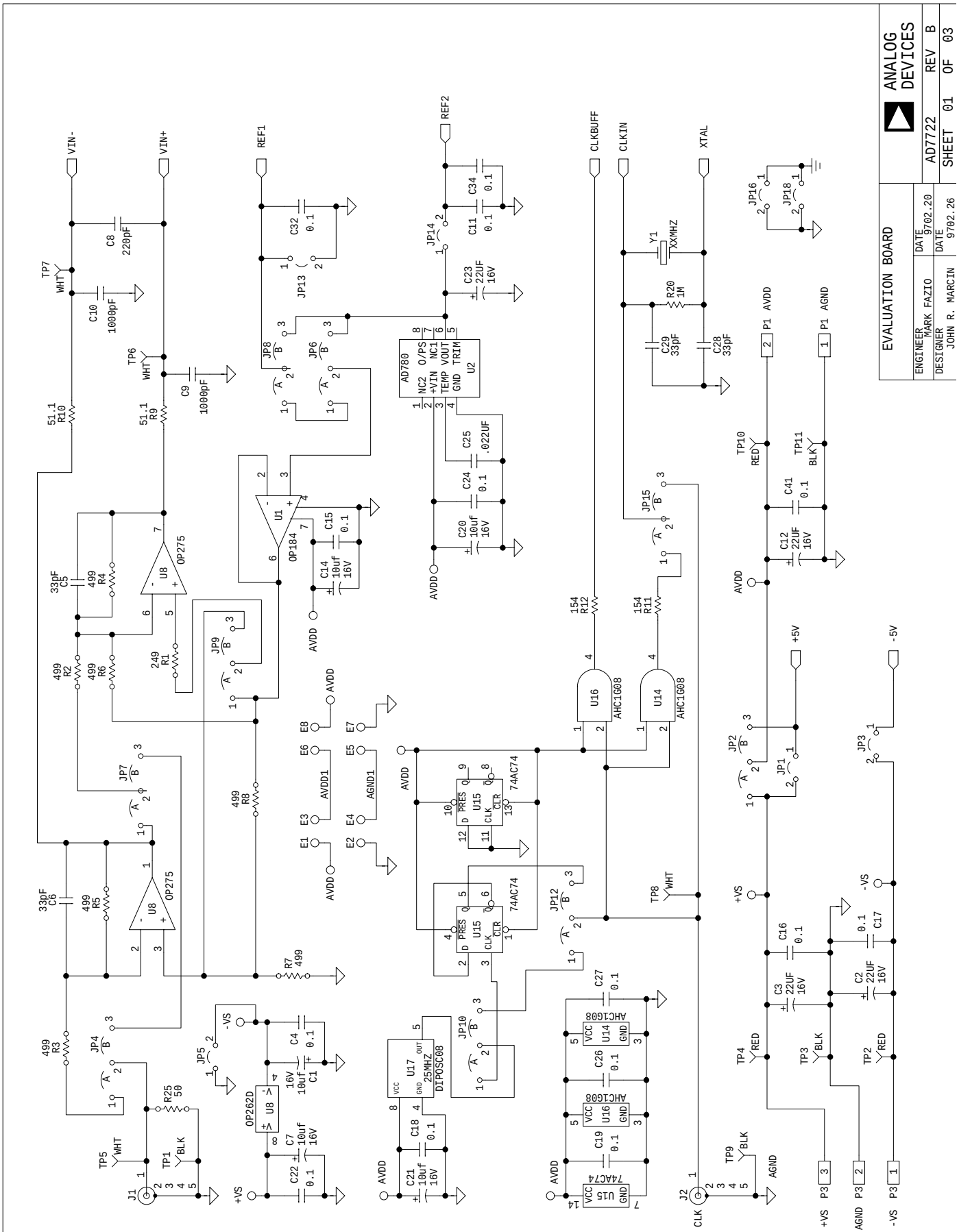

Figure 6. AD7722 Evaluation Board Schematic Sheet 1.

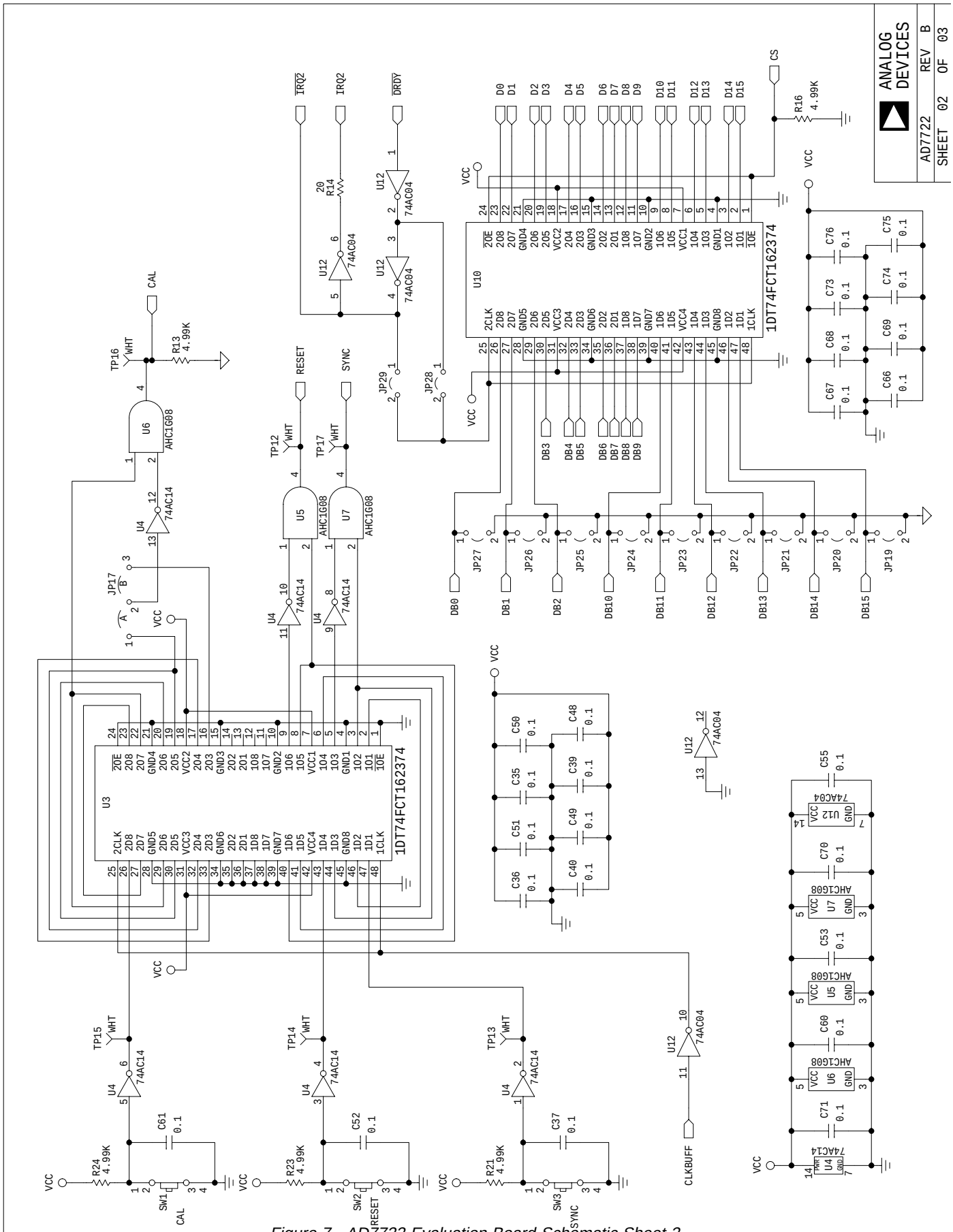

Figure 7. AD7722 Evaluation Board Schematic Sheet 2.

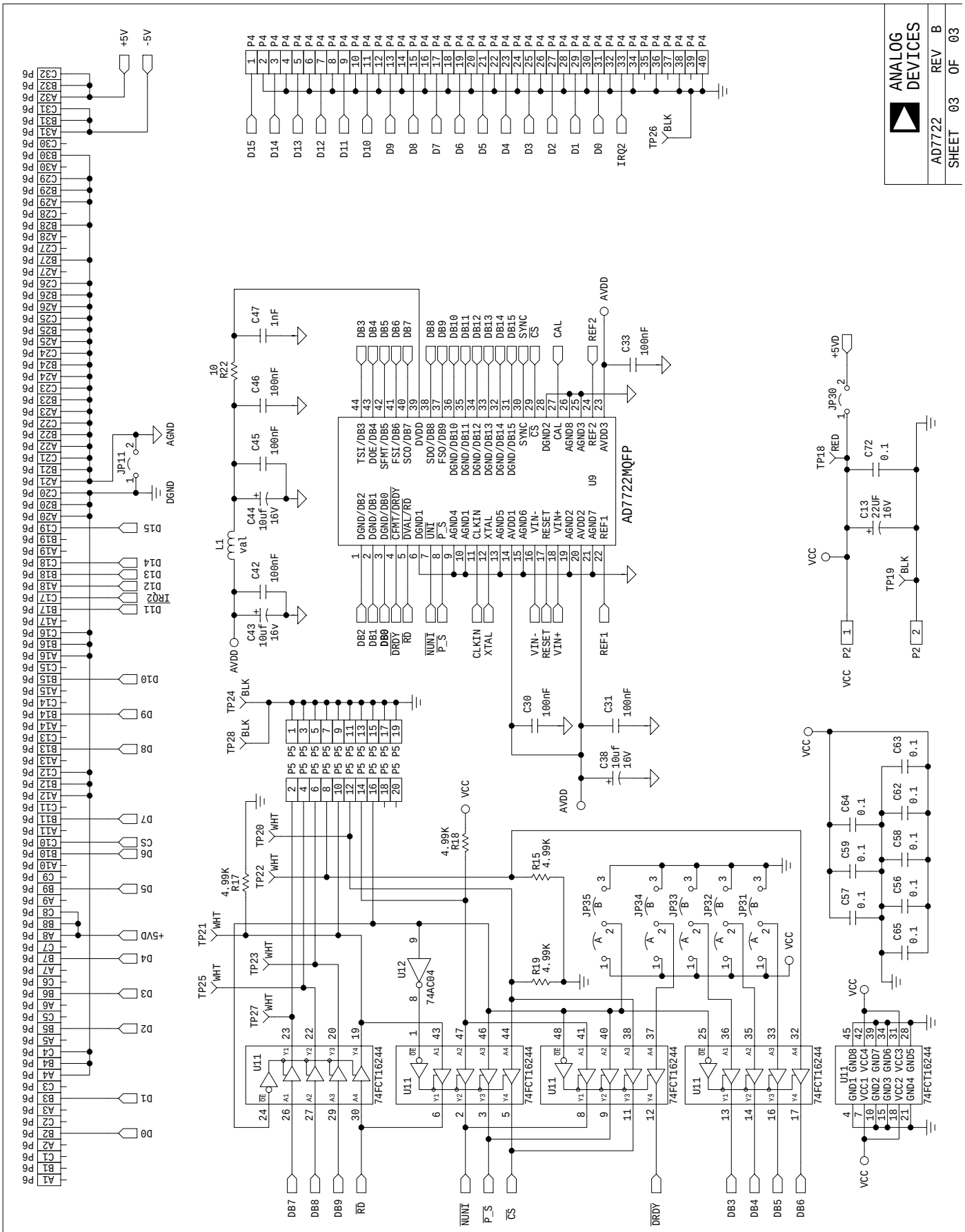

Figure 8. AD7722 Evaluation Board Schematic Sheet 3.

Table VIII. AD7722 Evaluation Board Bill of Materials

Item	Qty	Reference Designator	Description	Pkg	Manufacturer Distributor	Mfr P/N Dist P/N
1	1	Eval-AD7722CB Rev. B	Bare Board			
2	1	U1 *	Op-Amp (Single)	DIP8	ADI ADI	OP184EP OP184EP
3	1	U2 *	Voltage Reference	DIP8	ADI ADI	AD780AN AD780AN
4	2	U3 U10	Fast CMOS 16-bit 3 state register	SO48	IDT AVNET	74FCT162374TPV IDT74FCT162374TPV
5	1	U4	Schmitt Trigger Invertor	SO14	TI NEWARK	SN74AC140 52F2308
6	5	U5 U6 U7 U14 U16	Signle AND Gate	SOT353	PHILIPS AVNET	74HC1G08 74HC1G08GW-G
7	1	U8 *	Dual op-amp	DIP8	ADI ADI	OP275GP OP275GP
8	1	U9	ADC	PQFP44	ADI ADI	AD7722AS AD7722AS
9	1	U11	Buffer/Line Driver	SSOP48	IDT AVNET	74FCT162244TPV 74FCT162244TPV
10	1	U12	Hex Invertor	SO14	TI NEWARK	SN74AC04D 52F2306
11	1	U15	Dual D-Type Flip Flop with Set & Reset	SO14	TI NEWARK	SN74AC74D 52F2310
12	1	U17 *	25 MHZ Clock Osc.	DIP8-04	ECS DIGIKEY	OECS-250-2-A401A XC252-ND
13	0	(Y1)	25MHz Crystal	HC49/U	CTS DIGIKEY	 CTX171-ND
14	1	R1 *	249W Metal Film Res 1% 0.25W	RC07	WELWYN FARNELL	RC55 249W 338-590
15	6	R2-R5 R7 R8 *	499W Metal Film Res 1% 0.25W	RC07	WELWYN FARNELL	RC55 499W 338-886
16	2	R9 R10	51.1W Metal Film Res 1% 0.125W	1206	PANASONIC DIGIKEY	ERJ-8ENF51.1 P51.1FCT-ND
17	2	R11 R12	154W Metal Film Res 1% 0.125W	1206	PANASONIC DIGIKEY	ERJ-8ENF154 P154FCT-ND
18	9	R13 R15-19 R21 R23 R24	4.99KW Metal Film Res 1% 0.125W	1206	PANASONIC DIGIKEY	ERJ-8ENF4.99K P4.99KFCT-ND
19	1	R14	20W Metal Film Res 1% 0.125W	1206	PANASONIC DIGIKEY	ERJ-8ENF20 P20.0FCT-ND
20	0	(R20)	1MW Metal Film Res 1% 0.125W	1206	PANASONIC DIGIKEY	ERJ-8ENF1.0M P1.0MFCT-ND
21	1	R22	10W Metal Film Res 1% 0.125W	1206	PANASONIC DIGIKEY	ERJ-8ENF10 P10.0FCT-ND
22	0	(R25)	49.9W Metal Film Res 1% 0.25W	RC07	YAGO DIGIKEY	 49.9XBK-ND
23	8	C1 C7 C14 C20 C21 C38 C43 C44	Capacitor Chip Tant. 10uF 16V T49 Series	C CASE	KEMET NEWARK	T491C106K016AS 89F5043
24	5	C2 C3 C12 C13 C23	Capacitor Chip Tant. 22uF 20V T49 Series	D CASE	KEMET NEWARK	T491C226K020AS 89F5048
25	26	C4 C11 C15 C16 - C19 C22 C24 C26 C27 C30 - C34 C37 C41 C42 C45 C46 C52 C55 C61 C71 C72	Capacitor Chip Ceramic 0.1uF 50V X7R 10%	1206	PANASONIC DIGIKEY	ECU-V1H104KBM PCC104BCT-ND

EVAL-AD7722CB

Item	Qty	Reference Designator	Description	Pkg	Manufacturer / Distributor	Mfr P/N / Dist P/N
2	C5 C6	10pF 100V 5% COG	Cap Monolithic CK05	0.1" centre DIGIKEY	PANASONIC P4837-ND	ECU-S21100JCA 26
27	1	C8	Cap Monolithic 220pF 5% COG CK05	0.1" centre DIGIKEY	PANASONIC P4804-ND	ECU-S1T221SCA
28	0	(C9 C10)	Cap Monolithic 1nF 100V 10% X7R CK05	0.1" centre DIGIKEY	PANASONIC P4898-ND	ECU-S2A102KBA
29	1	C25	Capacitor Chip Ceramic 22000pF	1206	PANASONIC DIGIKEY	ECU-V1H223KBM PCC223BCT-ND
30	0	(C28 C29)	Capacitor Chip Ceramic 33pF 50V NPO 5%	O805	PANASONIC DIGIKEY	ECU-V1H330JCG PCC330CGCT-ND
31	27	C35 C36 C39 C40 C48-51 C53 C56-60 C62-70 C73-76	Capacitor Chip Ceramic 0.1uF 25V 10%	O805	MURATA NEWARK	GRM40X7A104K0258L 96F9510
32	1	C47	Capacitor Chip Ceramic 0.01uF 50V X7R 10%	1206	PANASONIC DIGIKEY	ECU-V1H103KBM PCC103BCT-ND
33	3	SW1 SW2 SW3	Push Button Switch Keyboard Switch	SPNO	OMRON FARNELL	B3S1000 177-807
34	1	L1	Ferrite Bead	RC07	MURATA NEWARK	BL01RN1-A62 90F2258
35	8	TP1 TP3 TP9 TP11 TP19 TP24 TP26 TP28	Test Point - Black	THRU	W HUGHES FARNELL	100-103 240-369
36	4	TP2 TP4 TP10 TP18	Test Point - Red	THRU	W HUGHES FARNELL	100-107 240-370
37	16	TP5-8 TP12-17 TP20-23 TP25 TP27	Test Point - White	THRU	W HUGHES	
38	2	P1 P2	Power Connector 2 Pin PCB Mount	10MM	WIELAND FARNELL	8191/02 151-794
39	1	P3	Power Connector 2 Pin PCB Mount	10MM	WIELAND FARNELL	8191/03 151-795
40	1	P4	Male IDC Header 40 pin	CON40	HARTING FARNELL	0918-540-6324 864-742
41	1	P5	Connector Header Straight 20 Pin	CON20	HARWIN FARNELL	M20-9982005 512-151
42	1	P6	DIN41612 Conn. Rt. Ang. 96 Pin	DIN41612	SIEMENS FARNELL	V42254-B1200-C960 269-888
43	2	J1 J2	BNC Connector Straight Round	BNC Round	M/A-COM FARNELL	B35N61H999X99 149-452
44	9	JP1 JP3 JP5 JP11 JP13 JP14 JP28 JP29 JP30	Jumper Header 2 Pin .025" Sq. Pins, 0.1" Centres	SIP2	HARWIN FARNELL	M20-9990206 511-705
45	15	JP2 JP4 JP6-10 JP12 JP15 JP17 JP131-35	Jumper Header 3 Pin .025" Sq. Pins, 0.1" Centres	SIP3	HARWIN FARNELL	M20-9990306 511-717
46	21	JP1-4 JP6 JP7 JP9-15 JP17 JP29-35	Jumper Shunt 2 Pin .025" Sq. Pins, 0.1" Centres		HARWIN FARNELL	M7567-05 150-410
47	28	U1 U2 U8 U17	Ultra Low Profile Strip Sockets (0.043" hole)		HARWIN FARNELL	D016020001 519-959
48	16	R1-R8	Socket, Loose (0.053"hole) 0.015 - 0.026 Lead		MILL-MAX	0555-0-15-01-20-27-10-0
49	4	Each Corner	Rubber Stick-on Feet		3M FARNELL	SJ5076 148-922

Notes

1. Put Jumper Wires from E1 to E3, E2 to E4 & E6 to E8.
2. When Reference Deisgnator is in brackets"( )" - do not insert the component.
3. Components marked with "*" are to be socketed.

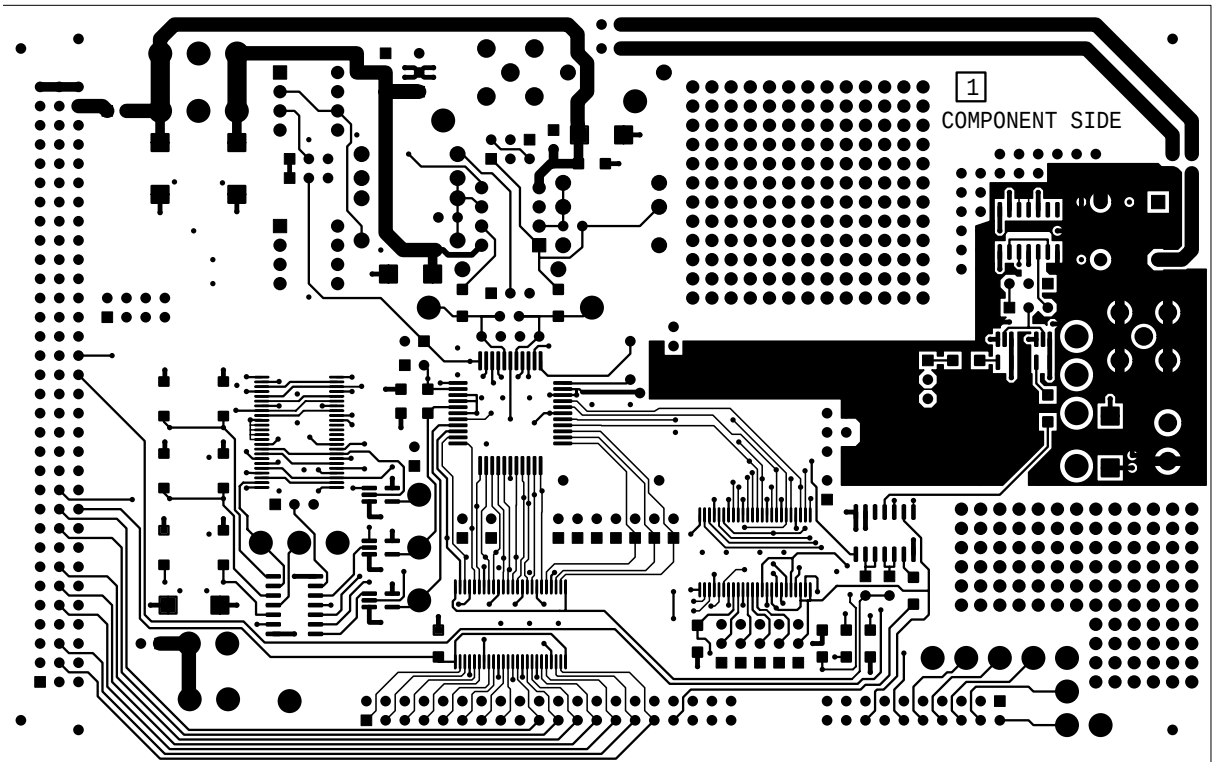

Figure 9. AD7722 Evaluation Board, Component Side Artwork.

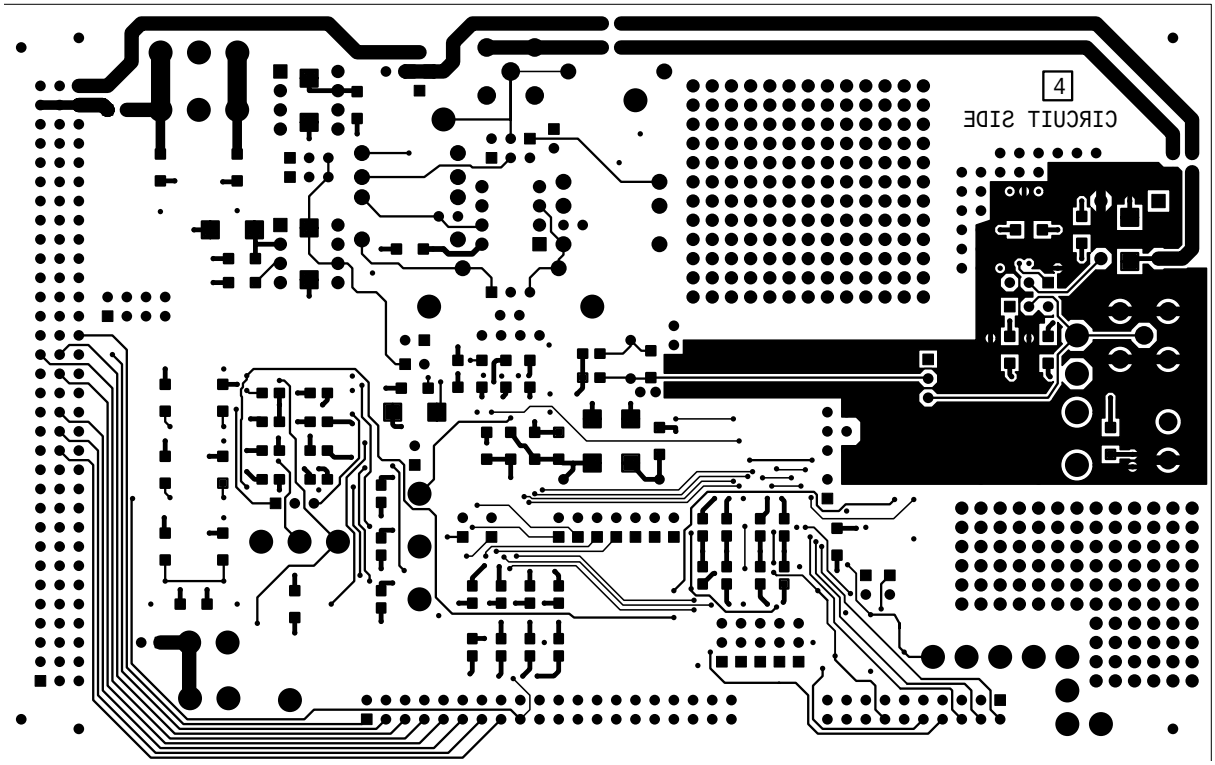

Figure 10. AD7722 Evaluation Board, Solder Side Artwork.

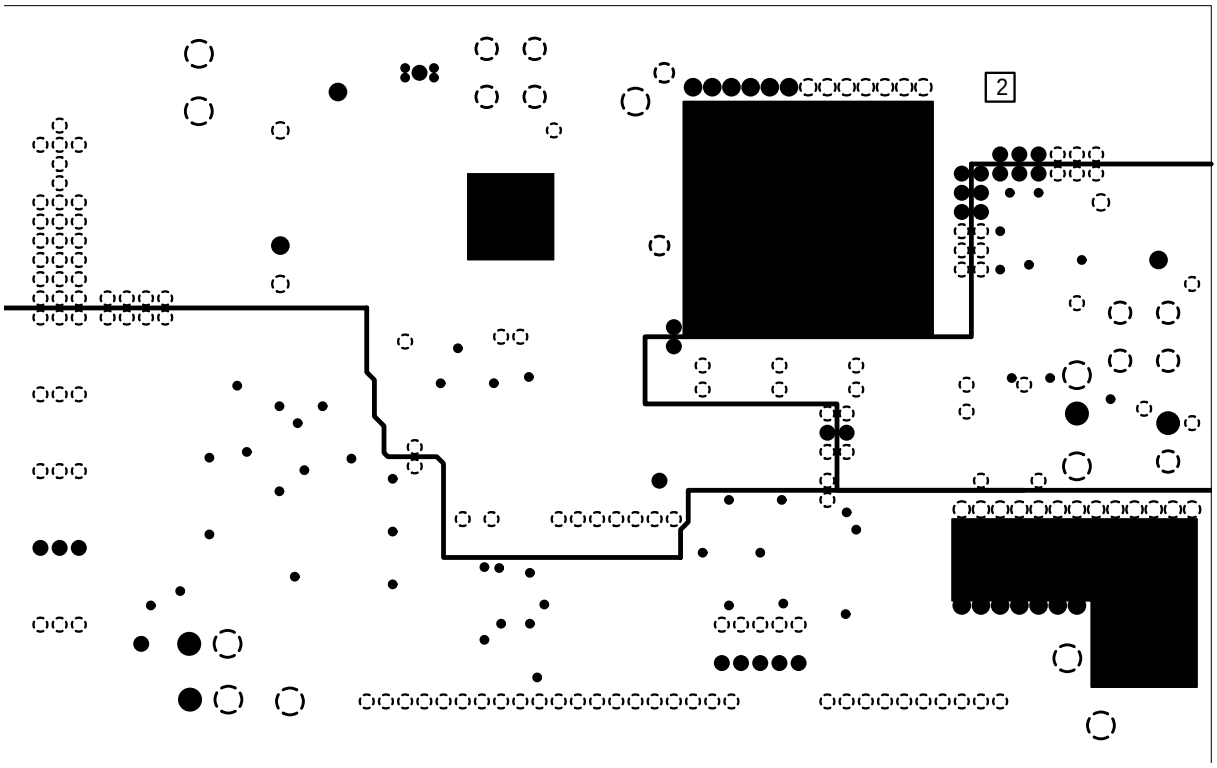

Figure 11. AD7722 Evaluation Board, Layer 2 Artwork - Ground Planes.

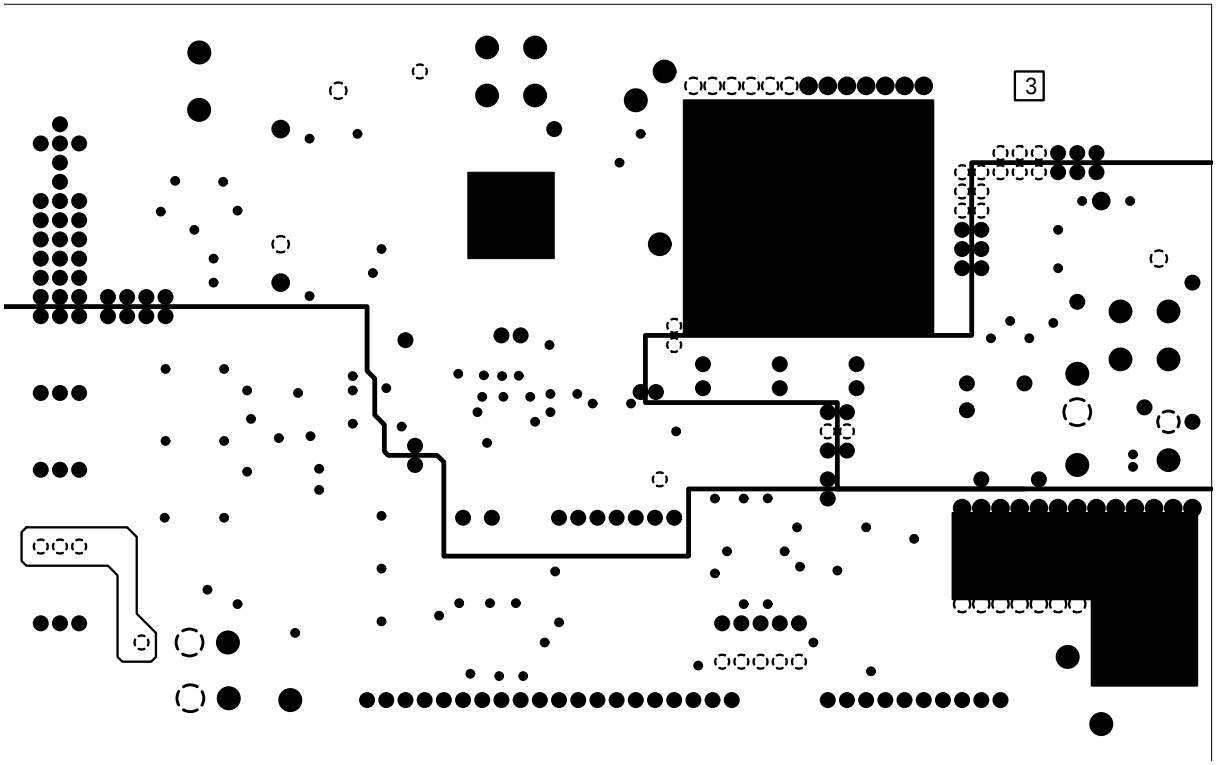

Figure 12. AD7722 Evaluation Board, Layer 3 Artwork - Power Planes.

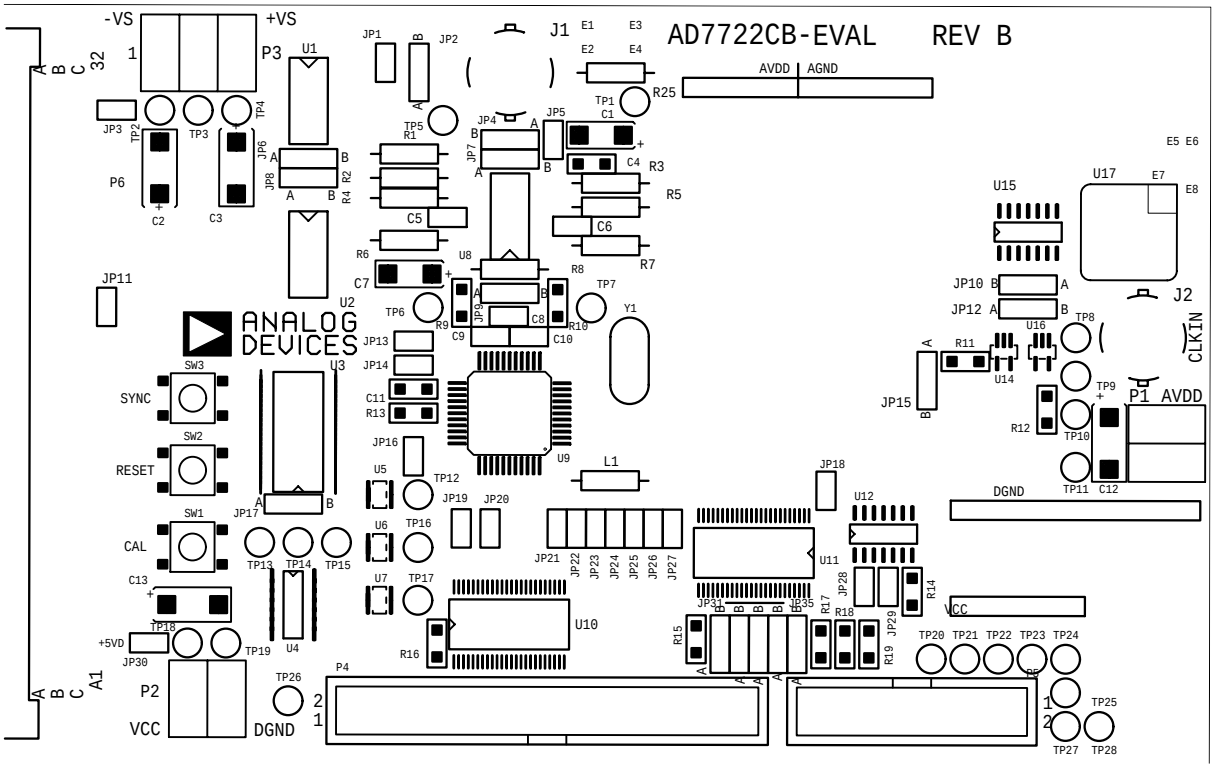

Figure 13. AD7722 Evaluation Board, Component Side Silkscreen Artwork.

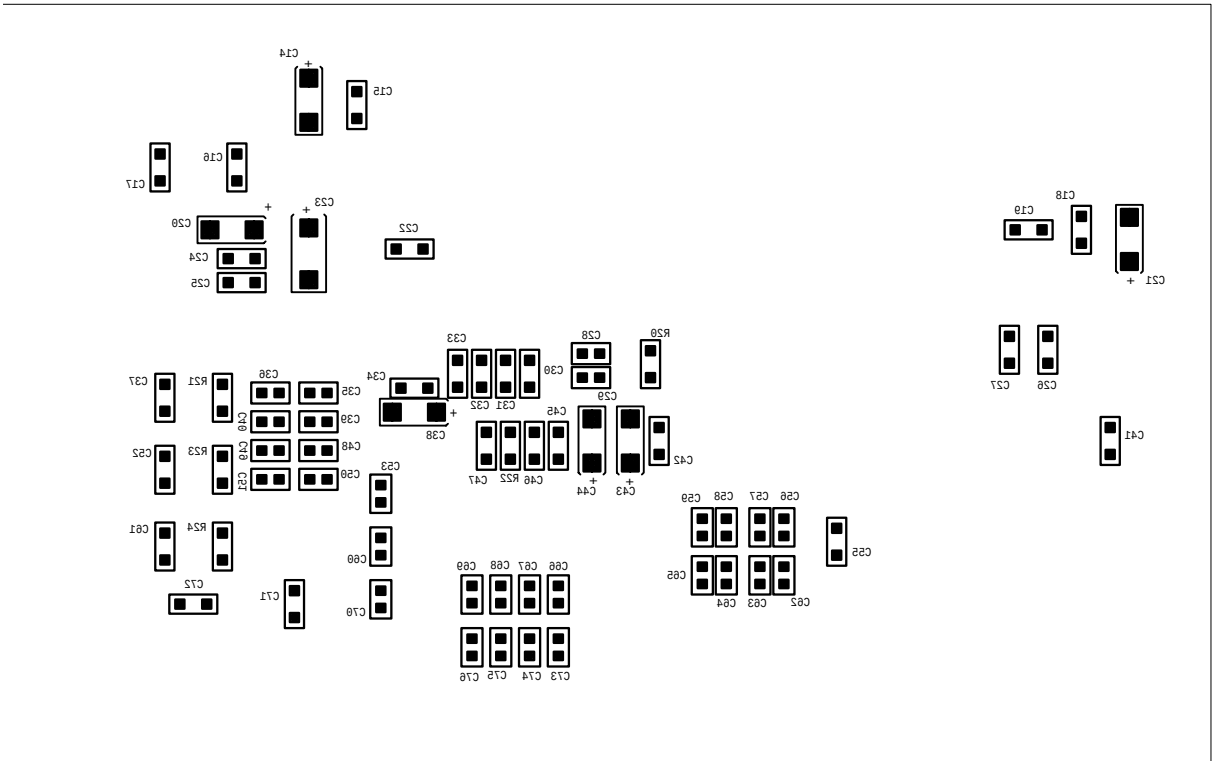

Figure 14. AD7722 Evaluation Board, Solder Side Silkscreen Artwork.