

## IR2131(J)(S) & (PbF)

### 3 HIGH SIDE AND 3 LOW SIDE DRIVER

#### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 high side & 3 low side drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- 28-Lead SOIC & 44-Lead PLCC are also available in Lead-Free.

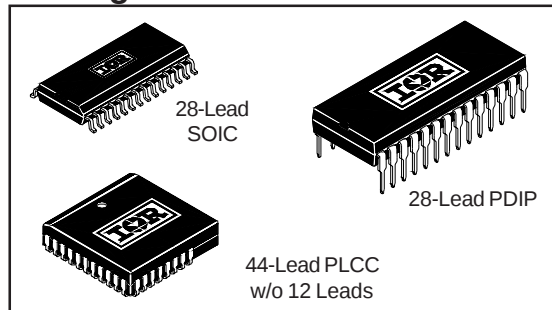
#### Description

The IR2131(J)(S) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. A shutdown input is provided for a customized shutdown function. An open drain FAULT signal is provided to indicate that any of the shutdowns has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

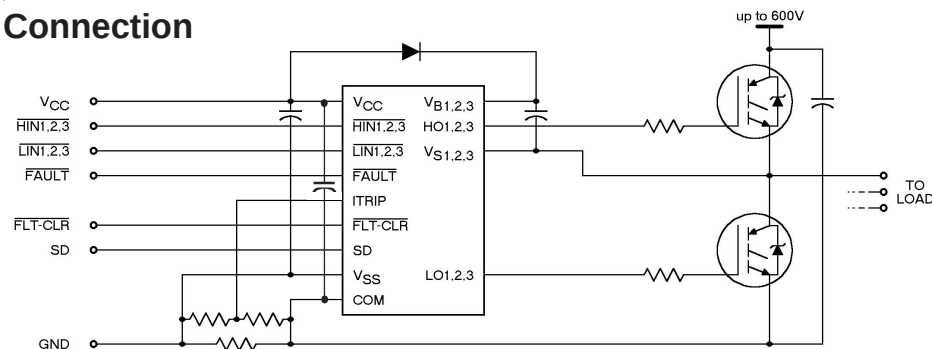
#### Product Summary

|                                  |                         |
|----------------------------------|-------------------------|
| <b>V<sub>OFFSET</sub></b>        | <b>600V max.</b>        |
| <b>I<sub>O</sub>+/-</b>          | <b>160 mA / 360 mA</b>  |
| <b>V<sub>OUT</sub></b>           | <b>10 - 20V</b>         |
| <b>t<sub>on/off</sub> (typ.)</b> | <b>1.3 &amp; 0.6 μs</b> |
| <b>Deadtime (typ.)</b>           | <b>700 ns</b>           |

#### Packages



#### Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

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## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional Information is shown in Figures 7 through 10.

| Symbol        | Definition                                                      | Min.               | Max.                                                       | Units              |
|---------------|-----------------------------------------------------------------|--------------------|------------------------------------------------------------|--------------------|
| $V_{B1,2,3}$  | High Side Floating Supply Voltage                               | -0.3               | 625                                                        |                    |
| $V_{S1,2,3}$  | High Side Floating Offset Voltage                               | $V_{B1,2,3} - 25$  | $V_{B1,2,3} + 0.3$                                         | V                  |
| $V_{HO1,2,3}$ | High Side Floating Output Voltage                               | $V_{S1,2,3} - 0.3$ | $V_{B1,2,3} + 0.3$                                         |                    |
| $V_{CC}$      | Low Side and Logic Fixed Supply Voltage                         | -0.3               | 25                                                         |                    |
| $V_{SS}$      | Logic Ground                                                    | $V_{CC} - 25$      | $V_{CC} + 0.3$                                             |                    |
| $V_{LO1,2,3}$ | Low Side Output Voltage                                         | -0.3               | $V_{CC} + 0.3$                                             |                    |
| $V_{IN}$      | Logic Input Voltage (HIN1,2,3, LIN1,2,3, FLT - CLR, SD & ITRIP) | $V_{SS} - 0.3$     | ( $V_{SS} + 15$ ) or ( $V_{CC} + 0.3$ ) whichever is lower |                    |
| $V_{FLT}$     | FAULT Output Voltage                                            | $V_{SS} - 0.3$     | $V_{CC} + 0.3$                                             |                    |
| $dV_S/dt$     | Allowable Offset Supply Voltage Transient                       | —                  | 50                                                         | V/ns               |
| $P_D$         | Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$        | (28 Lead DIP)      | 1.5                                                        | W                  |
|               |                                                                 | (28 Lead SOIC)     | 1.6                                                        |                    |
|               |                                                                 | (44 Lead PLCC)     | 2.0                                                        |                    |
| $R_{thJA}$    | Thermal Resistance, Junction to Ambient                         | (28 Lead DIP)      | 83                                                         | $^\circ\text{C/W}$ |
|               |                                                                 | (28 Lead SOIC)     | 78                                                         |                    |
|               |                                                                 | (44 Lead PLCC)     | 63                                                         |                    |
| $T_J$         | Junction Temperature                                            | —                  | 150                                                        | $^\circ\text{C}$   |
| $T_S$         | Storage Temperature                                             | -55                | 150                                                        |                    |
| $T_L$         | Lead Temperature (Soldering, 10 seconds)                        | —                  | 300                                                        |                    |

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

| Symbol        | Definition                                                      | Min.              | Max.              | Units            |
|---------------|-----------------------------------------------------------------|-------------------|-------------------|------------------|
| $V_{B1,2,3}$  | High Side Floating Supply Voltage                               | $V_{S1,2,3} + 10$ | $V_{S1,2,3} + 20$ | V                |
| $V_{S1,2,3}$  | High Side Floating Offset Voltage                               | Note 1            | 600               |                  |
| $V_{HO1,2,3}$ | High Side Floating Output Voltage                               | $V_{S1,2,3}$      | $V_{B1,2,3}$      |                  |
| $V_{CC}$      | Low Side and Logic Fixed Supply Voltage                         | 10                | 20                |                  |
| $V_{SS}$      | Logic Ground                                                    | -5                | 5                 |                  |
| $V_{LO1,2,3}$ | Low Side Output Voltage                                         | 0                 | $V_{CC}$          |                  |
| $V_{IN}$      | Logic Input Voltage (HIN1,2,3, LIN1,2,3, FLT - CLR, SD & ITRIP) | $V_{SS}$          | $V_{SS} + 5$      | $^\circ\text{C}$ |
| $V_{FLT}$     | FAULT Output Voltage                                            | $V_{SS}$          | $V_{CC}$          |                  |
| $T_A$         | Ambient Temperature                                             | -40               | 125               |                  |

Note 1: Logic operational for  $V_S$  of -5V to +600V. Logic state held for  $V_S$  of -5V to  $-V_{BS}$ . (Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins, CA- and CAO pins are internally clamped with a 5.2V zener diode.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15V,  $V_{S1,2,3} = V_{SS} = \text{COM}$ ,  $C_L = 1000 \text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The dynamic electrical characteristics are defined in Figures 4 through 5.

| Parameter Definition |                                            | Value |      |      | Units | Test Conditions                                             |
|----------------------|--------------------------------------------|-------|------|------|-------|-------------------------------------------------------------|
| Symbol               |                                            | Min.  | Typ. | Max. |       |                                                             |
| t <sub>on</sub>      | Turn-On Propagation Delay                  | 0.6   | 1.3  | 2.0  | μs    | V <sub>IN</sub> = 0 & 5V<br>V <sub>S1,2,3</sub> = 0 to 600V |
| t <sub>off</sub>     | Turn-Off Propagation Delay                 | 0.2   | 0.6  | 1.0  |       |                                                             |
| t <sub>r</sub>       | Turn-On Rise Time                          | —     | 80   | 150  |       |                                                             |
| t <sub>f</sub>       | Turn-Off Fall Time                         | —     | 40   | 100  | ns    |                                                             |
| t <sub>itrip</sub>   | ITRIP to Output Shutdown Propagation Delay | 400   | 700  | 1000 |       | V <sub>ITRIP</sub> = 1V                                     |
| t <sub>bl</sub>      | ITRIP Blanking Time                        | —     | 400  | —    |       | V <sub>IN</sub> , V <sub>ITRIP</sub> = 0 & 5V               |
| t <sub>flt</sub>     | ITRIP to FAULT Indication Delay            | 400   | 700  | 1000 |       | V <sub>IN</sub> = 0 & 5V                                    |
| t <sub>flt,in</sub>  | Input Filter Time (All Six Inputs)         | —     | 310  | —    |       | V <sub>IN</sub> , V <sub>IT</sub> , V <sub>FC</sub> = 0&5V  |
| t <sub>fltclr</sub>  | FLT - CLR to FAULT Clear Time              | 400   | 800  | 1200 |       | V <sub>IN</sub> , V <sub>SD</sub> = 0 & 5V                  |
| t <sub>sd</sub>      | SD to Output Shutdown Propagation Delay    | 400   | 700  | 1000 |       | V <sub>IN</sub> = 0 & 5V                                    |
| DT                   | Deadtime                                   | 400   | 700  | 1200 |       |                                                             |

NOTE: For high side PWM, HIN pulse width must be  $\geq 1.5\mu\text{sec}$

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15V,  $V_{S1,2,3} = V_{SS} = \text{COM}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all six logic input leads: HIN1,2,3 & LIN1,2,3. The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

| Symbol        | Parameter Definition                        | Value |      |      | Units         | Test Conditions                       |
|---------------|---------------------------------------------|-------|------|------|---------------|---------------------------------------|
|               |                                             | Min.  | Typ. | Max. |               |                                       |
| $V_{IH}$      | Logic "0" Input Voltage (OUT = LO)          | 2.2   | —    | —    | V             |                                       |
| $V_{IL}$      | Logic "1" Input Voltage (OUT = HI)          | —     | —    | 0.8  |               |                                       |
| $V_{FCLR,IH}$ | Logic "0" Fault Clear Input Voltage         | 2.2   | —    | —    |               |                                       |
| $V_{FCLR,IL}$ | Logic "1" Fault Clear Input Voltage         | —     | —    | 0.8  |               |                                       |
| $V_{SD,TH+}$  | Shutdown Input Positive Going Threshold     | 1.2   | 1.8  | 2.1  |               |                                       |
| $V_{SD,TH-}$  | Shutdown Input Negative Going Threshold     | 0.9   | 1.5  | 1.8  |               |                                       |
| $V_{IT,TH+}$  | ITRIP Input Positive Going Threshold        | 250   | 485  | 600  | mV            |                                       |
| $V_{IT,TH-}$  | ITRIP Input Negative Going Threshold        | 200   | 400  | 550  |               |                                       |
| $V_{OH}$      | High Level Output Voltage, $V_{BIAS} - V_O$ | —     | —    | 100  |               | $V_{IN} = 0\text{V}, I_O = 0\text{A}$ |
| $V_{OL}$      | Low Level Output Voltage, $V_O$             | —     | —    | 100  | $\mu\text{A}$ | $V_{IN} = 5\text{V}, I_O = 0\text{A}$ |
| $I_{LK}$      | Offset Supply Leakage Current               | —     | —    | 50   |               | $V_B = V_S = 600\text{V}$             |
| $I_{QBS}$     | Quiescent $V_{BS}$ Supply Current           | —     | 30   | 100  |               | $V_{IN} = 0\text{V}$ or $5\text{V}$   |
| $I_{QCC}$     | Quiescent $V_{CC}$ Supply Current           | —     | 3.0  | 4.5  | mA            | $V_{IN} = 0\text{V}$ or $5\text{V}$   |
| $I_{IN+}$     | Logic "1" Input Bias Current (OUT = HI)     | —     | 190  | 300  | $\mu\text{A}$ | $V_{IN} = 0\text{V}$                  |
| $I_{IN-}$     | Logic "0" Input Bias Current (OUT = LO)     | —     | 50   | 100  |               | $V_{IN} = 5\text{V}$                  |
| $I_{ITRIP+}$  | "High" ITRIP Bias Current                   | —     | 75   | 150  |               | ITRIP = 5V                            |
| $I_{ITRIP-}$  | "Low" ITRIP Bias Current                    | —     | —    | 100  | nA            | ITRIP = 0V                            |
| $I_{FCLR+}$   | Logic "1" Fault Clear Bias Current          | —     | 125  | 250  | $\mu\text{A}$ | FLT - CLR = 0V                        |
| $I_{FCLR-}$   | Logic "0" Fault Clear Bias Current          | —     | 75   | 150  |               | FLT - CLR = 5V                        |
| $I_{SD+}$     | Logic "1" Shutdown Bias Current             | —     | 75   | 150  |               | SD = 5V                               |
| $I_{SD-}$     | Logic "0" Shutdown Bias Current             | —     | —    | 100  | nA            | SD = 0V                               |

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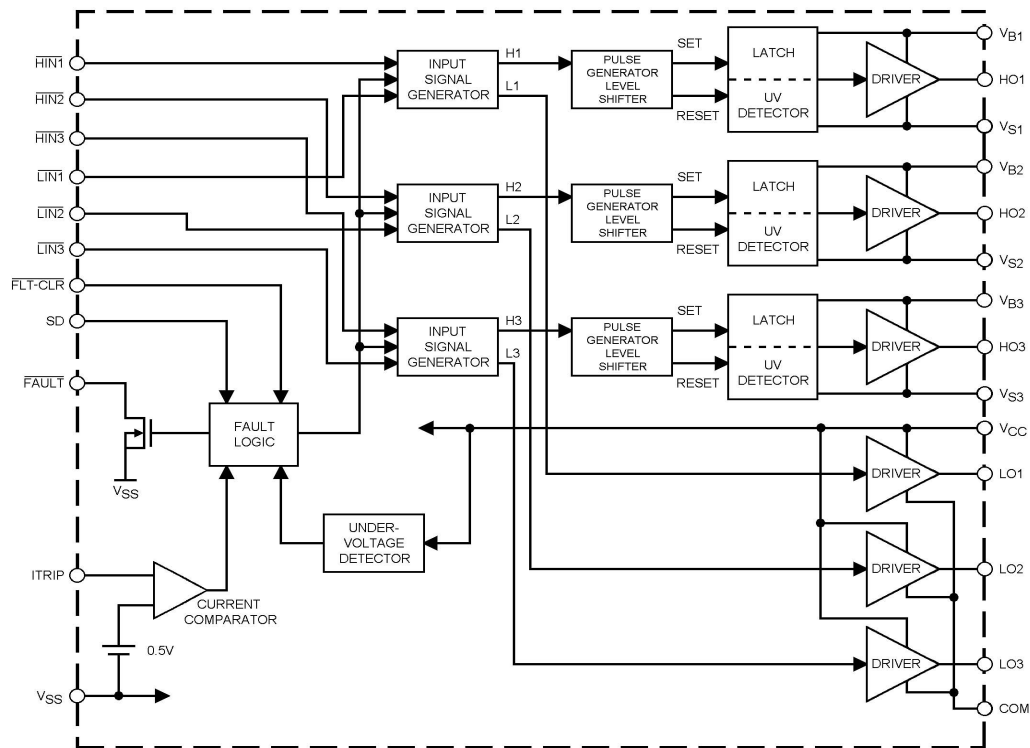
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## Static Electrical Characteristics -- Continued

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15V,  $V_{S1,2,3} = V_{SS} = COM$  and  $T_A = 25^\circ C$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all six logic input leads:  $HIN1,2,3$  &  $LIN1,2,3$ . The  $V_O$  and  $I_O$  parameters are referenced to  $COM$  and  $V_{S1,2,3}$  and are applicable to the respective output leads:  $HO1,2,3$  or  $LO1,2,3$ .

| Symbol       | Parameter Definition                                  | Value |      |      | Units    | Test Conditions                                |
|--------------|-------------------------------------------------------|-------|------|------|----------|------------------------------------------------|
|              |                                                       | Min.  | Typ. | Max. |          |                                                |
| $V_{BSUV+}$  | $V_{BS}$ Supply Undervoltage Positive Going Threshold | 8.2   | 8.7  | 9.2  | V        |                                                |
| $V_{BSUV-}$  | $V_{BS}$ Supply Undervoltage Negative Going Threshold | 7.8   | 8.3  | 8.8  |          |                                                |
| $V_{CCUV+}$  | $V_{CC}$ Supply Undervoltage Positive Going Threshold | 8.2   | 8.7  | 9.2  |          |                                                |
| $V_{CCUV-}$  | $V_{CC}$ Supply Undervoltage Negative Going Threshold | 7.8   | 8.3  | 8.8  |          |                                                |
| $R_{on,FLT}$ | $\overline{FAULT}$ Low On-Resistance                  | —     | 55   | 75   | $\Omega$ |                                                |
| $I_{O+}$     | Output High Short Circuit Pulsed Current              | 160   | 250  | —    | mA       | $V_O = 0V, V_{IN} = 0V$<br>$PW \leq 10 \mu s$  |
| $I_{O-}$     | Output Low Short Circuit Pulsed Current               | 360   | 500  | —    |          | $V_O = 15V, V_{IN} = 5V$<br>$PW \leq 10 \mu s$ |

## Functional Block Diagram



## Lead Definitions

| Lead      |                                                                                        |
|-----------|----------------------------------------------------------------------------------------|
| Symbol    | Description                                                                            |
| HIN1,2,3  | Logic inputs for high side gate driver outputs (HO1,2,3), out of phase                 |
| LIN1,2,3  | Logic inputs for low side gate driver output (LO1,2,3), out of phase                   |
| FLT - CLR | Logic input for fault clear                                                            |
| SD        | Logic input for shutdown                                                               |
| FAULT     | Indicates over-current or undervoltage lockout (low side) has occurred, negative logic |
| VCC       | Low side and logic fixed supply                                                        |
| ITRIP     | Input for over-current shutdown                                                        |
| VSS       | Logic ground                                                                           |
| VB1,2,3   | High side floating supplies                                                            |
| HO1,2,3   | High side gate drive outputs                                                           |
| VS1,2,3   | High side floating supply returns                                                      |
| LO1,2,3   | Low side gate drive outputs                                                            |
| COM       | Low side return                                                                        |

## Lead Assignments

|                                         |                                                        |                                                       |
|-----------------------------------------|--------------------------------------------------------|-------------------------------------------------------|
| <p>28 Lead DIP</p> <p><b>IR2131</b></p> | <p>44 Lead PLCC w/o 12 Leads</p> <p><b>IR2131J</b></p> | <p>28 Lead SOIC (Wide Body)</p> <p><b>IR2131S</b></p> |
| <b>Part Number</b>                      |                                                        |                                                       |

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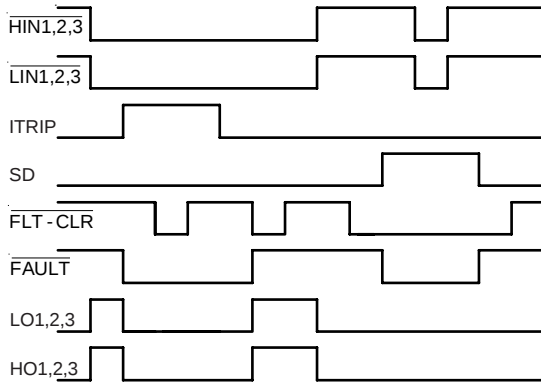


Figure 1. Input/Output Timing Diagram

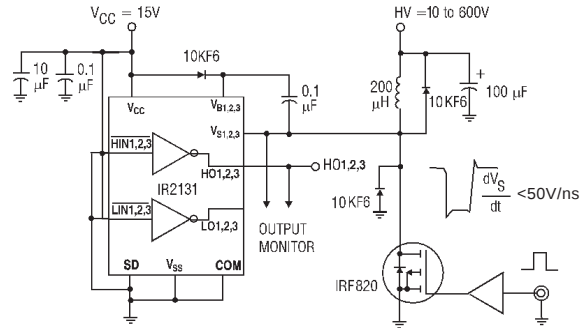


Figure 2. Floating Supply Voltage Transient Test Circuit

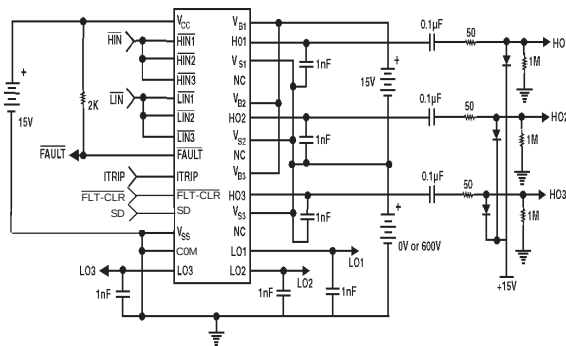


Figure 3. Switching Time Test Circuit

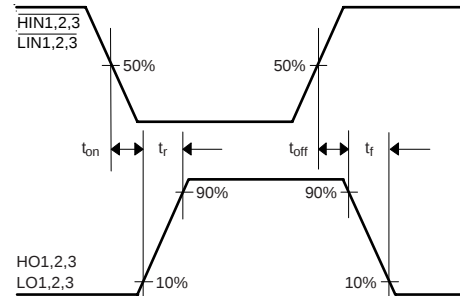


Figure 4. Switching Time Waveform Definitions

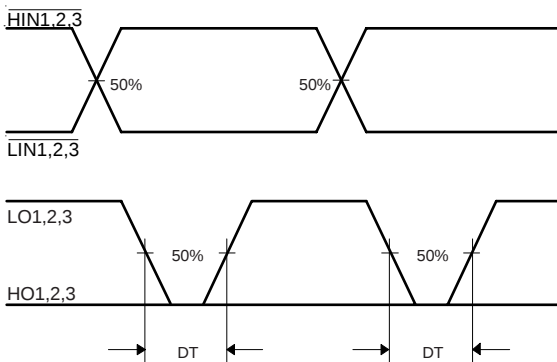


Figure 5. Deadtime Waveform Definitions

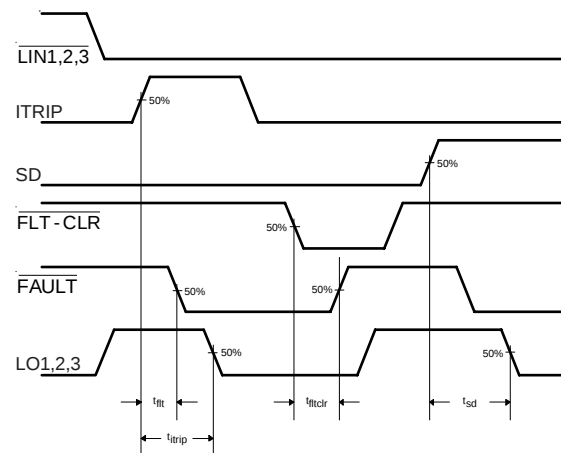


Figure 6. Shutdown Waveform Definitions

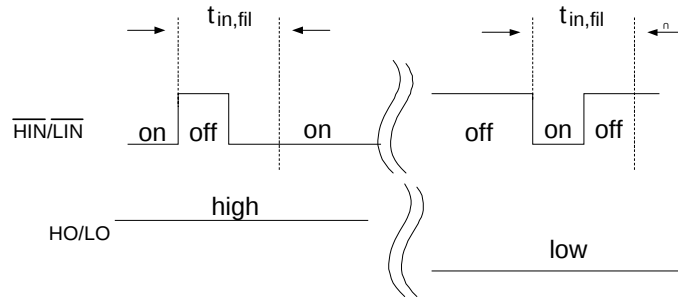


Figure 6.5 Input Filter Function

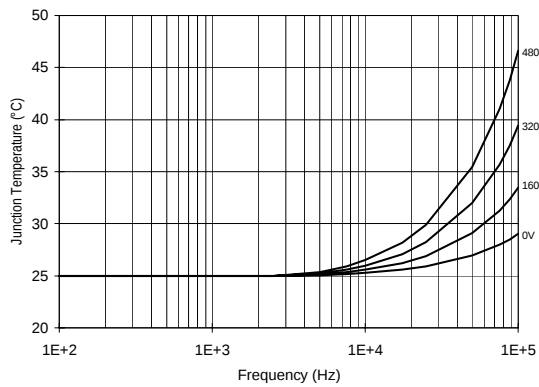


Figure 7. IR2131  $T_j$  vs. Frequency (IRF820)  
 $R_{GATE} = 33\Omega$ ,  $V_{CC} = 15V$

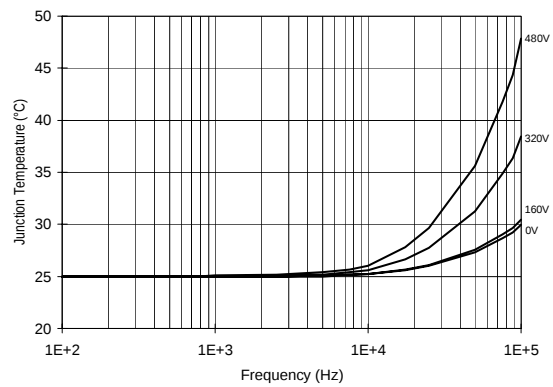


Figure 8. IR2131  $T_j$  vs. Frequency (IRF830)  
 $R_{GATE} = 20\Omega$ ,  $V_{CC} = 15V$

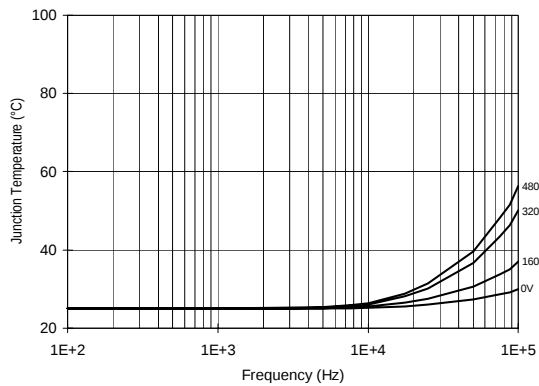


Figure 9. IR2131  $T_j$  vs. Frequency (IRF840)  
 $R_{GATE} = 15\Omega$ ,  $V_{CC} = 15V$

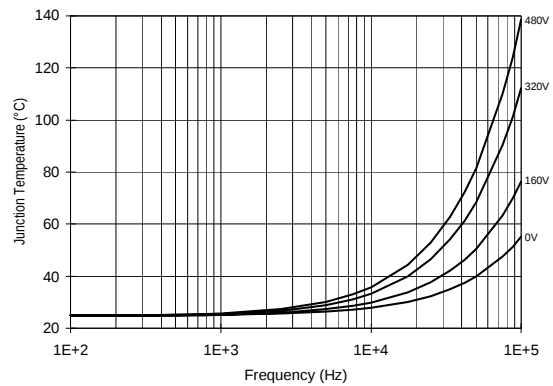


Figure 10. IR2131  $T_j$  vs. Frequency (IRF450)  
 $R_{GATE} = 10\Omega$ ,  $V_{CC} = 15V$

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**28-Lead PDIP (wide body)**

**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [0.010].

**Top View Dimensions:**

- Overall Width: 39.75 [1.565] (35.06 [1.380] to datum -A)
- Lead Width: 1.77 [0.070] (0.77 [0.030] to datum -B)
- Lead Spacing: 28X
- Lead Length: 14.73 [0.580] (12.32 [0.485] to datum -B)
- Pin 1 Indicator: 1
- Pin 28 Indicator: 28
- Pin 14 Indicator: 14
- Pin 15 Indicator: 15

**Side View Dimensions:**

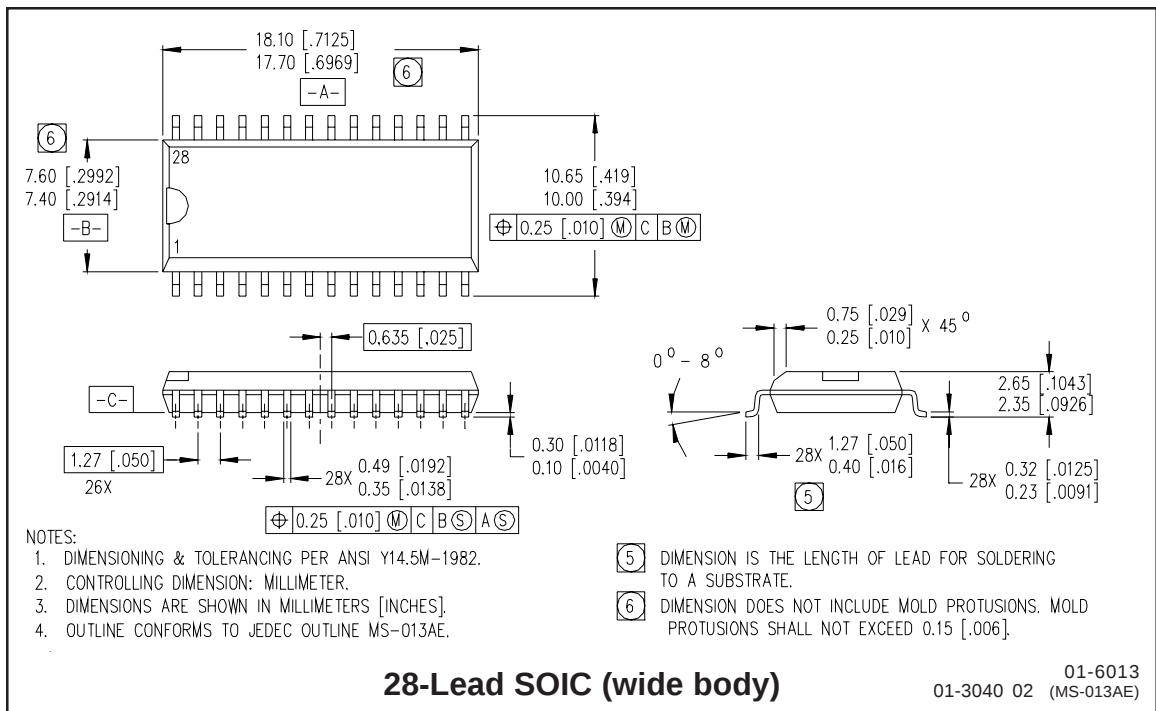
- Lead Height: 0.39 [0.015] MIN.
- Lead Thickness: 1.27 [0.050]
- Lead Angle: 0° to 15°
- Lead Spacing: 28X
- Lead Length: 15.24 [0.600]
- Lead Width: 0.381 [0.015] (0.204 [0.008] to datum -C)
- Lead Thickness: 0.558 [0.022] (0.356 [0.014] to datum -C)
- Lead Spacing: 28X
- Lead Length: 2.54 [0.100] (26X)
- Lead Thickness: 6.35 [0.250] MAX.

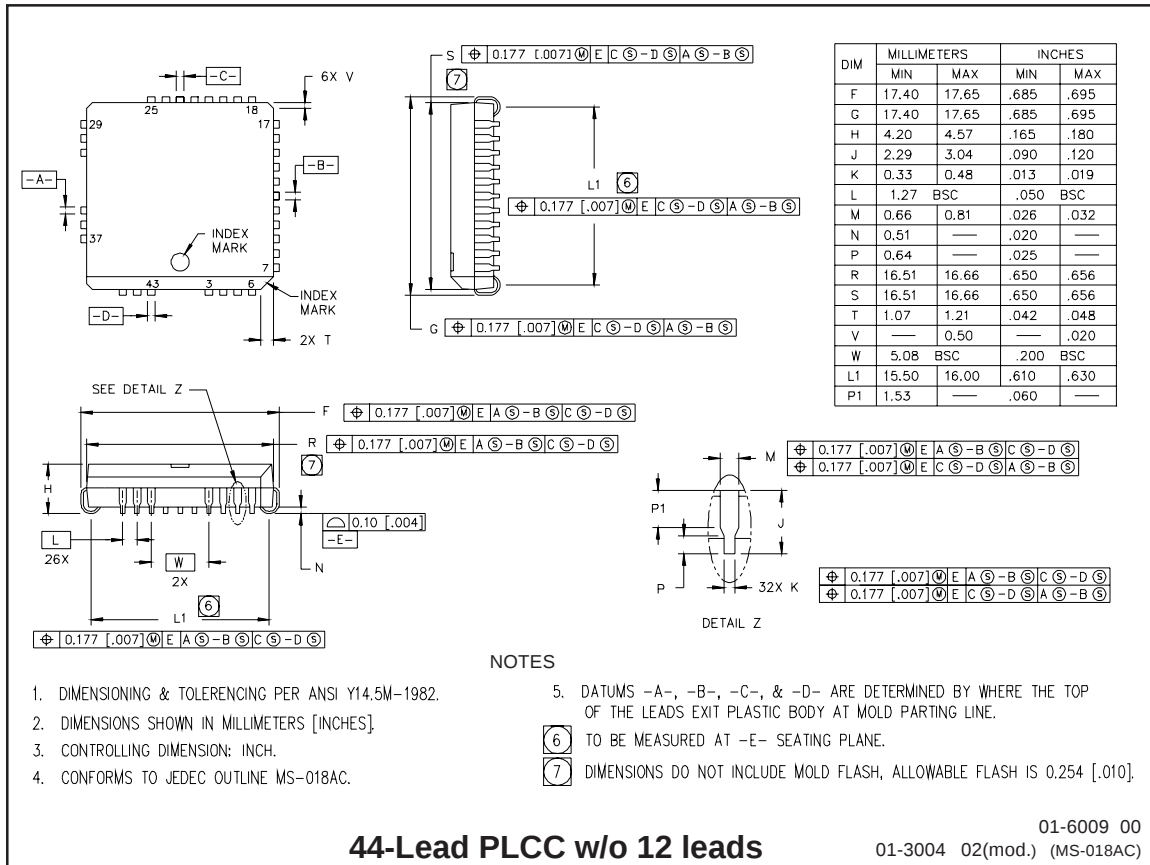
**End View Dimensions:**

- Lead Width: 0.39 [0.015] MIN.
- Lead Thickness: 1.27 [0.050]
- Lead Angle: 0° to 15°
- Lead Spacing: 28X
- Lead Length: 15.24 [0.600]
- Lead Width: 0.381 [0.015] (0.204 [0.008] to datum -C)
- Lead Thickness: 0.558 [0.022] (0.356 [0.014] to datum -C)
- Lead Spacing: 28X
- Lead Length: 2.54 [0.100] (26X)
- Lead Thickness: 6.35 [0.250] MAX.

**Feature Callouts:**

- A: Datum A (Top Surface)
- B: Datum B (Right Side Surface)
- C: Datum C (Lead Surface)
- ⑤: Feature 5 (Lead Surface)
- ⑥: Feature 6 (Lead Surface)

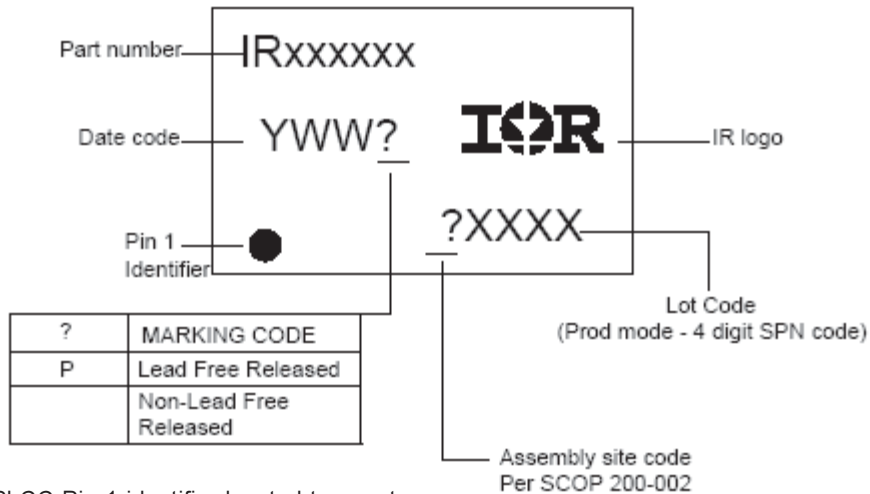




# IR2131(J)(S) & (PbF)

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## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

### Basic Part (Non-Lead Free)

|              |         |               |
|--------------|---------|---------------|
| 28-Lead PDIP | IR2131  | order IR2131  |
| 28-Lead SOIC | IR2131S | order IR2131S |
| 44-Lead PLCC | IR2131J | order IR2131J |

### Lead-Free Part

|              |         |                     |
|--------------|---------|---------------------|
| 28-Lead PDIP | IR2131  | order Not available |
| 28-Lead SOIC | IR2131S | order IR2131SPbF    |
| 44-Lead PLCC | IR2131J | order IR2131JPbF    |

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This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.  
Data and specifications subject to change without notice.

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at [www.irf.com](http://www.irf.com) for sales contact information.

10/11/04