



STP15NM65N STF15NM65N

N-channel 650 V, 0.35 Ω , 12 A TO-220, TO-220FP
second generation MDmesh™ Power MOSFET

Features

Order codes	V _{DSS} @T _{jmax}	R _{DS(on)} max.	I _D
STP15NM65N	710 V	0.38 Ω	12 A
STF15NM65N	710 V	0.38 Ω	12 A

- 100 % avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

These devices are N-channel Power MOSFETs realized using the second generation MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

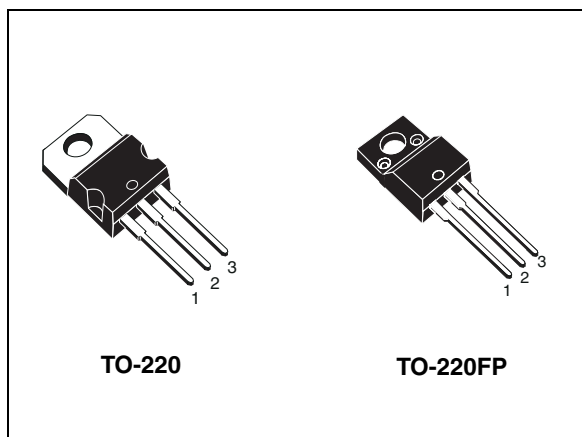


Figure 1. Internal schematic diagram

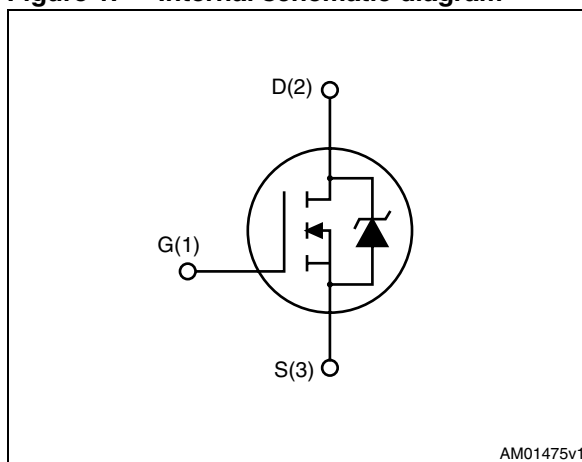


Table 1. Device summary

Order code	Marking	Package	Packaging
STP15NM65N	15NM65N	TO-220	Tubes
STF15NM65N	15NM65N	TO-220FP	Tubes

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain source voltage	650		V
V_{GS}	Gate source voltage	± 25		V
I_D	Drain current continuous $T_c=25\text{ }^{\circ}\text{C}$	12	12 ⁽¹⁾	A
I_D	Drain current continuous $T_c=100\text{ }^{\circ}\text{C}$	7.56	7.56	A
$I_{DM}^{(2)}$	Drain current pulsed	48	48	A
P_{TOT}	Total dissipation at $T_c=25\text{ }^{\circ}\text{C}$	125	30	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
V_{iso}	Insulation withstand voltage (RMS from all three leads to external heatsink ($t=1\text{ s}$; $T_c=25\text{ }^{\circ}\text{C}$))	-	2500	V
T_J	Operating junction temperature	-55 to 150		$^{\circ}\text{C}$
T_{sg}	Storage temperature			$^{\circ}\text{C}$

1. Limited only by maximum temperature allowed.

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameters	Value		Unit
		TO-220	TO-220FP	
R_{thjc}	Thermal resistance junction-case	1.0	4.17	$^{\circ}\text{C}/\text{W}$
R_{thja}	Thermal resistance junction-ambient	62.5		$^{\circ}\text{C}/\text{W}$
T_J	Max. lead temperature for soldering purposes	300		$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameters	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	3	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^{\circ}\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	187	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS}=0$)	$V_{DD} = \text{max rating}$			1	μA
		$V_{DD} = \text{max rating @ } T_C = 125\text{ }^{\circ}\text{C}$			100	μA
I_{GSS}	Gate body leakage ($V_{DS}=0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = V_{DS}$	2	3	4	V
$R_{DS(on)}$	Static $R_{DS(on)}$ -resistance	$I_D = 6\text{ A}$, $V_{GS} = 10\text{ V}$		0.35	0.38	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	983	-	pF
C_{oss}	Output capacitance			57		pF
C_{rss}	Reverse capacitance			4.5		pF
$C_{osseq}^{(1)}$	Equivalent out. capacitance	$V_{DS} = 0\text{ V to } V_{GS} = 0$	-	146	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	4.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 10\text{ V}$	-	33.3	-	nC
Q_{gs}	Gate source charge			5.7		nC
Q_{gd}	Gate-drain charge			17		nC

1. Cross eq; defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80 % V_{DSS} .

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 6\text{ A}$ $R_g = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	55.5	-	ns
t_r	Rise time			8.5		ns
$t_{d(off)}$	Turn-off-delay time		-	14	-	ns
t_f	Fall time			11.4		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source drain current Source drain current (pulsed)		-		12 48	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 25$	-	428 4.7 21.5		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150$	-	570 6.2 22		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

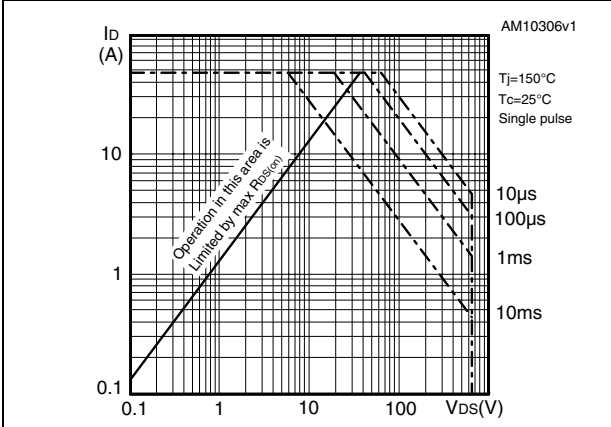


Figure 3. Thermal impedance for TO-220

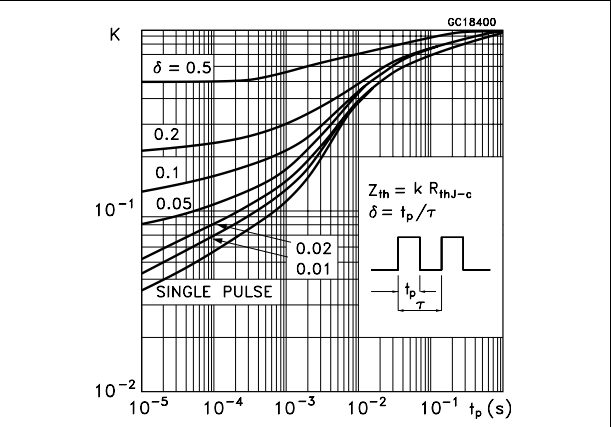


Figure 4. Safe operating area for TO-220FP

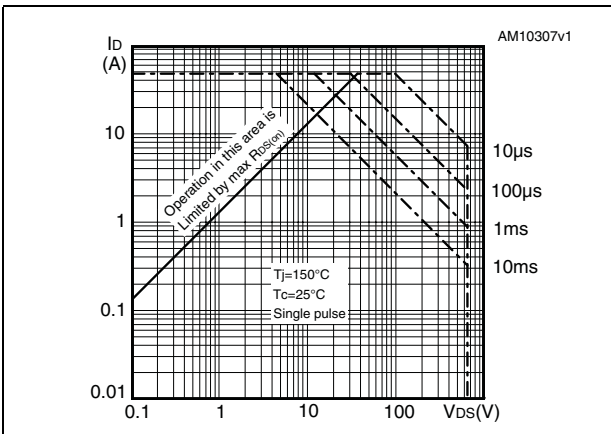


Figure 5. Thermal impedance for TO-220FP

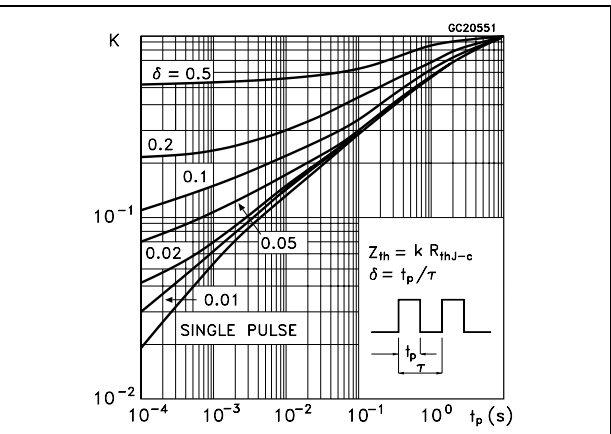


Figure 6. Output characteristics

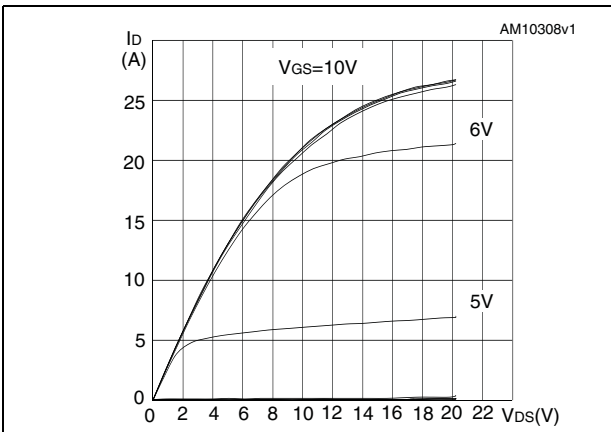


Figure 7. Transfer characteristics

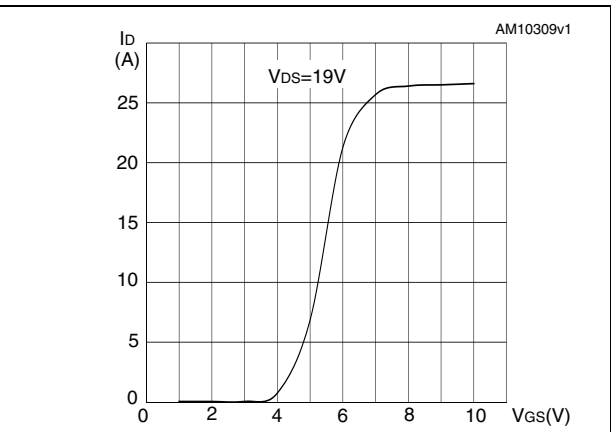


Figure 8. Static drain-source on resistance

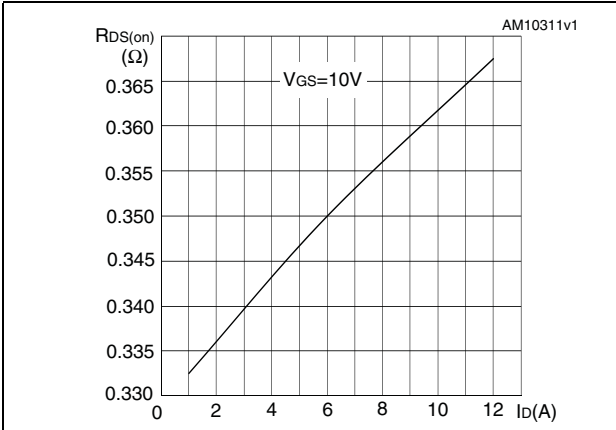


Figure 9. Gate charge vs gate-source voltage

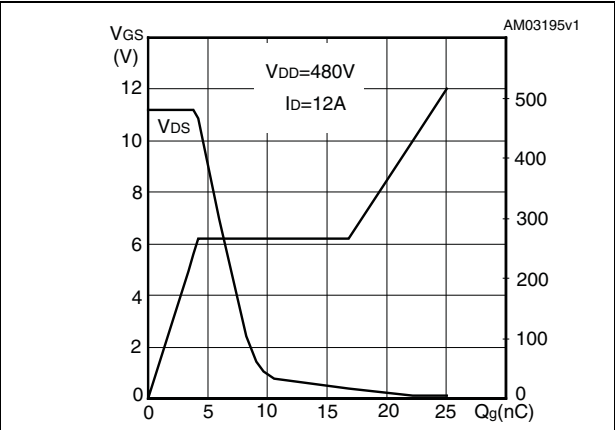


Figure 10. Capacitance variations

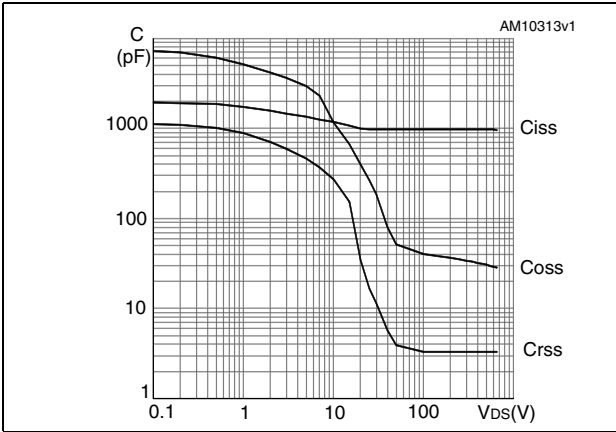


Figure 11. Normalized gate threshold voltage vs temperature

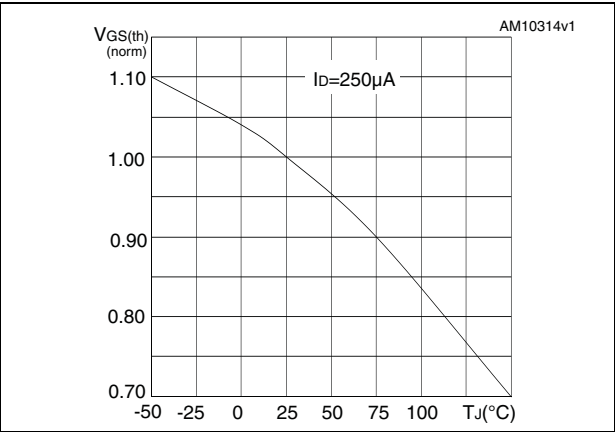


Figure 12. Normalized on resistance vs temperature

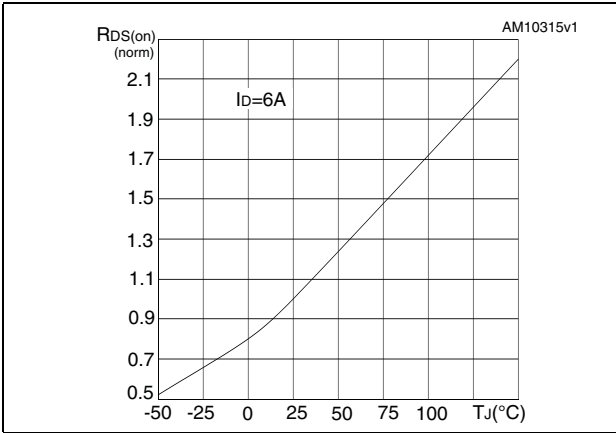


Figure 13. Source-drain diode forward characteristics

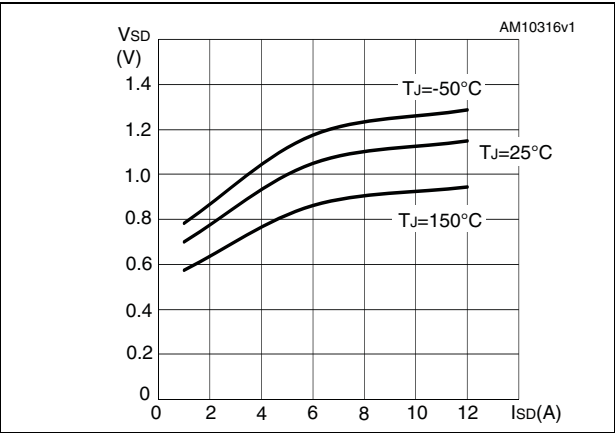
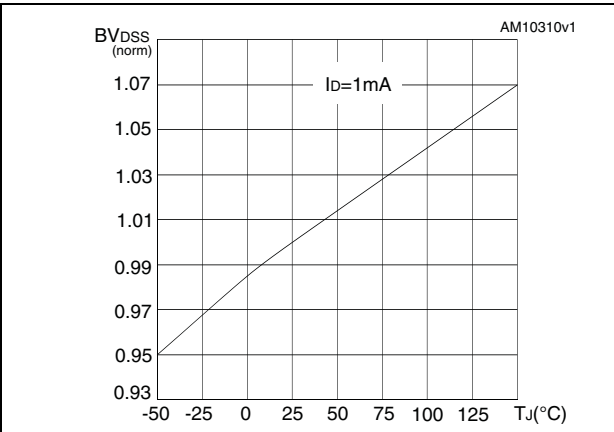


Figure 14. Normalized $B_{V_{DS}}$ vs temperature



3 Test circuits

Figure 15. Switching times test circuit for resistive load

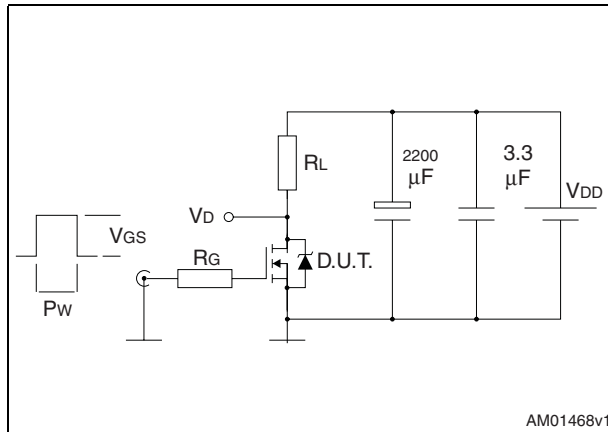


Figure 16. Gate charge test circuit

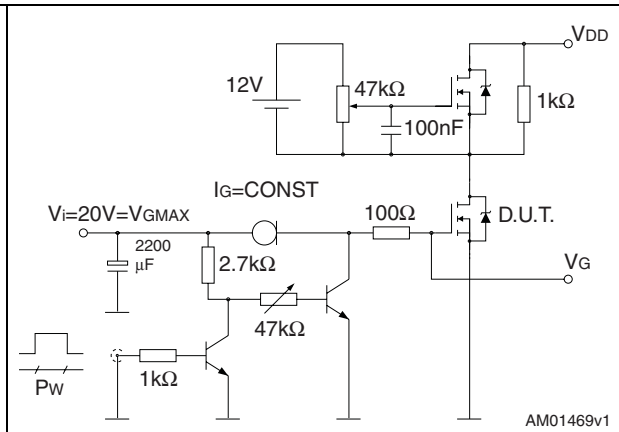


Figure 17. Test circuit for inductive load switching and diode recovery times

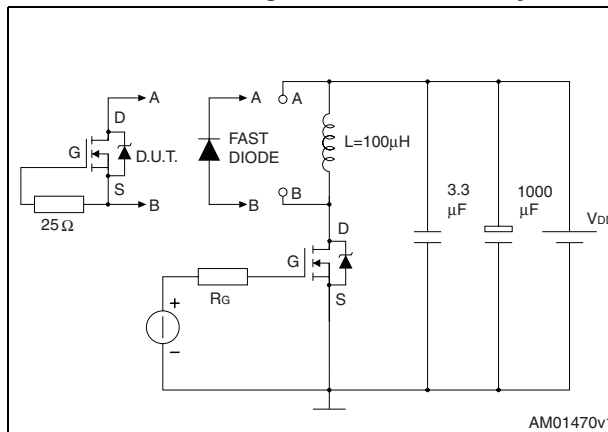


Figure 18. Unclamped inductive load test circuit

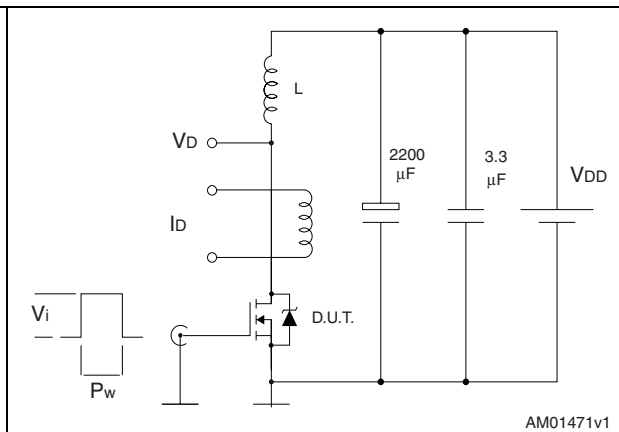


Figure 19. Unclamped inductive waveform

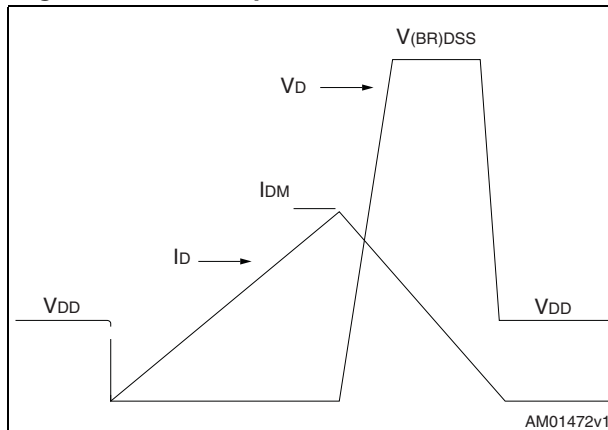
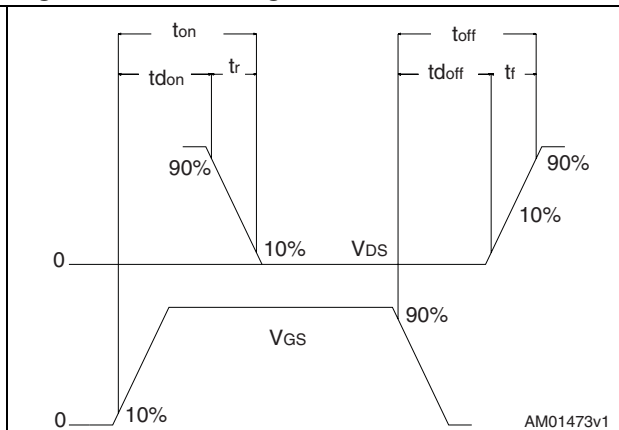


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 21. TO-220 type A drawing

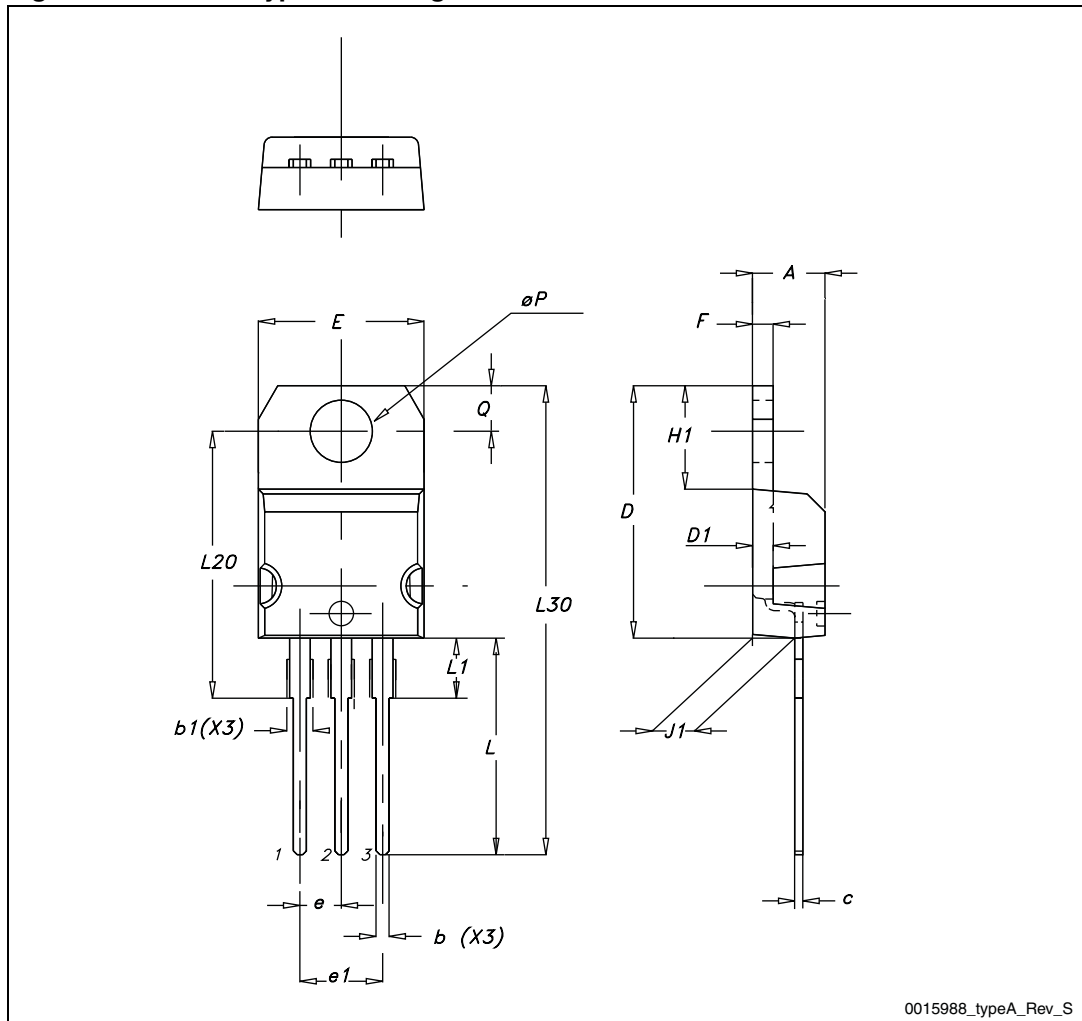
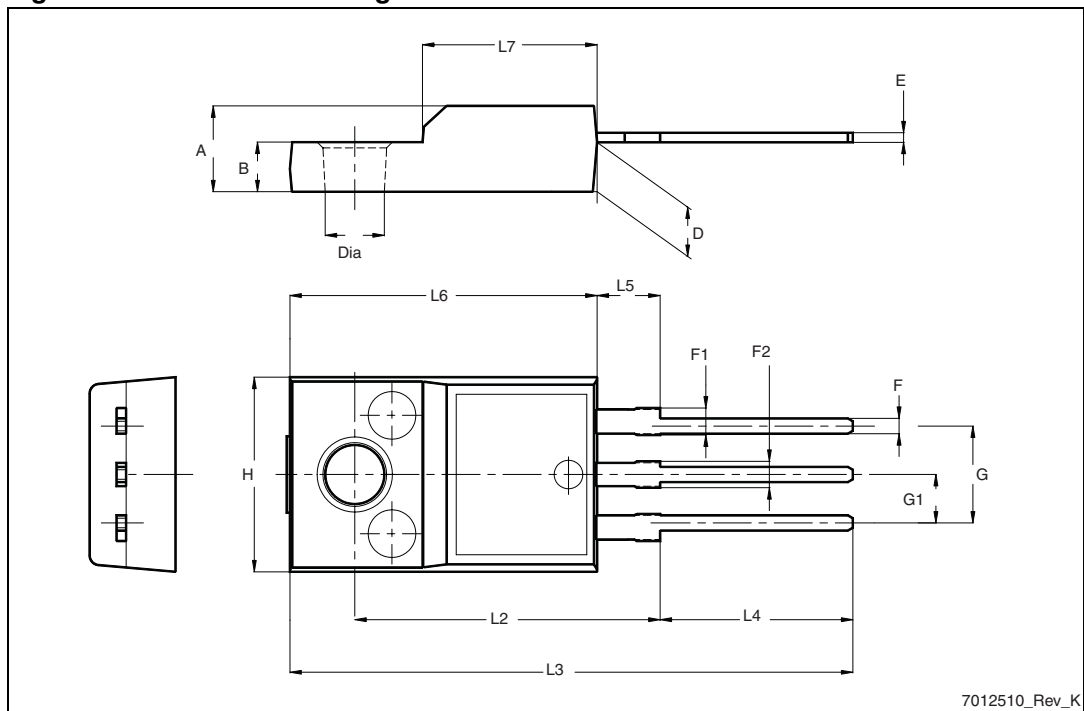


Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 22. TO-220FP drawing



5 Revision history

Table 11. Revision history

Date	Revision	Changes
11-May-2011	1	Initial release.
21-Jun-2011	2	Document status promoted from preliminary data to datasheet, added Section 2.1: Electrical characteristics (curves) .

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