DATA SHEET

PCA9516
5-channel I^2C hub

Product data
Supersedes data of 2002 May 13

2003 Nov 10

Philips
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5-channel I²C hub PCA9516

DESCRIPTION

The PCA9516 is a BiCMOS integrated circuit intended for application in I²C and SMBus systems.

While retaining all the operating modes and features of the I²C system, it permits extension of the I²C-bus by buffering both the data (SDA) and the clock (SCL) lines, thus enabling five buses of 400 pF.

The I²C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9516 enables the system designer to divide the bus into five segments off of a hub where any segment to segment transition sees only one repeater delay.

It can also be used to run different buses at 5 V and 3.3 V or 400 kHz and 100 kHz buses where the 100 kHz bus is isolated when 400 kHz operation of the other bus is required.

Two or more PCA9516s cannot be put in series. The PCA9516 design does not allow this configuration. Since there is no direction pin, slightly different “legal” low voltage levels are used to avoid lock-up conditions between the input and the output of each repeater in the hub. A ”regular low” applied at the input of a PCA9516 will be propagated as a “buffered low” with a slightly higher value on all the enabled outputs. When this “buffered low” is applied to another PCA9515, PCA9516, or PCA9518 in series, the second PCA9515, PCA9516, or PCA9518 will not recognize it as a “regular low” and will not propagate it as a “buffered low” again. The PCA9511/9513/9514 and PCA9512 cannot be used in series with the PCA9515, PCA9516, or PCA9518 but can be used in series with themselves since they use shifting instead of static offsets to avoid lock-up conditions.

FEATURES

- 5 channel, bi-directional buffer
- I²C-bus and SMBus compatible
- Active high individual repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates standard mode and fast mode I²C devices and multiple masters
- Powered-off high impedance I²C pins
- Operating supply voltage range of 3.0 V to 3.6 V
- 5 V tolerant I²C and enable pins
- 0 to 400 kHz clock frequency[1]
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101.
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA.
- Package offerings: SO and TSSOP

PIN CONFIGURATION

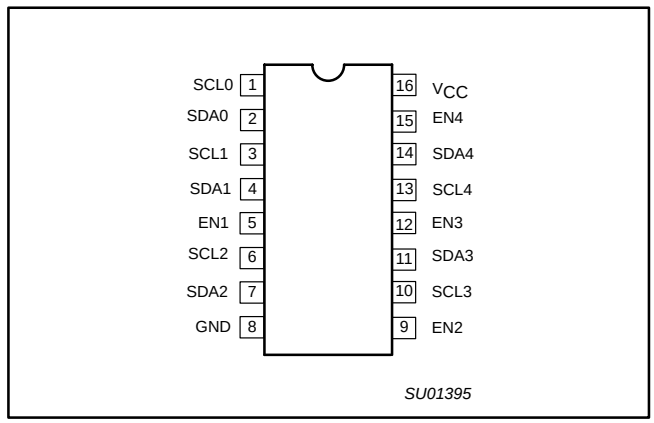


Figure 1. Pin configuration

PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
1	SCL0	Serial clock bus 0
2	SDA0	Serial data bus 0
3	SCL1	Serial clock bus 1
4	SDA1	Serial data bus 1
5	EN1	Active High Bus 1 enable Input
6	SCL2	Serial clock bus 2
7	SDA2	Serial data bus 2
8	GND	Supply ground
9	EN2	Active High Bus 2 enable Input
10	SCL3	Serial clock bus 3
11	SDA3	Serial data bus 3
12	EN3	Active High Bus 3 enable Input
13	SCL4	Serial clock bus 4
14	SDA4	Serial data bus 4
15	EN4	Active High Bus 4 enable Input
16	V_{CC}	Supply power

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
16-pin plastic SO	-40 to +85 °C	PCA9516D	PCA9516D	SOT109-1
16-pin plastic TSSOP	-40 to +85 °C	PCA9516PW	PCA9516	SOT403-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

1. The maximum system operating frequency may be less than 400 KHz because of the delays added by the repeater.

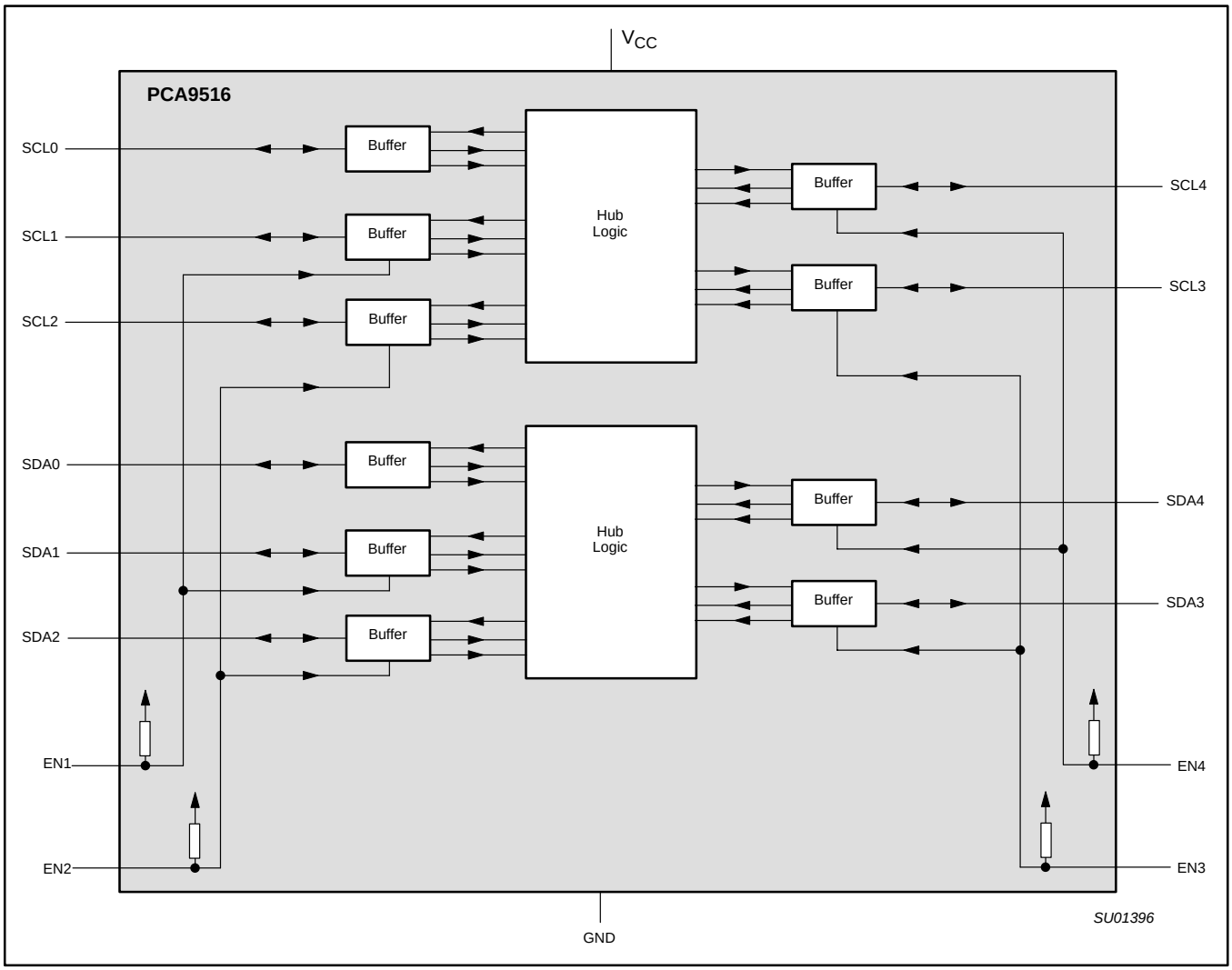


Figure 2. Block Diagram: PCA9516

A more detailed view of Figure 2 buffer is shown in Figure 3.

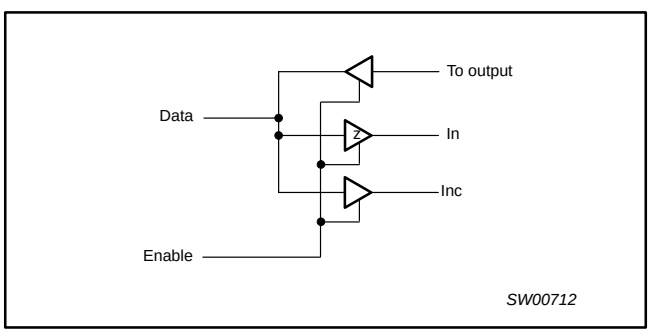


Figure 3.

The output pull-down of each internal buffer is set for approximately 0.5 V, while the input threshold of each internal buffer is set about 0.07 V lower, when the output is internally driven low. This prevents a lock-up condition from occurring.

FUNCTIONAL DESCRIPTION

The PCA9516 BiCMOS integrated circuit is a five way hub repeater, which enables I²C and similar bus systems to be expanded with only one repeater delay and no functional degradation of system performance.

The PCA9516 BiCMOS integrated circuit contains five bi-directional, open drain buffers specifically designed to support the standard low-level-contention arbitration of the I²C-bus. Except during arbitration or clock stretching, the PCA9516 acts like five pairs of non-inverting, open drain buffers, one for SDA and one for SCL.

Enable

The enable pins EN1 through EN4 are active high and have internal pull-up resistors. Each enable pin ENn controls its associated SDAn and SCLn ports. When low the ENn pin blocks the inputs from SDAn and SCLn as well as disabling the output drivers on the SDAn and SCLn pins. The enable pins should only change state when both the global bus and the local port are in an idle state to prevent system failures.

The active high enable pins allow the use of open drain drivers which can be wire-ORed to create a distributed enable where either centralized control signal (master) or spoke signal (submaster) can enable the channel when it is idle.

I²C Systems

As with the standard I²C system, pull-up resistors are required to provide the logic HIGH levels on the Buffered bus. (Standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with standard mode and fast mode I²C devices in addition to SMBus devices. Standard mode I²C devices only specify 3 mA output drive, this limits the termination current to 3 mA in a generic I²C system where standard mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used. Please see Application Note AN255 *"I²C & SMBus Repeaters, Hubs and Expanders"* for additional information on sizing resistors and precautions when using more than one PCA9515/PCA9516 in a system or using the PCA9515/16 in conjunction with the P82B96.

APPLICATION INFORMATION

A typical application is shown in Figure 4. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. All buses run at 100 kHz unless slave 3 and 4 are isolated and then the master bus and slave 1 and 2 can run at 400 kHz.

Any segment of the hub can talk to any other segment of the hub. Bus masters and slaves can be located on all five segments with 400 pF load allowed on each segment.

The PCA9516 is 5 V tolerant so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9516 is pulled low by a device on the I²C-bus, a CMOS hysteresis type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side to also go low. The side driven low by the PCA9516 will typically be at V_{OL} = 0.5 V.

In order to illustrate what would be seen in a typical application, refer to Figures 5 and 6. If the bus master in Figure 4 were to write to the slave through the PCA9516, we would see the waveform shown in Figure 5 on Bus 0. This looks like a normal I²C transmission until the falling edge of the 8th clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it low through the PCA9516. Because the V_{OL} of the PCA9516 is typically around 0.5 V, a step in the SDA will be seen. After the master has transmitted the 9th clock pulse, the slave releases the data line.

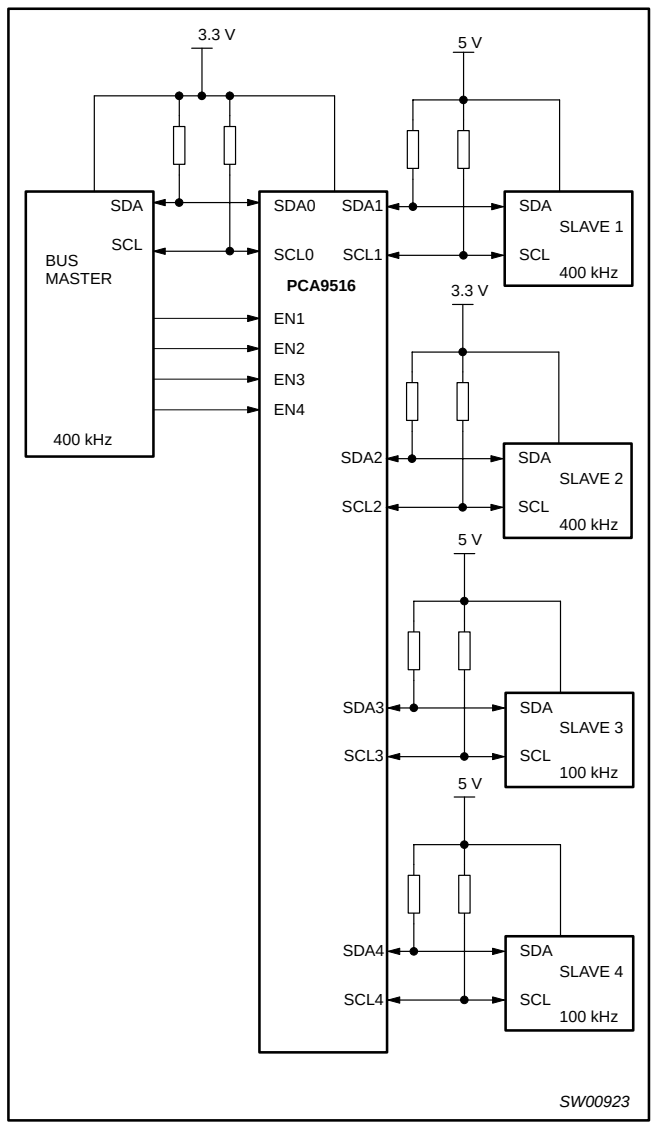


Figure 4. Typical application

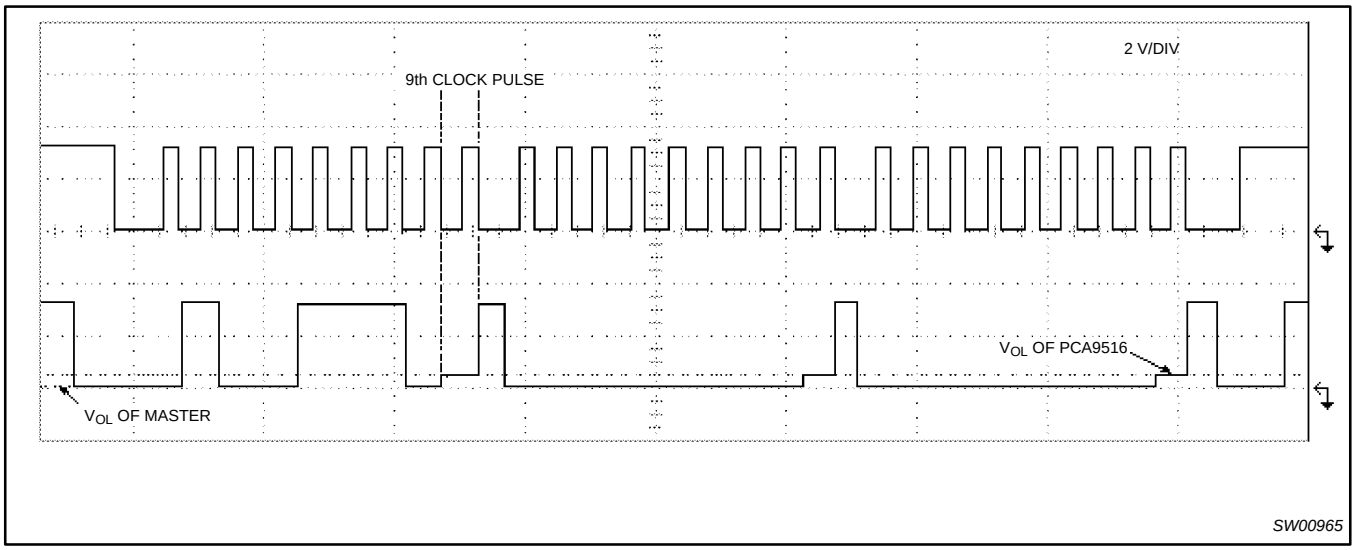


Figure 5. Bus 0 waveform

On the Bus 1 side of the PCA9516, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9516. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the slave device that is very close to ground in our example.

It is important to note that any arbitration or clock stretching events on Bus 1 require that the V_{OL} of the devices on Bus 1 be 70 mV below the V_{OL} of the PCA9516 (see V_{OL} - V_{ilc} in the DC Characteristics section) to be recognized by the PCA9516 and then transmitted to Bus 0.

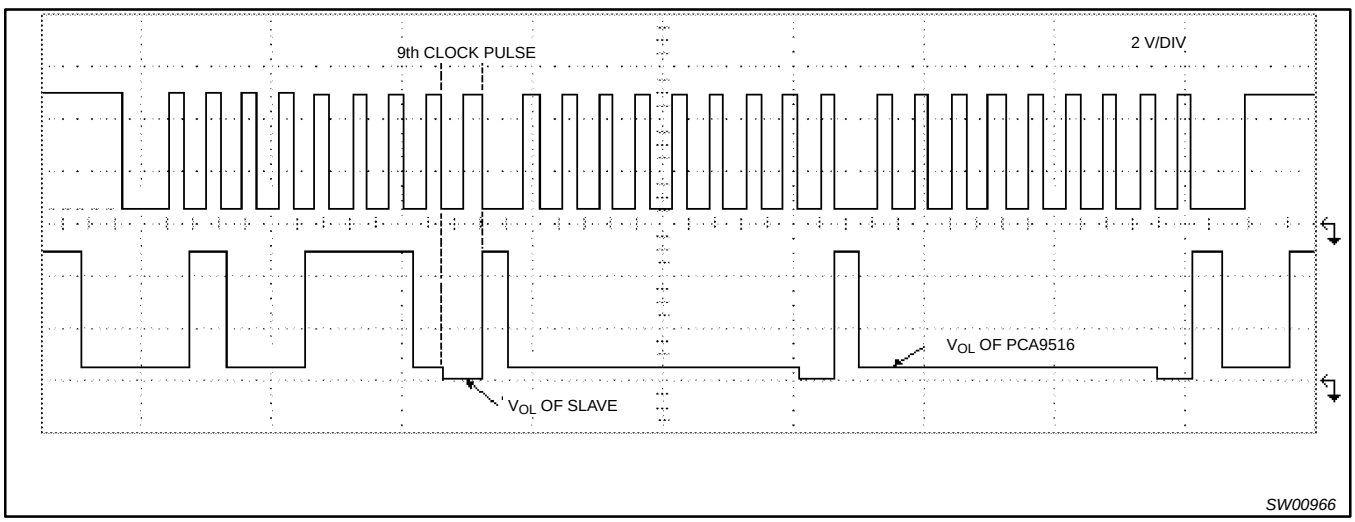


Figure 6. Bus 1 waveform

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC} to GND	Supply voltage range V_{CC}	-0.5	+7	V
V_{bus}	Voltage range I^2C-bus, SCL or SDA	-0.5	+7	V
I	DC current (any pin)	—	50	mA
P_{tot}	Power dissipation	—	300	mW
T_{stg}	Storage temperature range	-55	+125	°C
T_{amb}	Operating ambient temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 to 3.6 V; GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Supplies						
V_{CC}	DC supply voltage		3.0	3.3	3.6	V
I_{CCH}	Quiescent supply current, both channels HIGH	V_{CC} = 3.6 V; SDAn = SCLn = V_{CC}	—	7	10	mA
I_{CCL}	Quiescent supply current, both channels LOW	V_{CC} = 3.6 V; one SDA and one SCL = GND, other SDA and SCL open	—	6.8	10	mA
I_{CCLc}	Quiescent supply current in contention	V_{CC} = 3.6 V; SDAn = SCLn = GND	—	7	10	mA
Input SCL; input/output SDA						
V_{IH}	HIGH-level input voltage		0.7 V_{CC}	—	5.5	V
V_{IL}	LOW-level input voltage (Note 1)		-0.5	—	0.3 V_{CC}	V
V_{ILc}	LOW-level input voltage contention (Note 1)		-0.5	—	0.4	V
V_{IK}	Input clamp voltage	I_I = -18 mA	—	—	-1.2	V
I_I	Input leakage current	V_I = 3.6 V	—	—	±1	µA
I_{IL}	Input current LOW, SDA, SCL	V_I = 0.2 V, SDA, SCL	—	—	5	µA
V_{OL}	LOW-level output voltage	I_{OL} = 0 or 6 mA	0.47	0.52	0.6	V
V_{OL}-V_{ILc}	LOW-level input voltage below output low level voltage	Guaranteed by design	—	—	70	mV
I_{OH}	Output HIGH-level leakage current	V_O = 3.6 V	—	—	10	µA
C_I	Input capacitance	V_I = 3 V or 0 V	—	6	10	pF
Enable 1-4						
V_{IL}	LOW-level input voltage		-0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{IL}	Input current LOW, EN1-EN4	V_I = 0.2 V, EN1-EN4	—	10	30	µA
I_{LI}	Input leakage current		-1	—	1	µA
C_I	Input capacitance	V_I = 3.0 V or 0 V	—	6	7	pF

NOTE:
1. V_{IL} specification is for enable input and the first low level seen by the SDAx/SCLx lines. V_{ILc} is for the second and subsequent low levels seen by the SDAx/SCLx lines.

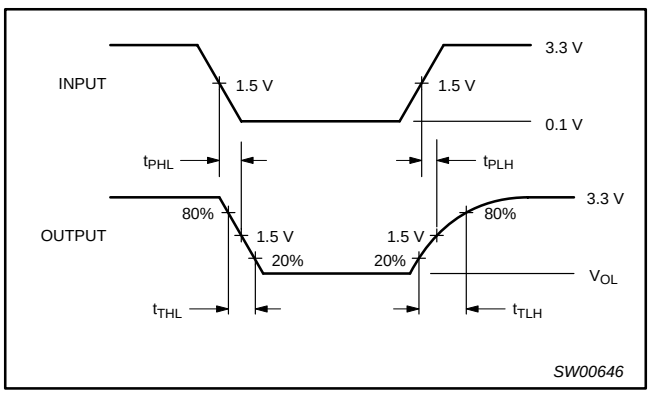
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
t_{PHL}	Propagation delay	Waveform 1	57	115	170	ns
t_{PLH}	Propagation delay	Waveform 1	33	55	78	ns
t_{THL}	Transition time	Waveform 1		67		ns
t_{TLH}	Transition time	Waveform 1; Note 1		135		ns
t_{SET}	Enable to Start condition		100			ns
t_{HOLD}	Enable after Stop condition		100			ns

NOTE:

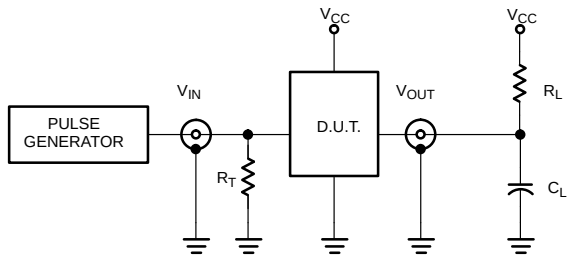
1. The t_{TLH} transition time is guaranteed with loads of 1.35 kΩ pull-up resistance and 7 pF load capacitance, plus an additional 50 pF load capacitance. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

AC WAVEFORMS



Waveform 1.

TEST CIRCUIT



Test Circuit for Open Drain Outputs

DEFINITIONS

R_L = Load resistor; 1.35 kΩ

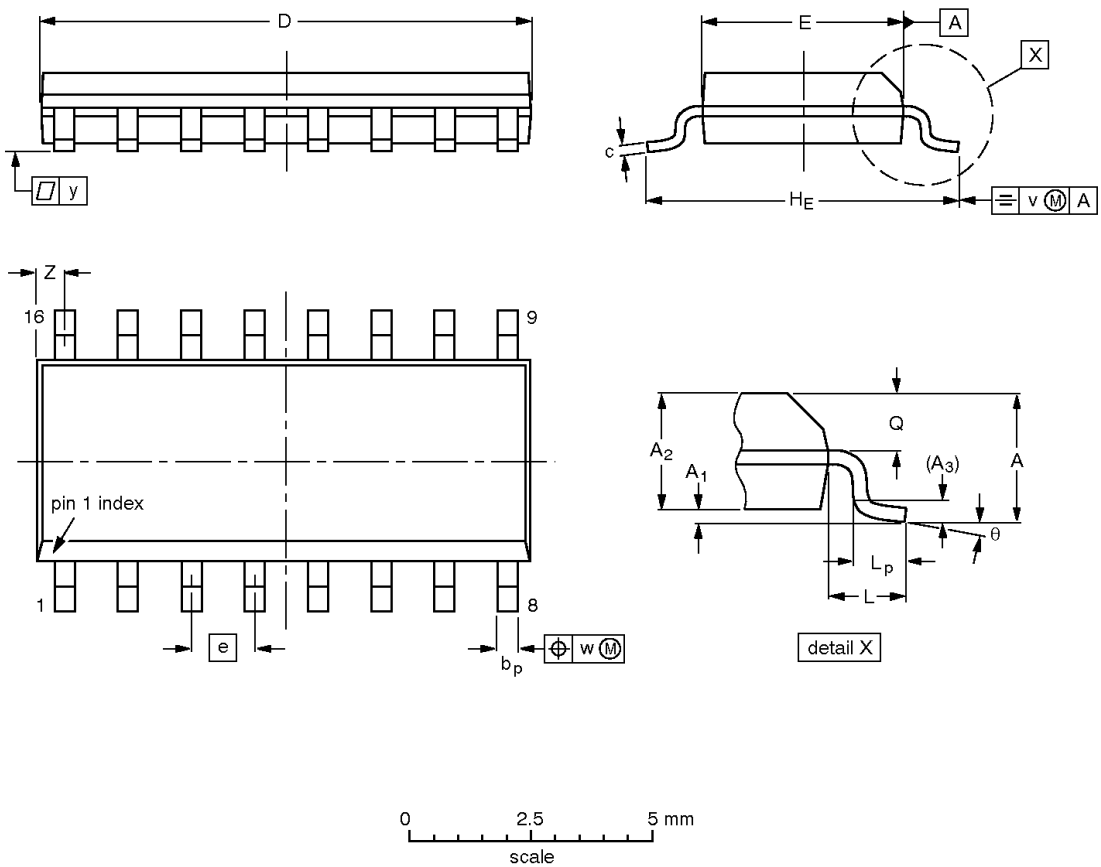
C_L = Load capacitance includes jig and probe capacitance; 7 pF

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00792

Figure 7. Test circuit

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

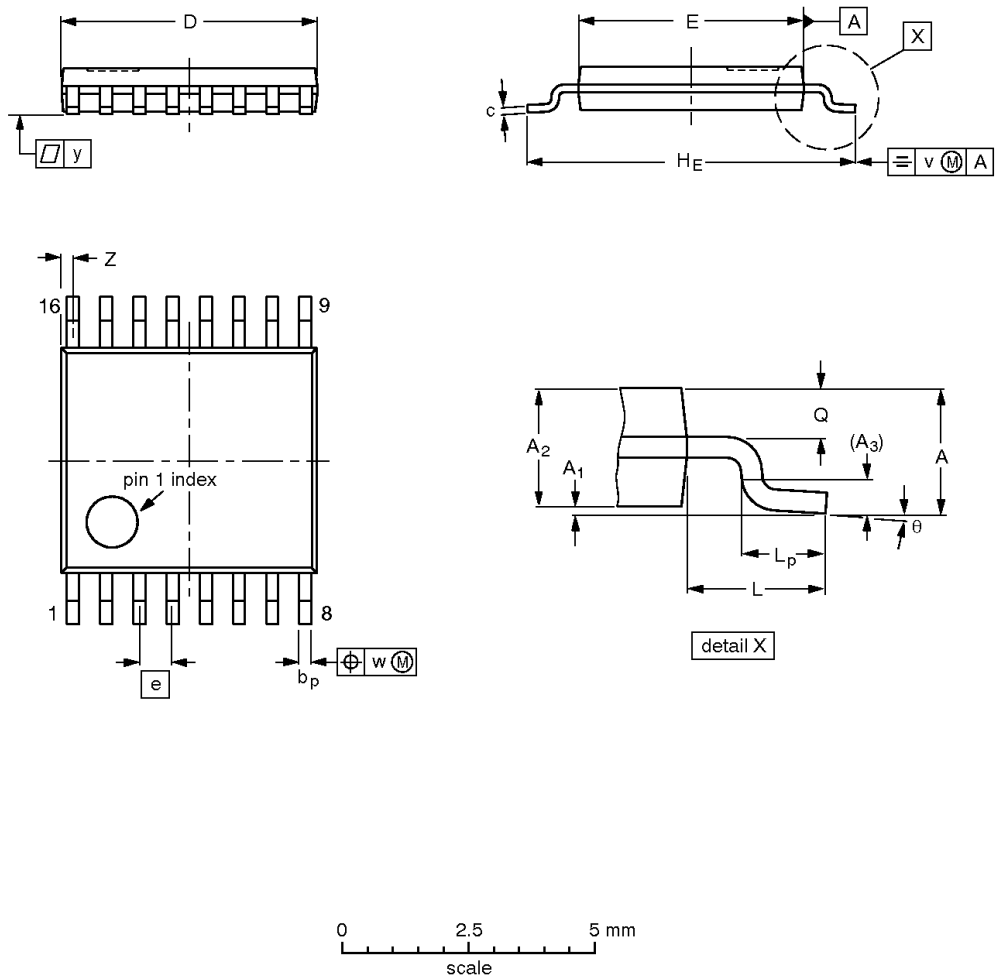
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
_4	20031110	**Product data (9397 750 12291); ECN 853-2234 30410 dated 03 October 2003. Supersedes data of 2002 May 13 (9397 750 09814).** Modifications: • Added additional text to the description to better describe the operation of the device and how it operates with other bus buffers.
_3	20020513	Product data (9397 750 09815); ECN: 853-2234 28185 (2002 May 13)

5-channel I²C hub PCA9516

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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