FAIRCHILD SEMICONDUCTOR®

February 2008

MM74HC74A
Dual D-Type Flip-Flop with Preset and Clear

Features

- Typical propagation delay: 20ns
- Wide power supply range: 2V–6V
- Low quiescent current: 40µA maximum (74HC Series)
- Low input current: 1µA maximum
- Fanout of 10 LS-TTL loads

General Description

The MM74HC74A utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Ordering Information

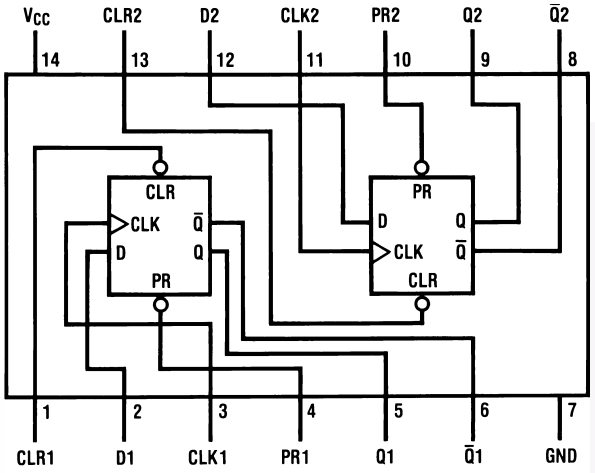
Order Number	Package Number	Package Description
MM74HC74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC74ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC74AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Truth Table

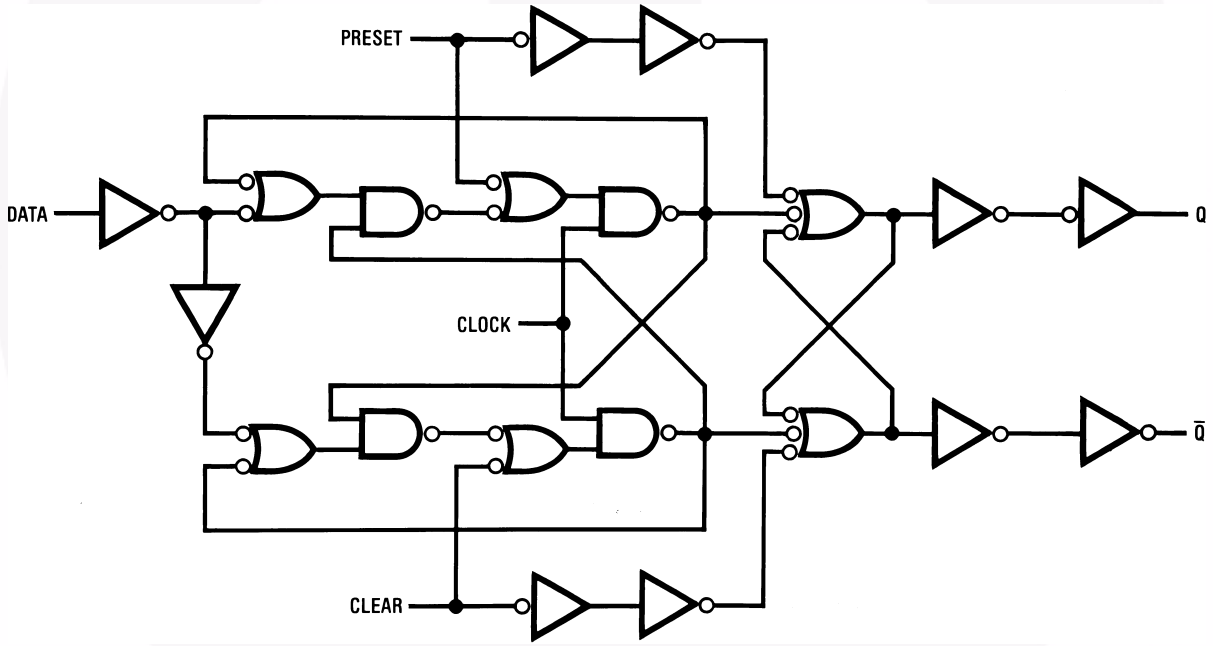
Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note:

Q0 = the level of Q before the indicated input conditions were established.

1. This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

Logic Diagram



Absolute Maximum Ratings(2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC}+1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC}+0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation Note 3	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

2. Unless otherwise specified all voltages are referenced to ground.
3. Power Dissipation temperature derating — plastic “N” package: –12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise or Fall Times V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics[4]

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$	$T_A = -40°C$ to 85°C	$T_A = -55°C$ to 125°C	Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	2.0			1.5	1.5	1.5	V
		4.5			3.15	3.15	3.15	
		6.0			4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage	2.0			0.5	0.5	0.5	V
		4.5			1.35	1.35	1.35	
		6.0			1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 20\mu A$	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 4.0mA$	4.3	3.98	3.84	3.7	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 5.2mA$	5.2	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 20\mu A$	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 4.0mA$	0.2	0.26	0.33	0.4	
		6.0	$\|V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT}\| \le 5.2mA$	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	6.0	$V_{I N} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		4.0	40	80	µA

Note:

4. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, $t_r = t_f = 6ns$

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		72	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation, Delay Clock to Q or $\overline{Q}$		10	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation, Delay Preset or Clear to Q or $\overline{Q}$		17	40	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		6	5	ns
t_s	Minimum Setup Time, Data to Clock		10	20	ns
t_H	Minimum Hold Time, Clock to Data		0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics

C_L = 50 pF, $t_r = t_f$ = 6ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C	T_A = –40°C to 85°C	T_A = –55°C to 125°C		Units
				Typ.	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0	22	6	5	4	MHz
			4.5	72	30	24	20	
			6.0	94	35	28	24	
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0	34	110	140	165	ns
			4.5	12	22	28	33	
			6.0	10	19	24	28	
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear to Q or $\overline{Q}$		2.0	66	150	190	225	ns
			4.5	20	30	38	45	
			6.0	16	26	33	38	
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		2.0	20	50	65	75	ns
			4.5	6	10	13	15	
			6.0	5	9	11	13	
t_s	Minimum Setup Time Data to Clock		2.0	35	80	100	120	ns
			4.5	10	16	20	24	
			6.0	8	14	17	20	
t_H	Minimum Hold Time Clock to Data		2.0		0	0	0	ns
			4.5		0	0	0	
			6.0		0	0	0	
t_W	Minimum, Pulse Width Clock, Preset or Clear		2.0	30	80	101	119	ns
			4.5	9	16	20	24	
			6.0	8	14	17	20	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0	25	75	95	110	ns
			4.5V	7	15	19	22	
			6.0V	6	13	16	19	
t_r, t_f	Maximum Input Rise and Fall Time		2.0		1000	1000	1000	ns
			4.5		500	500	500	
			6.0		400	400	400	
C_{PD}	Power Dissipation Capacitance(5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note:

5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions

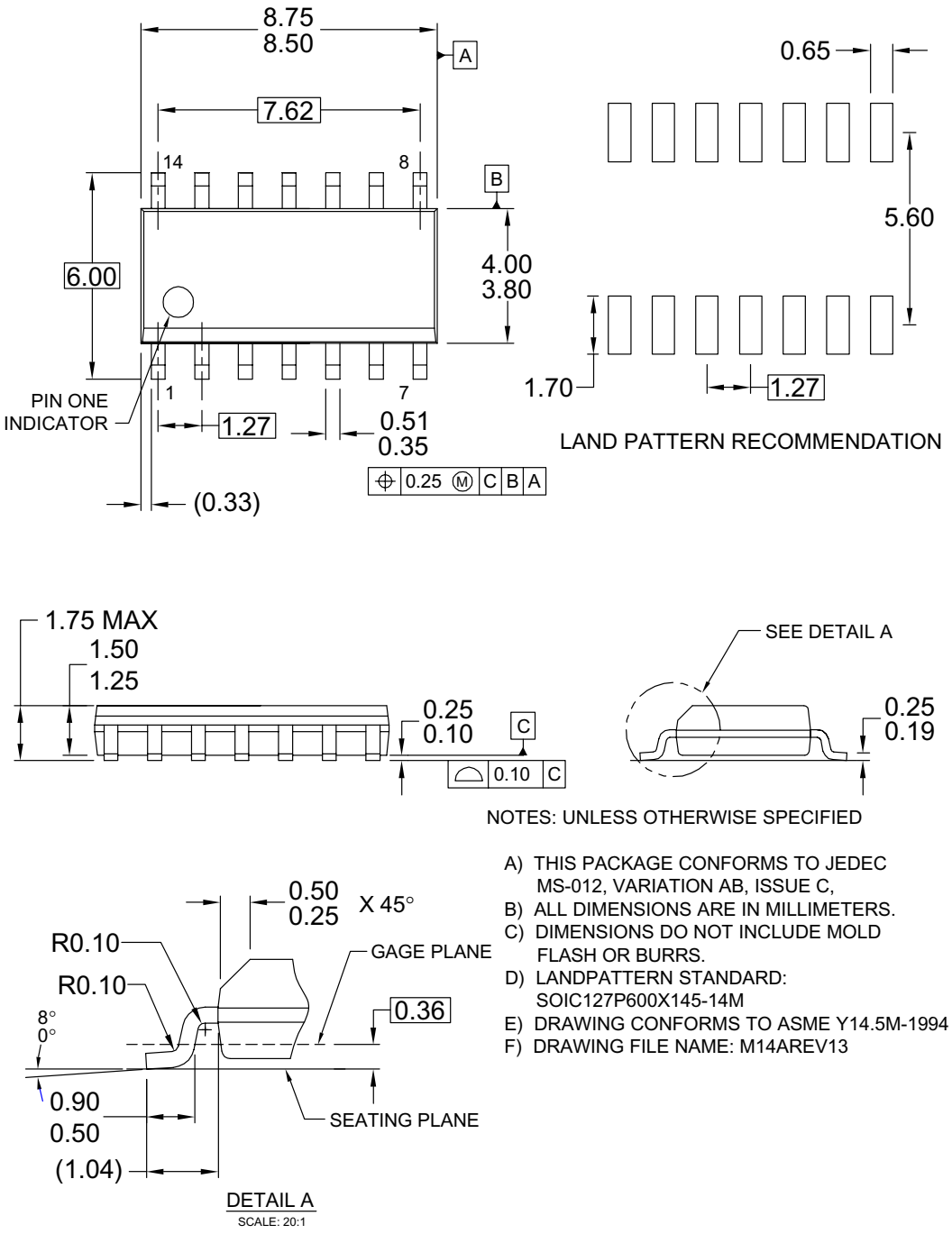


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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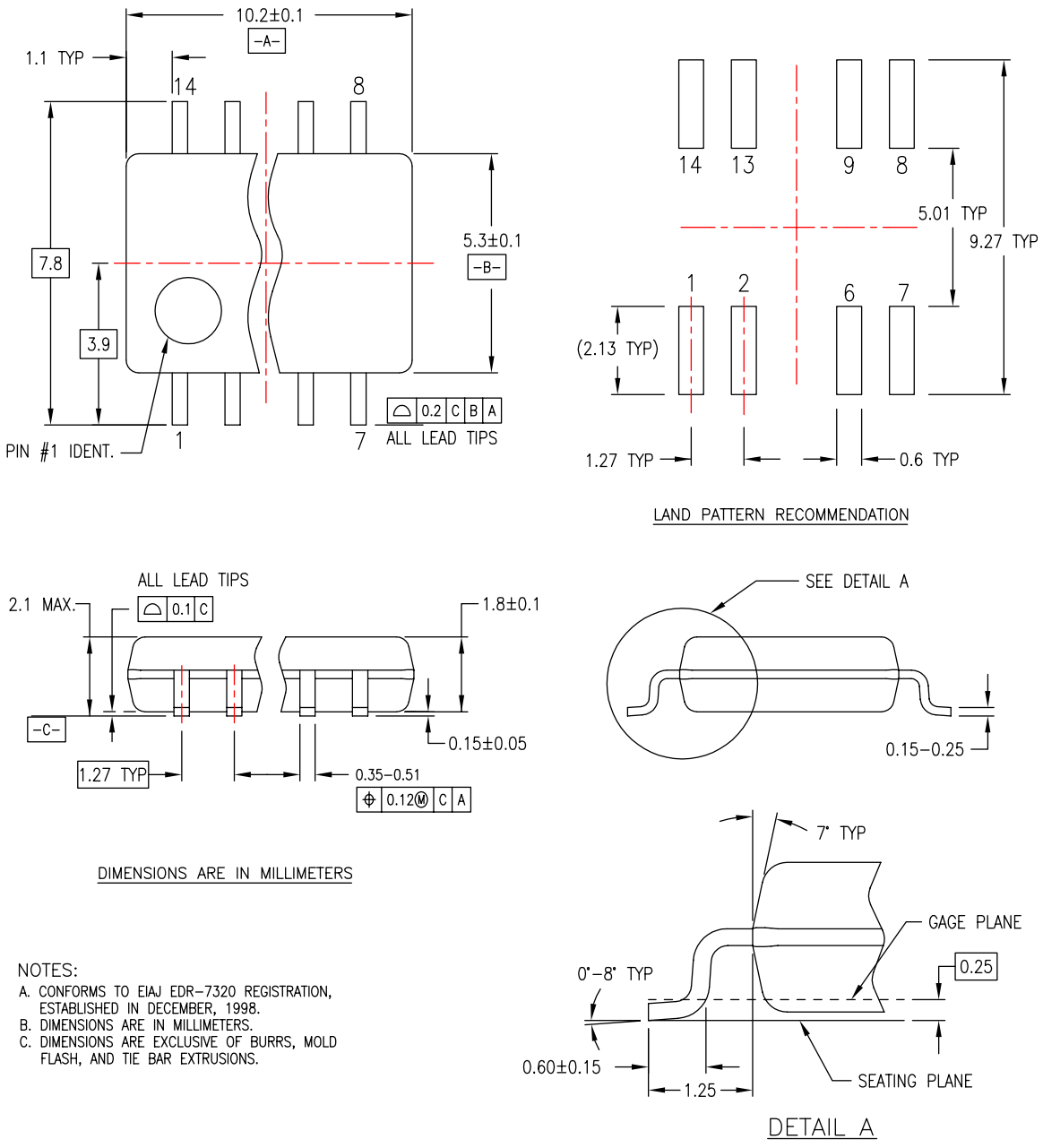
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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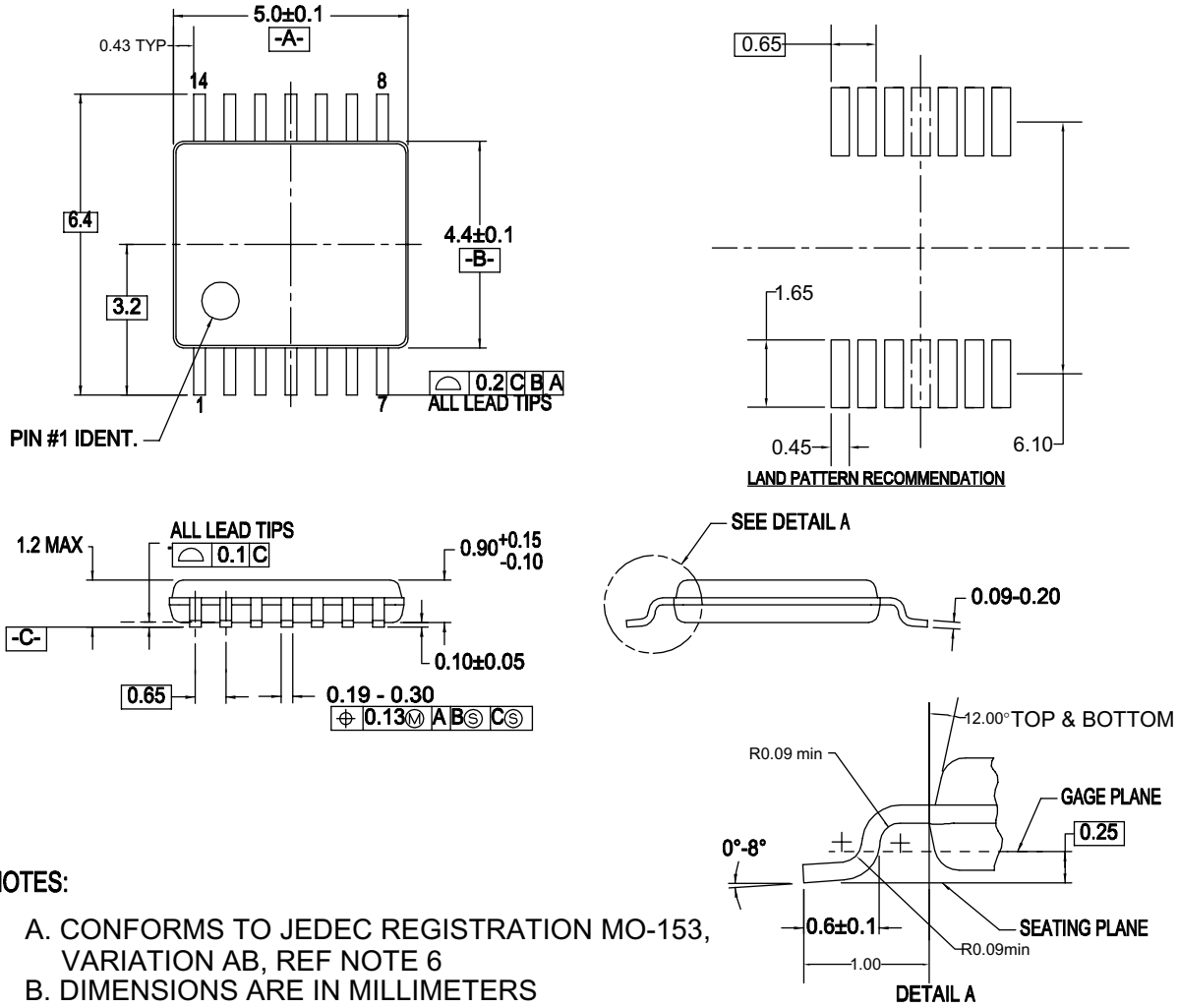
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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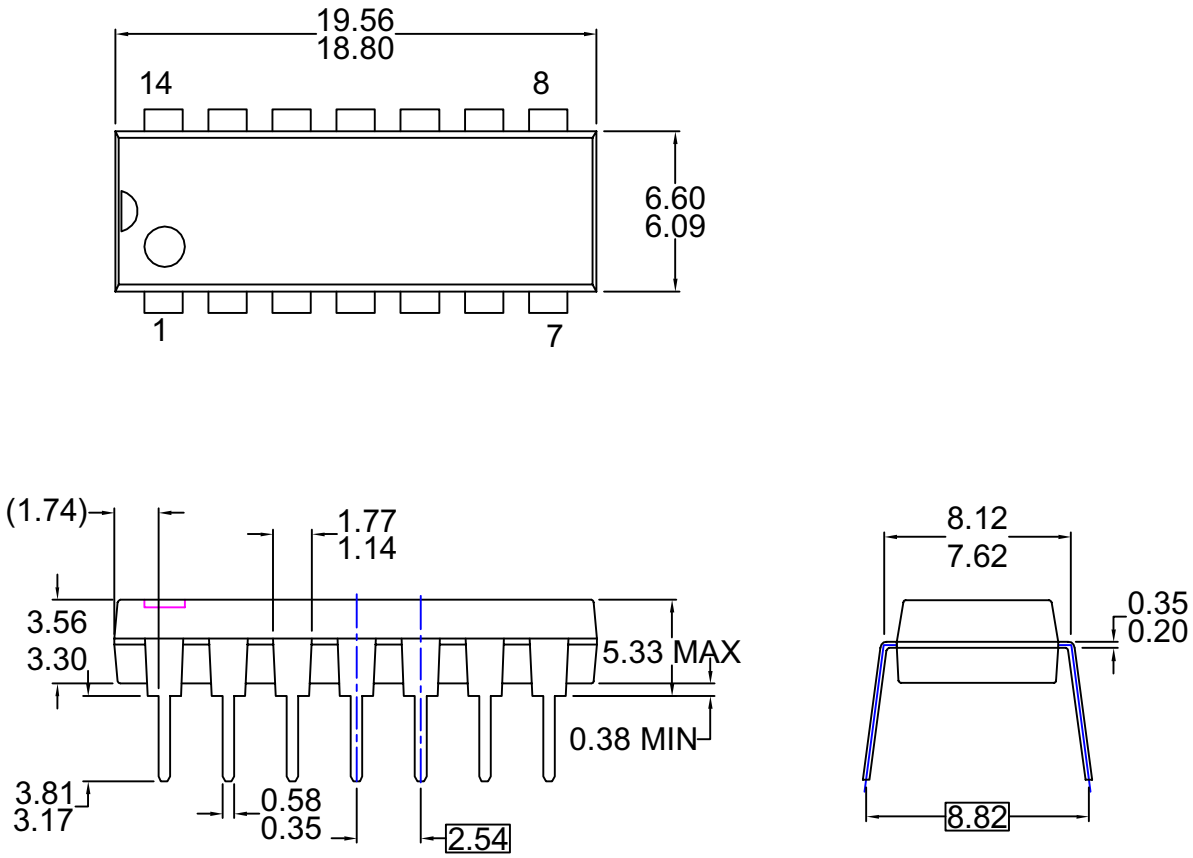
Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

THIS PACKAGE CONFORMS TO

A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.
DIMENSIONS ARE EXCLUSIVE OF BURRS,

C) MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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