

Evaluation Board for AD5696R/AD5696/AD5694R/AD5694 16-Bit/12-Bit, Quad Channel Voltage Output DAC

FEATURES

Full-featured evaluation board for the [AD5696R](#), [AD5696](#), [AD5694R](#), and [AD5694](#)

On-board references

Various link options

PC control in conjunction with Analog Devices, Inc., [system demonstration platform \(SDP\)](#)

PACKAGE CONTENTS

[AD5696/AD5696R](#) or [AD5694/AD5694R](#) evaluation board
CD includes

Self-installing software that allows users to control the board and exercise all functions of the device

Electronic version of the [AD5696R](#), [AD5696](#), [AD5694R](#), and [AD5694](#) data sheets

Electronic version of UG-532

GENERAL DESCRIPTION

This user guide details the operation of the evaluation board for the [AD5696R](#), [AD5696](#), [AD5694R](#), and [AD5694](#) quad channel, voltage output digital-to-analog converters (DACs).

The [EVAL-AD5696RSDZ](#) supports both the [AD5696R](#) and [AD5696](#), and the [EVAL-AD5694RSDZ](#) supports both the [AD5694R](#) and [AD5694](#).

AD569x(R) is used in this user guide to refer to the [AD5696R](#), [AD5696](#), [AD5694R](#), and [AD5694](#).

The evaluation board is designed to help customers quickly prototype new AD569x(R) circuits and reduce design time. The AD569x(R) operates from a single 2.7 V to 5.5 V supply. The [AD5696R](#) and [AD5694R](#) incorporate an internal 2.5 V reference to give an output voltage span of 2.5 V or 5 V. The [AD5696](#) and [AD5694](#) require an external reference.

Full data on the AD569x(R) can be found in the appropriate data sheet available from Analog Devices and should be consulted in conjunction with this user guide when using the evaluation board.

The evaluation board interfaces to the USB port of a PC via the [SDP](#) board. Software is supplied with the evaluation board to allow the user to program the AD569x(R).

This evaluation board requires the [EVAL-SDP-CB1Z](#) board (SDP-B controller board), which is available for order on the Analog Devices website at www.analog.com.

EVALUATION BOARD BLOCK DIAGRAM

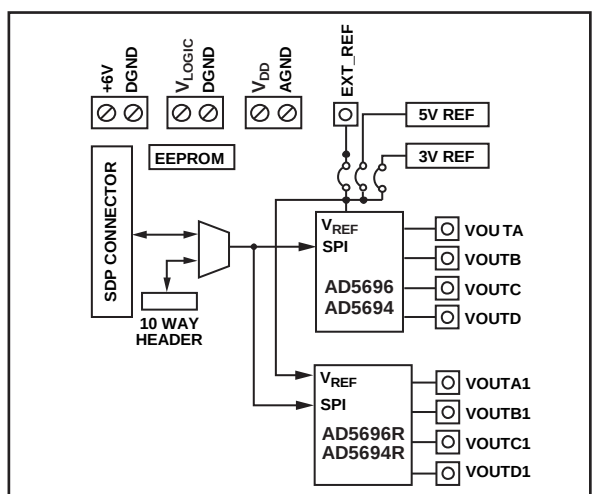


Figure 1.

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REVISION HISTORY

3/13—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

To use the evaluation board with the [SDP](#) board, a 6 V power supply is required, which is connected to Connector J3. The evaluation board can be used without the SDP board. In this case, the J1 and J2 connectors are used as the power supply inputs.

Both AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location close to the AD569x(R). It is recommended that AGND and DGND not be connected elsewhere in the system to avoid ground loop problems.

All supplies are decoupled to ground with 10 μ F tantalum and 0.1 μ F ceramic capacitors.

Table 1. Power Supply Connectors

Connector Number	Voltage
J1	External, V_{LOGIC} supply
J2	Analog power supply, V_{DD}
J3	6 V board positive power supply

LINK OPTIONS

A number of link options are incorporated in the evaluation board and must be set for the required operating conditions before using the board. The functions of these link options are described in detail in Table 3. Table 2 lists the positions of the different links controlled by PC, via the USB port, and the SDP board in single-supply mode is required.

Table 2. Link Options Setup for SDP Control (Default)

Link Number	Option
LK1	A
LK2	A
LK3	A
LK4	A
LK5	A
LK6	A

Table 3. Link Functions

Link Number	Option
LK1	This link selects the DAC analog voltage source. Position A selects the internal voltage source (INT_VDD) from the ADP3331 . Position B selects an external supply voltage (EXT_VDD).
LK2	This link selects the DAC digital voltage (V_{LOGIC}) source. Position A selects the digital voltage source from the SDP board (V_{IO}). Position B selects an external digital supply voltage (EXT_VLOGIC). Position C selects the same supply as the V_{DD} pin.
LK3	This link selects the reference source for the AD5696/AD5694 . Position A selects the internal reference of the AD5696R/AD5694R as the reference source for the AD5696/AD5694 . Position B selects the on-board 2.5 V reference as the reference source. Position C selects the on-board 5 V reference as the reference source. Position D selects an off board voltage reference via the EXT_REF connector.
LK4	This link selects the gain setting of the AD5696/AD5694 . Position A selects gain of 2. Position B selects gain of 1.
LK5	This link selects the gain setting of the AD5696R/AD5694R . Position A selects gain of 2. Position B selects gain of 1.
LK6	This link selects which supply the I ² C pull up resistors are connected to. Position A selects V_{IO} . This option should be used when the board is connected to the SDP. Position B selects VLOGIC. This option should be used when the SDP is not used.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The evaluation kit for the AD569x(R) includes self-installing software on the CD. The software is compatible with Windows® XP, Windows Vista (32-bit), and Windows 7 (32-bit and 64-bit). The software must be installed before connecting the SDP board to the USB port of the PC to ensure that the SDP board is recognized when it connects to the PC.

To install the software, take the following steps:

1. Start the Windows operating system and insert the CD.
2. The installation software should open automatically. If it does not open automatically, run the **setup.exe** file from the CD.
3. After installation is complete, power up the evaluation board as described in the Power Supplies section.
4. Connect the evaluation board to the SDP board and the SDP board into the PC using the USB cable included in the box.
5. When the software detects the evaluation board, proceed through any dialog boxes that appear to finalize the installation.

RUNNING THE SOFTWARE

To run the program, do the following:

1. Connect the evaluation board to the SDP board and connected the USB cable between the SDP board and the PC.
2. Power the SDP and the evaluation board by connecting 6 V to the J3 connector.

3. Click **Start > All Programs > Analog Devices > AD56x(R)**. Each **AD5696R**, **AD5696**, **AD5694R**, and **AD5694** has its own version of software. Click the appropriate one to run the software. As the software connects to the evaluation board, the message in Figure 2 displays.

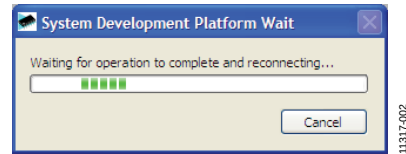


Figure 2. Connection Message

If the SDP board is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 3). Simply connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

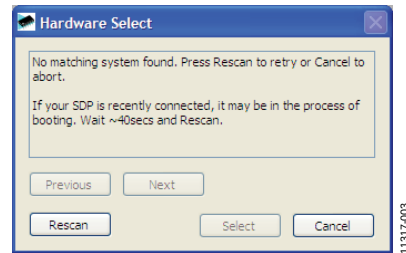


Figure 3. Connectivity Error

Alternatively, the software can be used without an evaluation board. The software runs in simulation mode displaying expected outputs based on the input data. The main window of the AD569x(R) evaluation software then opens, as shown in Figure 4.

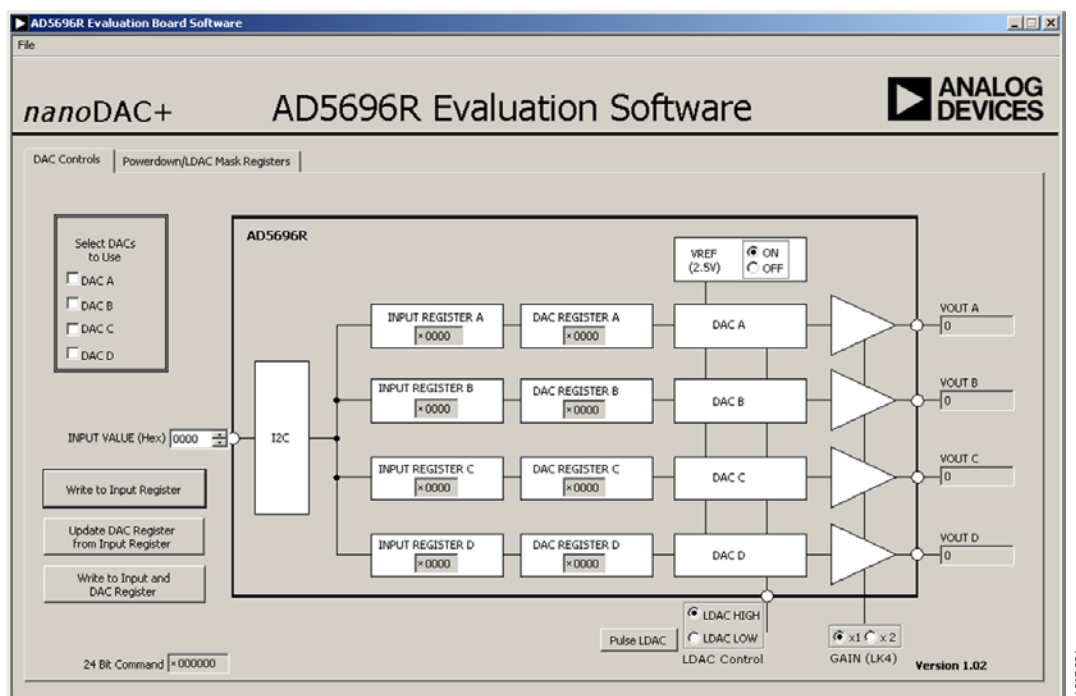


Figure 4. AD569x(R) Evaluation Board Software Main Window

SOFTWARE OPERATION

The software for the AD569x(R) allows the user to program values to the input and DAC registers of each DAC individually or collectively.

Write to Input Register

Select **Write to Input Register** to load the value in the input data control to the input register of any DACs selected in the **Select DACs to Use** box.

Update DAC Register from Input Register

Select **Update DAC Register from Input Register** to copy the value in a DAC input register to the corresponding DAC register. DAC outputs are automatically updated with the appropriated voltage.

Write to Input and DAC Register

Select **Write to DAC Register** to load the value in the input data control to the Input and DAC register of any DACs selected in the **Select DACs to Use** box. The DAC outputs are automatically updated with the appropriated voltage.

LDAC CONTROL

Select **Pulse LDAC** to bring the $\overline{\text{LDAC}}$ pin low and then back high. This copies the data from the input registers to the DAC registers, and the outputs update accordingly. Any DAC updates disabled by the LDAC mask settings are ignored.

The $\overline{\text{LDAC}}$ pin can also be set high or low by clicking the appropriate radio button.

GAIN Control

The logic level of the GAIN pin is set externally by LK4 or LK5. To display the correct voltage, the gain selection must be set to match the level of the pin.

Reference Control

The AD5696R and AD5694R have an on-chip reference that can be disabled to reduce power consumption. The AD5696R and AD5694R software has a control that allows this function to be used.

The AD5696 and AD5694 require an external reference. The software for the AD5696 and AD5694 has a control that allows the user to set the reference voltage.

Power-Down Control

Each of the DACs can be powered down individually. Each of the DACs has an associated selection box allowing the part to operate in normal mode, powered down with either a 1 k Ω or a 100 k Ω resistor to ground or tristate. When the power-down setting for each DAC is selected, click **Write to Part** to write the appropriate values to the AD569x(R).

LDAC Mask Register

Each of the DACs can be set to accept or ignore $\overline{\text{LDAC}}$ pulses by writing to the LDAC Mask Register. When the LDAC selections are completed, click **Write to Part** to write the appropriate values to the AD569x(R).

24-BIT COMMAND

On both control tabs of the software, the 24-bit commands sent to the DAC are displayed. This shows what must be written to the AD569x(R) to replicate the function of the evaluation board.

EVALUATION BOARD SCHEMATICS AND ARTWORK

13131-005

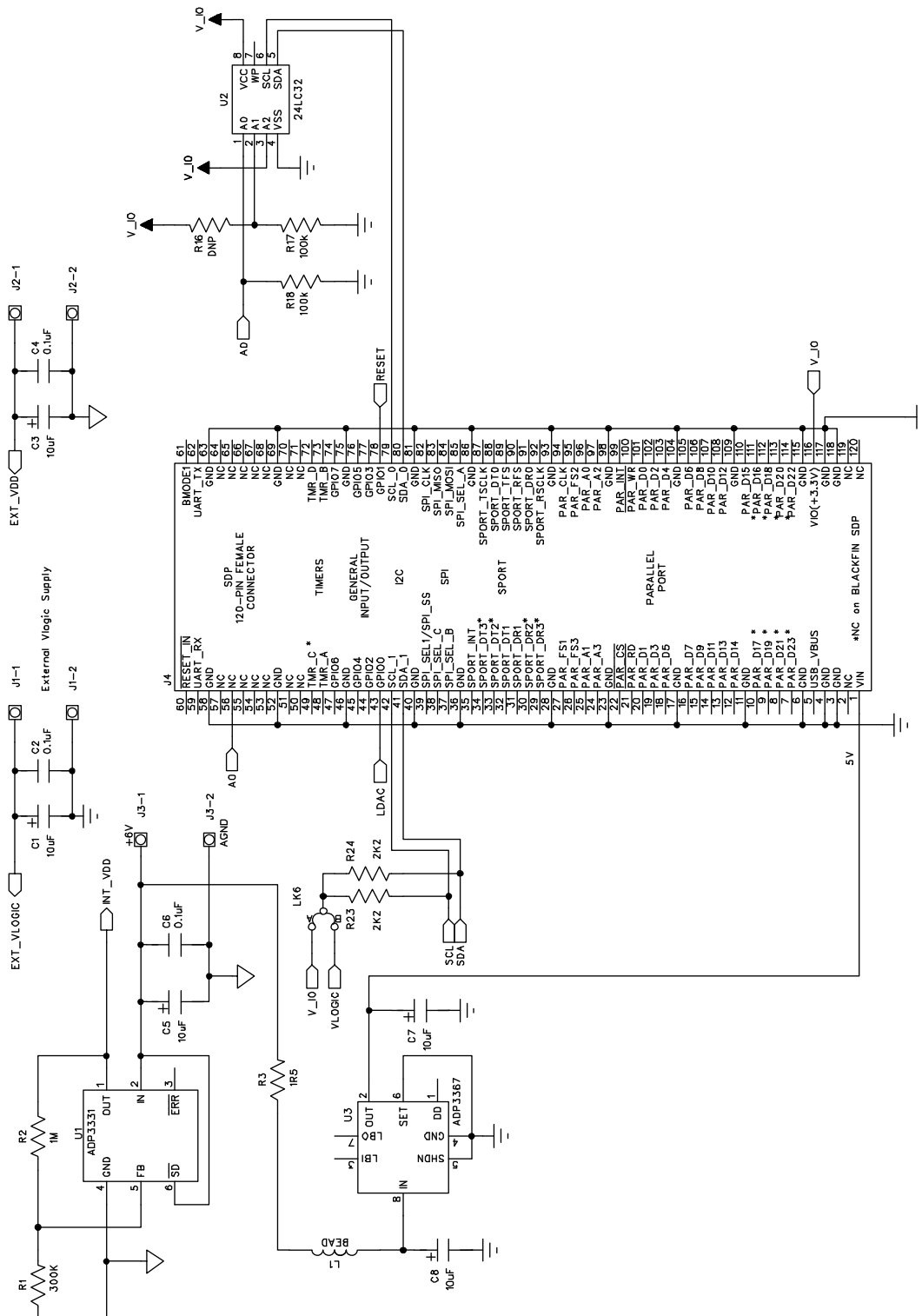


Figure 5. AD569x(R) Schematic (Page 1 of 2)

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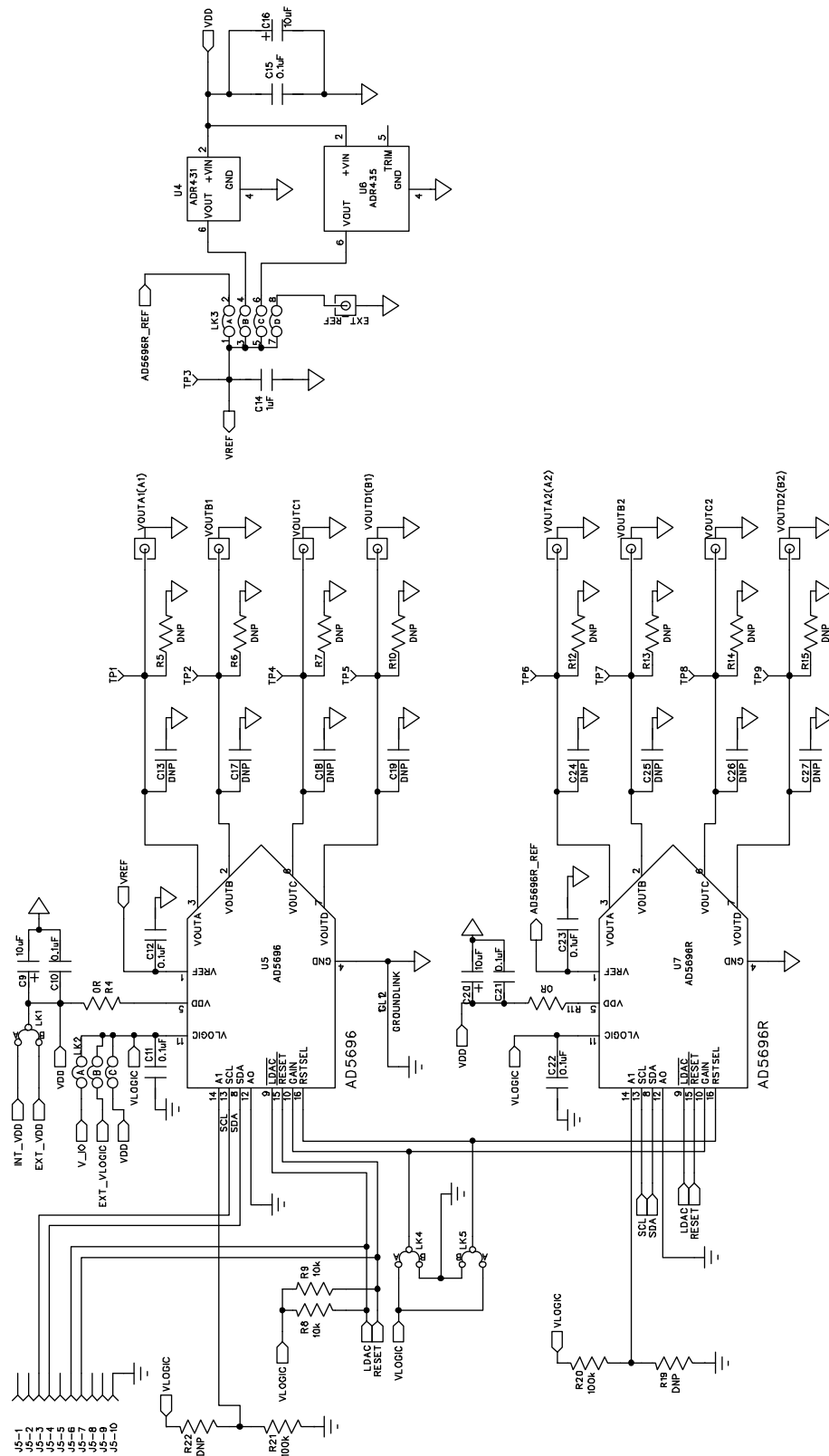


Figure 6. AD569x(R) Schematic (Page 2 of 2)

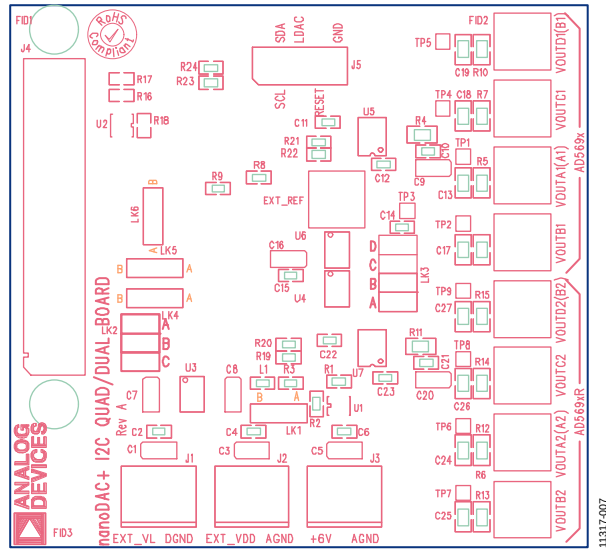


Figure 7. AD569x(R) Component Silkscreen

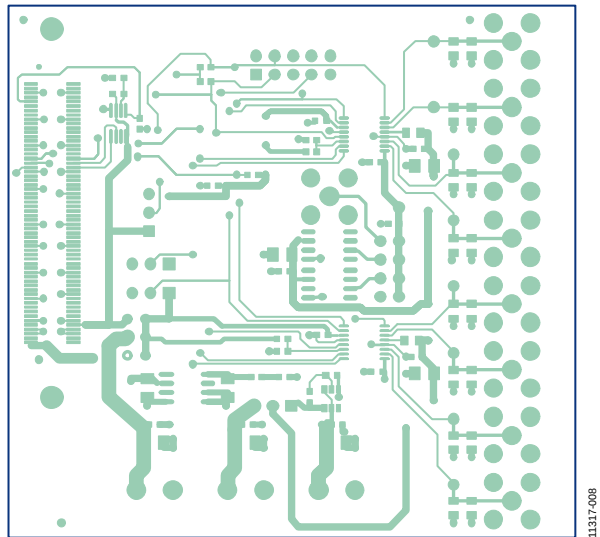


Figure 8. AD569x(R) Top Side Routing

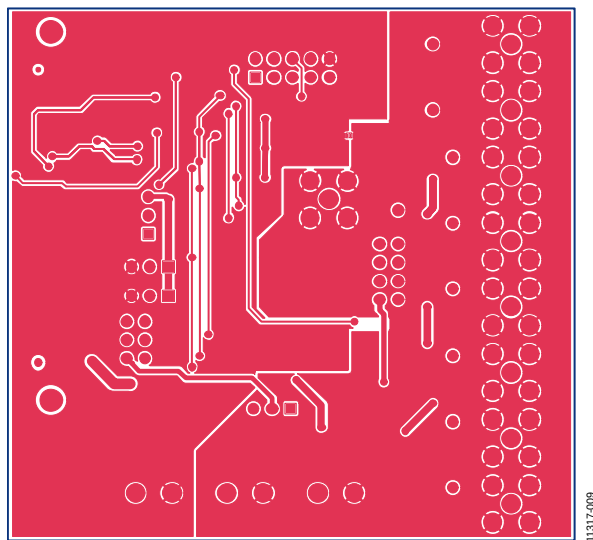


Figure 9. AD569x(R) Bottom Side Routing

ORDERING INFORMATION

COMPONENTS LIST

Table 4.

Qty	Reference Designator	Description	Supplier/Part Number
8	C1, C3, C5, C7, C8, C9, C16, C20	10 μ F, 10 V capacitor, Case A	FEC 197-130
10	C2, C4, C6, C10 to C12, C15, C21 to C23	100 nF, 50 V capacitor, 0603	FEC 8820023
8	C13, C17 to C19, C24 to C27	N/A	Not inserted
1	C14	1 μ F, 10 V capacitor, 0603,	FEC 318-8840
3	J1, J2, J3	2-pin terminal block (5 mm pitch)	FEC 151789
1	J4	120-way female connector, 0.6mm pitch	FEC 1324660 or Digi-Key H1219-ND
1	J5	10-pin (2 $\times$ 5) 0.1" pitch SMT header	FEC 1022244 (36-pin strip)
1	L1	Ferrite bead	Digi-Key 490-1024-1-ND
4	LK1, LK4, LK5, LK6	Jumper block using 3-pin SIP header	FEC 1022248 and 150410
1	LK2	6-pin (3 $\times$ 2) 0.1" header and shorting block	FEC 148-535 and 150-411 (36-pin strip)
1	LK3	8-pin (4 $\times$ 2) 0.1" header and shorting block	FEC 1022244 and 150-411 (36-pin strip)
1	R1	300 k Ω resistor, 0603	Digi-Key 541-300KHCT-ND
1	R2	1 M Ω resistor, 0603	Digi-Key RMC1/161MFRCT-ND
1	R3	1.5 Ω resistor, 0603	FEC 9331832
2	R4, R11	0 Ω resistor, 0805	FEC 9333681
11	R5 to R7, R10, R12 to R16, R19, R22	N/A	Not inserted
2	R8 to R9	10 k Ω resistor, 0603	FEC 933-0399
4	R17 to R18, R20 to R21	10 k Ω resistor, 0603	FEC 933-0402
2	R23, R24	2.2 k Ω resistor, 0603	FEC 157 7611
9	TP1 to TP9	Red test point	FEC 8731144 (pack)
1	U1	Adjustable LDO regulator	Analog Devices ADP3331 ARTZ
1	U2	32K I ² C serial EEPROM	FEC 1331330
1	U3	+5 V voltage regulator	Analog Devices ADP3367 ARZ
1	U4	Voltage reference	Analog Devices ADR431 ARZ
1	U5	Quad, 16-/16-Bit <i>nano</i> DAC+ with I ² C interface	Analog Devices AD5694 BRUZ/ AD5696 BRUZ
1	U6	Voltage reference	Analog Devices ADR435 ARZ
1	U7	Quad, 16-/16-bit <i>nano</i> DAC+ with 2 ppm/ $^{\circ}$ C on-chip reference and I ² C interface	Analog Devices AD5694R BRUZ/ AD5696R BRUZ
9	EXT_REF, VOUTA1, VOUTA2, VOUTB1, VOUTB2, VOUTC1, VOUTC2, VOUTD1, VOUTD2	Straight PCB mount SMB jack-50 Ω	FEC 1206013

NOTES

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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