

FEATURES

Precision supply voltage monitor

2.63 V (ADM706P, ADM706R, ADM708R)

2.93 V (ADM706S, ADM708S)

3.08 V (ADM706T, ADM708T)

100 μ A quiescent current

200 ms reset pulse width

Debounced manual reset input ($\overline{\text{MR}}$)

Independent watchdog timer

1.6 sec timeout (ADM706x)

Reset Output

Active high (ADM706P)

Active low (ADM706R/ADM706S/ADM706T)

Both active high and active low

(ADM708R/ADM708S/ADM708T)

Voltage monitor for power-fail or low battery warning

Guaranteed $\overline{\text{RESET}}$ valid with $V_{\text{CC}} = 1 \text{ V}$

Superior upgrade for MAX706P/R/S/T, MAX708R/S/T

APPLICATIONS

Microprocessor systems

Computers

Controllers

Intelligent instruments

Critical microprocessor monitoring

Automotive systems

Battery-operated systems

Portable instruments

GENERAL DESCRIPTION

The ADM706P/ADM706R/ADM706S/ADM706T and the ADM708R/ADM708S/ADM708T microprocessor supervisory circuits are suitable for monitoring either 3 V or 3.3 V power supplies.

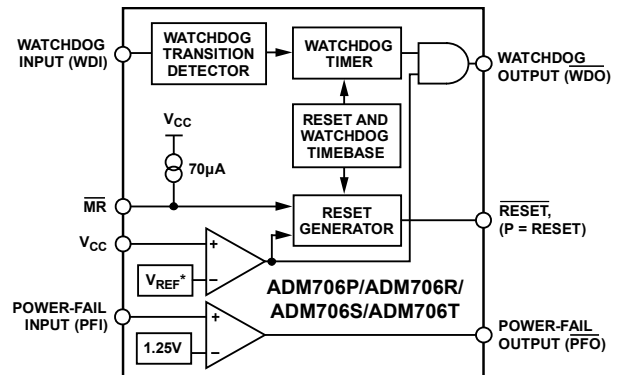
The ADM706P/ADM706R/ADM706S/ADM706T provide the following functions:

1. Power-supply monitoring circuitry that generates a reset output during power-up, power-down, and brownout conditions. The reset output remains operational with V_{CC} as low as 1 V.
2. Independent watchdog monitoring circuitry that is activated if the watchdog input has not been toggled within 1.6 sec.
3. A 1.25 V threshold detector for power-fail warning, low battery detection, or to monitor an additional power supply.
4. An active low debounced $\overline{\text{MR}}$ input.

Rev. B

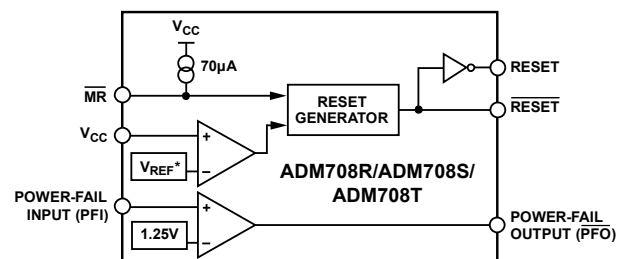
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

FUNCTIONAL BLOCK DIAGRAMS



* VOLTAGE REFERENCE = 2.63V (P/R), 2.93V (S), 3.08V (T)

Figure 1. ADM706P/ADM706R/ADM706S/ADM706T



* VOLTAGE REFERENCE = 2.63V (R), 2.93V (S), 3.08V (T)

Figure 2. ADM708R/ADM708S/ADM708T

The ADM706R, ADM706S, and ADM706T are identical except for the reset threshold monitor levels, which are 2.63 V, 2.93 V, and 3.08 V, respectively. The ADM706P is identical to the ADM706R in that the reset threshold is 2.63 V. It differs only in that it has an active high reset output.

The ADM708R/ADM708S/ADM708T provide the same functionality as the ADM706R/ADM706S/ADM706T and only differ in that:

1. A watchdog timer function is not available.
2. An active high reset output (RESET) in addition to the active low ($\overline{\text{RESET}}$) output is available.

All parts are available in narrow 8-lead PDIP and 8-lead SOIC packages.

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

TABLE OF CONTENTS

Features	1	Power-Fail Reset	9
Applications.....	1	Manual Reset.....	9
Functional Block DiagramS	1	Watchdog Timer (ADM706x)	9
General Description	1	Power-Fail Comparator	10
Revision History	2	Adding Hysteresis to the Power-Fail Comparator	10
Specifications.....	3	Valid $\overline{\text{RESET}}$ Below 1 V V_{CC}	10
Absolute Maximum Ratings.....	5	Applications Information	11
ESD Caution.....	5	Monitoring Additional Supply Levels.....	11
Pin Configuration and Function Descriptions.....	6	Microprocessors with Bidirectional $\overline{\text{RESET}}$	11
Typical Performance Characteristics	7	Outline Dimensions	12
Circuit Information	9	Ordering Guide	13

REVISION HISTORY

2/07—Rev. A to Rev. B

Updated Format	Universal
Changes to Table 1	3
Updated Outline Dimensions	12
Changes to Ordering Guide	13

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

SPECIFICATIONS

$V_{CC} = 2.70\text{ V to }5.5\text{ V}$ (ADM706P/ADM70xR), $V_{CC} = 3.00\text{ V to }5.5\text{ V}$ (ADM70xS), $V_{CC} = 3.15\text{ V to }5.5\text{ V}$ (ADM70xT), $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		100	200	μA	$V_{CC} < 3.6\text{ V}$
		150	350	μA	$V_{CC} < 5.5\text{ V}$
LOGIC OUTPUT					
Reset Threshold (V_{RST})	2.55	2.63	2.70	V	ADM706P/ADM70xR
	2.85	2.93	3.00	V	ADM70xS
	3.00	3.08	3.15	V	ADM70xT
Reset Threshold Hysteresis		20		mV	
RESET PULSE WIDTH					
	160	200	280	ms	ADM706P/ADM70xR, $V_{CC} = 3\text{ V}$
	160	200	280	ms	ADM70xS/T, $V_{CC} = 3.3\text{ V}$
		200		ms	$V_{CC} = 5.0\text{ V}$
RESET OUTPUT VOLTAGE (ADM70xR/ADM70xS/ADM70xT)					
V_{OH}	$0.8 \times V_{CC}$			V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$, $I_{SOURCE} = 500\ \mu\text{A}$
V_{OL}			0.3	V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$, $I_{SINK} = 1.2\text{ mA}$
V_{OH}	$V_{CC} - 1.5\text{ V}$			V	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $I_{SOURCE} = 800\ \mu\text{A}$
V_{OL}			0.4	V	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $I_{SINK} = 3.2\text{ mA}$
V_{OL}			0.3	V	$V_{CC} = 1\text{ V}$, $I_{SINK} = 100\ \mu\text{A}$
RESET OUTPUT VOLTAGE (ADM706P)					
V_{OH}	$V_{CC} - 0.6\text{ V}$			V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$, $I_{SOURCE} = 215\ \mu\text{A}$
V_{OL}			0.3	V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$, $I_{SINK} = 1.2\text{ mA}$
V_{OH}	$V_{CC} - 1.5\text{ V}$			V	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $I_{SOURCE} = 800\ \mu\text{A}$
V_{OL}			0.4	V	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $I_{SINK} = 3.2\text{ mA}$
RESET OUTPUT VOLTAGE (ADM708x)					
V_{OH}	$0.8 \times V_{CC}$			V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$, $I_{SOURCE} = 500\ \mu\text{A}$
V_{OL}			0.3	V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$, $I_{SINK} = 500\ \mu\text{A}$
V_{OH}	$V_{CC} - 1.5\text{ V}$			V	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $I_{SOURCE} = 800\ \mu\text{A}$
V_{OL}			0.4	V	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $I_{SINK} = 1.2\text{ mA}$
WATCHDOG INPUT(ADM706x)					
Watchdog Timeout Period	1.00	1.60	2.25	sec	ADM706P/ADM706R: $V_{CC} = 3\text{ V}$; ADM706S/ADM706T: $V_{CC} = 3.3\text{ V}$; $V_{IL} = 0.4\text{ V}$, $V_{IH} = V_{CC} \times 0.8\text{ V}$
WDI Pulse Width	100			ns	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$
	50			ns	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$
WDI Input Threshold					
V_{IL}			0.6	V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$
V_{IH}	$0.7 \times V_{CC}$			V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$
V_{IL}			0.8	V	$V_{CC} = 5.0\text{ V}$
V_{IH}	3.5			V	$V_{CC} = 5.0\text{ V}$
WDI Input Current	-1.0	+0.02	+1.0	μA	WDI = 0 V or V_{CC}
WDO OUTPUT VOLTAGE					
V_{OH}	$0.8 \times V_{CC}$			V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$, $I_{SOURCE} = 500\ \mu\text{A}$
	$V_{CC} - 1.5\text{ V}$			V	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $I_{SOURCE} = 800\ \mu\text{A}$
V_{OL}			0.3	V	$V_{RST}(\text{max}) < V_{CC} < 3.6\text{ V}$, $I_{SINK} = 500\ \mu\text{A}$
			0.4	V	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$, $I_{SINK} = 1.2\text{ mA}$

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MANUAL RESET INPUT					
$\overline{\text{MR}}$ Pull-Up Current ($\overline{\text{MR}} = 0 \text{ V}$)	25	70	250	μA	$V_{\text{RST}}(\text{max}) < V_{\text{CC}} < 3.6 \text{ V}$
	100	250	600	μA	$4.5 \text{ V} < V_{\text{CC}} < 5.5 \text{ V}$
$\overline{\text{MR}}$ Pulse Width	500			ns	$V_{\text{RST}}(\text{max}) < V_{\text{CC}} < 3.6 \text{ V}$
	150			ns	$4.5 \text{ V} < V_{\text{CC}} < 5.5 \text{ V}$
MR INPUT THRESHOLD					
V_{IL}			0.6	V	$V_{\text{RST}}(\text{max}) < V_{\text{CC}} < 3.6 \text{ V}$
V_{IH}	$0.7 \times V_{\text{CC}}$			V	$V_{\text{RST}}(\text{max}) < V_{\text{CC}} < 3.6 \text{ V}$
V_{IL}			0.8	V	$4.5 \text{ V} < V_{\text{CC}} < 5.5 \text{ V}$
V_{IH}	2.0			V	$4.5 \text{ V} < V_{\text{CC}} < 5.5 \text{ V}$
MR TO RESET OUTPUT DELAY					
			750	ns	$V_{\text{RST}}(\text{max}) < V_{\text{CC}} < 3.6 \text{ V}$
			250	ns	$4.5 \text{ V} < V_{\text{CC}} < 5.5 \text{ V}$
POWER-FAIL INPUT					
PFI Input Threshold	1.2	1.25	1.3	V	ADM70xP/ADM70xR, $V_{\text{CC}} = 3 \text{ V}$ ADM70xS/ADM70xT, $V_{\text{CC}} = 3.3 \text{ V}$, PFI falling
PFI Input Current	-25	+0.01	+25	nA	
PFO OUTPUT VOLTAGE					
V_{OH}	$0.8 \times V_{\text{CC}}$			V	$V_{\text{RST}}(\text{max}) < V_{\text{CC}} < 3.6 \text{ V}$, $I_{\text{SOURCE}} = 500 \mu\text{A}$
V_{OL}			0.3	V	$V_{\text{RST}}(\text{max}) < V_{\text{CC}} < 3.6 \text{ V}$, $I_{\text{SINK}} = 1.2 \text{ mA}$
V_{OH}	$V_{\text{CC}} - 1.5 \text{ V}$			V	$4.5 \text{ V} < V_{\text{CC}} < 5.5 \text{ V}$, $I_{\text{SOURCE}} = 800 \mu\text{A}$
V_{OL}			0.4	V	$4.5 \text{ V} < V_{\text{CC}} < 5.5 \text{ V}$, $I_{\text{SINK}} = 3.2 \text{ mA}$

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 2.

Parameter	Rating
V _{CC}	−0.3 V to +6 V
All Other Inputs	−0.3 V to V _{CC} + 0.3 V
Input Current	
V _{CC}	20 mA
GND	20 mA
Digital Output Current	20 mA
Power Dissipation, N-8 (PDIP)	727 mW
θ _{JA} Thermal Impedance	135°C/W
Power Dissipation, R-8 (SOIC)	470 mW
θ _{JA} Thermal Impedance	110°C/W
Operating Temperature Range	
Industrial (Version A)	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Storage Temperature Range	−65°C to +150°C
ESD Rating	>5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

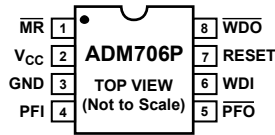


Figure 3. ADM706P

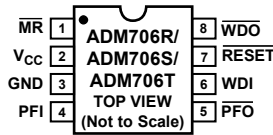


Figure 4. ADM706R/ADM706S/ADM706T

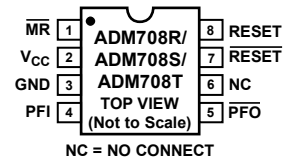


Figure 5. ADM708R/ADM708S/ADM708T

Table 3. Pin Function Descriptions

Mnemonic	Pin No.		Description
	ADM706P/ ADM706R/ ADM706S/ ADM706T	ADM708R/ ADM708S/ ADM708T	
MR	1	1	Manual Reset Input. When taken below 0.6 V a RESET is generated. MR can be driven from TTL, CMOS logic or from a manual reset switch as it is internally debounced. An internal 70 μ A pull-up current holds the input high when floating.
V _{CC}	2	2	Power Supply Input.
GND	3	3	Ground reference for all signals (0 V).
PFI	4	4	Power-Fail Input. PFI is the noninverting input to the power-fail comparator. When PFI is less than 1.25 V, PFO goes low. If unused, PFI should be connected to GND.
PFO	5	5	Power-Fail Output. PFO is the output from the power-fail comparator. It goes low when PFI is less than 1.25 V.
WDI	6	N/A	Watchdog Input. WDI is a 3-level input. If WDI remains either high or low for longer than the watchdog timeout period, the watchdog output WDO goes low. The timer resets with each transition at the WDI input. Either a high-to-low or a low-to-high transition clears the counter. The internal timer is also cleared whenever reset is asserted. The watchdog timer is disabled when WDI is left floating or connected to a three-state buffer.
NC	N/A	6	No Connect.
RESET	7 (ADM706R/ ADM706S/ ADM706T Only)	7	Logic Output. RESET goes low for 200 ms when triggered. It can be triggered either by V _{CC} being below the reset threshold or by a low signal on the MR input. RESET remains low whenever V _{CC} is below the reset threshold. It remains low for 200 ms after V _{CC} goes above the reset threshold or MR goes from low to high. A watchdog timeout does not trigger RESET unless WDO is connected to MR.
RESET	7 (ADM706P Only)	8	Logic Output. RESET is an active high output suitable for systems that use active high RESET logic. It is the inverse of RESET.
WDO	8	N/A	Logic Output/Watchdog Output. WDO goes low if the internal watchdog timer times out as a result of inactivity on the WDI input. It remains low until the watchdog timer is cleared. WDO also goes low during low line conditions. Whenever V _{CC} is below the reset threshold, WDO remains low. As soon as V _{CC} goes above the reset threshold, WDO goes high immediately.

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

TYPICAL PERFORMANCE CHARACTERISTICS

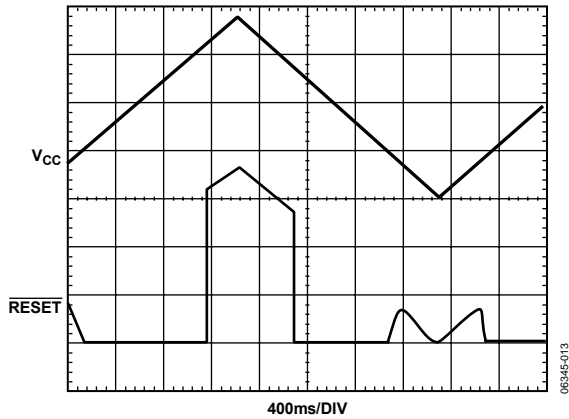


Figure 6. ADM70xR/ADM70xS/ADM70xT
RESET Output Voltage vs. Supply Voltage

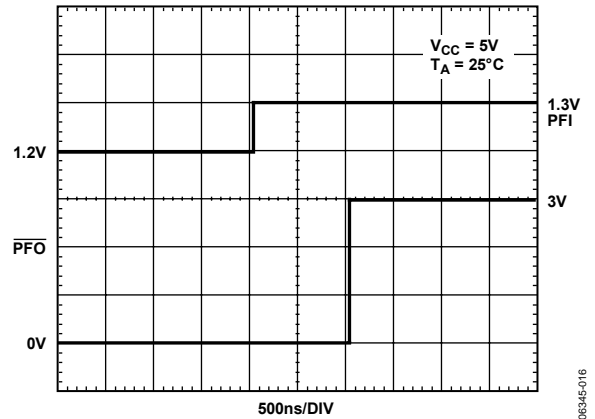


Figure 9. PFI Deassertion Response Time

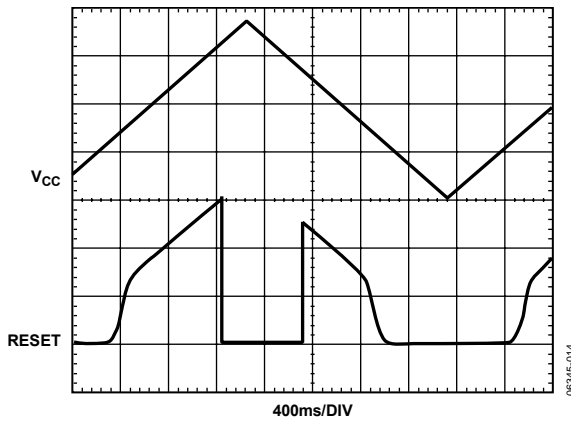


Figure 7. RESET Output Voltage vs. Supply Voltage

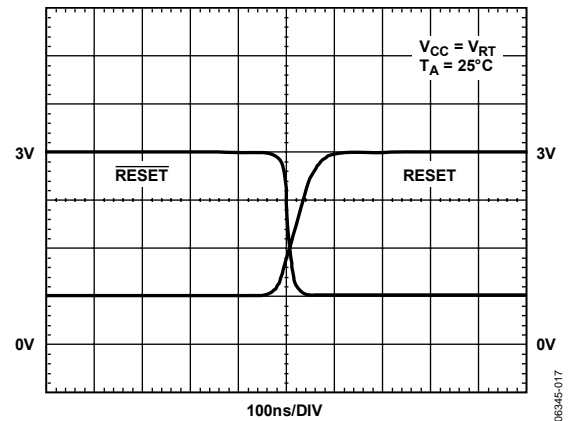


Figure 10. RESET, RESET Assertion

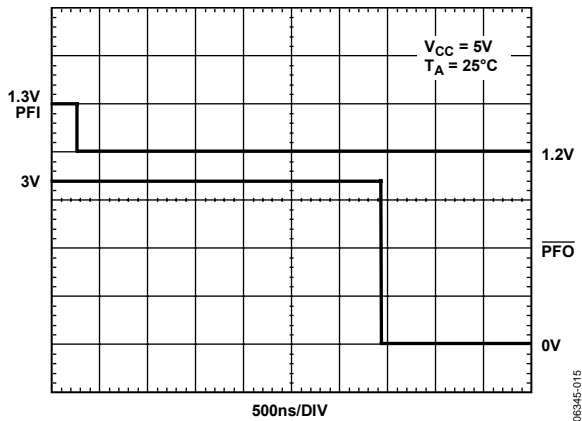


Figure 8. PFI Assertion Response Time

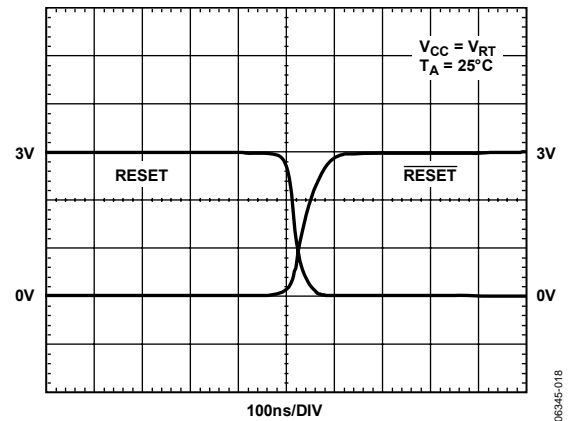


Figure 11. RESET, RESET Deassertion

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

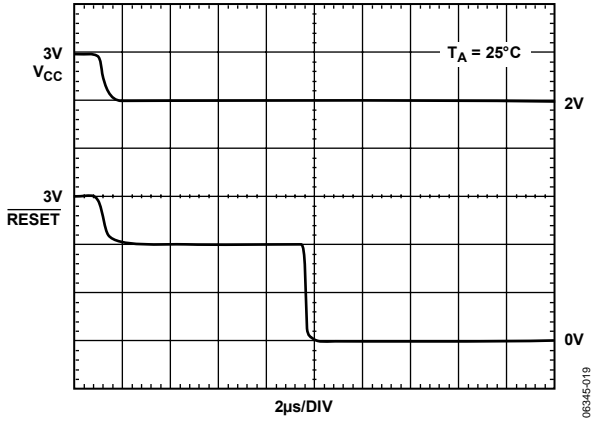


Figure 12. ADM70xR/ADM70xS/ADM70xT \overline{RESET} Response Time

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

CIRCUIT INFORMATION

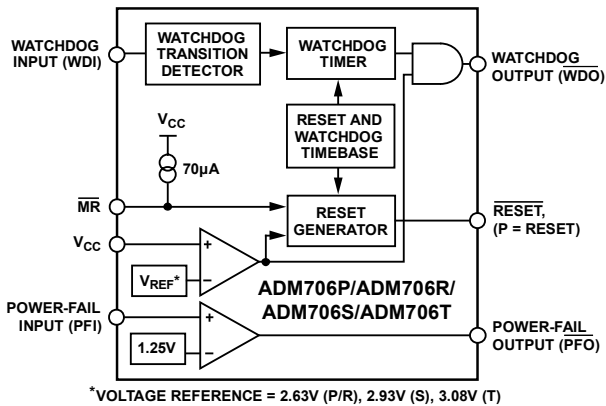


Figure 13. ADM706 Functional Block Diagram

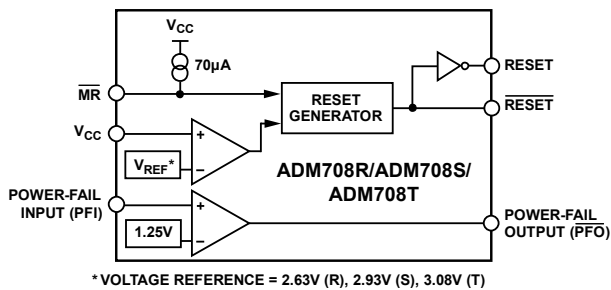


Figure 14. ADM708 Functional Block Diagram

POWER-FAIL RESET

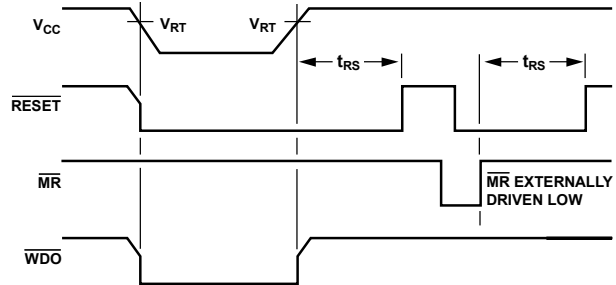
The reset output provides a reset ($\overline{\text{RESET}}$ or RESET) output signal to the microprocessor whenever the V_{CC} input is below the reset threshold. The actual reset threshold voltage is dependent on whether a P, R, S, or T suffix device is used. An internal timer holds the reset output active for 200 ms after the voltage on V_{CC} rises above the threshold. This is intended as a power-on reset signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset line is similarly activated and remains active for 200 ms after the supply recovers. If another interruption occurs during an active reset period, the reset timeout period continues for an additional 200 ms.

The reset output is guaranteed to remain valid with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply starts up.

The ADM706P provides an active high RESET signal; the ADM706R/ADM706S/ADM706T provide an active low $\overline{\text{RESET}}$ signal; and the ADM708R/ADM708S/ADM708T provide both RESET and $\overline{\text{RESET}}$.

MANUAL RESET

The $\overline{\text{MR}}$ input allows other reset sources, such as a manual reset switch, to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typical). The $\overline{\text{MR}}$ input is TTL-/CMOS-compatible; it can also be driven by any logic reset output. If unused, the $\overline{\text{MR}}$ input can be tied high or left floating.



NOTES
RESET = COMPLEMENT OF $\overline{\text{RESET}}$

Figure 15. $\overline{\text{RESET}}$, $\overline{\text{MR}}$, and $\overline{\text{WDO}}$ Timing

WATCHDOG TIMER (ADM706x)

The watchdog timer circuit can be used to monitor the activity of the microprocessor to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the watchdog input (WDI) line. If this line is not toggled within the timeout period (1.6 sec), the watchdog output ($\overline{\text{WDO}}$) is driven low. The $\overline{\text{WDO}}$ output can be connected to a nonmaskable interrupt (NMI) on the processor. Therefore, if the watchdog timer times out, an interrupt is generated. The interrupt service routine should then be used to rectify the problem.

The watchdog timer is cleared by either a high-to-low or by a low-to-high transition on WDI. Pulses as narrow as 50 ns are detected. The timer is also cleared by $\overline{\text{RESET}}$ /RESET going active. Therefore, the watchdog timeout period begins after reset goes inactive.

When V_{CC} falls below the reset threshold, $\overline{\text{WDO}}$ is forced low whether or not the watchdog timer has timed out. Normally, this generates an interrupt, but it is overridden by $\overline{\text{RESET}}$ /RESET going active.

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

The watchdog monitor can be deactivated by floating the watchdog input (WDI). The WDO output can now be used as a low line output because it only goes low when V_{CC} falls below the reset threshold.

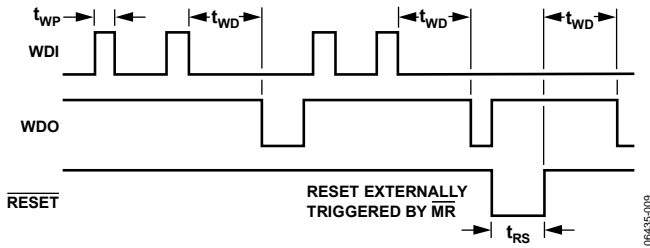


Figure 16. Watchdog Timing

POWER-FAIL COMPARATOR

The power-fail comparator is an independent comparator that can be used to monitor the input power supply. The comparator's inverting input is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input can be used to monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output (PFO) goes low indicating a power failure. For early warning of power failure, the comparator can be used to monitor the preregulator input simply by choosing an appropriate resistive divider network. The PFO output can be used to interrupt the processor so that a shutdown procedure is implemented before the power is lost.

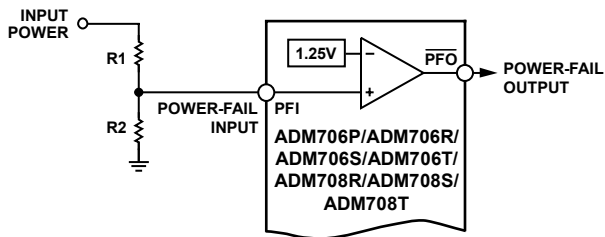


Figure 17. Power-Fail Comparator

ADDING HYSTERESIS TO THE POWER-FAIL COMPARATOR

For increased noise immunity, hysteresis can be added to the power-fail comparator. Because the comparator circuit is noninverting, hysteresis can be added simply by connecting a resistor between the PFO output and the PFI input as shown in Figure 18. When PFO is low, Resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, Resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity can be achieved by connecting a capacitor between PFI and GND.

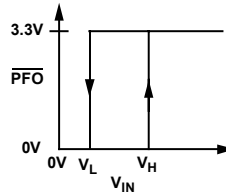
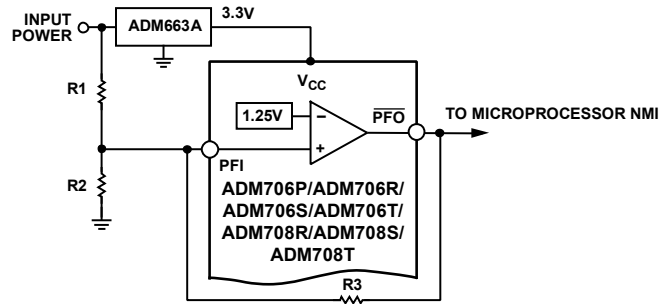


Figure 18. Adding Hysteresis to the Power-Fail Comparator

$$V_H = 1.25 \left[1 + \left(\frac{R2 + R3}{R2 \times R3} \right) R1 \right]$$

$$V_L = 1.25 + R1 \left(\frac{1.25}{R2} - \frac{V_{CC} - 1.25}{R3} \right)$$

$$V_{MID} = 1.25 \left(\frac{R1 + R2}{R2} \right)$$

VALID RESET BELOW 1 V V_{CC}

The ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T family of products are guaranteed to provide a valid reset level with V_{CC} as low as 1 V. Refer to the Typical Performance Characteristics section. As V_{CC} drops below 1 V, the internal transistor does not have sufficient drive to hold it on so the voltage on RESET is no longer held at 0 V. A pull-down resistor as shown in Figure 19 can be connected externally to hold the line low if it is required.

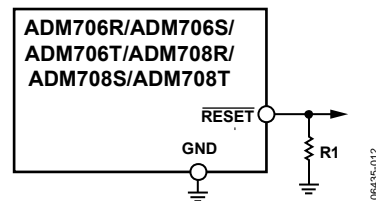


Figure 19. RESET Valid Below 1 V

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

APPLICATIONS INFORMATION

A typical operating circuit is shown in Figure 20. The unregulated dc input supply is monitored using the PFI input via the resistive divider network. Resistor R1 and Resistor R2 should be selected so that when the supply voltage drops below the desired level (for example, 5 V), the voltage on PFI drops below the 1.25 V threshold, thereby generating an interrupt to the microprocessor. Monitoring the preregulator input gives additional time to execute an orderly shutdown procedure before power is lost.

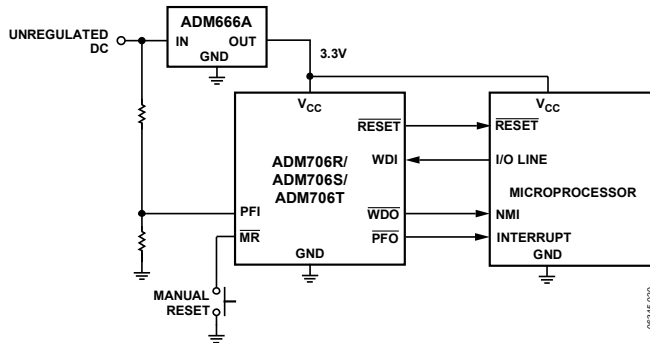


Figure 20. Typical Application Circuit

Microprocessor activity is monitored using the WDI input. This is driven using an output line from the processor. The software routines should toggle this line at least once every 1.6 seconds. If a problem occurs and this line is not toggled, then WDO goes low and a nonmaskable interrupt is generated. This interrupt routine can be used to clear the problem.

If, in the event of inactivity on the WDI line, a system reset is required, the WDO output should be connected to the input as shown in Figure 21.

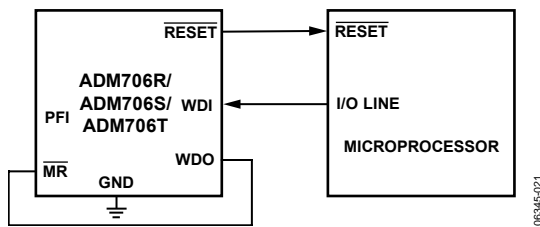


Figure 21. RESET from WDO

MONITORING ADDITIONAL SUPPLY LEVELS

It is possible to use the power-fail comparator to monitor a second supply as shown in Figure 22. The two sensing resistors, R1 and R2, are selected such that the voltage on PFI drops below 1.25 V at the minimum acceptable input supply. The PFO output can be connected to the $\overline{\text{MR}}$ input so that a RESET is generated when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, a RESET is generated.

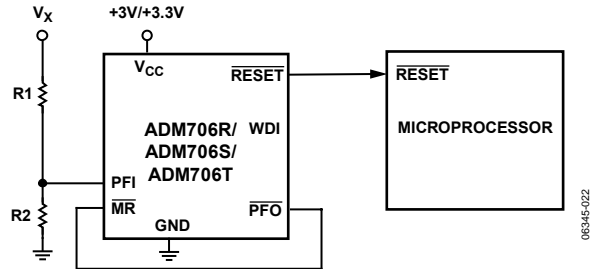


Figure 22. Monitoring 3 V/3.3 V and an Additional Supply, V_x

MICROPROCESSORS WITH BIDIRECTIONAL RESET

To prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor should be inserted between the ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T RESET output pin and the microprocessor reset pin. This limits the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 k Ω . If the reset output is required for other uses, it should be buffered as shown in Figure 23.

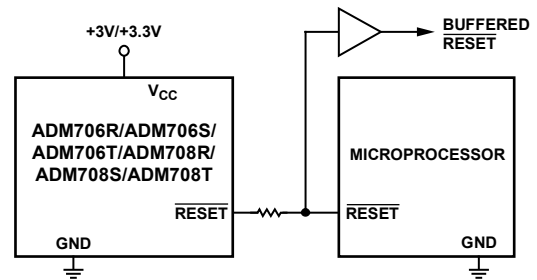
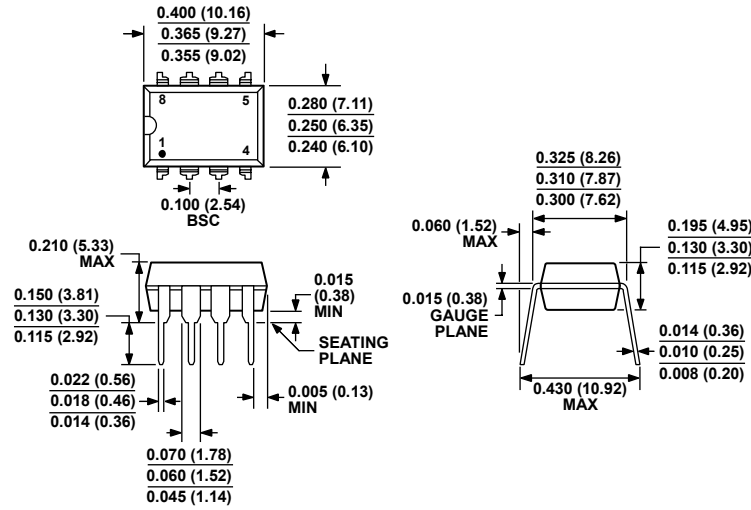


Figure 23. Bidirectional Input/Output RESET

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

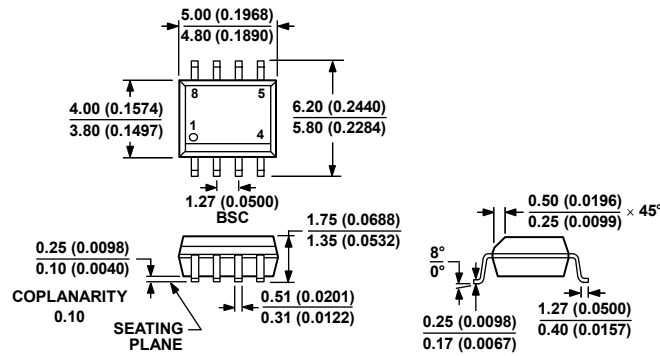
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 24. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimension shown in inches and (millimeters)

070606-A



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

060506-A

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM706PAN	-40°C to +85°C	8-Lead PDIP	N-8
ADM706PANZ ¹	-40°C to +85°C	8-Lead PDIP	N-8
ADM706PAR	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706PAR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706PARZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706PARZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RAN	-40°C to +85°C	8-Lead PDIP	N-8
ADM706RANZ ¹	-40°C to +85°C	8-Lead PDIP	N-8
ADM706RAR	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RAR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RAR-REEL7	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RARZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RARZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706RARZ-REEL7 ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706SAN	-40°C to +85°C	8-Lead PDIP	N-8
ADM706SANZ ¹	-40°C to +85°C	8-Lead PDIP	N-8
ADM706SAR	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706SAR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706SARZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706SARZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706TAN	-40°C to +85°C	8-Lead PDIP	N-8
ADM706TANZ ¹	-40°C to +85°C	8-Lead PDIP	N-8
ADM706TAR	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706TAR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706TARZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM706TARZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708RAN	-40°C to +85°C	8-Lead PDIP	N-8
ADM708RANZ ¹	-40°C to +85°C	8-Lead PDIP	N-8
ADM708RAR	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708RAR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708RARZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708RARZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708SAN	-40°C to +85°C	8-Lead PDIP	N-8
ADM708SANZ ¹	-40°C to +85°C	8-Lead PDIP	N-8
ADM708SAR	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708SAR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708SARZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708SARZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708TAN	-40°C to +85°C	8-Lead PDIP	N-8
ADM708TANZ ¹	-40°C to +85°C	8-Lead PDIP	N-8
ADM708TAR	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708TAR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708TARZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM708TARZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8

¹ Z = Pb-free part.

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

NOTES

NOTES

ADM706P/ADM706R/ADM706S/ADM706T, ADM708R/ADM708S/ADM708T

NOTES