HARRIS SEMICONDUCTOR

ML Series

Multilayer Surface Mount Transient Voltage Surge Suppressors

February 1998

Features

- **Leadless 0603, 0805, 1206 and 1210 Chip Sizes**
- **Multilayer Ceramic Construction Technology**
- **-55°C to 125°C Operating Temperature Range**
- **Wide Operating Voltage Range $V_{M(DC)}$ = 3.5V to 120V**
- **Rated for Surge Current (8 x 20)**
- **Rated for Energy (10 x 1000)**
- **Inherent Bidirectional Clamping**
- **No Plastic or Epoxy Packaging Assures Better than 94V-0 Flammability Rating**
- **Standard Low Capacitance Types Available**
- **Available with Nickel/Tin End Terminations**

Applications

- **Suppression of Inductive Switching or Other Transient Events Such as EFT and Surge Voltage at the Circuit Board Level**
- **ESD Protection for Components Sensitive to IEC 1000-4-2, MIL-STD-883C Method 3015.7, and Other Industry Specifications (See Also the MLE Series)**
- **Provides On-Board Transient Voltage Protection for ICs and Transistors**
- **Used to Help Achieve Electromagnetic Compliance of End Products**
- **Replace Larger Surface Mount TVS Zeners in Many Applications**

Description

The ML Series is a family of Transient Voltage Surge Suppression devices based on the Harris Multilayer fabrication technology. These components are designed to suppress a variety of transient events, including those specified by the IEC or other standards used for Electromagnetic Compliance (EMC). The ML Series is typically applied to protect integrated circuits and other components at the circuit board level.

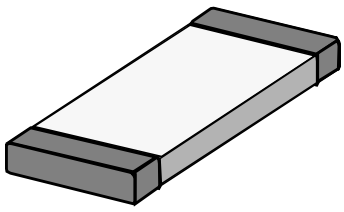
The wide operating voltage and energy range make the ML Series suitable for numerous applications on power supply, control and signal lines.

The ML Series is manufactured from semiconducting ceramics providing bidirectional voltage clamping and is supplied in leadless, surface mount form, compatible with modern reflow and wave soldering procedures.

Harris manufactures other Multilayer Series products. See the MLE Series data sheet (Harris AnswerFAX, 407-724-7800, doc #2463) for ESD applications. See the AUML Series for automotive applications (AnswerFAX doc #3387).

Packaging

ML SERIES (LEADLESS CHIP)



File Number **2461.9**

Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

	ML SERIES	UNITS
Continuous:		
Steady State Applied Voltage:		
DC Voltage Range ($V_{M(DC)}$)	3.5 to 68	V
AC Voltage Range ($V_{M(AC)RMS}$)	2.5 to 50	V
Transient:		
Non-Repetitive Surge Current, 8/20μs Waveform, (I_{TM})	30 to 250	A
Non-Repetitive Surge Energy, 10/1000μs Waveform, (W_{TM})	0.1 to 1.2	J
Operating Ambient Temperature Range (T_A)	-55 to 125	^oC
Storage Temperature Range (T_{STG})	-55 to 150	^oC
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/^oC

Device Ratings and Specifications

PART NUMBER	MAXIMUM RATINGS (125^oC)					SPECIFICATIONS (25^oC)		
	MAXIMUM CONTINUOUS WORKING VOLTAGE		MAXIMUM NON-REPETITIVE SURGE CURRENT (8/20μs)	MAXIMUM NON-REPETITIVE SURGE ENERGY (10/1000μs)	MAXIMUM CLAMPING VOLTAGE AT 10A (OR AS NOTED) (8/20μs)	NOMINAL VOLTAGE AT 1mA DC TEST CURRENT		TYPICAL CAPACITANCE AT f = 1MHz
	$V_{M(DC)}$	$V_{M(AC)}$	I_{TM}	W_{TM}	V_C	$V_{N(DC)}$ MIN	$V_{N(DC)}$ MAX	C
	(V)	(V)	(A)	(J)	(V)	(V)	(V)	(pF)
V3.5MLA0603	3.5	2.5	30	0.1	10 at 2A	3.7	7.0	1100
V3.5MLA0805	3.5	2.5	120	0.3	10 at 5A	3.7	7.0	2200
V3.5MLA0805L	3.5	2.5	40	0.1	10 at 2A	3.7	7.0	1200
V3.5MLA1206	3.5	2.5	100	0.3	14	3.7	7.0	6000
V5.5MLA0603	5.5	4.0	30	0.1	15.5 at 2A	7.1	9.3	660
V5.5MLA0805	5.5	4.0	120	0.3	15.5 at 5A	7.1	9.3	1600
V5.5MLA0805L	5.5	4.0	40	0.1	15.5 at 2A	7.1	9.3	860
V5.5MLA1206	5.5	4.0	150	0.4	15.5	7.1	9.3	4500
V9MLA0603	9.0	6.5	30	0.1	23 at 2A	11.0	16.0	420
V9MLA0805L	9.0	6.5	40	0.1	20 at 2A	11	14	450
V12MLA0805L	12	9.0	40	0.1	25 at 2A	14	18.5	350
V14MLA0603	14	10	30	0.1	30 at 2A	15.9	20.3	150
V14MLA0805	14	10	120	0.3	30 at 5A	15.9	20.3	480
V14MLA0805L	14	10	40	0.1	30 at 2A	15.9	20.3	270
V14MLA1206	14	10	150	0.4	30	15.9	20.3	1600

Device Ratings and Specifications (Continued)

PART NUMBER	MAXIMUM RATINGS (125°C)					SPECIFICATIONS (25°C)		
	MAXIMUM CONTINUOUS WORKING VOLTAGE		MAXIMUM NON-REPETITIVE SURGE CURRENT (8/20μs)	MAXIMUM NON-REPETITIVE SURGE ENERGY (10/1000μs)	MAXIMUM CLAMPING VOLTAGE AT 10A (OR AS NOTED) (8/20μs)	NOMINAL VOLTAGE AT 1mA DC TEST CURRENT		TYPICAL CAPACITANCE AT f = 1MHz
	$V_{M(DC)}$	$V_{M(AC)}$	I_{TM}	W_{TM}	V_C	$V_{N(DC)}$ MIN	$V_{N(DC)}$ MAX	C
	(V)	(V)	(A)	(J)	(V)	(V)	(V)	(pF)
V18MLA0603	18	14	30	0.1	40 at 2A	22	28.0	125
V18MLA0805	18	14	120	0.3	40 at 5A	22	28.0	450
V18MLA0805L	18	14	40	0.1	40 at 2A	22	28.0	250
V18MLA1206	18	14	150	0.4	40	22	28.0	1100
V18MLA1210	18	14	500	2.5	40	22	28.0	1250
V26MLA0603	26	20	30	0.1	58 at 2A	31	38	90
V26MLA0805	26	20	100	0.3	58 at 5A	29.5	38.5	190
V26MLA0805L	26	20	40	0.1	58 at 2A	29.5	38.5	115
V26MLA1206	26	20	150	0.6	56	29.5	38.5	900
V26MLA1210	26	20	300	1.2	54	29.5	38.5	1000
V30MLA0603	30	25	30	0.1	65 at 2A	37	46	75
V30MLA0805L	30	25	30	0.1	65 at 2A	37	46	80
V30MLA1210	30	25	280	1.2	62	35	43	1575
V30MLA1210L	30	25	220	0.9	62	35	43	1530
V33MLA1206	33	26	180	0.8	72	38	49	550
V42MLA1206	42	30	180	0.8	86	46	60	550
V48MLA1210	48	40	250	1.2	100	54.5	66.5	450
V48MLA1210L	48	40	220	0.9	100	54.5	66.5	430
V56MLA1206	56	40	180	1.0	110	61	77	150
V60MLA1210	60	50	250	1.5	120	67	83	375
V68MLA1206	68	50	180	1.0	130	76	90	150
V85MLA1210	85	67	250	2.5	160	95	115	225
V120MLA1210	120	107	125	2.0	230	135	165	65

NOTES:

1. L suffix is a low capacitance and energy version. Contact Sales for custom capacitance requirements.
2. Typical leakage at 25°C < 25μA, maximum leakage 50μA at $V_{M(DC)}$.
3. Average power dissipation of transients for 0603, 0805, 1206 and 1210 sizes not to exceed 0.05, 0.10W, 0.10W and 0.15W, respectively.

Power Dissipation Ratings

When transients occur in rapid succession the average power dissipation is the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Characteristics table for the specific device. Certain parameter ratings must be derated at high temperatures as shown in Figure 1.

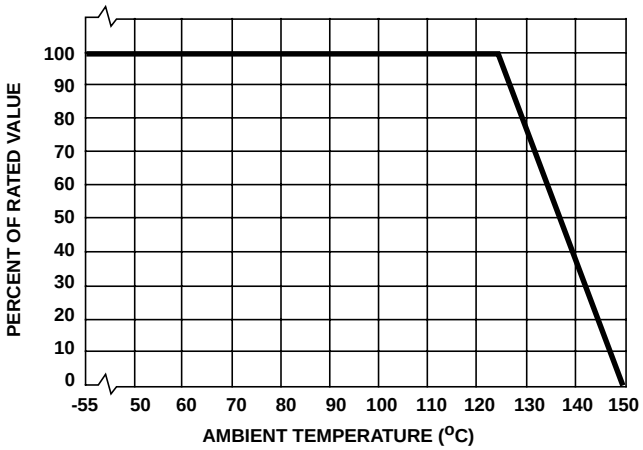
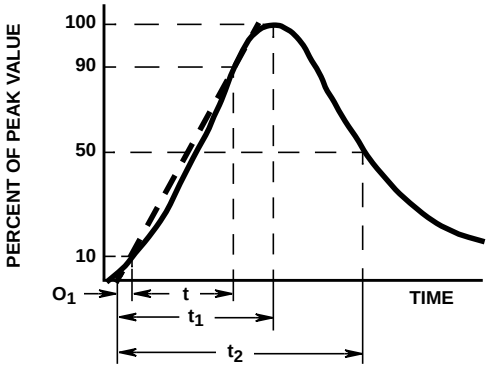


FIGURE 1. CURRENT, ENERGY AND POWER DERATING CURVE



O_1 = VIRTUAL ORIGIN OF WAVE
t = TIME FROM 10% TO 90% OF PEAK
t_1 = VIRTUAL FRONT TIME = 1.25 x t
t_2 = VIRTUAL TIME TO HALF VALUE (IMPULSE DURATION)

EXAMPLE:
FOR AN 8/20μs CURRENT WAVEFORM:
8μs = t_1 = VIRTUAL FRONT TIME
20μs = t_2 = VIRTUAL TIME TO HALF VALUE

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM

Maximum Transient V-I Characteristic Curves

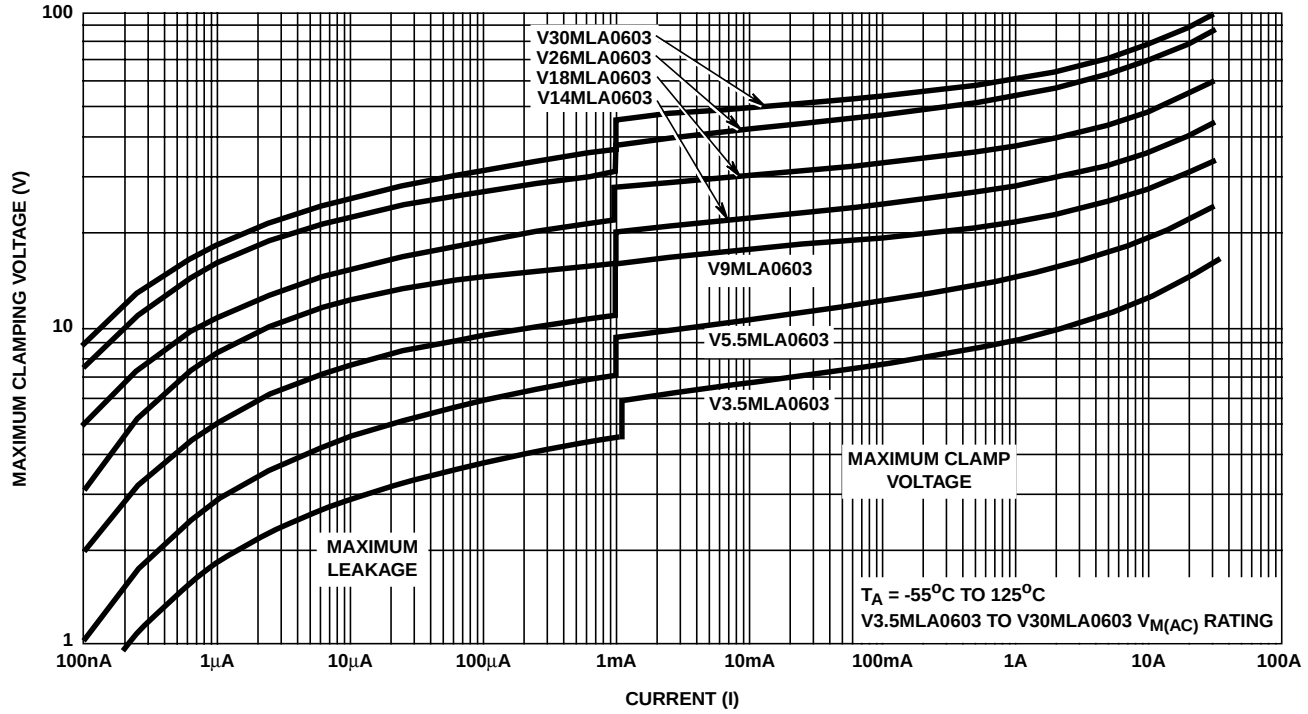


FIGURE 3. V3.5MLA0603 TO V30MLA0603 MAXIMUM V-I CHARACTERISTIC CURVES

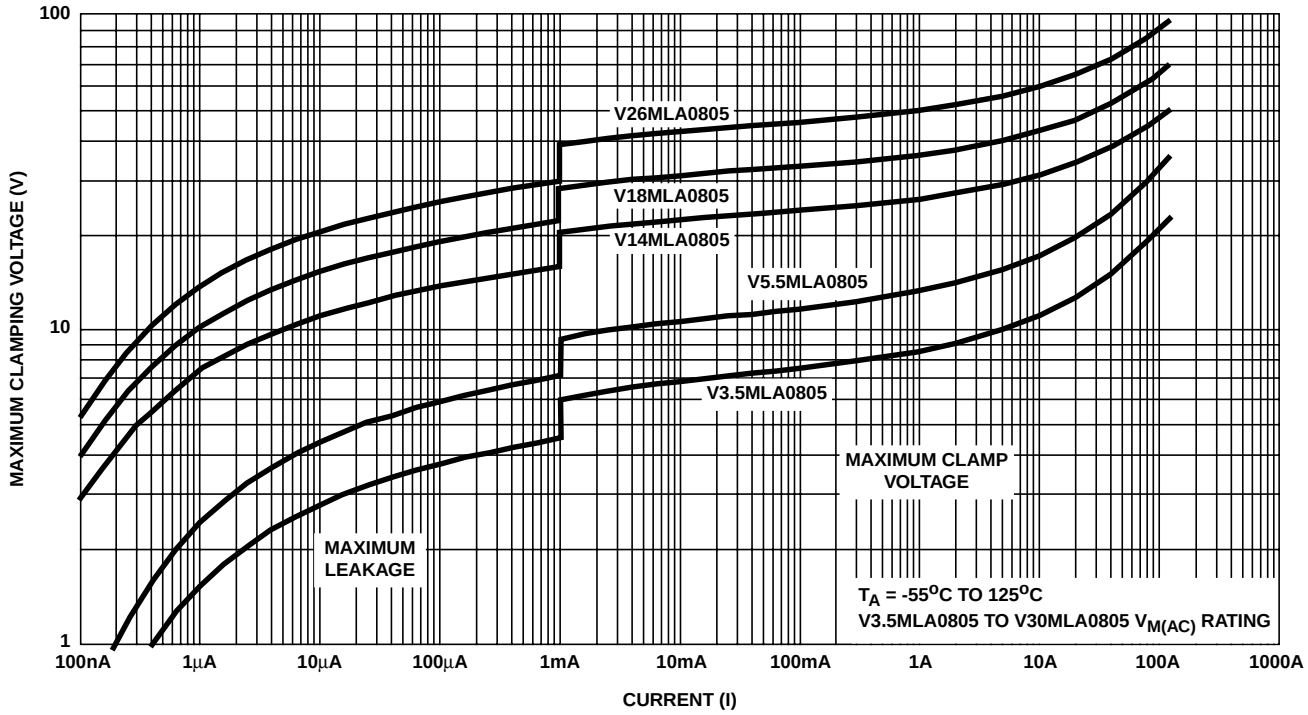


FIGURE 4. V3.5MLA0805 TO V26MLA0805 MAXIMUM V-I CHARACTERISTIC CURVES

Maximum Transient V-I Characteristic Curves (Continued)

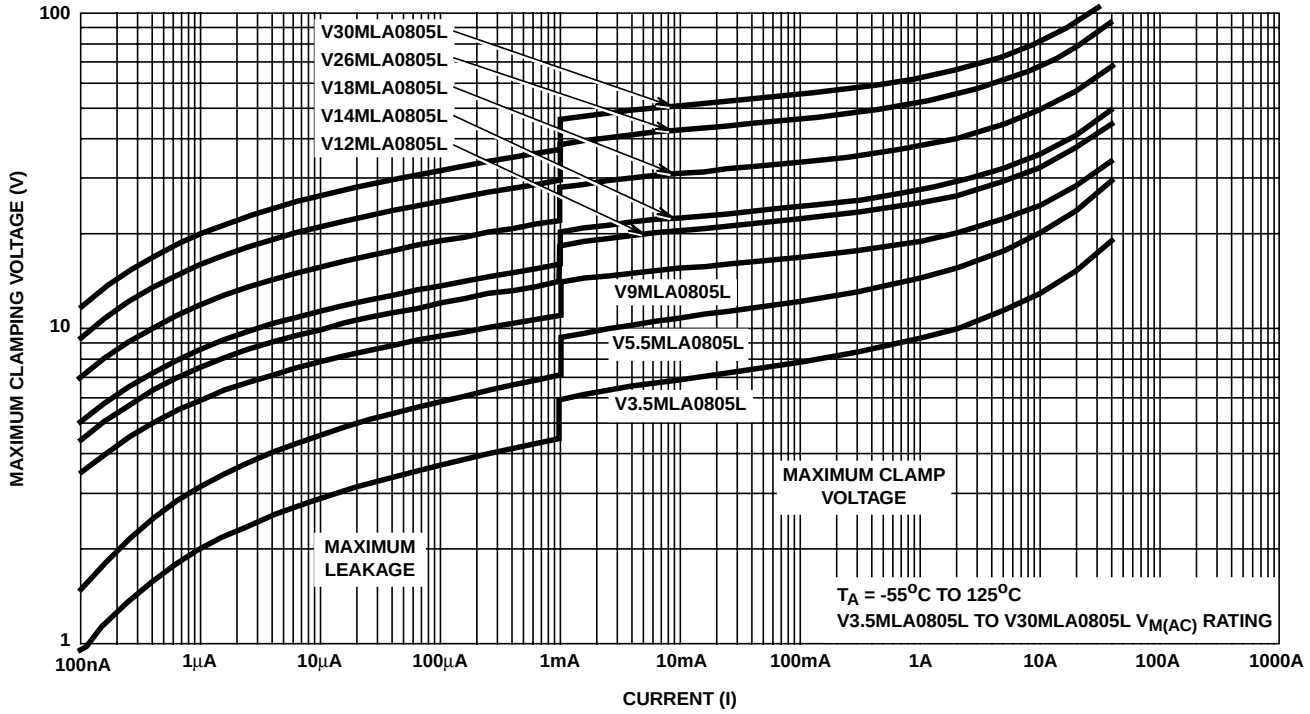


FIGURE 5. V3.5MLA0805L TO V30MLA0805L MAXIMUM V-I CHARACTERISTIC CURVES

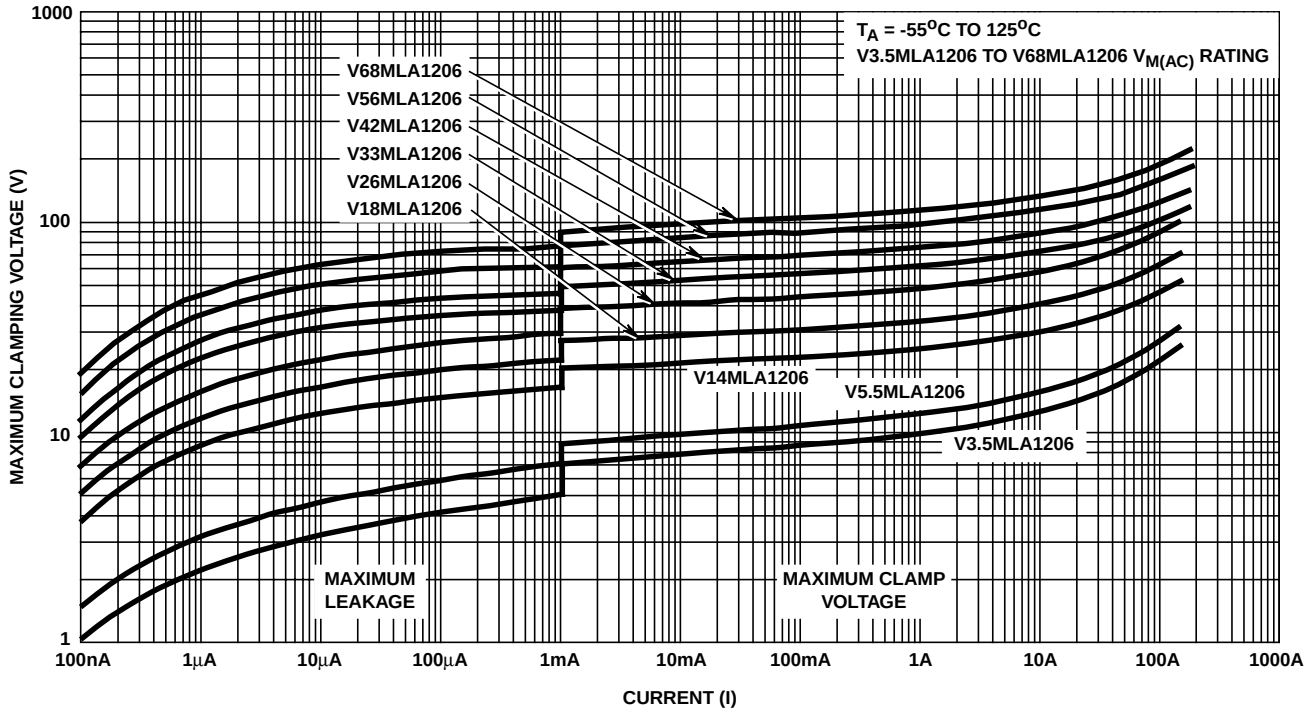


FIGURE 6. V3.5MLA1206 TO V68MLA1206 MAXIMUM V-I CHARACTERISTIC CURVES

Maximum Transient V-I Characteristic Curves (Continued)

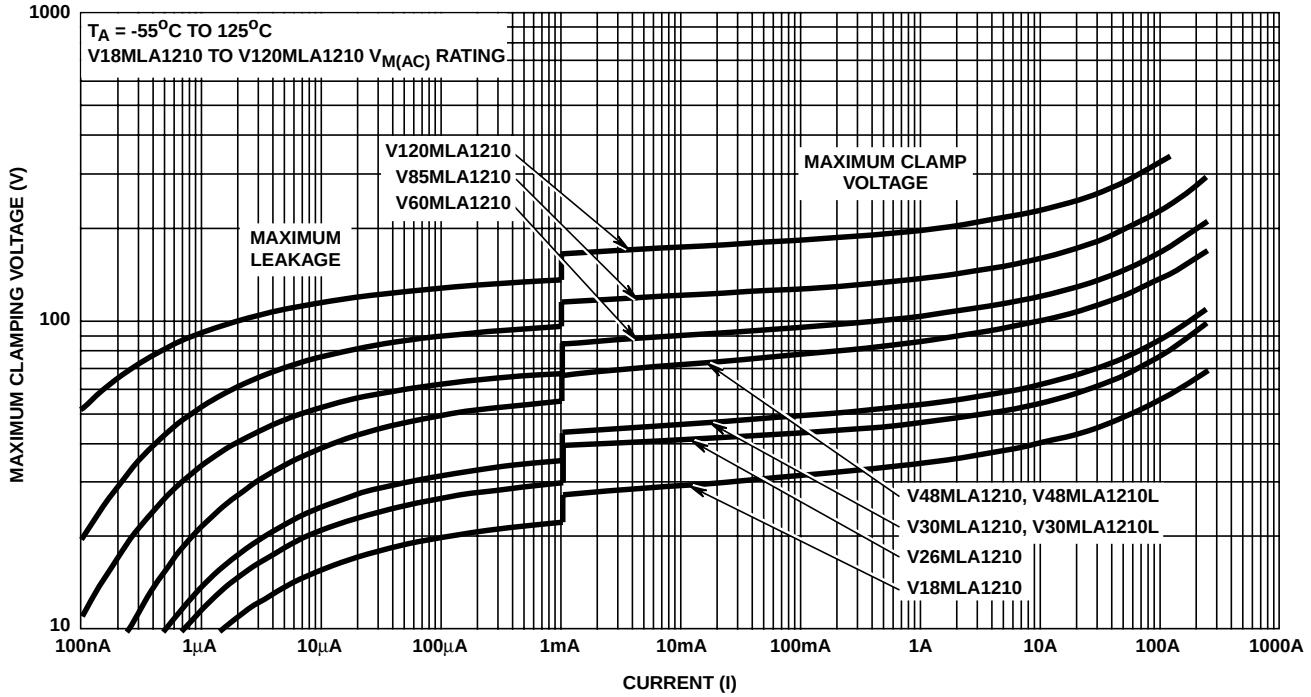


FIGURE 7. V18MLA1210 TO V120MLA1210 MAXIMUM V-I CHARACTERISTIC CURVES

Device Characteristics

At low current levels, the V-I curve of the multilayer transient voltage suppressor approaches a linear (ohmic) relationship and shows a temperature dependent affect (Figure 8). At or below the maximum working voltage, the suppressor is in a high resistance mode (approaching $10^6\Omega$ at its maximum rated working voltage). Leakage currents at maximum rated voltage are below 50μA, typically 25μA.

When clamping transients at and above the 10mA range, the multilayer suppressor approaches a 1Ω -10Ω characteristic. Here, the multilayer becomes virtually temperature independent (Figure 9).

Speed of Response

The Multilayer Suppressor is a leadless device. Its response time is not limited by the parasitic lead inductances found in other surface mount packaging. The response time of the Zinc Oxide dielectric material is less than 1 nanosecond and the ML can clamp very fast dV/dT events such as ESD. Additionally, in “real world” applications, the associated circuit wiring is often the greatest factor effecting speed of response. Therefore, transient suppressor placement within a circuit can be considered important in certain instances.

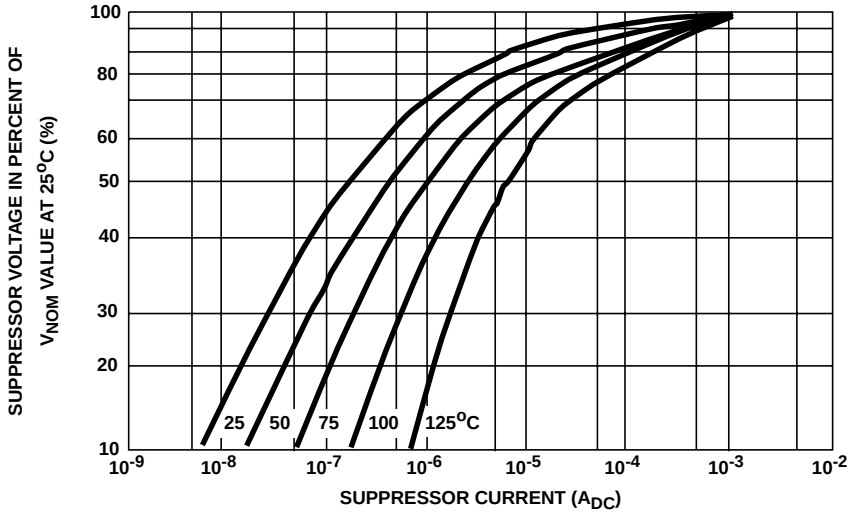


FIGURE 8. TYPICAL TEMPERATURE DEPENDENCE OF THE CHARACTERISTIC CURVE IN THE LEAKAGE REGION

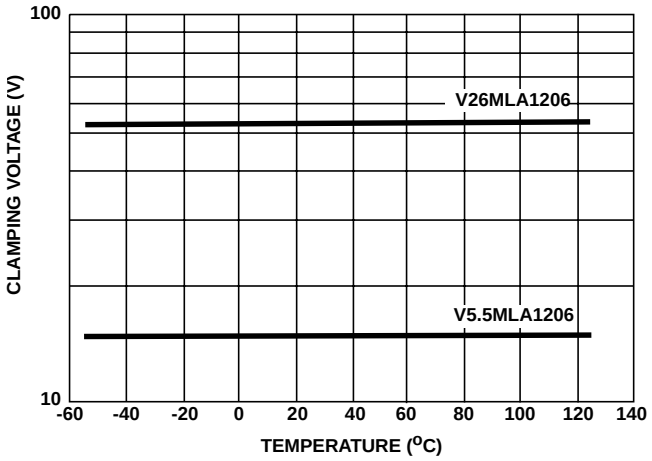


FIGURE 9. CLAMPING VOLTAGE OVER TEMPERATURE (V_C AT 10A)

Energy Absorption/Peak Current Capability

Energy dissipated within the ML is calculated by multiplying the clamping voltage, transient current and transient duration. An important advantage of the multilayer is its interdigitated electrode construction within the mass of dielectric material. This results in excellent current distribution and the peak temperature per energy absorbed is very low. The matrix of semiconducting grains combine to absorb and distribute transient energy (heat) (Figure 10). This dramatically reduces peak temperature, thermal stresses and enhances device reliability.

As a measure of the device capability in energy handling and peak current, the V26MLA1206A part was tested with multiple pulses at its peak current rating (150A, 8/20µs). At the end of the test, 10,000 pulses later, the device voltage characteristics are still well within specification (Figure 11).

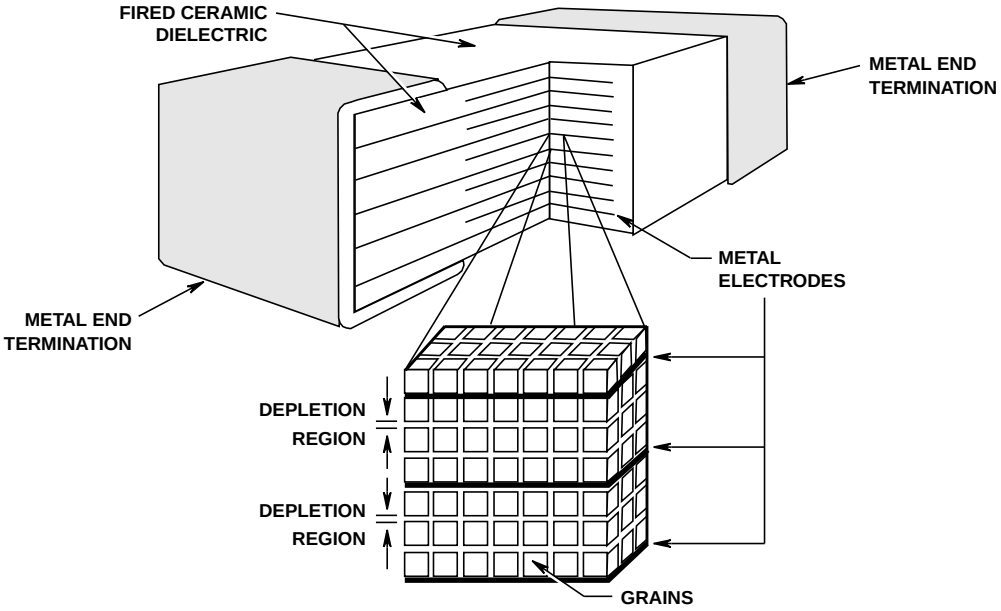


FIGURE 10. MULTILAYER INTERNAL CONSTRUCTION

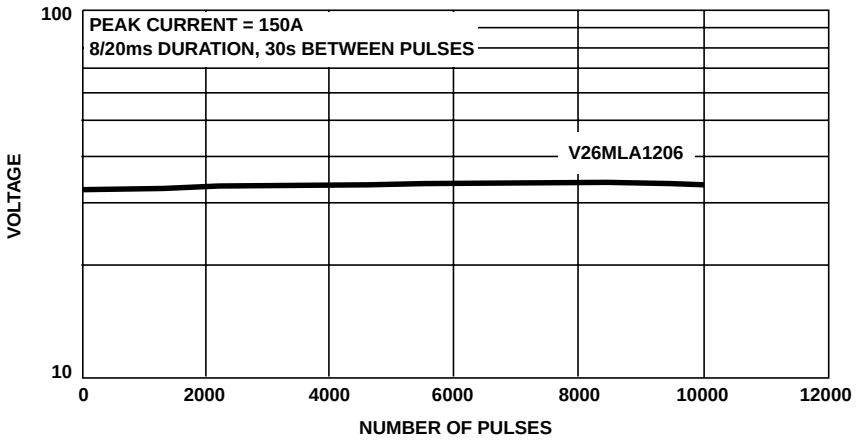


FIGURE 11. REPETITIVE PULSE CAPABILITY

Soldering Recommendations

The principal techniques used for the soldering of components in surface mount technology are Infra Red (IR) Reflow, Vapor Phase Reflow and Wave Soldering. When wave soldering, the ML suppressor is attached to the substrate by means of an adhesive. The assembly is then placed on a conveyor and run through the soldering process. With IR and Vapor Phase Reflow the device is placed in a solder paste on the substrate. As the solder paste is heated it reflows, and solders the unit to the board.

With the ML suppressor, the recommended solder is a 62/36/2 (Sn/Pb/Ag), 60/40 (Sn/Pb), or 63/37 (Sn/Pb). Harris also recommends an RMA solder flux. Wave soldering operation is the most strenuous of the processes. To avoid the possibility of generating stresses due to thermal shock, a preheat stage in the soldering process is recommended, and the peak temperature of the solder process should be rigidly controlled.

When using a reflow process, care should be taken to ensure that the ML chip is not subjected to a thermal gradient steeper than 4 degrees per second; the ideal gradient being 2 degrees per second. During the soldering process, preheating to within 100 degrees of the solders peak temperature is essential to minimize thermal shock. Examples of the soldering conditions for the ML series of suppressors are given in the tables below.

Once the soldering process has been completed, it is still necessary to ensure that any further thermal shocks are avoided. One possible cause of thermal shock is hot printed circuit boards being removed from the solder process and subjected to cleaning solvents at room temperature. The boards must be allowed to cool to less than 50^{o}C before cleaning.

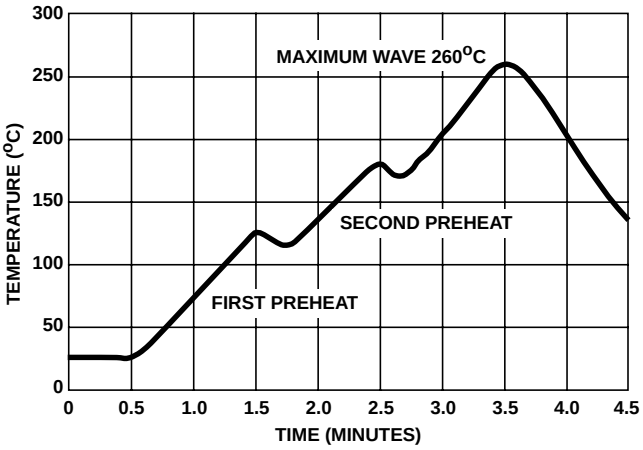


FIGURE 12. WAVE SOLDER PROFILE

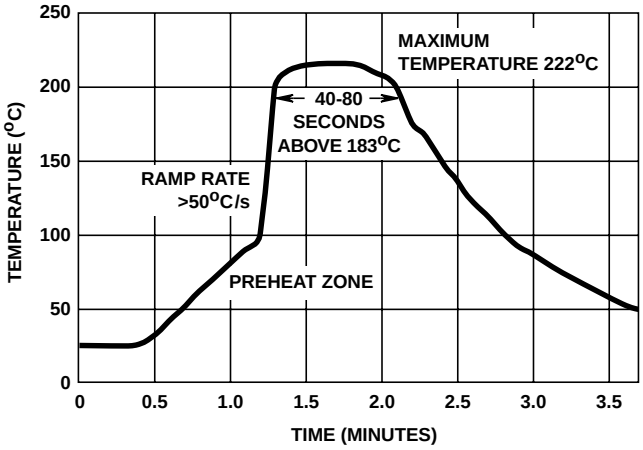


FIGURE 13. VAPOR PHASE SOLDER PROFILE

Termination Options

Harris offers three types of termination finish on the Multilayer product series:

1. Silver/Platinum (standard)
2. Silver/Palladium (optional)
3. Nickel/Tin (optional)

(The ordering information section describes how to designate them.)

The Nickel/Tin plated termination can provide certain solder process application benefits such as:

- A better match to Tin/Lead solders resulting in improved solder wetting and solder fillet height (typically 70% of component height).
- An enhanced resistance to solder leaching permits greater flexibility/latitude in the design and control of solder processes. (See the temperature-time graph below.)
- An alternative material when silver end terminations are restricted.

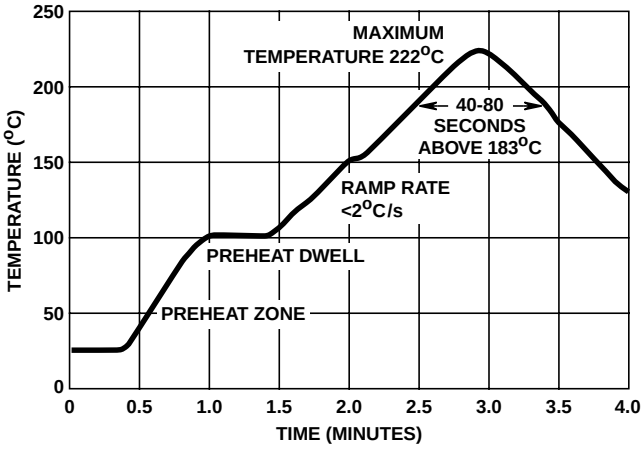


FIGURE 14. REFLOW SOLDER PROFILE

Solder Process Time Advantages for Nickel/Tin Terminated Multilayer Suppressors

Certain surface mount soldering processes require long duration or multiple soldering cycles for top and bottom side assemblies and/or for reworking rejected product. In these instances, devices with a Nickel/Tin finish offer greater dwell time, for example, when end termination leaching is of concern. The Solder Temperature-Time Curve shown can be used as a guideline when designing process variables and rework operations and illustrates the greater latitude afforded with this material.

Since end termination leaching is a function of the cumulative molten dwell time, then the molten time duration allowed at subsequent operations is reduced by the percentage of time used by the initial operation. Using the curve for the applicable material,

$$\frac{\text{Total Time at Initial Temp - Actual Time at Initial Temp}}{\text{Total Time at Initial Temp}} \times \text{Total Time Permitted at the Subsequent Temp}$$

For example, if the initial process is for 20 seconds at 220°C and the next process is at 260°C, then the maximum time allowed at 260°C is:

For Nickel/Tin Termination:

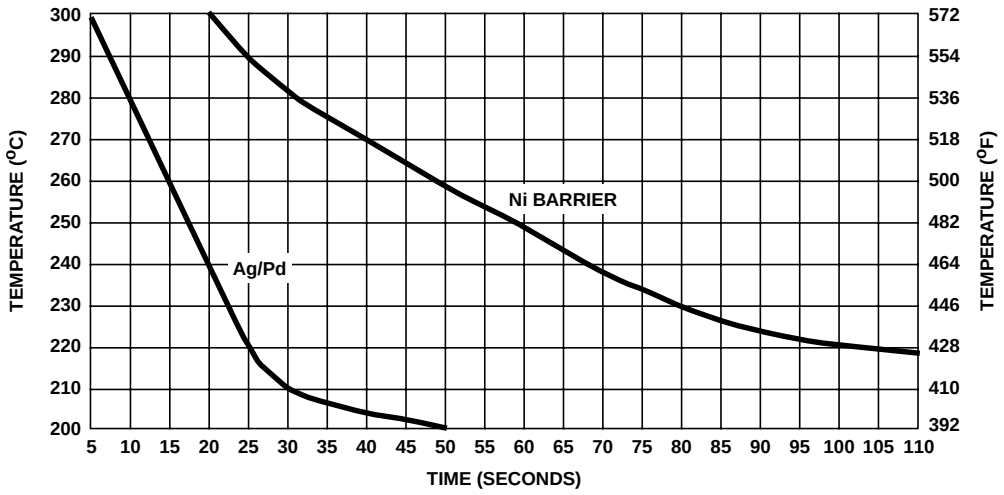
$$\frac{100 - 20}{100} \times 48 = 38.4 \text{ seconds}$$

For Ag/Pd Termination:

$$\frac{25 - 20}{25} \times 15 = 3.0 \text{ seconds}$$

Also, if the initial soldering process is for 10 seconds at 280°C, the Nickel/Tin termination can withstand a further 20 seconds at 280°C or an equivalent percentage of time at a subsequent temperature. For example, If the next soldering process is at 230°C, the total time allowed at this temperature is:

$$\frac{30 - 10}{30} \times 80 = 53 \text{ seconds}$$

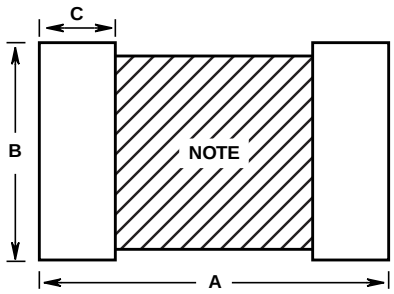


NOTES:

4. Comparative Temperature-Time data for Silver/Palladium and Nickel/Tin terminated Multilayer Suppressors.
5. The curves indicate the point at which 5% leaching of the termination will occur after immersion in a static solder bath for an 0805 size device.
6. Static solder bath = Sn/Pb (63/67). RMA no clean flux.

FIGURE 15. SOLDER TEMPERATURE-TIME CURVE

Recommended Pad Outline



NOTE: Avoid metal runs in this area.

SYMBOL	PAD SIZE							
	FOR 1210 SIZE DEVICE		FOR 1206 SIZE DEVICE		FOR 0805 SIZE DEVICE		FOR 0603 SIZE DEVICE	
	IN	MM	IN	MM	IN	MM	IN	MM
A	0.219	5.53	0.203	5.15	0.144	3.65	0.11	2.8
B	0.147	3.73	0.103	2.62	0.084	2.13	0.064	1.62
C	0.073	1.85	0.065	1.65	0.058	1.48	0.044	1.12

Explanation of Terms

Rated DC Voltage ($V_{M(DC)}$)

This is the maximum continuous DC voltage which may be applied up to the maximum operating temperature of the device. The rated DC operating voltage (working voltage) is also used as the reference point for leakage current. This voltage is always less than the breakdown voltage of the device.

Rated AC Voltage ($V_{M(AC)RMS}$)

This is the maximum continuous sinusoidal rms voltage which may be applied. This voltage may be applied at any temperature up to the maximum operating temperature of the device.

Maximum Non-Repetitive Surge Current (I_{TM})

This is the maximum peak current which may be applied for an 8/20μs impulse, with rated line voltage also applied, without causing device failure. The pulse can be applied to the device in either polarity with the same confidence factor. See Figure 2 for waveform description.

Maximum Non-Repetitive Surge Energy (W_{TM})

This is the maximum rated transient energy which may be dissipated for a single current pulse at a specified impulse duration (10/1000μs), with the rated DC or RMS voltage applied, without causing device failure.

Leakage (I_L) at Rated DC Voltage

In the nonconducting mode, the device is at a very high impedance (approaching $10^6\Omega$ at its maximum rated voltage) and appears essentially as an open circuit in the system. The leakage current drawn at this level is very low, as specified in the Device Ratings table.

Nominal Voltage ($V_{N(DC)}$)

This is the voltage at which the device changes from the off (standby state) to the on (clamping state) and enters its conduction mode of operation. The voltage value is usually characterized at the 1mA point and has a specified minimum and maximum voltage range.

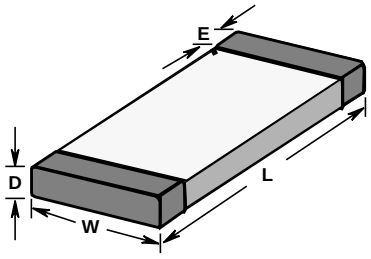
Clamping Voltage (V_C)

This is the peak voltage appearing across the suppressor when measured at conditions of specified pulse current and specified waveform.

Capacitance (C)

This is the capacitance of the device at a specified frequency (1MHz) and bias ($1V_{P-P}$)

Mechanical Dimensions

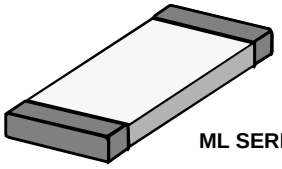


SYMBOL	CHIP SIZE							
	1210		1206		0805		0603	
	IN	MM	IN	MM	IN	MM	IN	MM
D Max.	0.113	2.87	0.071	1.80	0.043	1.1	0.035	0.9
E	0.02 ±0.01	0.50 ±0.25	0.02 ±0.01	0.50 ±0.25	0.01 to 0.029	0.25 to 0.75	0.015 ±0.008	0.4 ±0.2
L	0.125 ±0.012	3.20 ±0.30	0.125 ±0.012	3.20 ±0.03	0.079 ±0.008	2.01 ±0.2	0.063 ±0.006	1.6 ±0.15
W	0.10 ±0.012	2.54 ±0.30	0.06 ±0.011	1.60 ±0.28	0.049 ±0.008	1.25 ±0.2	0.032 ±0.006	0.8 ±0.15

Ordering Information

VXXML TYPES

V 18 ML X 1206 X X X



ML SERIES

DEVICE FAMILY
Harris TVSS Device

MAXIMUM DC WORKING VOLTAGE

MULTILAYER DESIGNATOR

PERFORMANCE DESIGNATOR
A: Standard
E: ESD (See MLE Data Sheet)

DEVICE SIZE:
i.e., 120 mil x 60 mil

CAPACITANCE OPTION
No Letter: Standard
L: Low Capacitance Version
(Where available - see device ratings for standard versions)

END TERMINATION OPTION
No Letter: Ag/P_t (Standard)
W: Ag/P_d
N: Ni/Sn

PACKING OPTIONS
A: <100 pc Bulk Pak
H: 7in (178mm) Diameter Reel (Note)
T: 13in (330mm) Diameter Reel (Note)

NOTE: See quantity table.

Standard Shipping Quantities

DEVICE SIZE	"13" INCH REEL ("T" OPTION)	"7" INCH REEL ("H" OPTION)	BULK PACK ("A" OPTION)
1210	8,000	2,000	100
1206	10,000	2,500	100
0805	10,000	2,500	100
0603	10,000	2,500	100

Tape and Reel Specifications

- **Conforms to EIA - 481, Revision A**
- **Can be Supplied to IEC Publication 286 - 3**

SYMBOL	DESCRIPTION	MILLIMETERS
A_0	Width of Cavity	Dependent on Chip Size to Minimize Rotation.
B_0	Length of Cavity	Dependent on Chip Size to Minimize Rotation.
K_0	Depth of Cavity	Dependent on Chip Size to Minimize Rotation.
W	Width of Tape	8 ±0.2
F	Distance Between Drive Hole Centers and Cavity Centers	3.5 ±0.5
E	Distance Between Drive Hole Centers and Tape Edge	1.75 ±0.1
P_1	Distance Between Cavity Center	4 ±0.1
P_2	Axial Distance Between Drive Hole Centers and Cavity Centers	2 ±0.1
P_0	Axial Distance Between Drive Hole Centers	4 ±0.1
D_0	Drive Hole Diameter	1.55 ±0.05
D_1	Diameter of Cavity Piercing	1.05 ±0.05
t_1	Embossed Tape Thickness	0.3 max
t_2	Top Tape Thickness	0.1 max

NOTE: Dimensions in millimeters.