

IPS022G/IPS024G

DUAL/QUAD FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

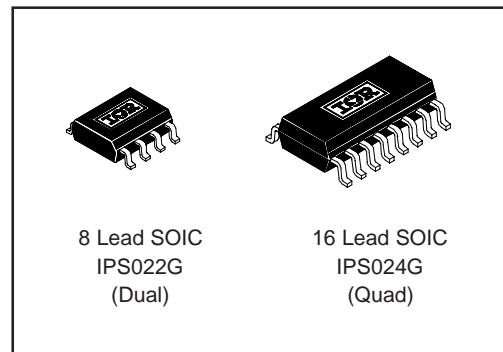
Description

The IPS022G/IPS024G are fully protected dual/quad low side SMART POWER MOSFETs respectively. They feature over-current, over-temperature, ESD protection and drain to source active clamp. These device combine a HEXFET POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 5A. These device restart once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

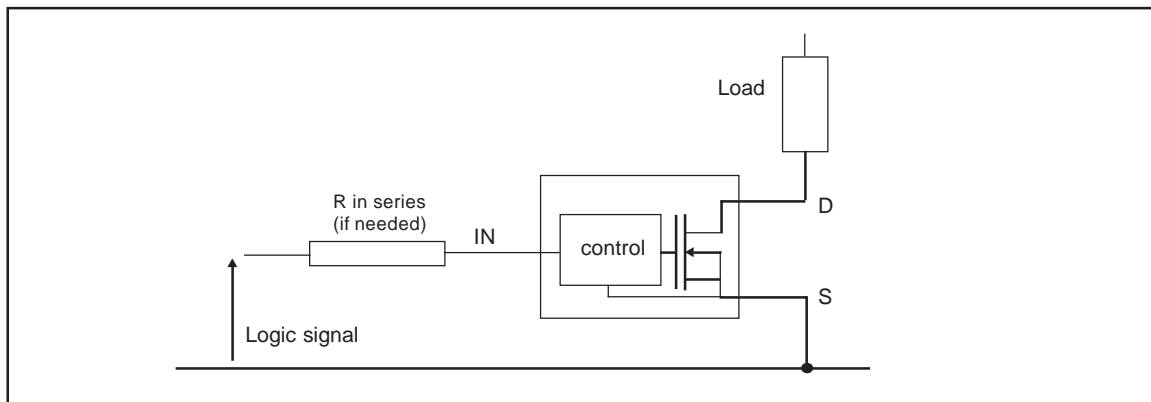
Product Summary

| | |
|------------------|---------------------|
| $R_{ds(on)}$ | 150m Ω (max) |
| V_{clamp} | 50V |
| $I_{shutdown}$ | 5A |
| T_{on}/T_{off} | 1.5 μ s |

Available Package



Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicates sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient} = 25^{\circ}C$ unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness. The values are determined by simulation and characterization.

| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|-----------------|--|------|------|-------------|--------------------------------------|
| V_{ds} | Maximum drain to source voltage | — | 47 | V | |
| V_{in} | Maximum input voltage | -0.3 | 7 | | |
| $I_{in, max}$ | Maximum IN current | -10 | +10 | mA | |
| $I_{sd cont.}$ | Diode max. continuous current ⁽¹⁾ (ΣI_{sd} mosfets, $r_{th}=125^{\circ}C/W$) | — | 1.4 | A | |
| $I_{sd pulsed}$ | Diode max. pulsed current ⁽¹⁾ (for ea. mosfet) | — | 10 | | |
| P_d | Maximum power dissipation ⁽¹⁾ (ΣP_d mosfets, $r_{th}=125^{\circ}C/W$) | — | 1 | W | |
| ESD1 | Electrostatic discharge voltage (Human Body) | — | 5 | kV | C=100pF, R=1500 Ω , |
| ESD2 | Electrostatic discharge voltage (Machine Model) | — | 0.6 | | C=200pF, R=0 Ω , L=10 μH |
| T_j max. | Max. storage & operating junction temp. | -40 | +150 | $^{\circ}C$ | |

Thermal Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|-------------------------|---|------|------|------|---------------|-----------------|
| R_{th1} (2 mos on) | Thermal resistance with standard footprint (2 mosfets on) | — | 100 | 125 | $^{\circ}C/W$ | SOIC-8 |
| R_{th2} (1 mos on) | Thermal resistance with standard footprint (1 mosfet on) | — | 127 | — | | |
| R_{th3} (2 mos on) | Thermal resistance with 1" square footprint (2 mosfets on) | — | — | 80 | | |
| R_{th1} (4 mos on) | Thermal resistance with standard footprint (4 mosfets on) | — | 75 | — | | SOIC-16 |
| R_{th2} (1 mos on) | Thermal resistance with standard footprint (1 mosfet on) | — | 120 | — | | |
| R_{th3} (4 mos on) | Thermal resistance with 1" square footprint (4 mosfets on) | — | 60 | — | | |

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

| Symbol | Parameter | Min. | Max. | Units |
|-------------------------|---|------|------|-------|
| V _{ds} (max) | Continuous drain to source voltage | — | 35 | V |
| V _{IH} | High level input voltage | 4 | 6 | |
| V _{IL} | Low level input voltage | 0 | 0.5 | |
| I _{ds} | Continuous drain current | — | 1 | A |
| T _{amb} =85°C | (T _{Ambient} = 85°C, I _N = 5V, r _{th} = 100°C/W, T _J = 85°C) IPS022G (T _{Ambient} = 85°C, I _N = 5V, r _{th} = 100°C/W, T _J = 125°C) IPS024G | | — | |
| R _{in} | Recommended resistor in series with IN pin | 0.5 | 5 | kΩ |
| T _{r-in} (max) | Max recommended rise time for IN signal (see fig. 2) | — | 1 | μS |
| Fr-lsc ⁽²⁾ | Max. frequency in short circuit condition (V _{cc} = 14V) | 0 | 1 | kHz |

Static Electrical Characteristics

Standard footprint 70 μm copper thickness. (T_J = 25°C unless otherwise specified.)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|-----------------------|---|----------|------------|------------|-------|---|
| R _{ds(on)} | ON state resistance T _J = 25°C T _J = 150°C | 100 — | 130 220 | 150 280 | mΩ | V _{in} = 5V, I _{ds} = 1A |
| I _{dss 1} | Drain to source leakage current | 0 | 0.01 | 25 | μA | V _{cc} = 14V, T _J = 25°C |
| I _{dss 2} | Drain to source leakage current | 0 | 0.1 | 50 | | V _{cc} = 40V, T _J = 25°C |
| V _{clamp 1} | Drain to source clamp voltage 1 | 48 | 54 | 56 | V | I _d = 20mA (see Fig.3 & 4) |
| V _{clamp 2} | Drain to source clamp voltage 2 | 50 | 56 | 60 | | I _d =I _{shutdown} (see Fig.3 & 4) |
| V _{in clamp} | IN to source clamp voltage | 7 | 8 | 9.5 | | I _{in} = 1 mA |
| V _{th} | IN threshold voltage | 1 | 1.5 | 2 | | I _d = 50mA, V _{ds} = 14V |
| I _{in, -on} | ON state IN positive current | 25 | 90 | 200 | μA | V _{in} = 5V |
| I _{in, -off} | OFF state IN positive current | 50 | 130 | 250 | | V _{in} = 5V over-current triggered |

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 10Ω, R_{input} = 50Ω, 100μsec pulse, T_J = 25°C, (unless otherwise specified).

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|------------------|---|------|------|------|-------|----------------------|
| T _{on} | Turn-on delay time | 0.15 | 0.5 | 1 | μsec | See figure 2 |
| T _r | Rise time | 0.4 | 0.9 | 2 | | |
| T _{rf} | Time to (final R _{ds(on)}) 1.3) | 2 | 6 | 12 | | |
| T _{off} | Turn-off delay time | 0.8 | 2 | 3.5 | μsec | See figure 2 |
| T _f | Fall time | 0.5 | 1.3 | 2.5 | | |
| Q _{in} | Total gate charge | — | 30 | — | nC | V _{in} = 5V |

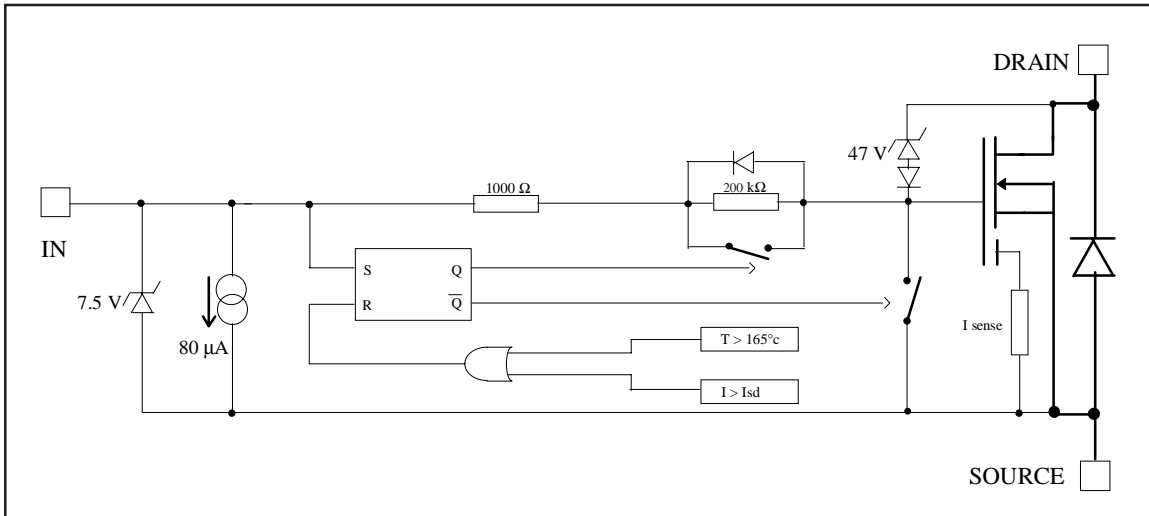
(2) Operations at higher switching frequencies is possible. See Appl. notes.

Protection Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|-------------------|---|------|------|------|--------------------|-----------------------|
| T_{sd} | Over temperature threshold | — | 165 | — | $^{\circ}\text{C}$ | See fig. 1 |
| I_{sd} | Over current threshold | 4 | 5.5 | 7 | A | See fig. 1 |
| $V_{in,min,prot}$ | Minimum IN voltage for protection | 1.5 | 2.3 | 3 | V | |
| T_{reset} | Minimum time for protection reset | 2 | 10 | 40 | μs | $V_{in} = 0\text{V}$ |
| EOI_OT | Short circuit energy (see application note) | — | 400 | — | μJ | $V_{cc} = 14\text{V}$ |

Functional Block Diagram

All values are typical



Lead Assignments

| | |
|-------------------------------|--------------------------------|
| <p>8 Lead SOIC (Dual)</p> | <p>16 Lead SOIC (Quad)</p> |
| IPS022G | IPS024G |
| Part Number | |

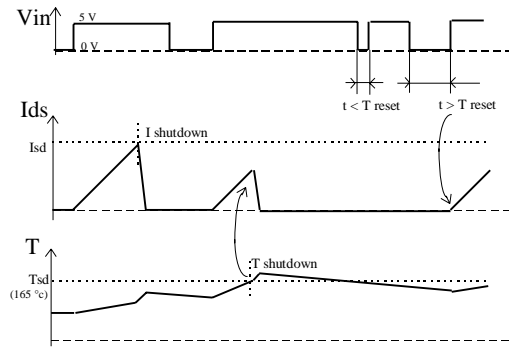


Figure 1 - Timing diagram

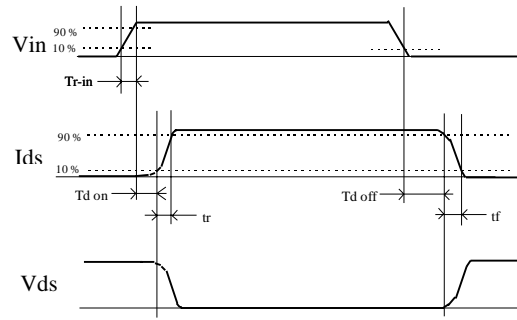


Figure 2 - IN rise time & switching time definitions

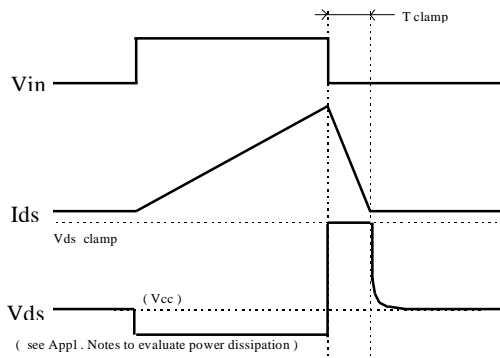


Figure 3 - Active clamp waveforms

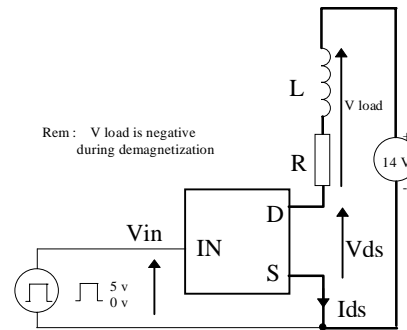


Figure 4 - Active clamp test circuit

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All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

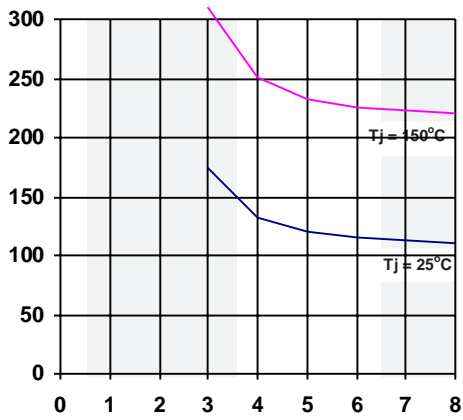


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

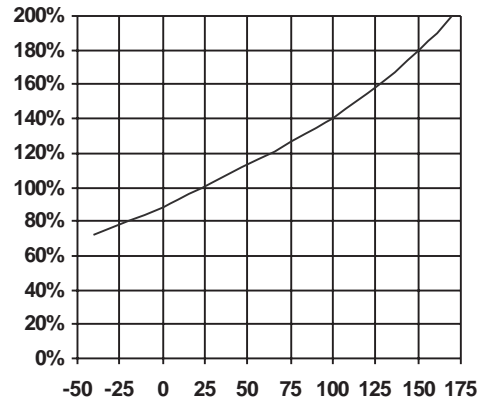


Figure 6 - Normalized Rds(on) Vs Tj (°C)

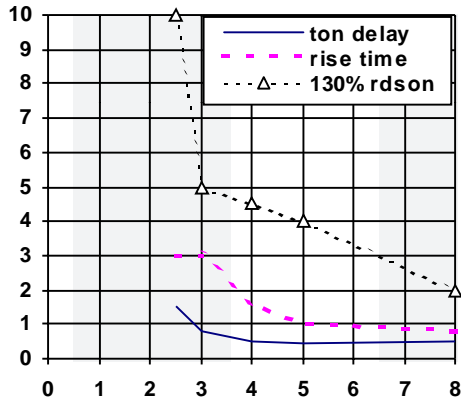


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) Vs Input Voltage (V)

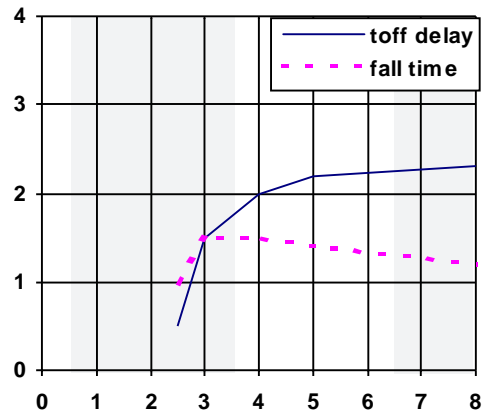


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

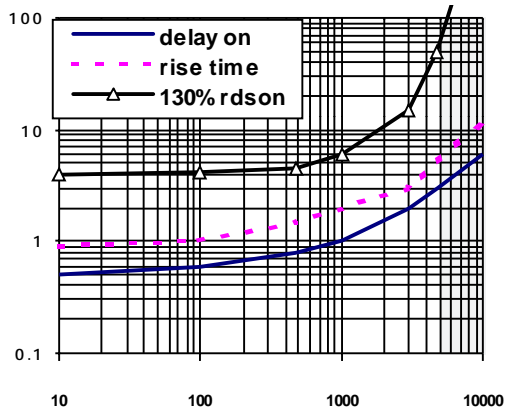


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) Vs IN Resistor (Ω)

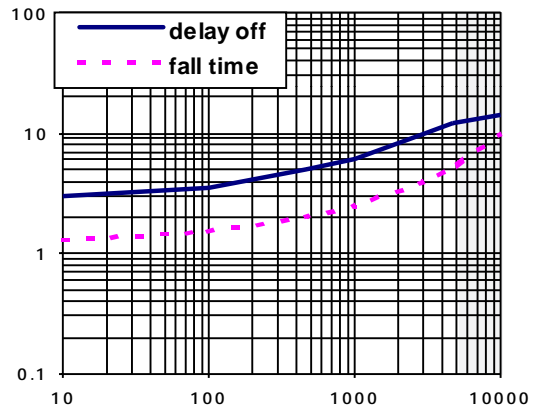


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

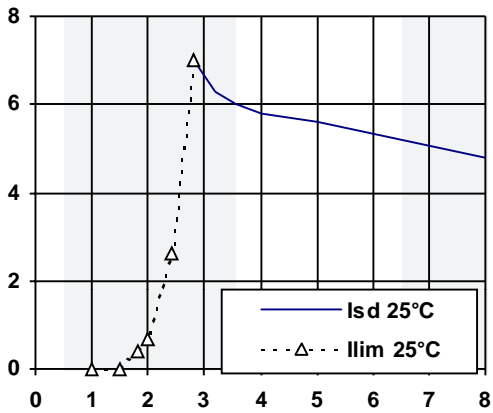


Figure 11 - Current lim. & Isshutdown (A) Vs Vin (V)

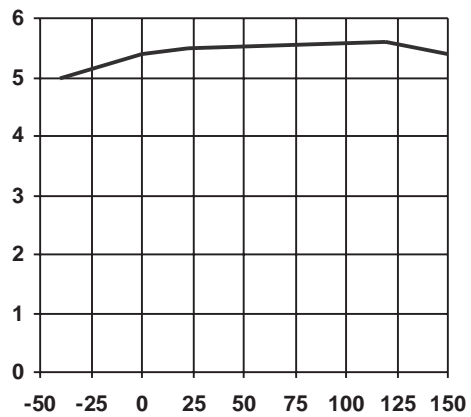


Figure 12 - Over-current (A) Vs Tjunction (°C)

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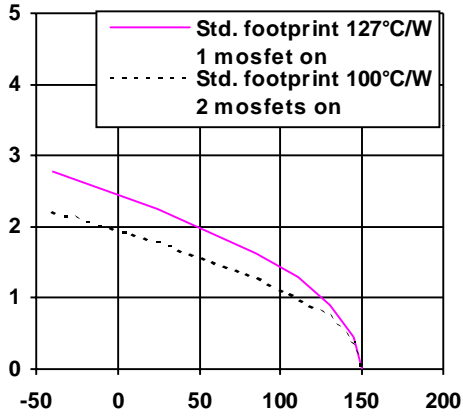


Figure 13a - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) - IPS022G

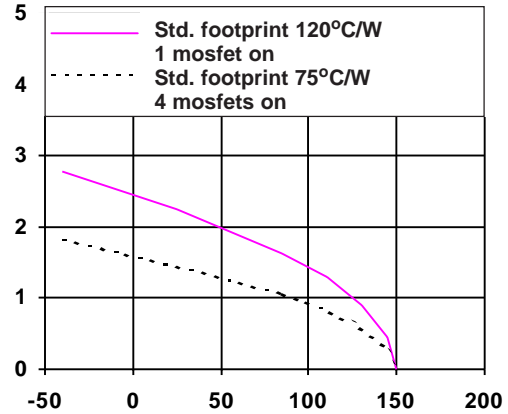


Figure 13b - Max.Cont. Ids (A)
Vs Amb. Temperature (°C) - IPS024G

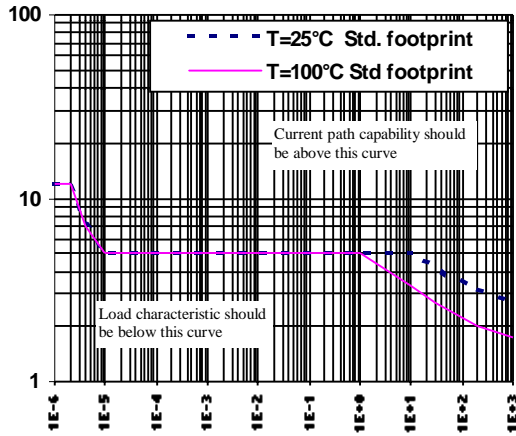


Figure 14 - Ids (A) Vs Protection Resp. Time (s)
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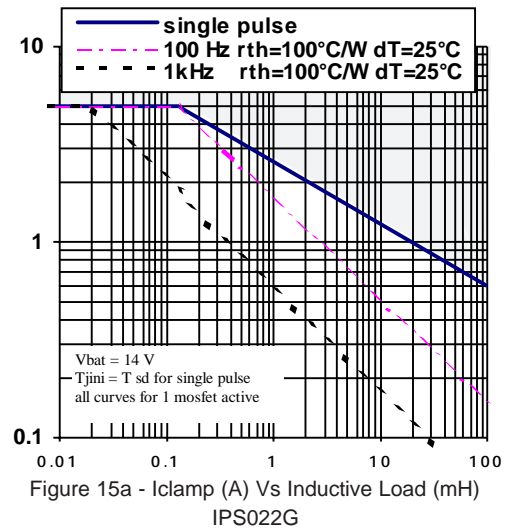


Figure 15a - Iclamp (A) Vs Inductive Load (mH)
IPS022G

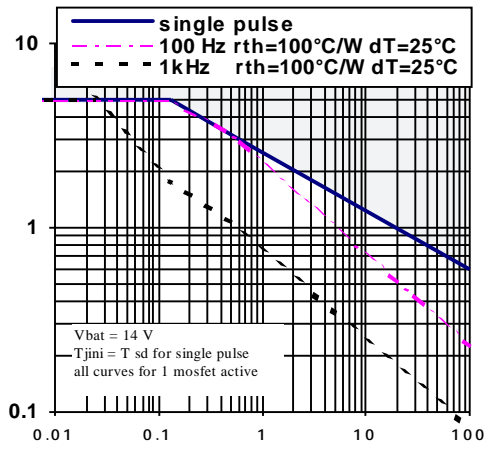


Figure 15b - Max. Iclamp (A) Vs Inductive Load (mH) - IPS024G

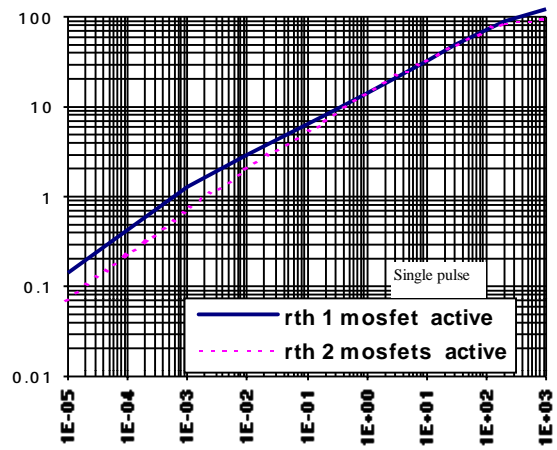


Figure 16a - Transient Thermal Imped. (°C/W) Vs Time (s) - IPS022G

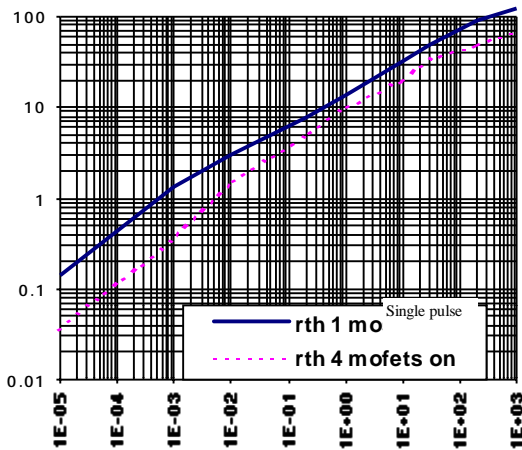


Figure 16b - Transient Thermal Imped. (°C/W) Vs Time (s) - IPS024G

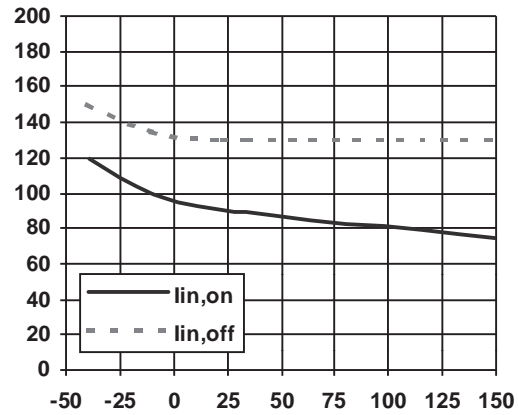


Figure 17 - Input Current (uA) Vs Junction Temperature (°C)

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International
IOR Rectifier

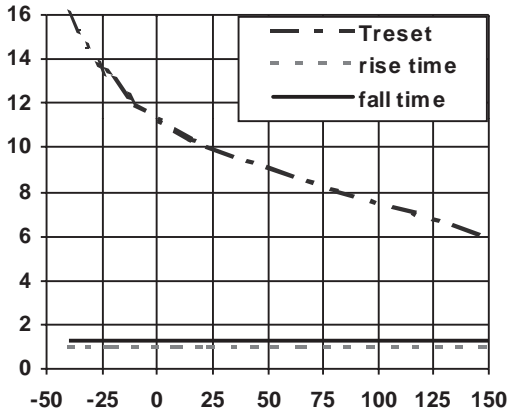


Figure 18 - Rise Time, Fall Time and Treset (µsec)
Vs Tjunction (°C)

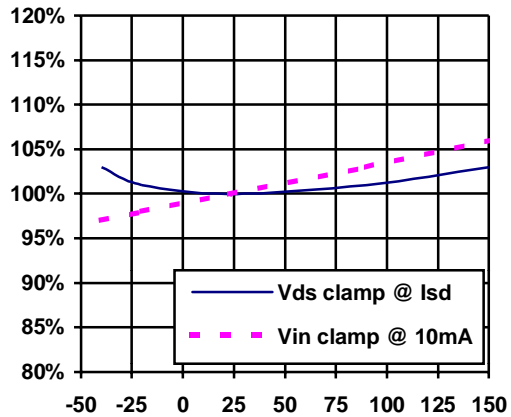
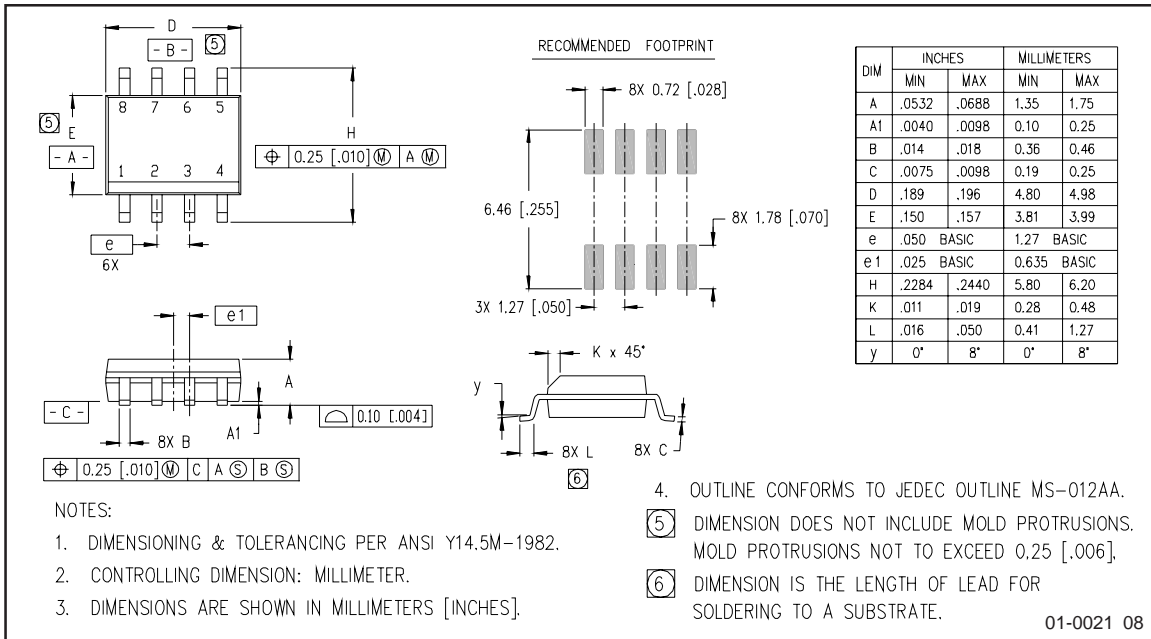


Figure 19 -V_{in} clamp and V_{ds} clamp2 Vs
Tjunction (°C)

Case Outline - 8 Lead SOIC



Case Outline - 16 Lead SOIC (narrow body)

