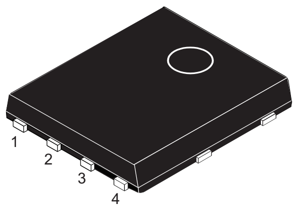
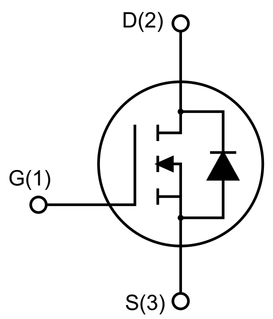
# N-channel 650 V, 0.335 Ω typ., 10 A MDmesh™ V Power MOSFET in a PowerFLAT™ 5x6 HV package

**Datasheet — production data**




**PowerFLAT™ 5x6 HV**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STL15N65M5 | 710 V | < 0.375 Ω | 10 A(1) |

1. The value is rated according to $R_{thj\text{-}case}$ and limited by package

- Outstanding $R_{DS(on)}$*area
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitance
- 100% avalanche tested

## Applications

- Switching applications

## Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL15N65M5 | 15N65M5 | PowerFLAT™ HV | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 650 | V |
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | 10 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 100 °C | 5 | A |
| $I_{DM}$ (1),(2) | Drain current (pulsed) | 40 | A |
| $P_{TOT}$(1) | Total dissipation at $T_C$ = 25 °C | 52 | W |
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max) | 2.5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 160 | mJ |
| dv/dt (3) | Peak diode recovery voltage slope | 160 | V/ns |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | 150 | °C |

1. The value is rated according to $R_{thj-case}$ and limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq$ 10 A, di/dt $\leq$ 400 A/µs, $V_{Peak} \leq V_{(BR)DSS}$, $V_{DD}$ = 400 V.

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj-case}$ | Thermal resistance junction-case max | 2.4 | °C/W |
| $R_{thj-pcb}$(1) | Thermal resistance junction-pcb max | 59 | °C/W |

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS}$ = 0) | $I_D$ = 1 mA | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 650 V | | | 1 | µA |
| | | $V_{DS}$ = 650 V, $T_C$=125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 25 V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 5 A | | 0.335 | 0.375 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 816 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 23 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.6 | - | pF |
| $C_{o(tr)}$(1) | Equivalent capacitance time related | $V_{DS}$ = 0 to 520 V, $V_{GS}$ = 0 | - | 70 | - | pF |
| $C_{o(er)}$(2) | Equivalent capacitance energy related | | - | 21 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 5 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 5.5 A, $V_{GS}$ = 10 V (see *Figure 16*) | - | 22 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 5.5 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 11 | - | nC |

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d\ (on)}$ | Turn-on delay time | $V_{DD}$ = 400 V, $I_D$ = 7 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 17*), (see *Figure 20*) | - | 30 | - | ns |
| $t_r$ | Rise time | | - | 8 | - | ns |
| $t_{d\ (off)}$ | Turn-off delay time | | - | 11 | - | ns |
| $t_f$ | Fall time | | - | 12.5 | - | ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ (1) | Source-drain current | | - | | 10 | A |
| $I_{SDM}$ (1), (2) | Source-drain current (pulsed) | | - | | 40 | A |
| $V_{SD}$ (3) | Forward on voltage | $I_{SD}$ = 10 A, $V_{GS}$ = 0 | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 10 A, di/dt = 100 A/µs $V_{DD}$ = 100 V (see *Figure 17*) | - | 244 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.35 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 19.2 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 10 A, di/dt = 100 A/µs $V_{DD}$ = 100 V, $T_j$ = 150 °C (see *Figure 17*) | - | 308 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.93 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 19 | | A |

1. The value is rated according to $R_{thj\text{-}case}$ and limited by package
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

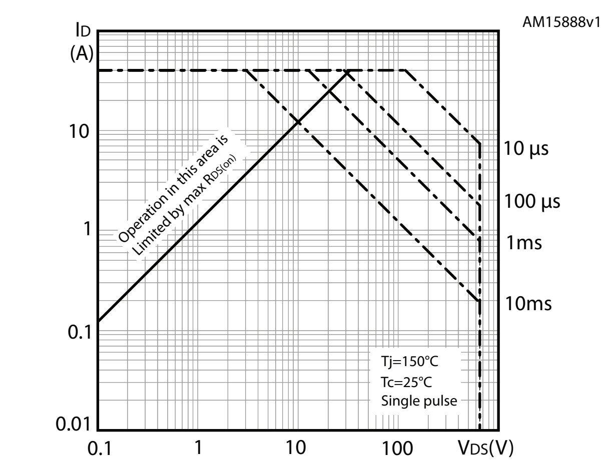



Figure 3. Thermal impedance

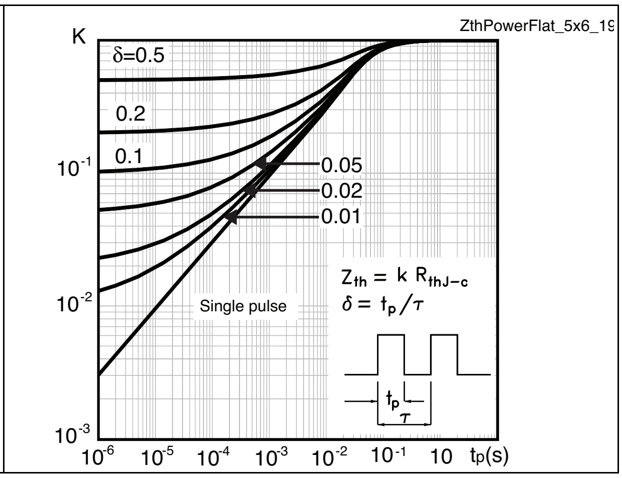



Figure 4. Output characteristics

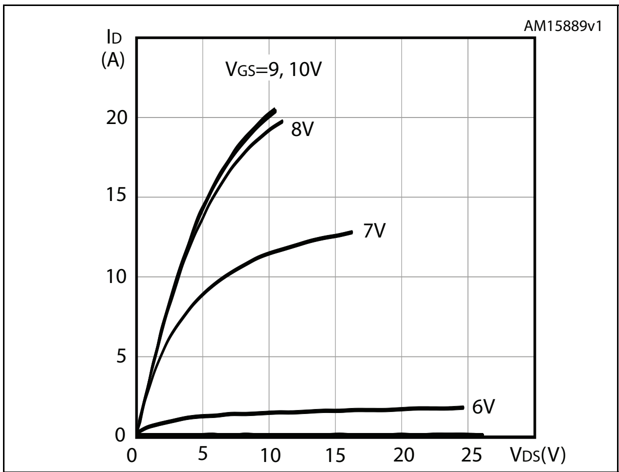



Figure 5. Transfer characteristics

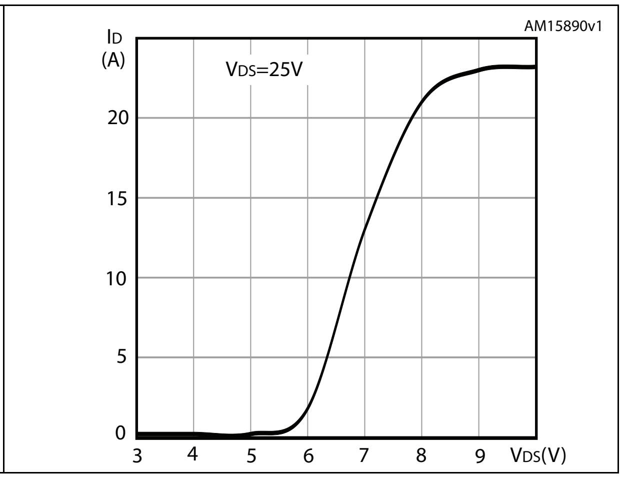



Figure 6. Static drain-source on-resistance

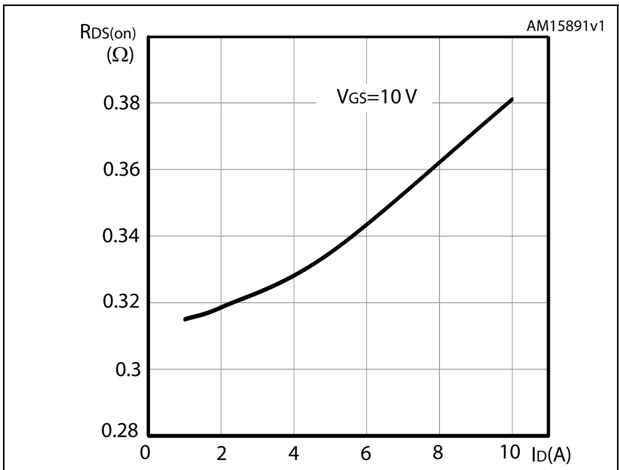



Figure 7. Gate charge vs gate-source voltage

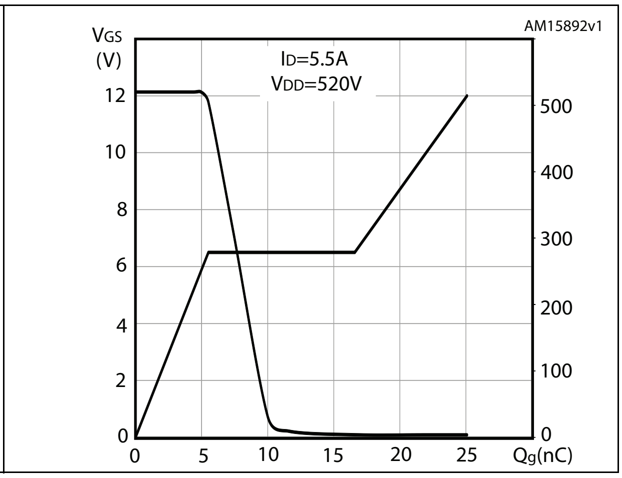


**Figure 8. Capacitance variations**

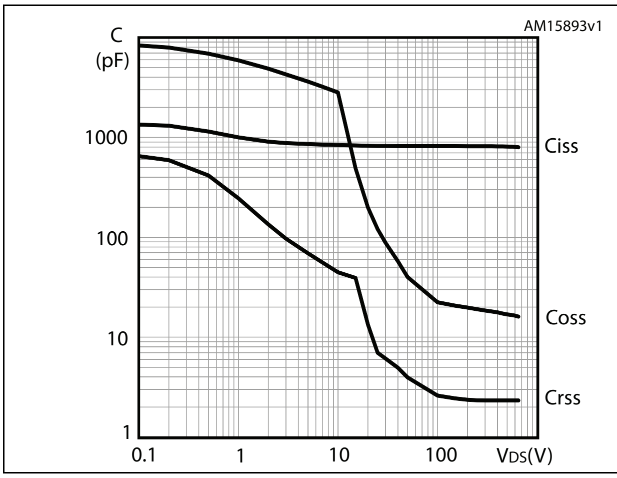



**Figure 9. Output capacitance stored energy**

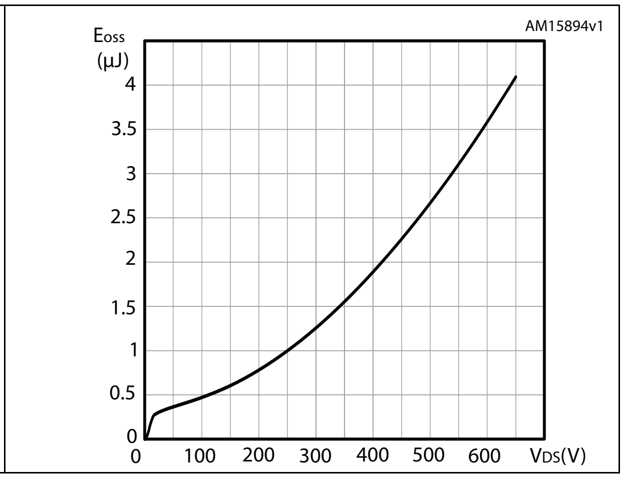



**Figure 10. Normalized gate threshold voltage vs temperature**

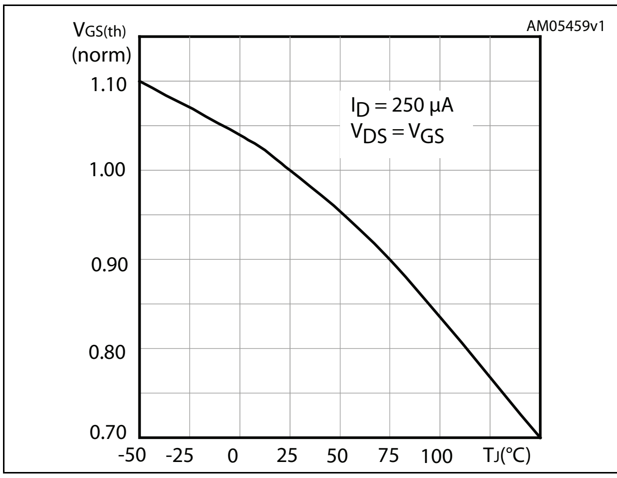



**Figure 11. Normalized on-resistance vs temperature**

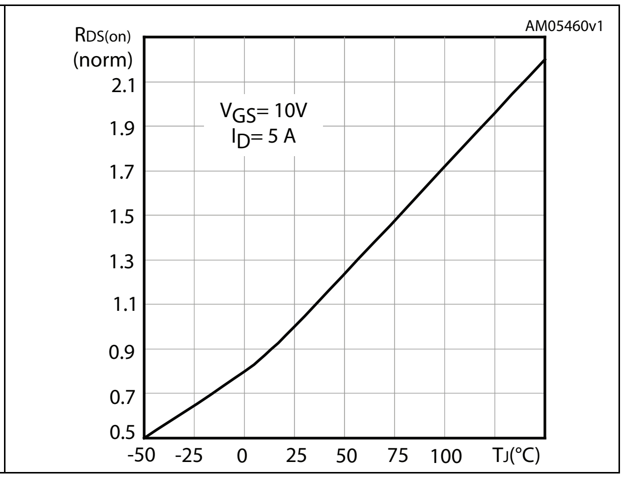



**Figure 12. Source-drain diode forward characteristics**

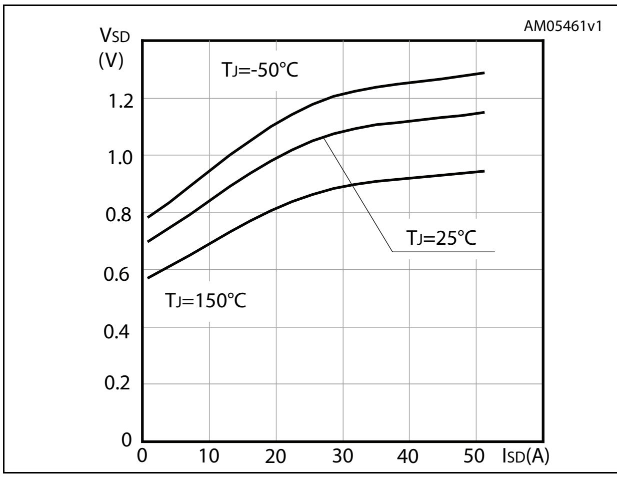



**Figure 13. Normalized $B_{VDSS}$ vs temperature**

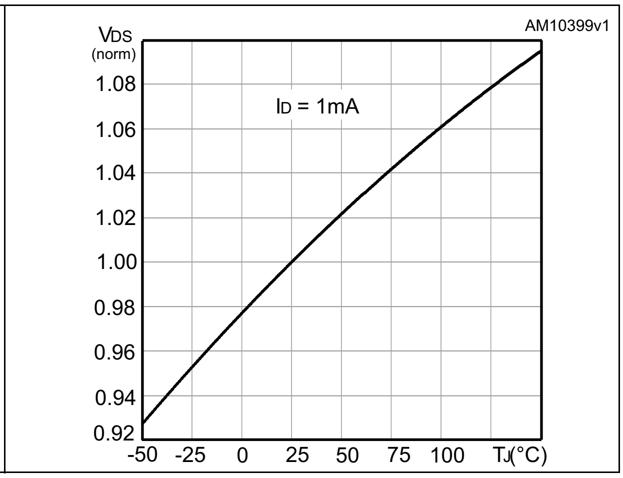
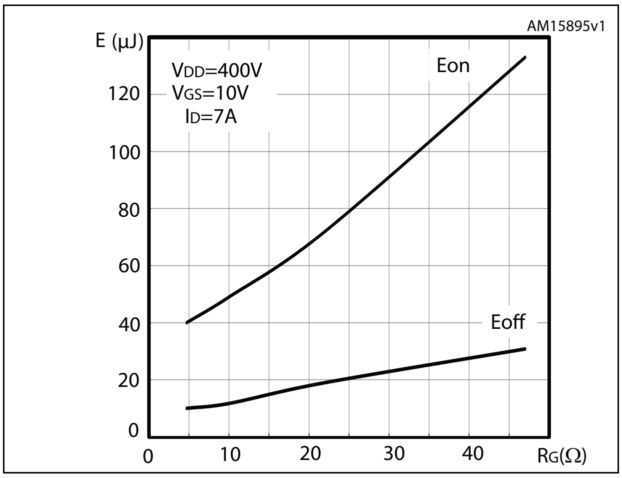


**Figure 14. Switching losses vs gate resistance (1)**




1. Eon including reverse recovery of a SiC diode

# 3 Test circuits

Figure 15. Switching times test circuit for resistive load

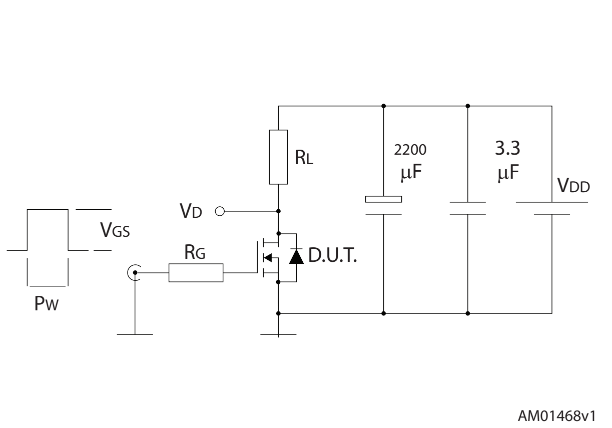



Figure 16. Gate charge test circuit

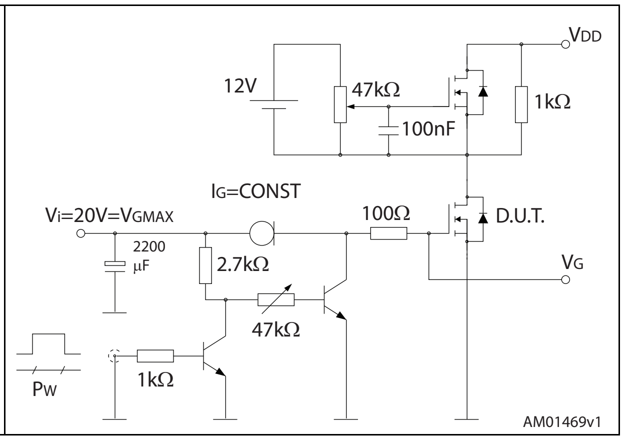



Figure 17. Test circuit for inductive load switching and diode recovery times

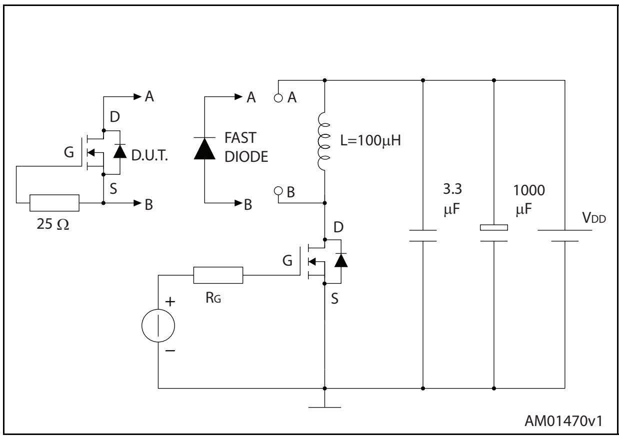



Figure 18. Unclamped inductive load test circuit

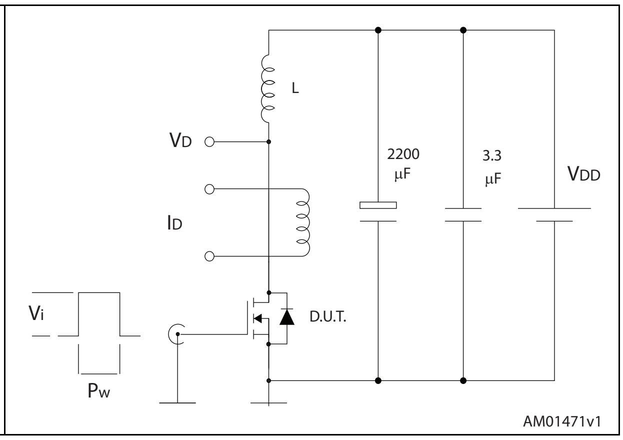



Figure 19. Unclamped inductive waveform

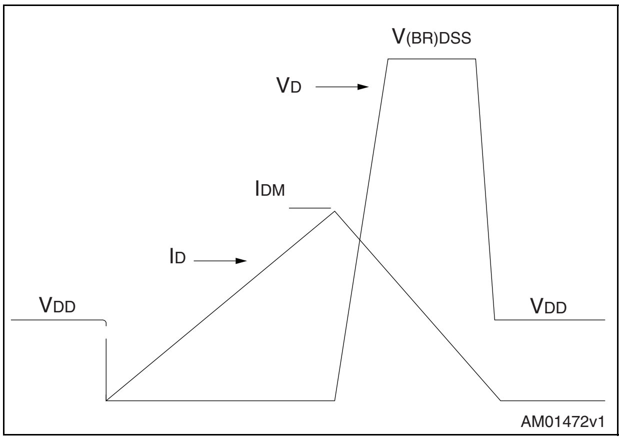
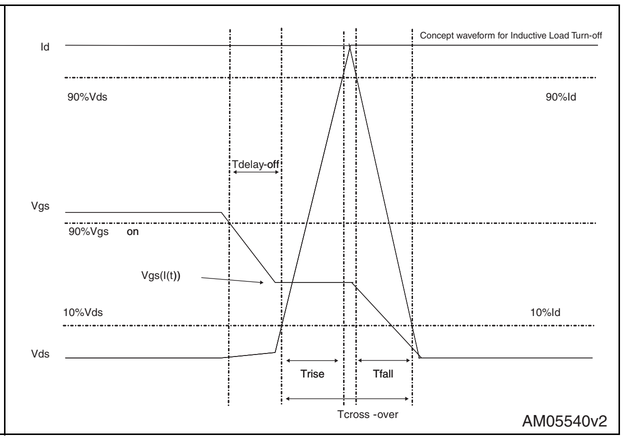



Figure 20. Switching time waveform



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. PowerFLAT™ 5x6 HV creepage

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | 5.00 | 5.20 | 5.40 |
| E | 5.95 | 6.15 | 6.35 |
| D2 | 4.30 | 4.40 | 4.50 |
| E2 | 3.10 | 3.20 | 3.30 |
| e | | 1.27 | |
| L | 0.50 | 0.55 | 0.60 |
| K | 1.90 | 2.00 | 2.10 |
| aaa | | 0.15 | |
| bbb | | 0.15 | |
| ccc | | 0.10 | |
| eee | | 0.10 | |

**Figure 21. PowerFLAT™ 5x6 HV creepage**

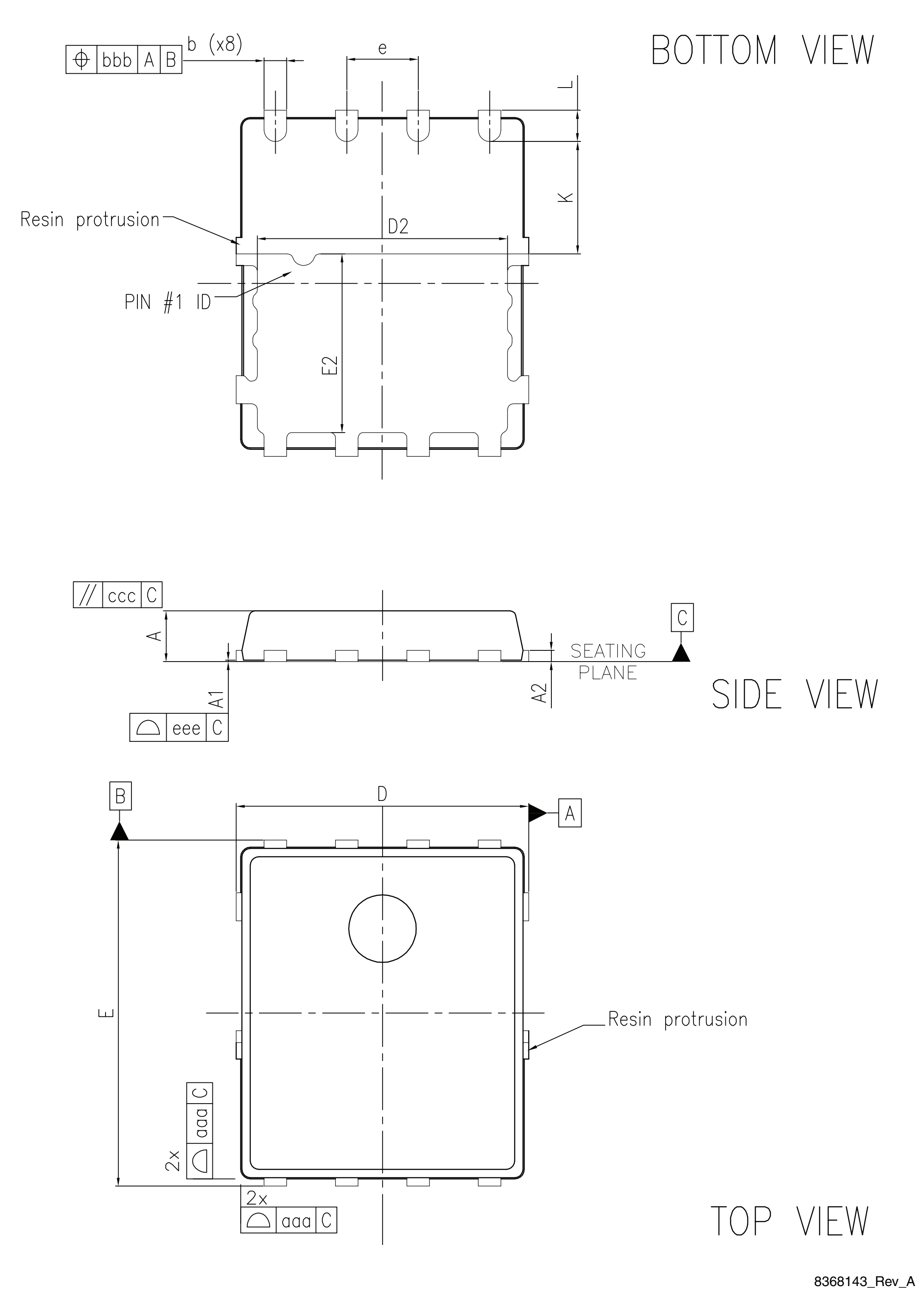
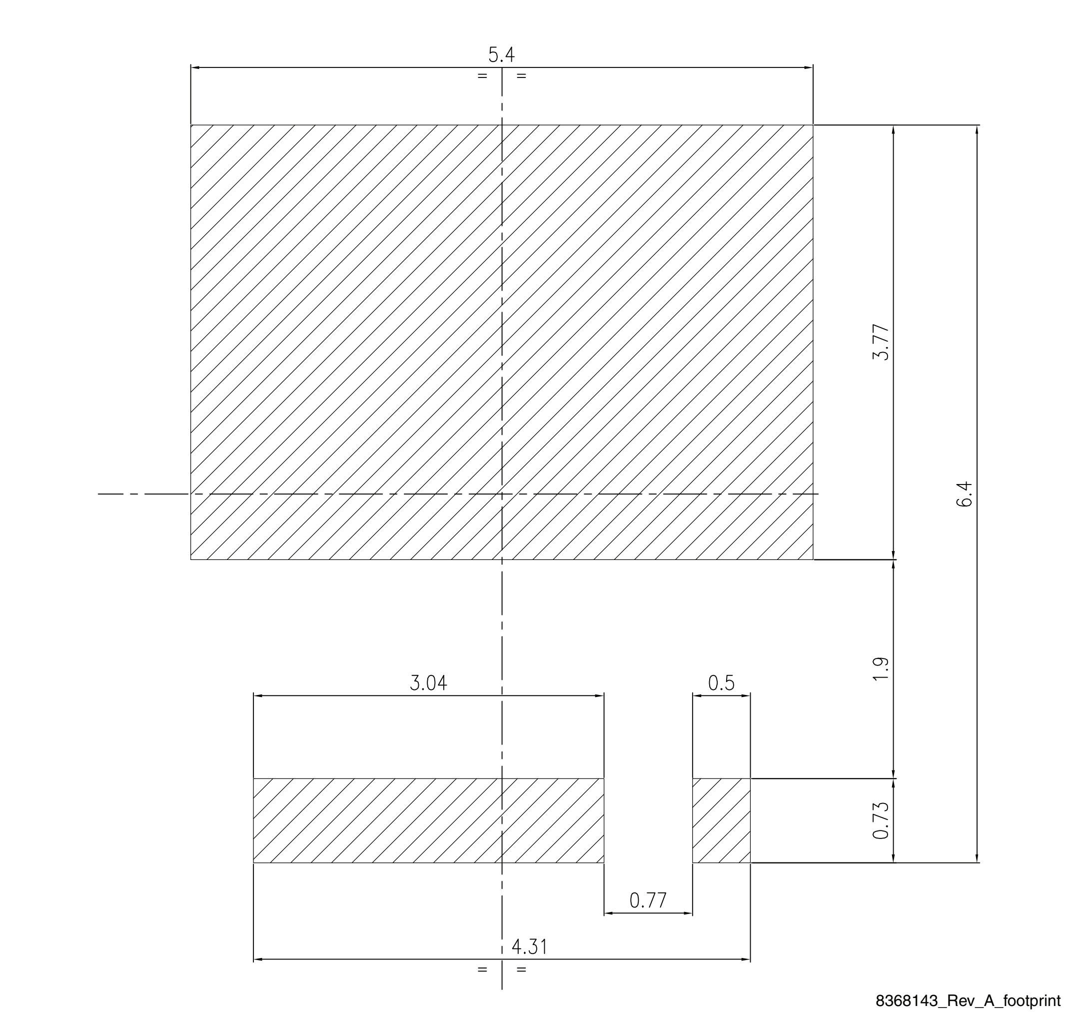


**Figure 22. PowerFLAT™ 5x6 HV creepage (dimensions are in mm)**



# 5 Packaging mechanical data

**Figure 23. PowerFLAT™ 5x6 tape[(a)]**

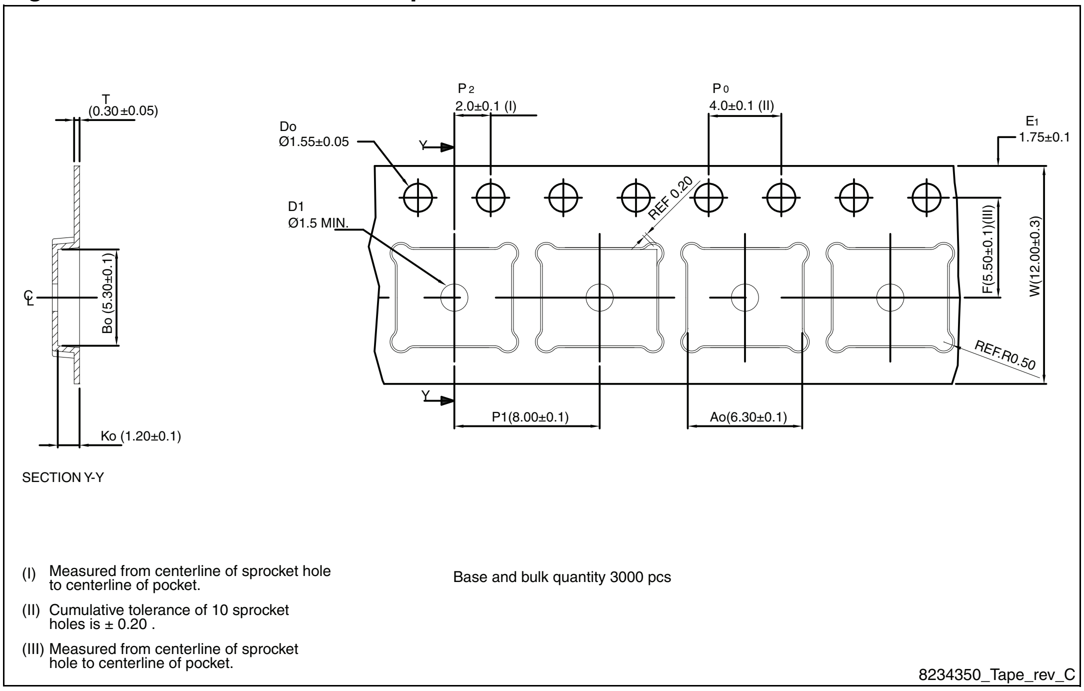
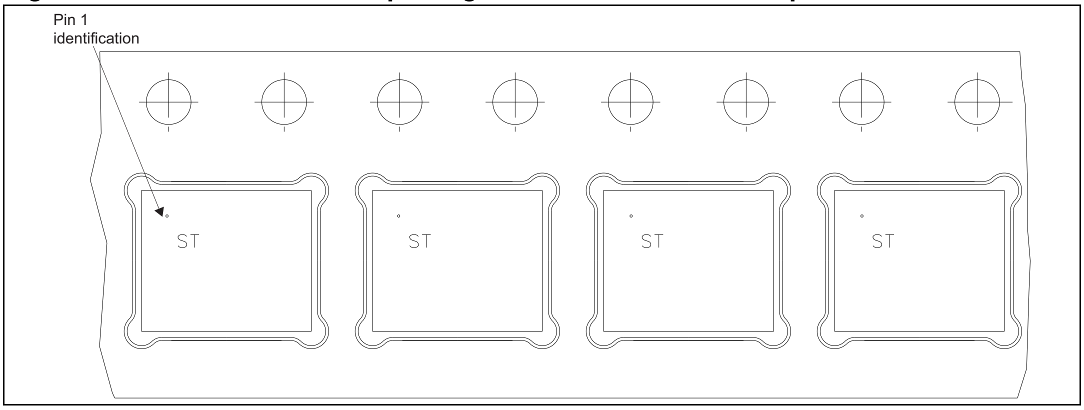
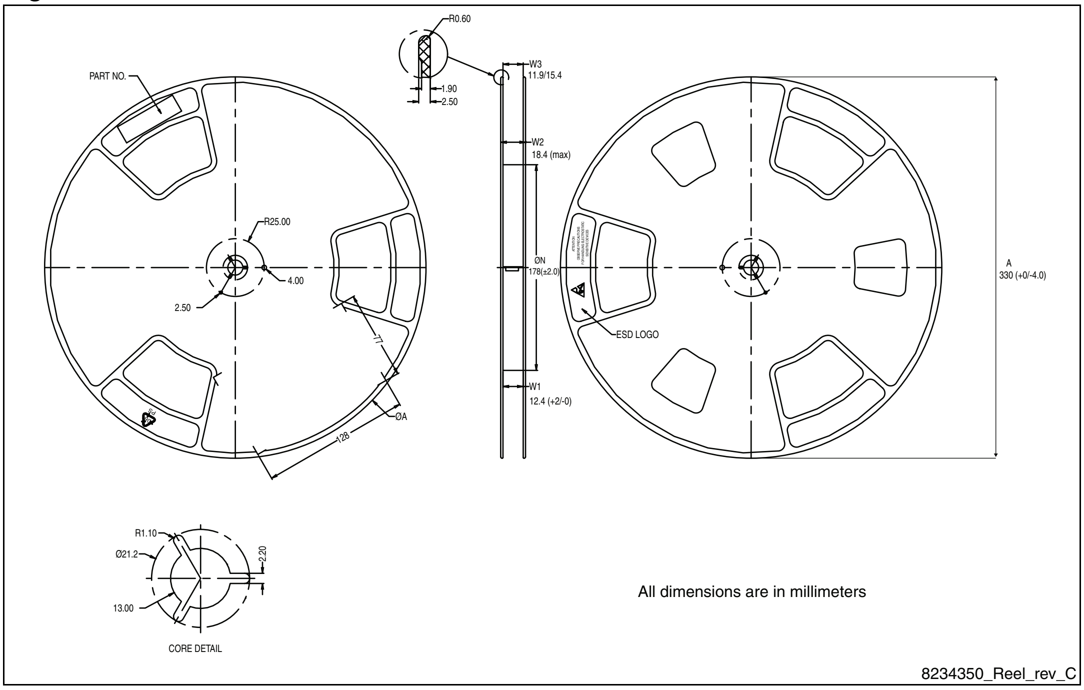



**Figure 24. PowerFLAT™ 5x6 package orientation in carrier tape.**




a. All dimensions are in millimeters.

**Figure 25. PowerFLAT™ 5x6 reel**



# 6 Revision history

**Table 9. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 26-Jun-2013 | 1 | First release |