

IRG4PSC71UPbF

INSULATED GATE BIPOLAR TRANSISTOR

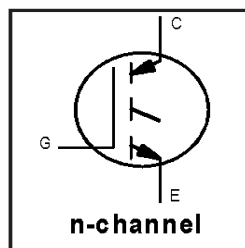
UltraFast Speed IGBT

Features

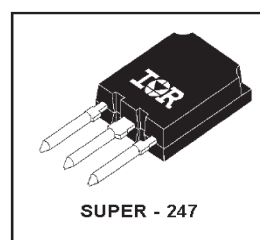
- UltraFast switching speed optimized for operating frequencies 8 to 40kHz in hard switching, 200kHz in resonant mode soft switching
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency (minimum switching and conduction losses) than prior generations
- Industry-benchmark Super-247 package with higher power handling capability compared to same footprint TO-247
- Creepage distance increased to 5.35mm
- Lead-Free

Benefits

- Generation 4 IGBT's offer highest efficiencies available
- Maximum power density, twice the power handling of the TO-247, less space than TO-264
- IGBTs optimized for specific application conditions
- Cost and space saving in designs that require multiple, paralleled IGBTs



$V_{CES} = 600V$
$V_{CE(on)} \text{ typ.} = 1.67V$
@ $V_{GE} = 15V, I_C = 60A$



Absolute Maximum Ratings

	Parameter	Max.	Units
V _{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I _C @ T _C = 25°C	Continuous Collector Current	85⑥	A
I _C @ T _C = 100°C	Continuous Collector Current	60	
I _{CM}	Pulsed Collector Current ①	200	
I _{LM}	Clamped Inductive Load Current ②	200	
V _{GE}	Gate-to-Emitter Voltage	± 20	V
E _{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
P _D @ T _C = 25°C	Maximum Power Dissipation	350	W
P _D @ T _C = 100°C	Maximum Power Dissipation	140	
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
		300 (0.063 in. (1.6mm from case))	

Thermal Resistance\ Mechanical

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.36	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	38	
	Recommended Clip Force	20.0(2.0)	—	—	N (kgf)
	Weight	—	6 (0.21)	—	g (oz)

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	$V_{GE} = 0V, I_C = 1.0A$
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.45	—	V/°C	$V_{GE} = 0V, I_C = 5.0mA$
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.67	2.0	V	$I_C = 60A, V_{GE} = 15V$
		—	1.95	—		$I_C = 100A, V_{GE} = 15V$
		—	1.71	—		$I_C = 60A, T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	$V_{CE} = V_{GE}, I_C = 1.0mA$
g_{fe}	Forward Transconductance ⑤	47	70	—	S	$V_{CE} = 50V, I_C = 60A$
I_{CES}	Zero Gate Voltage Collector Current	—	—	500	μA	$V_{GE} = 0V, V_{CE} = 600V$
		—	—	2.0		$V_{GE} = 0V, V_{CE} = 10V, T_J = 25^\circ\text{C}$
		—	—	5.0	mA	$V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	340	520	nC	$I_C = 60A$
Q_{ge}	Gate - Emitter Charge (turn-on)	—	44	66		$V_{CC} = 400V$
Q_{gc}	Gate - Collector Charge (turn-on)	—	160	240		$V_{GE} = 15V$
$t_{d(on)}$	Turn-On Delay Time	—	34	—	ns	$T_J = 25^\circ\text{C}$ $I_C = 60A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 5.0\Omega$ Energy losses include "tail"
t_r	Rise Time	—	50	—		
$t_{d(off)}$	Turn-Off Delay Time	—	56	84		
t_f	Fall Time	—	86	130		
E_{on}	Turn-On Switching Loss	—	0.42	—	mJ	See Fig. 10, 11, 13, 14
E_{off}	Turn-Off Switching Loss	—	1.99	—		
E_{ts}	Total Switching Loss	—	2.41	3.2		
$t_{d(on)}$	Turn-On Delay Time	—	30	—	ns	$T_J = 150^\circ\text{C}$, $I_C = 60A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 5.0\Omega$ Energy losses include "tail"
t_r	Rise Time	—	49	—		
$t_{d(off)}$	Turn-Off Delay Time	—	129	—		
t_f	Fall Time	—	175	—		
E_{ts}	Total Switching Loss	—	4.5	—	mJ	See Fig. 13, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	7500	—	pF	$V_{GE} = 0V$
C_{oes}	Output Capacitance	—	720	—		$V_{CC} = 30V$
C_{res}	Reverse Transfer Capacitance	—	93	—		$f = 1.0MHz$

Notes:

- ① Repetitive rating; $V_{GE} = 20V$, pulse width limited by max. junction temperature. (See fig. 13b)
- ② $V_{CC} = 80\%(V_{CES})$, $V_{GE} = 20V$, $L = 10\mu H$, $R_G = 5.0\Omega$, (See fig. 13a)
- ③ Repetitive rating; pulse width limited by maximum junction temperature.
- ④ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
- ⑤ Pulse width $5.0\mu s$, single shot.
- ⑥ Current limited by the package, (Die current = 100A)

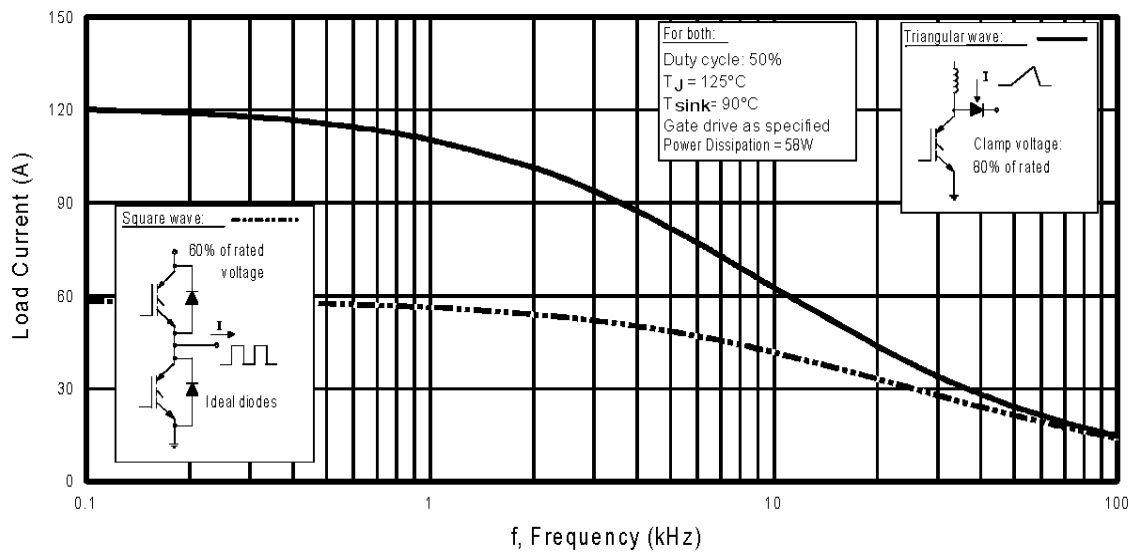


Fig. 1 - Typical Load Current vs. Frequency
(For square wave, $I = I_{\text{RMS}}$ of fundamental; for triangular wave, $I = I_{\text{PK}}$)

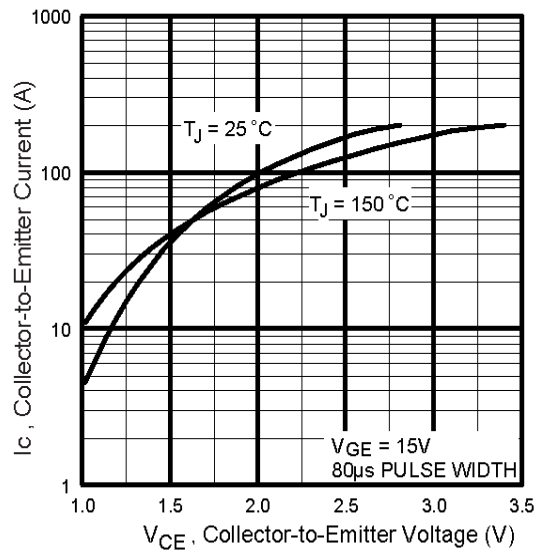


Fig. 2 - Typical Output Characteristics

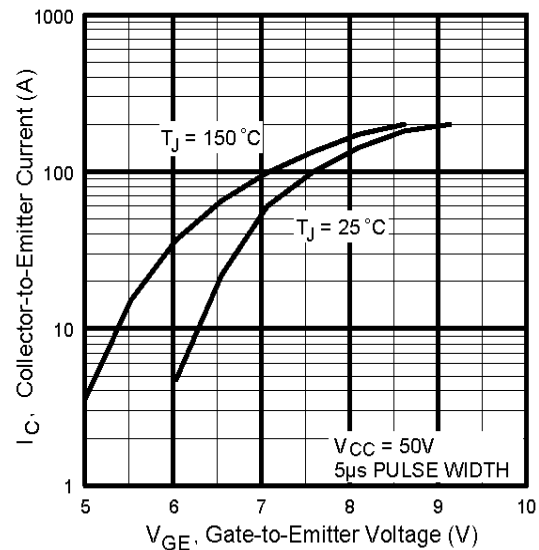


Fig. 3 - Typical Transfer Characteristics

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International
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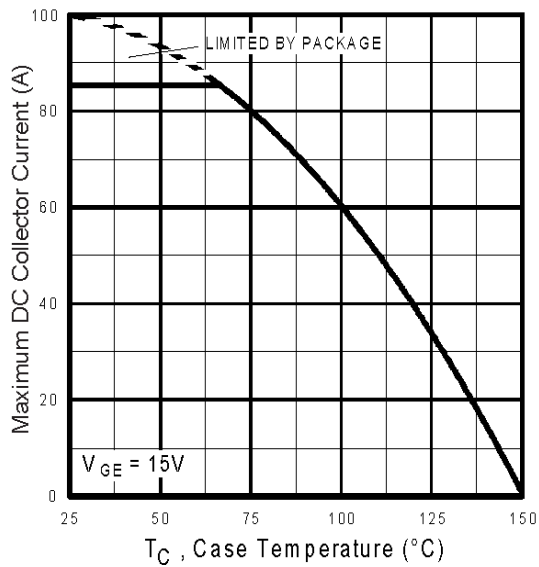


Fig. 4 - Maximum Collector Current vs. Case Temperature

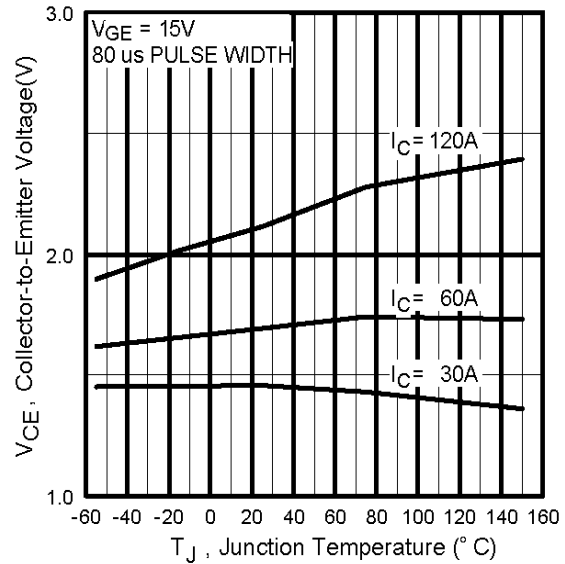


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

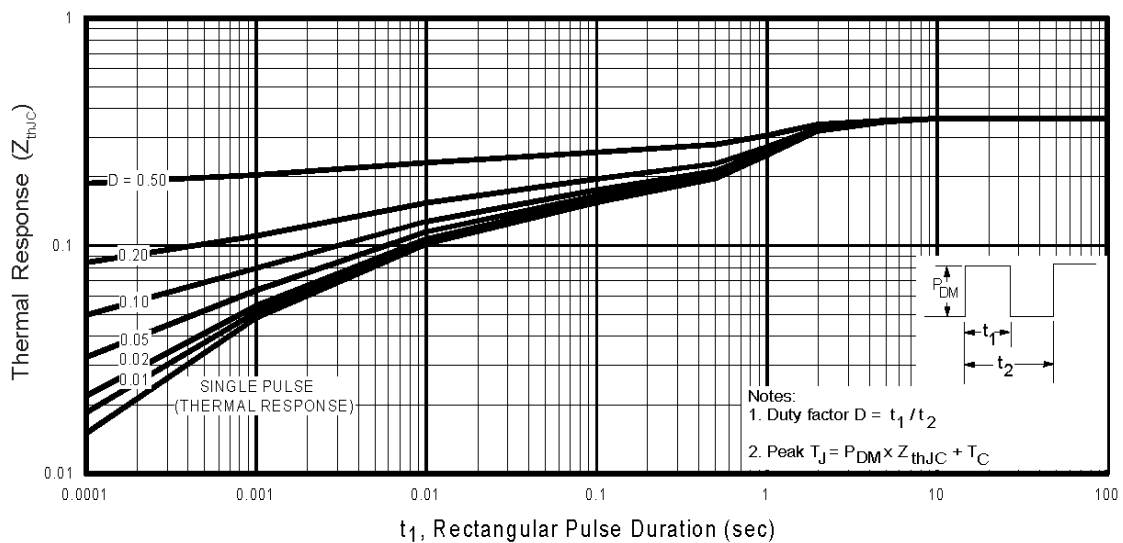


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

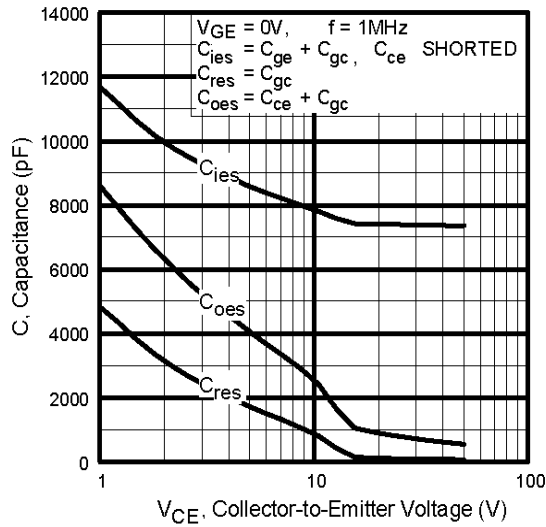


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

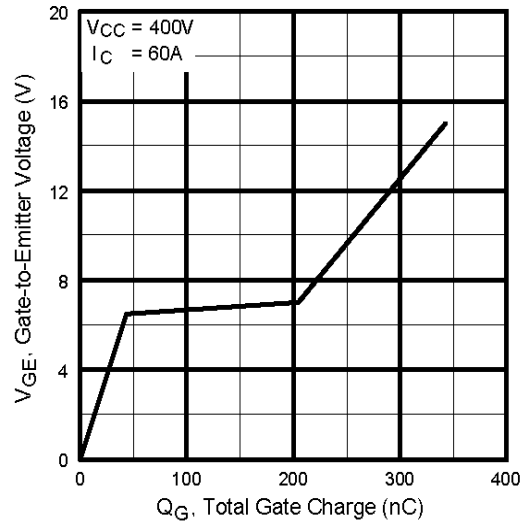


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

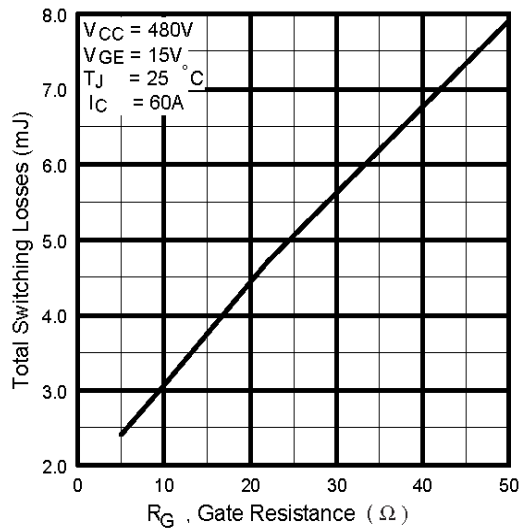


Fig. 9 - Typical Switching Losses vs. Gate Resistance

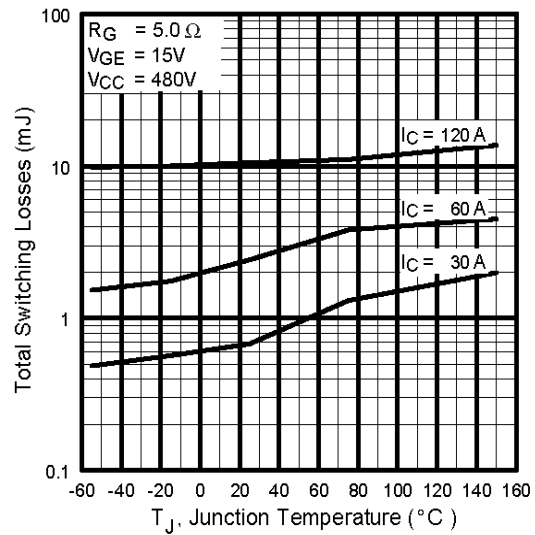


Fig. 10 - Typical Switching Losses vs. Junction Temperature

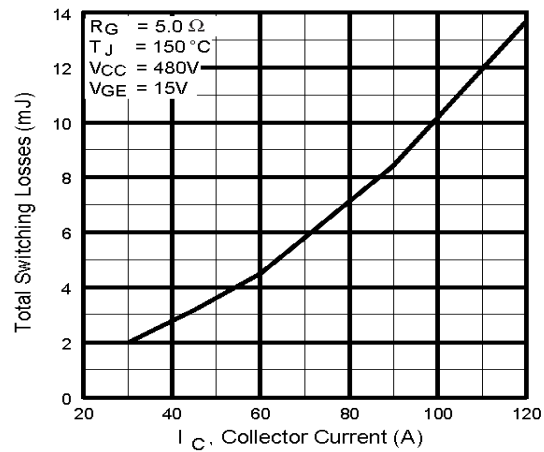


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

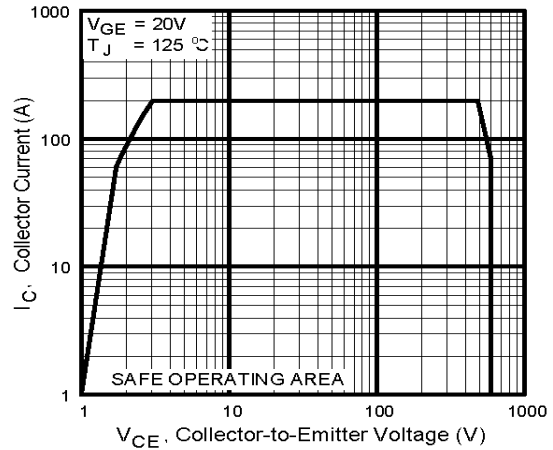
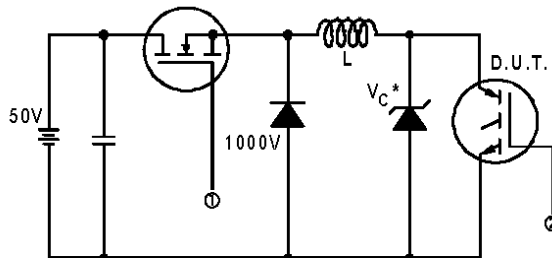


Fig. 12 - Turn-Off SOA



* Driver same type as D.U.T.; $V_c = 80\%$ of $V_{ce(max)}$
 * Note: Due to the 50V power supply, pulse width and inductor will increase to obtain rated I_d .

Fig. 13a - Clamped Inductive Load Test Circuit

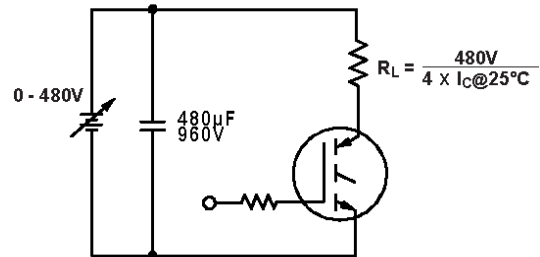


Fig. 13b - Pulsed Collector Current Test Circuit

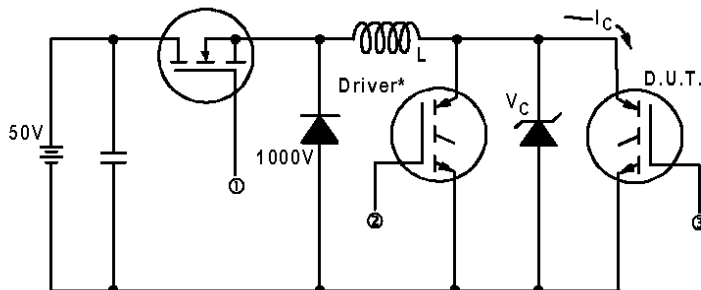


Fig. 14a - Switching Loss Test Circuit

* Driver same type as D.U.T., $V_c = 480V$

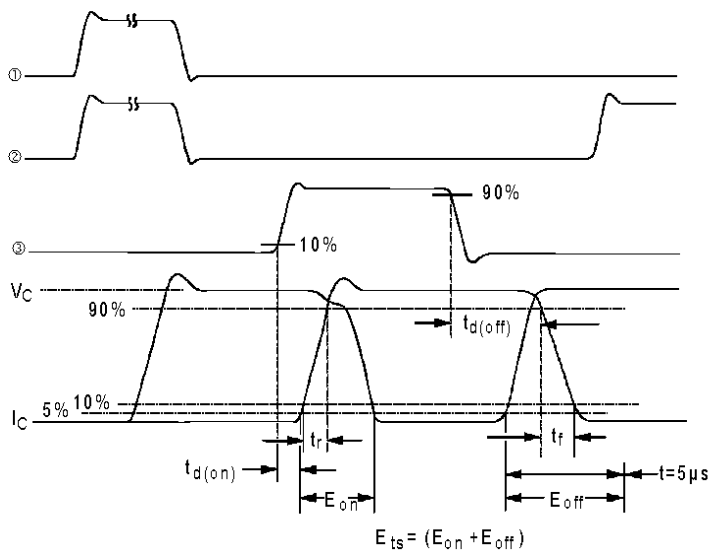


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — Super-247

[illegible]

NOTES:	LEAD ASSIGNMENTS	
	<u>MOSFET</u>	<u>IGBT</u>
1. DIMENSIONS & TOLERANCING PER ASME Y14.5M-1994	1 - GATE	1 - GATE
2. CONTROLLING DIMENSION: MILLIMETER	2 - DRAIN	2 - COLLECTOR
3. DIMENSIONS ARE SHOWN IN MILLIMETRES [INCHES]	3 - SOURCE	3 - EMITTER
	4 - DRAIN	4 - COLLECTOR

Diagram illustrating the marking on the IRFP537N50A MOSFET package:

- PART NUMBER:** IRFP537N50A
- INTERNATIONAL RECTIFIER LOGO:** IRL
- DATE CODE:** 719C
- ASSEMBLY LOT CODE:** 17
- TOP:** Indicated by an arrow pointing to the top of the package.

Additional information provided:

- YEAR 7 = 1997
- WEEK 19
- LINE C

Note: "P" in assembly line position indicates "Lead-Free"

Data and specifications subject to change without notice.

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