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Product Standards

Part No.	AN32183A
Package Code No.	SSOP024-P-0300F

Established : 2011-10-07
Revised : ####-##-##

Contents

AN32183A

81 Dots Matrix LED driver IC

■ Overview

AN32183A is a 81 dots Matrix LED driver. It can drive up to 27 RGB LEDs.

■ Feature

- LED 9 × 9 matrix driver (Total LED that can be driven = 81)
- LED Selectable Maximum Current
- LED Music Synchronizing function
- I²C interface (Standard Mode, Fast Mode and Fast Mode Plus) (4 Slave address selectable)

■ Applications

- LED driver IC

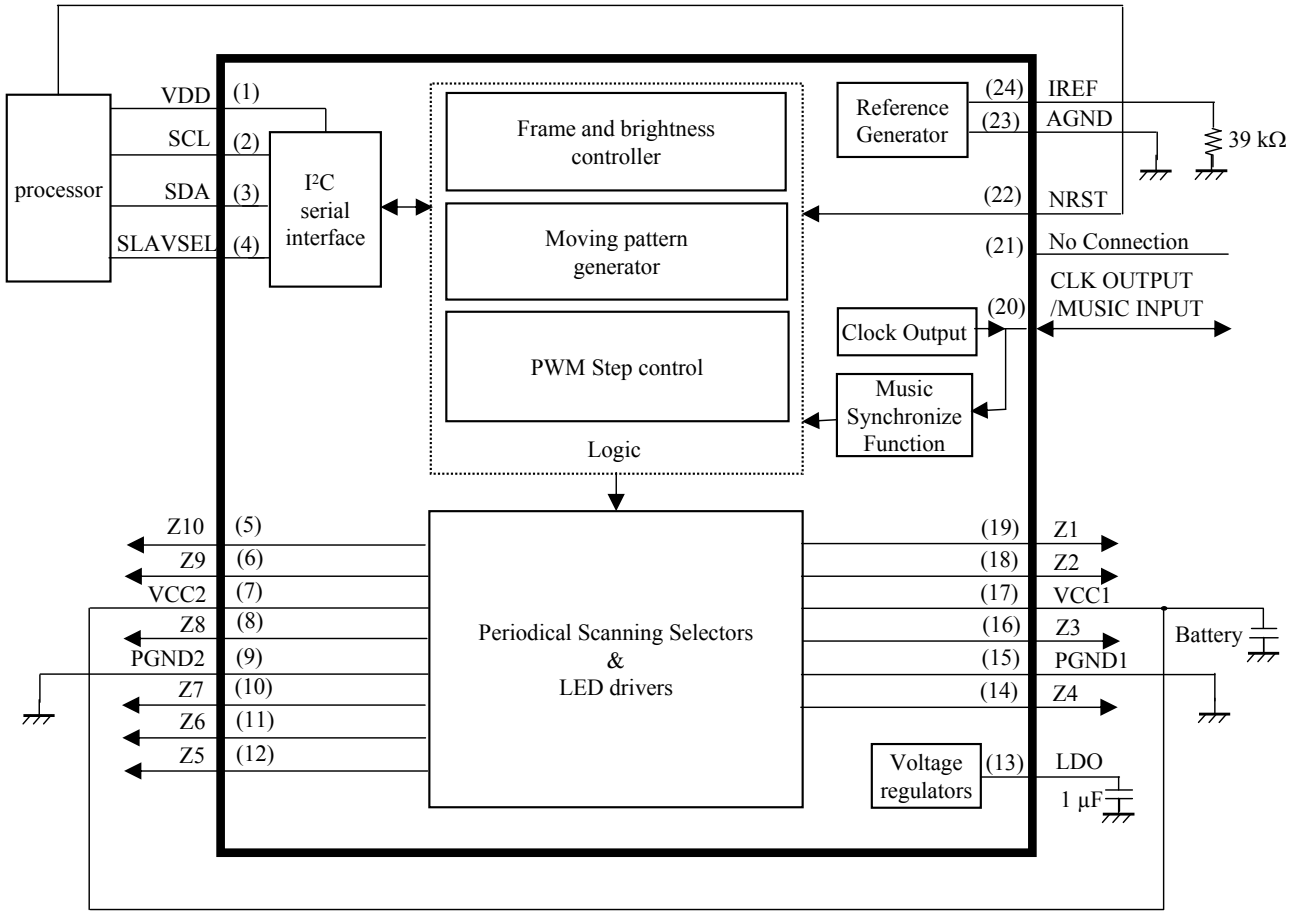
■ Package

- 24 pin Shrink Small Outline Package (SSOP24 Type)

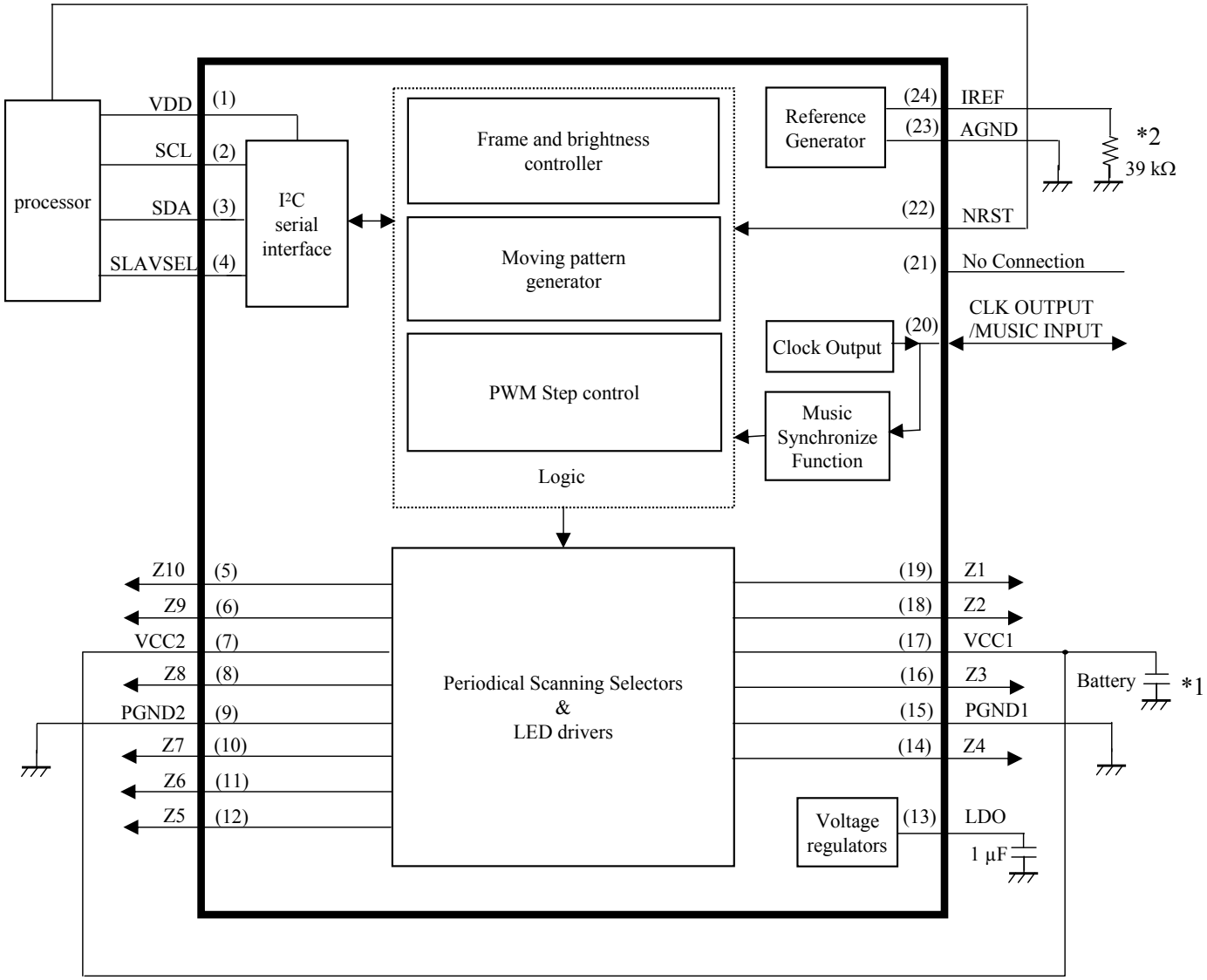
■ Type

- Bi-CMOS IC

■ System image



■ Application Circuit Example (Block Diagram)



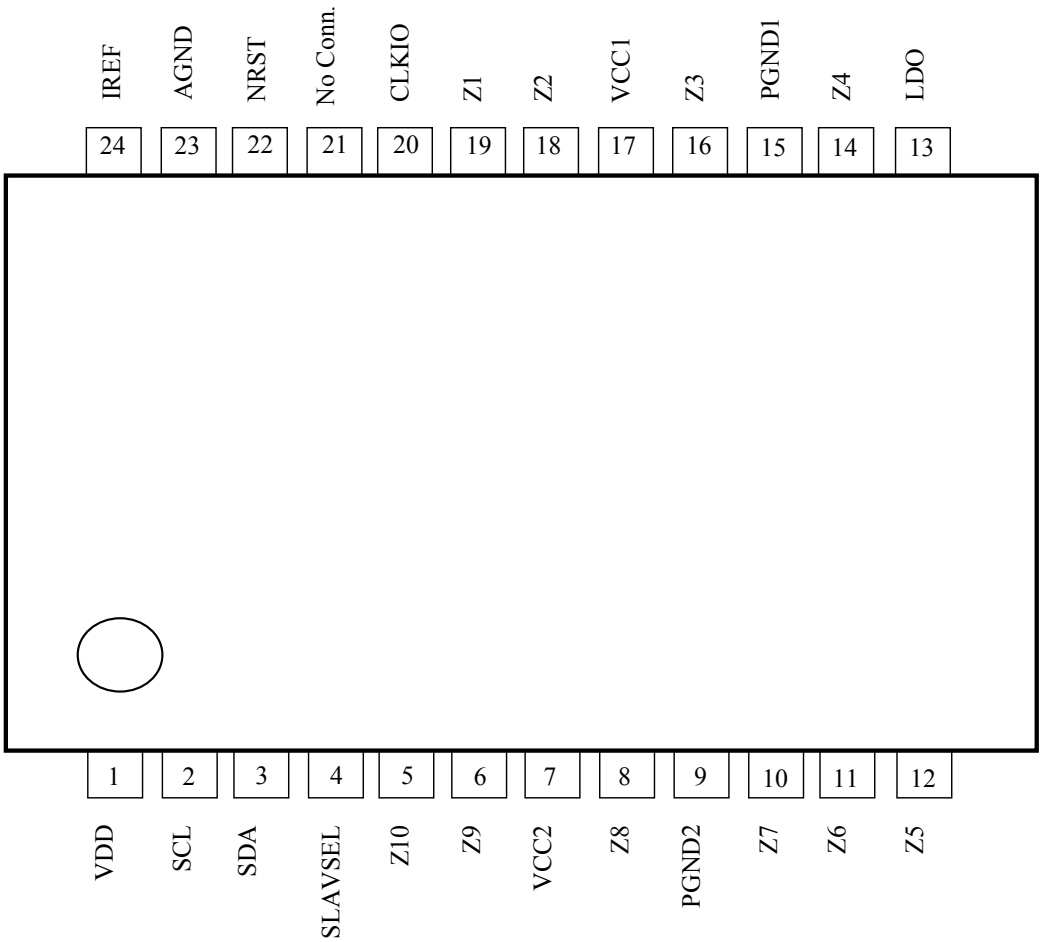
Notes) • This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

• This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

*1 : VCC capacitor is for noise cancellation. Please select an appropriate value according to PCB pattern etc.

*2 : To ensure the accuracy of the constant current of each LED, it is recommended to use Panasonic Resistor ERJ2RHD393X (±0.5% tolerance). To ensure the accuracy of the constant current of each LED, place the external resistor as close as possible to IC and parasitic capacitor of not more than 20 pF at IREF pin.

■ Pin Descriptions



■ Pin Descriptions (continued)

SSOP24 Pin No.	Pin name	Type	Description	Pin processing at unused
1	VDD	Power supply	Power supply for I^2C interface	(Required pin)
2	SCL	Input	Clock input pin for I^2C interface	(Required pin)
3	SDA	Input/Output	Data input / output pin for I^2C interface	(Required pin)
4	SLAVSEL	Input	Slave address selection pin for I^2C interface	GND or VCC or SCL or SDA
5	Z10	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
6	Z9	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
7	VCC2	Power supply	Power supply for matrix driver, Internal reference circuit	Battery or External power supply
8	Z8	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
9	PGND2	Ground	Power Ground pin	(Required pin)
10	Z7	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
11	Z6	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
12	Z5	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
13	LDO	Output	LDO output pin	(Required pin)
14	Z4	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
15	PGND1	Ground	Power Ground pin	(Required pin)
16	Z3	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
17	VCC1	Power supply	Power supply for matrix driver, Internal reference circuit	Battery or External power supply
18	Z2	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
19	Z1	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
20	CLKIO	Input/Output	Reference clock input output / Music Input pin	Open
21	—	—	N.C	—
22	NRST	Input	Reset input pin	(Required pin)
23	AGND	Ground	Ground pin	(Required pin)
24	IREF	Output	Resistor connection pin for constant current setup	(Required pin)

■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

A* No.	Parameter	Symbol	Range	Units	Note
1	Power Supply Voltage	VCC	6.0	V	*1
		VDD	6.0	V	*1
2	Power Supply Current	I_{CC}	—	A	—
3	Power Dissipation	P_D	156	mW	*2
4	Operating Ambient Temperature	T_{opr}	–30 to +85	°C	*3
5	Storage Temperature	T_{stg}	–55 to +125	°C	*3

Notes) * : A is a number for internal management of this page of Panasonic.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Power Supply Voltage Range	VCC	3.1 to 5.5	V	*1
	VDD	1.7 to 5.5	V	*1

Note) Maximum Operating Supply Voltages for VCC and VDD (VCC_{max} and VDD_{max}) are 5.5 V.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Allowable Voltage Range

Notes) • Allowable current and voltage ranges are limit ranges which do not result in damages to this IC, and IC operation is not guaranteed within these limit ranges.
• Voltage values, unless otherwise specified, are with respect to GND.
GND is voltage for AGND, PGND1, PGND2. AGND = PGND1 = PGND2
• Do not apply external currents or voltages to any pin not specifically mentioned.

SSOP Pin No.	Pin name	Absolute maximum Voltage	Unit	Remark
4	SLAVSEL	–0.3 to 6.0	V	—
20	CLKIO	–0.3 to 6.0	V	*1
22	NRST	–0.5 to 6.0	V	—
2	SCL	–0.5 to 6.0	V	—
3	SDA	–0.3 to 6.0	V	*1

Note) *1: This value is absolute maximum voltage when these terminals are used as input.
External Voltage and current are prohibited when these terminals are used as output.

■ Electrical Characteristics at VCC = 3.6 V, VDD = 1.85 V

Notes) Operating Ambient Temperature, T_a = 25°C±2°C, unless specifically mentioned

B* No.	Items	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Circuit Current									
1	Circuit Current (1) OFF Mode	ICC1	1	NRST = 0V ICC1 = IP1 + IP7 + IP17	—	0	1	µA	—
2	Circuit Current (2) OFF Mode	ICC2	1	NRST = High ICC1 = IP1 + IP7 + IP17	—	250	500	µA	—
Internal Oscillator									
3	Oscillation Frequency	FDC1	1	VCC = 3.6 V	1.92	2.40	2.88	MHz	—
SCAN Switch									
4	Switch On Resistance	RSCAN	1	VCC = 3.6 V IP5, 6, 8, 10, 11, 12, 14, 16, 18, 19 = –20 mA	—	1.5	3	Ω	—
Constant Voltage Source (LDO)									
5	Output voltage (1)	VL1	1	IP13 = –10 µA VL1 = VP13	2.75	2.85	2.95	V	—
6	Output voltage (2)	VL2	1	IP13 = –15 mA VL2 = VP13	2.75	2.85	2.95	V	—
CLKIO									
7	High Level Input Voltage Range	VIH1	1	High Level Acknowledged Voltage (At External CLK Input Mode)	0.7 × VDD	—	VDD + 0.3	V	—
8	Low Level Input Voltage Range	VIL1	1	Low Level Acknowledged Voltage (At External CLK Input Mode)	–0.3	—	0.3 × VDD	V	—
9	High Level Output Voltage	VOH1	1	IP20_2 = –1 mA (At Internal CLK Output Mode)	0.8 × VDD	—	VDD + 0.3	V	—
10	Low Level Output Voltage	VOL1	1	IP20_2 = +1 mA (At Internal CLK Output Mode)	–0.3	—	0.2 × VDD	V	—
11	High Level input Current	IIH1	1	VCC = 5.5 V VP20 = 5.5 V IIH1 = IP20	–1	0	1	µA	—
12	Low Level input Current	IIL1	1	VCC = 5.5 V VP20 = 0 V IIL1 = IP20	–1	0	1	µA	—

Notes) Please refer to the Test Circuit diagram on page 15 for symbols VP××, IP××.
* : Number B from page 9 to page 13 is for internal management of Panasonic.

■ Electrical Characteristics (continued) at VCC = 3.6 V, VDD = 1.85 V

Notes) Operating Ambient Temperature, T_a = 25°C±2°C, unless specifically mentioned

B No.	Item	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Constant Current Source (Matrix LED)									
13	Output Current (1)	IMX1	1	LED Current Setting = 20 mA IMAX = [011], BRTXX = [1010] VP5, 6, 8, 10, 11, 12, 14, 16, 18, 19 = 1 V IMX1 = IP5, 6, 8, 10, 11, 12, 14, 16, 18, 19	19	20	21	mA	*1
14	DAC Current Step	DACSTEP	1	DAC Constant Current Mode LED Current Setting = 20 mA IMAX = [011], BRTXX = [1010] VP5, 6, 8, 10, 11, 12, 14, 16, 18, 19 = 1V IDAC1 = IP5, 6, 8, 10, 11, 12, 14, 16, 18, 19 LED Current Setting = 22 mA IMAX = [011], BRTXX = [1011] VP5, 6, 8, 10, 11, 12, 14, 16, 18, 19 = 1 V IDAC2 = IP5, 6, 8, 10, 11, 12, 14, 16, 18, 19 DACSTEP = IDAC2 – IDAC1	0	2	4	mA	—
15	OFF Mode Leak Current1	IMXOFF1	1	VCC = 5.5 V, VDD = 5.5 V OFF Mode VP5, 6, 8, 10, 11, 12, 14, 16, 18, 19 = 5.5V IMXOFF1 = IP5, 6, 8, 10, 11, 12, 14, 16, 18, 19	–1	—	1	µA	—
16	OFF Mode Leak Current2	IMXOFF2	1	VCC = 5.5 V, VDD = 5.5 V OFF Mode VP5, 6, 8, 10, 11, 12, 14, 16, 18, 19 = 0 V IMXOFF2 = IP5, 6, 8, 10, 11, 12, 14, 16, 18, 19	–1	—	1	µA	—
17	Channel Difference	IMXCH	1	LED Current Setting = 20 mA IMAX = [011], BRTXX = [1010] Difference of Z1 to 10 current from the average current value	–5	—	5	%	—
Voltage at which LED driver can keep constant current value									
18	LED Driver Voltage	VLD2	1	LED Current Setting = 20 mA IMAX = [011], BRTXX = [1010] Voltage at which LED Current change within ±5% compared with LED Current of pin voltage = 0.5 V.	0.4	—	—	V	—

Note) *1 : This is allowable value when recommended parts (ERJ2RHD393X) are used for the terminal IREF.

■ Electrical Characteristics (continued) at VCC = 3.6 V, VDD = 1.85 V

Notes) Operating Ambient Temperature, T_a = 25°C±2°C, unless specifically mentioned

B No.	Item	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
SLAVSEL									
19	High Level Input Voltage Range	VIH2	1	High Level Acknowledged Voltage	0.7 × VDD	—	VDD + 0.3	V	—
20	Low Level Input Voltage Range	VIL2	1	Low Level Acknowledged Voltage	–0.3	—	0.3 × VDD	V	—
21	High Level Input Current	IIH2	1	VCC = 5.5 V VP4 = 3.6 V, IIH2 = IP4	–1	0	1	µA	—
22	Low Level Input Current	IIL2	1	VCC = 5.5 V VP4= 0 V, IIL2 = IP4	–1	0	1	µA	—
NRST									
23	High Level Input Voltage Range	VIH3	1	High Level Acknowledged Voltage	1.5	—	VCC + 0.3	V	—
24	Low Level Input Voltage Range	VIL3	1	Low Level Acknowledged Voltage	–0.3	—	0.6	V	—
25	High Level Input Current	IIH3	1	VCC = 5.5 V VP22 = 3.6 V, IIH3 = IP22	–1	0	1	µA	—
26	Low Level Input Current	IIL3	1	VCC = 5.5 V VP22 = 0 V, IIL3 = IP22	–1	0	1	µA	—
I²C bus (Internal I/O stage characteristics)									
27	Low-level input voltage	V_{IL}	1	Voltage which recognized that SDA and SCL are Low-level	–0.5	—	0.3 × VDD	V	*2
28	High-level input voltage	V_{IH}	1	Voltage which recognized that SDA and SCL are High-level	0.7 × VDD	—	VDD_{max} + 0.5	V	*2
29	Low-level output voltage 1	V_{OL1}	1	VDD > 2 V IP3_2(sink current) = 3 mA	0	—	0.4	V	—
30	Low-level output voltage 2	V_{OL2}	1	VDD < 2 V IP3_2(sink current) = 3 mA	0	—	0.2 × VDD	V	—
31	Low-level output current	I_{OL}	1	V_{OL} = 0.4 V	20	—	—	mA	—
32	Input current each I/O pin	I_i	1	VCC = 5.5 V, VDD = 5.5 V VP2, 3 = 0.1VDD_{max} to 0.9VDD_{max}	–10	0	10	µA	—
33	SCL clock frequency	f_{SCL}	1	—	0	—	1 000	kHz	—

Note) VDD_{max} refers to the maximum operating supply voltage of VDD.

*2 : The input threshold voltage of I²C bus (Vth) is linked to VDD (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not VDD, the threshold voltage (Vth) is fixed to ((VDD / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified. In this case, pay attention to Low-level (max.) value (V_{ILmax}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (VDD).

■ Electrical Characteristics (Reference values for design) at VCC = 3.6 V, VDD = 1.85 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test Circuit	Conditions	Reference values			Unit	Note
					Min	Typ	Max		
TSD (Thermal shutdown protection circuit)									
34	Detection temperature	Tdet	1	Temperature which Constant current circuit, and Matrix SW turn off.	110	150	180	°C	*3
Constant Voltage Source (LDO)									
35	Ripple rejection ratio (1)	PSL11	1	VCC = 3.6 V + 0.3 V[p-p] f = 1 kHz IP13 = –15 mA PSL11 = 20log(acVP13 / 0.2)	—	–50	–25	dB	—
36	Ripple rejection ratio (2)	PSL12	1	VCC = 3.6 V + 0.3 V[p-p] f = 10 kHz IP13 = –15 mA PSL12 = 20log(acVP13 / 0.2)	—	–40	–15	dB	—
37	Short-circuit protection current	IPT1	1	VP13 = 0 V IPT1 = IP13	20	40	80	mA	—
I^2C bus (Internal I/O stage characteristics) (Continued)									
38	Hysteresis of Schmitt trigger input 1	V_{hys1}	1	VDD > 2 V, Hysteresis of SDA, SCL	0.05 × VDD	—	—	V	*4
39	Hysteresis of Schmitt trigger input 2	V_{hys2}	1	VDD < 2 V, Hysteresis of SDA, SCL	0.1 × VDD	—	—	V	*4
40	Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	1	Bus capacitance: 10pF to 550pF $I_P \leq 20$ mA (V_{OLmax} = 0.4 V) I_P : Max. sink current	—	—	120	ns	*4
41	Pulse width of spikes which must be suppressed by the input filter	t_{SP}	1	—	0	—	50	ns	*4
42	Capacitance for each I/O pin	C_i	1	—	—	—	10	pF	*4

Notes) *3 : Constant current circuit, and Matrix SW turn off and IC reset when TSD operates.
*4 : The timing of Fast-mode Plus devices in I^2C-bus is specified as above. All values referred to V_{IHmin} and V_{ILmax} level.

■ Electrical Characteristics (Reference values for design) at VCC = 3.6 V, VDD = 1.85 V

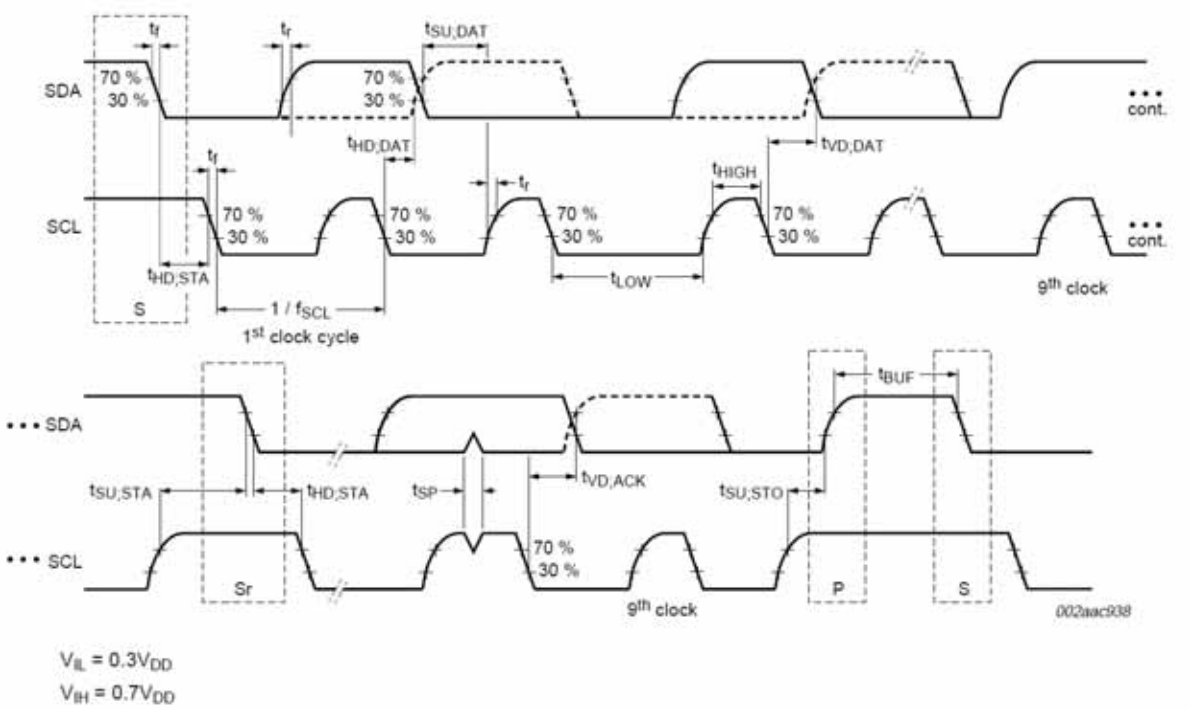
Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test Circuit	Conditions	Reference values			Unit	Note
					Min	Typ	Max		
I²C bus (Bus line specifications) (Continue)									
43	Hold time (repeated) START condition	$t_{HD:STA}$	1	The first clock pulse is generated after $t_{HD:STA.}$	0.26	—	—	µs	*4
44	Low period of the SCL clock	t_{LOW}	1	—	0.5	—	—	µs	*4
45	High period of the SCL clock	t_{HIGH}	1	—	0.26	—	—	µs	*4
46	Set-up time for a repeat START condition	$t_{SU:STA}$	1	—	0.26	—	—	µs	*4
47	Data hold time	$t_{HD:DAT}$	1	—	0	—	—	µs	*4
48	Data set-up time	$t_{SU:DAT}$	1	—	50	—	—	ns	*4
49	Rise time of both SDA and SCL signals	t_r	1	—	—	—	120	ns	*4
50	Fall time of both SDA and SCL signals	t_f	1	—	—	—	120	ns	*4
51	Set-up time of STOP condition	$t_{SU:STO}$	1	—	0.26	—	—	µs	*4
52	Bus free time between STOP and START condition	t_{BUF}	1	—	0.5	—	—	µs	*4
53	Capacitive load for each bus line	C_b	1	—	—	—	550	pF	*4
54	Data valid time	$t_{VD:DAT}$	1	—	—	—	0.45	µs	*4
55	Data valid acknowledge	$t_{VD:ACK}$	1	—	—	—	0.45	µs	*4
56	Noise margin at the Low-level for each connected device	V_{nL}	1	—	0.1 × VDD	—	—	V	*4
57	Noise margin at the High-level for each connected device	V_{nH}	1	—	0.2 × VDD	—	—	V	*4

Note) *4 : The timing of Fast-mode Plus devices in I²C-bus is specified as above. All values referred to V_{IHmin} and V_{ILmax} level.

■ Electrical Characteristics (Reference values for design) at VCC = 3.6 V, VDD = 1.85 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

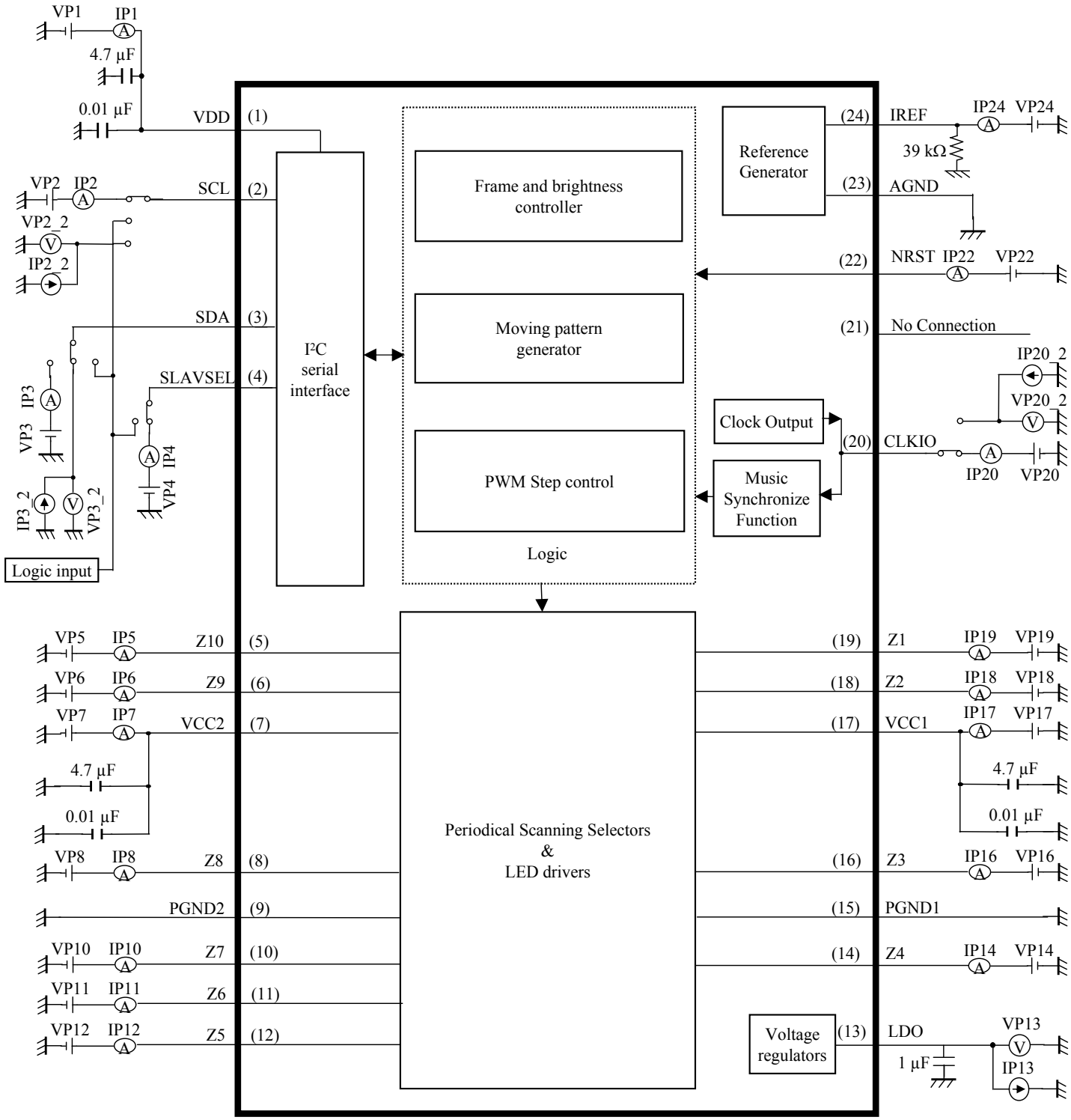


V_{IL} = 0.3V_{DD}
V_{IH} = 0.7V_{DD}

S : START condition
Sr : Repeat START condition
P : STOP condition

■ Test Circuit Diagram

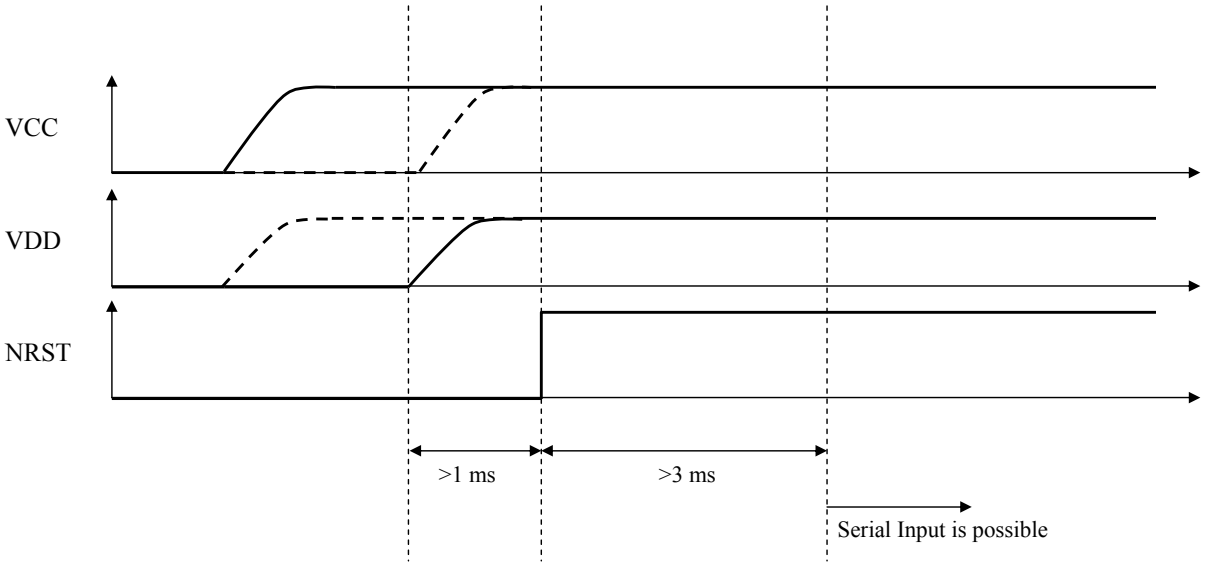
- Test Circuit 1



■ Technical Data

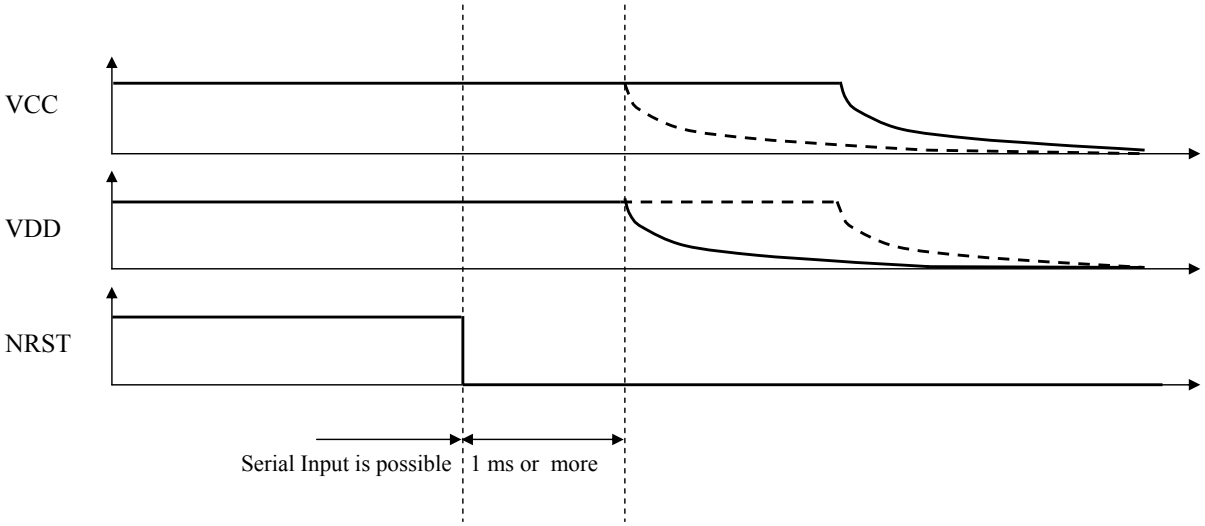
1. Power Supply Sequence

- Power ON



Note) For the Startup Timing of VCC and VDD, it is possible to be changed.

- Power OFF



Note) For the Shut down Timing of VCC and VDD, it is possible to be changed.

■ Technical Data (continued)

2. Register Map

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
01h	RST	00h	W	--	--	--	--	--	--	RAMRST	SRST
02h	POWERCNT	00h	R/W		--	--	--	--	--	--	OSCEN
03h	reserved	--	--	--	--	--	--	--	--	--	--
04h	OPTION	00h	R/W	--	--	--	--	ZPDEN	MLDACT	CLKOUT	EXTCLK
05h	MTXON	1Eh	R/W	--	--	--	IMAX Reserved	IMAX[2:0]			MTXON
06h	PWMEN1	00h	R/W	PWMA8	PWMA7	PWMA6	PWMA5	PWMA4	PWMA3	PWMA2	PWMA1
07h	PWMEN2	00h	R/W	PWMB7	PWMB6	PWMB5	PWMB4	PWMB3	PWMB2	PWMB1	PWMA9
08h	PWMEN3	00h	R/W	PWMC6	PWMC5	PWMC4	PWMC3	PWMC2	PWMC1	PWMB9	PWMB8
09h	PWMEN4	00h	R/W	PWMD5	PWMD4	PWMD3	PWMD2	PWMD1	PWMC9	PWMC8	PWMC7
0Ah	PWMEN5	00h	R/W	PWME4	PWME3	PWME2	PWME1	PWMD9	PWMD8	PWMD7	PWMD6
0Bh	PWMEN6	00h	R/W	PWMF3	PWMF2	PWMF1	PWME9	PWME8	PWME7	PWME6	PWME5
0Ch	PWMEN7	00h	R/W	PWMG2	PWMG1	PWMF9	PWMF8	PWMF7	PWMF6	PWMF5	PWMF4
0Dh	PWMEN8	00h	R/W	PWMH1	PWMG9	PWMG8	PWMG7	PWMG6	PWMG5	PWMG4	PWMG3
0Eh	PWMEN9	00h	R/W	PWMH9	PWMH8	PWMH7	PWMH6	PWMH5	PWMH4	PWMH3	PWMH2
0Fh	PWMEN10	00h	R/W	PWMI8	PWMI7	PWMI6	PWMI5	PWMI4	PWMI3	PWMI2	PWMI1
10h	PWMENI11	00h	R/W	--	--	--	--	--	--	--	PWMI9
11h	MLDEN1	00h	R/W	MLDA8	MLDA7	MLDA6	MLDA5	MLDA4	MLDA3	MLDA2	MLDA1
12h	MLDEN2	00h	R/W	MLDB7	MLDB6	MLDB5	MLDB4	MLDB3	MLDB2	MLDB1	MLDA9
13h	MLDEN3	00h	R/W	MLDC6	MLDC5	MLDC4	MLDC3	MLDC2	MLDC1	MLDB9	MLDB8
14h	MLDEN4	00h	R/W	MLDD5	MLDD4	MLDD3	MLDD2	MLDD1	MLDC9	MLDC8	MLDC7
15h	MLDEN5	00h	R/W	MLDE4	MLDE3	MLDE2	MLDE1	MLDD9	MLDD8	MLDD7	MLDD6
16h	MLDEN6	00h	R/W	MLDF3	MLDF2	MLDF1	MLDE9	MLDE8	MLDE7	MLDE6	MLDE5
17h	MLDEN7	00h	R/W	MLDG2	MLDG1	MLDF9	MLDF8	MLDF7	MLDF6	MLDF5	MLDF4
18h	MLDEN8	00h	R/W	MLDH1	MLDG9	MLDG8	MLDG7	MLDG6	MLDG5	MLDG4	MLDG3
19h	MLDEN9	00h	R/W	MLDH9	MLDH8	MLDH7	MLDH6	MLDH5	MLDH4	MLDH3	MLDH2
1Ah	MLDEN10	00h	R/W	MLDI8	MLDI7	MLDI6	MLDI5	MLDI4	MLDI3	MLDI2	MLDI1
1Bh	MLDENI11	00h	R/W	--	--	--	--	--	--	--	MLDI9
2Ah	MLDMODE1	00h	R/W	--	--	--	--	GRP9_9	GRP9_8	GRP9_2	GRP9_1
2Bh	THOLD	00h	R/W	THOLD[7:0]							

Note) "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used. For data bits indicated by "--" in other registers except from "reversed" registers, will return "zero" value if these bits are read. Writing to these bits will be ignored.
IMAX Reserved will give default value [1].

■ Technical Data (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
2Ch	CONSTX6_1	00h	R/W	--	--	X6	X5	X4	X3	X2	X1
2Dh	CONSTX10_7	00h	R/W	--	--	--	--	X10	X9	X8	X7
2Eh	CONSTY6_1	00h	R/W	--	--	Y6	Y5	Y4	Y3	Y2	Y1
2Fh	CONSTY9_7	00h	R/W	--	--	--	--	--	Y9	Y8	Y7
30h	MASKY6_1	00h	R/W	--	--	Y6MSK	Y5MSK	Y4MSK	Y3MSK	Y2MSK	Y1MSK
31h	MASKY9_7	00h	R/W	--	--	--	--	--	Y9MSK	Y8MSK	Y7MSK
32h	SLPTIME	00h	R/W	--	--	--	FADTIM	SLOPEEXTL[1:0]		SLOPEEXTH[1:0]	
33h	MLDCOM	03h	R/W	--	--	--	--	--	MLDCOM[2:0]		
34h	reserved	--	--	--	--	--	--	--	--	--	--
35h	reserved	--	--	--	--	--	--	--	--	--	--
36h	SCANSET	08h	R/W	--	--	--	--	SCANSET[3:0]			
40h	DTA1	00h	R/W	DTA1[7:0]							
41h	DTA2	00h	R/W	DTA2[7:0]							
42h	DTA3	00h	R/W	DTA3[7:0]							
43h	DTA4	00h	R/W	DTA4[7:0]							
44h	DTA5	00h	R/W	DTA5[7:0]							
45h	DTA6	00h	R/W	DTA6[7:0]							
46h	DTA7	00h	R/W	DTA7[7:0]							
47h	DTA8	00h	R/W	DTA8[7:0]							
48h	DTA9	00h	R/W	DTA9[7:0]							
49h	DTB1	00h	R/W	DTB1[7:0]							
4Ah	DTB2	00h	R/W	DTB2[7:0]							
4Bh	DTB3	00h	R/W	DTB3[7:0]							
4Ch	DTB4	00h	R/W	DTB4[7:0]							
4Dh	DTB5	00h	R/W	DTB5[7:0]							
4Eh	DTB6	00h	R/W	DTB6[7:0]							
4Fh	DTB7	00h	R/W	DTB7[7:0]							
50h	DTB8	00h	R/W	DTB8[7:0]							
51h	DTB9	00h	R/W	DTB9[7:0]							

Note) "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used. For data bits indicated by "--" in other registers except from "reversed" registers, will return "zero" value if these bits are read. Writing to these bits will be ignored.

■ Technical Data (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
52h	DTC1	00h	R/W	DTC1[7:0]							
53h	DTC2	00h	R/W	DTC2[7:0]							
54h	DTC3	00h	R/W	DTC3[7:0]							
55h	DTC4	00h	R/W	DTC4[7:0]							
56h	DTC5	00h	R/W	DTC5[7:0]							
57h	DTC6	00h	R/W	DTC6[7:0]							
58h	DTC7	00h	R/W	DTC7[7:0]							
59h	DTC8	00h	R/W	DTC8[7:0]							
5Ah	DTC9	00h	R/W	DTC9[7:0]							
5Bh	DTD1	00h	R/W	DTD1[7:0]							
5Ch	DTD2	00h	R/W	DTD2[7:0]							
5Dh	DTD3	00h	R/W	DTD3[7:0]							
5Eh	DTD4	00h	R/W	DTD4[7:0]							
5Fh	DTD5	00h	R/W	DTD5[7:0]							
60h	DTD6	00h	R/W	DTD6[7:0]							
61h	DTD7	00h	R/W	DTD7[7:0]							
62h	DTD8	00h	R/W	DTD8[7:0]							
63h	DTD9	00h	R/W	DTD9[7:0]							
64h	DTE1	00h	R/W	DTE1[7:0]							
65h	DTE2	00h	R/W	DTE2[7:0]							
66h	DTE3	00h	R/W	DTE3[7:0]							
67h	DTE4	00h	R/W	DTE4[7:0]							
68h	DTE5	00h	R/W	DTE5[7:0]							
69h	DTE6	00h	R/W	DTE6[7:0]							
6Ah	DTE7	00h	R/W	DTE7[7:0]							
6Bh	DTE8	00h	R/W	DTE8[7:0]							
6Ch	DTE9	00h	R/W	DTE9[7:0]							
6Dh	DTF1	00h	R/W	DTF1[7:0]							
6Eh	DTF2	00h	R/W	DTF2[7:0]							

■ Technical Data (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
6Fh	DTF3	00h	R/W	DTF3[7:0]							
70h	DTF4	00h	R/W	DTF4[7:0]							
71h	DTF5	00h	R/W	DTF5[7:0]							
72h	DTF6	00h	R/W	DTF6[7:0]							
73h	DTF7	00h	R/W	DTF7[7:0]							
74h	DTF8	00h	R/W	DTF8[7:0]							
75h	DTF9	00h	R/W	DTF9[7:0]							
76h	DTG1	00h	R/W	DTG1[7:0]							
77h	DTG2	00h	R/W	DTG2[7:0]							
78h	DTG3	00h	R/W	DTG3[7:0]							
79h	DTG4	00h	R/W	DTG4[7:0]							
7Ah	DTG5	00h	R/W	DTG5[7:0]							
7Bh	DTG6	00h	R/W	DTG6[7:0]							
7Ch	DTG7	00h	R/W	DTG7[7:0]							
7Dh	DTG8	00h	R/W	DTG8[7:0]							
7Eh	DTG9	00h	R/W	DTG9[7:0]							
7Fh	DTH1	00h	R/W	DTH1[7:0]							
80h	DTH2	00h	R/W	DTH2[7:0]							
81h	DTH3	00h	R/W	DTH3[7:0]							
82h	DTH4	00h	R/W	DTH4[7:0]							
83h	DTH5	00h	R/W	DTH5[7:0]							
84h	DTH6	00h	R/W	DTH6[7:0]							
85h	DTH7	00h	R/W	DTH7[7:0]							
86h	DTH8	00h	R/W	DTH8[7:0]							
87h	DTH9	00h	R/W	DTH9[7:0]							
88h	DTI1	00h	R/W	DTI1[7:0]							
89h	DTI2	00h	R/W	DTI2[7:0]							
8Ah	DTI3	00h	R/W	DTI3[7:0]							
8Bh	DTI4	00h	R/W	DTI4[7:0]							

■ Technical Data (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
8Ch	DTI5	00h	R/W	DTI5[7:0]							
8Dh	DTI6	00h	R/W	DTI6[7:0]							
8Eh	DTI7	00h	R/W	DTI7[7:0]							
8Fh	DTI8	00h	R/W	DTI8[7:0]							
90h	DTI9	00h	R/W	DTI9[7:0]							
91h	A1	00h	R/W	BRTA1[3:0]				--	SDTA1[2:0]		
92h	A2	00h	R/W	BRTA2[3:0]				--	SDTA2[2:0]		
93h	A3	00h	R/W	BRTA3[3:0]				--	SDTA3[2:0]		
94h	A4	00h	R/W	BRTA4[3:0]				--	SDTA4[2:0]		
95h	A5	00h	R/W	BRTA5[3:0]				--	SDTA5[2:0]		
96h	A6	00h	R/W	BRTA6[3:0]				--	SDTA6[2:0]		
97h	A7	00h	R/W	BRTA7[3:0]				--	SDTA7[2:0]		
98h	A8	00h	R/W	BRTA8[3:0]				--	SDTA8[2:0]		
99h	A9	00h	R/W	BRTA9[3:0]				--	SDTA9[2:0]		
9Ah	B1	00h	R/W	BRTB1[3:0]				--	SDTB1[2:0]		
9Bh	B2	00h	R/W	BRTB2[3:0]				--	SDTB2[2:0]		
9Ch	B3	00h	R/W	BRTB3[3:0]				--	SDTB3[2:0]		
9Dh	B4	00h	R/W	BRTB4[3:0]				--	SDTB4[2:0]		
9Eh	B5	00h	R/W	BRTB5[3:0]				--	SDTB5[2:0]		
9Fh	B6	00h	R/W	BRTB6[3:0]				--	SDTB6[2:0]		
A0h	B7	00h	R/W	BRTB7[3:0]				--	SDTB7[2:0]		
A1h	B8	00h	R/W	BRTB8[3:0]				--	SDTB8[2:0]		
A2h	B9	00h	R/W	BRTB9[3:0]				--	SDTB9[2:0]		
A3h	C1	00h	R/W	BRTC1[3:0]				--	SDTC1[2:0]		
A4h	C2	00h	R/W	BRTC2[3:0]				--	SDTC2[2:0]		
A5h	C3	00h	R/W	BRTC3[3:0]				--	SDTC3[2:0]		
A6h	C4	00h	R/W	BRTC4[3:0]				--	SDTC4[2:0]		
A7h	C5	00h	R/W	BRTC5[3:0]				--	SDTC5[2:0]		
A8h	C6	00h	R/W	BRTC6[3:0]				--	SDTC6[2:0]		

Note) Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read. Writing to these bits will be ignored.

■ Technical Data (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
A9h	C7	00h	R/W	BRTC7[3:0]				--	SDTC7[2:0]		
AAh	C8	00h	R/W	BRTC8[3:0]				--	SDTC8[2:0]		
ABh	C9	00h	R/W	BRTC9[3:0]				--	SDTC9[2:0]		
ACh	D1	00h	R/W	BRTD1[3:0]				--	SDTD1[2:0]		
ADh	D2	00h	R/W	BRTD2[3:0]				--	SDTD2[2:0]		
AEh	D3	00h	R/W	BRTD3[3:0]				--	SDTD3[2:0]		
AFh	D4	00h	R/W	BRTD4[3:0]				--	SDTD4[2:0]		
B0h	D5	00h	R/W	BRTD5[3:0]				--	SDTD5[2:0]		
B1h	D6	00h	R/W	BRTD6[3:0]				--	SDTD6[2:0]		
B2h	D7	00h	R/W	BRTD7[3:0]				--	SDTD7[2:0]		
B3h	D8	00h	R/W	BRTD8[3:0]				--	SDTD8[2:0]		
B4h	D9	00h	R/W	BRTD9[3:0]				--	SDTD9[2:0]		
B5h	E1	00h	R/W	BRTE1[3:0]				--	SDTE1[2:0]		
B6h	E2	00h	R/W	BRTE2[3:0]				--	SDTE2[2:0]		
B7h	E3	00h	R/W	BRTE3[3:0]				--	SDTE3[2:0]		
B8h	E4	00h	R/W	BRTE4[3:0]				--	SDTE4[2:0]		
B9h	E5	00h	R/W	BRTE5[3:0]				--	SDTE5[2:0]		
BAh	E6	00h	R/W	BRTE6[3:0]				--	SDTE6[2:0]		
BBh	E7	00h	R/W	BRTE7[3:0]				--	SDTE7[2:0]		
BCh	E8	00h	R/W	BRTE8[3:0]				--	SDTE8[2:0]		
BDh	E9	00h	R/W	BRTE9[3:0]				--	SDTE9[2:0]		
BEh	F1	00h	R/W	BRTF1[3:0]				--	SDTF1[2:0]		
BFh	F2	00h	R/W	BRTF2[3:0]				--	SDTF2[2:0]		
C0h	F3	00h	R/W	BRTF3[3:0]				--	SDTF3[2:0]		
C1h	F4	00h	R/W	BRTF4[3:0]				--	SDTF4[2:0]		
C2h	F5	00h	R/W	BRTF5[3:0]				--	SDTF5[2:0]		
C3h	F6	00h	R/W	BRTF6[3:0]				--	SDTF6[2:0]		
C4h	F7	00h	R/W	BRTF7[3:0]				--	SDTF7[2:0]		
C5h	F8	00h	R/W	BRTF8[3:0]				--	SDTF8[2:0]		

Note) Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read. Writing to these bits will be ignored.

■ Technical Data (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
C6h	F9	00h	R/W	BRTF9[3:0]				--	SDTF9[2:0]		
C7h	G1	00h	R/W	BRTG1[3:0]				--	SDTG1[2:0]		
C8h	G2	00h	R/W	BRTG2[3:0]				--	SDTG2[2:0]		
C9h	G3	00h	R/W	BRTG3[3:0]				--	SDTG3[2:0]		
CAh	G4	00h	R/W	BRTG4[3:0]				--	SDTG4[2:0]		
CBh	G5	00h	R/W	BRTG5[3:0]				--	SDTG5[2:0]		
CCh	G6	00h	R/W	BRTG6[3:0]				--	SDTG6[2:0]		
CDh	G7	00h	R/W	BRTG7[3:0]				--	SDTG7[2:0]		
CEh	G8	00h	R/W	BRTG8[3:0]				--	SDTG8[2:0]		
CFh	G9	00h	R/W	BRTG9[3:0]				--	SDTG9[2:0]		
D0h	H1	00h	R/W	BRTH1[3:0]				--	SDTH1[2:0]		
D1h	H2	00h	R/W	BRTH2[3:0]				--	SDTH2[2:0]		
D2h	H3	00h	R/W	BRTH3[3:0]				--	SDTH3[2:0]		
D3h	H4	00h	R/W	BRTH4[3:0]				--	SDTH4[2:0]		
D4h	H5	00h	R/W	BRTH5[3:0]				--	SDTH5[2:0]		
D5h	H6	00h	R/W	BRTH6[3:0]				--	SDTH6[2:0]		
D6h	H7	00h	R/W	BRTH7[3:0]				--	SDTH7[2:0]		
D7h	H8	00h	R/W	BRTH8[3:0]				--	SDTH8[2:0]		
D8h	H9	00h	R/W	BRTH9[3:0]				--	SDTH9[2:0]		
D9h	I1	00h	R/W	BRTI1[3:0]				--	SDTI1[2:0]		
DAh	I2	00h	R/W	BRTI2[3:0]				--	SDTI2[2:0]		
DBh	I3	00h	R/W	BRTI3[3:0]				--	SDTI3[2:0]		
DCh	I4	00h	R/W	BRTI4[3:0]				--	SDTI4[2:0]		
DDh	I5	00h	R/W	BRTI5[3:0]				--	SDTI5[2:0]		
DEh	I6	00h	R/W	BRTI6[3:0]				--	SDTI6[2:0]		
DFh	I7	00h	R/W	BRTI7[3:0]				--	SDTI7[2:0]		
E0h	I8	00h	R/W	BRTI8[3:0]				--	SDTI8[2:0]		
E1h	I9	00h	R/W	BRTI9[3:0]				--	SDTI9[2:0]		

Note) Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read. Writing to these bits will be ignored.

■ Technical Data (continued)

3. Register map Detailed Explanation

Register Name		RST							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
01h	R/W	--	--	--	--	--	--	RAMRST	SRST
Default	00h	0	0	0	0	0	0	0	0

D1 : RAMRST RAM reset
[0] : RAM can be overwrite (default)
[1] : Clear all PWM duty setting and intensity setting

D0 : SRST Soft reset control
[0] : Reset release state (default)
[1] : Reset reset

- This register will auto-return to zero when written with "High" logic value.

Register Name		POWERCNT							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
02h	R/W	--	--	--	--	--	--	--	OSCEN
Default	00h	0	0	0	0	0	0	0	0

D0 : OSCEN Internal oscillator ON/OFF bit
[0] : Internal oscillator OFF (default)
[1] : Internal oscillator ON

- Oscillator will auto turn ON if any of the LED drivers are enabled (MTXON = 1) even if this bit is Low.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		OPTION							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
04h	R/W	--	--	--	--	ZPDEN	MLDACT	CLKOUT	EXTCLK
Default	00h	0	0	0	0	0	0	0	0

D3 : ZPDEN Ghost Image Prevention Enable
[0] : Turn off ghost image prevention (default)
[1] : Turn on ghost image prevention

D2 : MLDACT External Melody Input Selection
[0] : Turn off melody mode (default)
[1] : Turn on melody mode

D1 : CLKOUT Internal clock output enable
[0] : Internal clock is not output from CLKOUT (default)
[1] : Internal clock is output from CLKOUT

D0 : EXTCLK Internal/external synchronous clock selection
[0] : Internal clock operation (default)
[1] : External clock operation

- For D2, D1 and D0 cannot be set to High at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Register Name		MTXON							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
05h	R/W	--	--	--	IMAX Reserved	IMAX[2:0]			MTXON
Default	1Eh	0	0	0	1	1	1	1	0

D3-1 : IMAX Maximum current setup selection
[000] : 7.5 mA
[001] : 15 mA
[010] : 22.5 mA
[011] : 30 mA
[100] : 37.5 mA
[101] : 45 mA
[110] : 52.5 mA
[111] : 60 mA (default)

D0 : MTXON LED Matrix Set up ON/OFF control
[0] : OFF (default)
[1] : ON

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		PWMEN1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
06h	R/W	PWMA8	PWMA7	PWMA6	PWMA5	PWMA4	PWMA3	PWMA2	PWMA1
Default	00h	0	0	0	0	0	0	0	0

D7 : PWMA8 A8 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D6 : PWMA7 A7 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D5 : PWMA6 A6 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D4 : PWMA5 A5 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D3 : PWMA4 A4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D2 : PWMA3 A3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D1 : PWMA2 A2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D0 : PWMA1 A1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

- The definition for register addresses #07h to #10h is the same as address #06h.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		MLDEN1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
11h	R/W	MLDA8	MLDA7	MLDA6	MLDA5	MLDA4	MLDA3	MLDA2	MLDA1
Default	00h	0	0	0	0	0	0	0	0

D7 : MLDA8 A8 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D6 : MLDBA7 A7 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D5 : MLDA6 A6 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D4 : MLDA5 A5 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D3 : MLDA4 A4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D2 : MLDA3 A3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D1 : MLDA2 A2 Melody mode enable
[0] : Not PWM mode (default)
[1] : Melody mode

D0 : MLDA1 A1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

- The definition for register addresses #12h to #1Bh is the same as address #11h.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

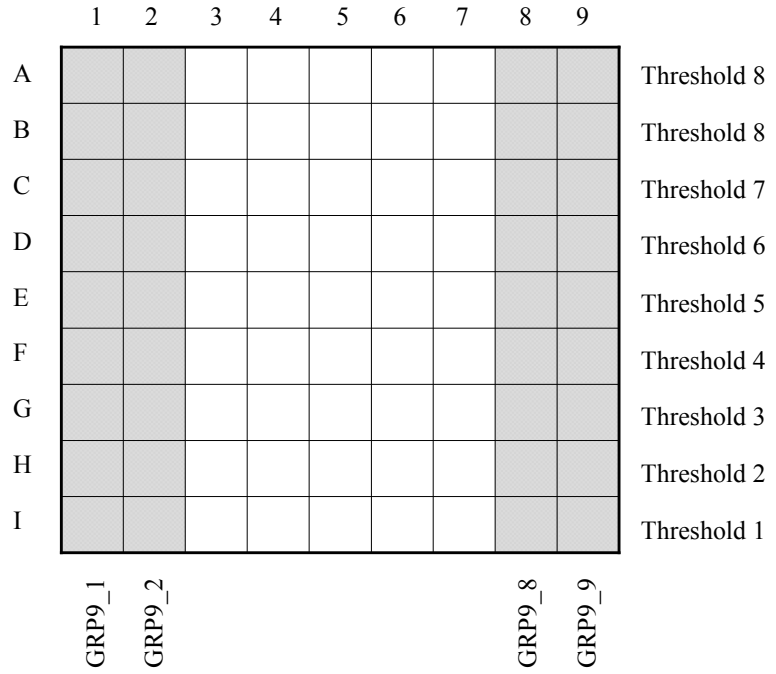
Register Name		MLDMODE1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Ah	R/W	--	--	--	--	GRP9_9	GRP9_8	GRP9_2	GRP9_1
Default	00h	0	0	0	0	0	0	0	0

D3 : GRP9_9 Column 9 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (I9 → H9 → G9 → F9 → E9 → D9 → C9 → B9 → A9)

D2 : GRP9_8 Column 8 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (I8 → H8 → G8 → F8 → E8 → D8 → C8 → B8 → A8)

D1 : GRP9_2 Column 2 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (I2 → H2 → G2 → F2 → E2 → D2 → C2 → B2 → A2)

D0 : GRP9_1 Column 1 blink with external input as a group
[0] : Normal (default)
[1] : Melody mode (I1 → H1 → G1 → F1 → E1 → D1 → C1 → B1 → A1)



- During Bar Mode, auto threshold detection should be used. This IC does not support Bar Mode with fixed threshold setting.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		THOLD							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Bh	R/W	THOLD[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7 : THOLD[7] Threshold 8 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 8 is used. (Threshold 8 is about 1.93 V)

D6 : THOLD[6] Threshold 7 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 7 is used. (Threshold 7 is about 1.80 V)

D5 : THOLD[5] Threshold 6 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 6 is used. (Threshold 6 is about 1.67 V)

D4 : THOLD[4] Threshold 5 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 5 is used. (Threshold 5 is about 1.55 V)

D3 : THOLD[3] Threshold 4 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 4 is used. (Threshold 4 is about 1.42 V)

D2 : THOLD[2] Threshold 3 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 3 is used. (Threshold 3 is about 1.30 V)

D1 : THOLD[1] Threshold 2 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 2 is used. (Threshold 2 is about 1.17 V)

D0 : THOLD[0] Threshold 1 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 1 is used. (Threshold 1 is about 1.04 V)

- When all bits are set zero, threshold is in auto-detection mode (default)
- Do not set more than 1 register bit to logic "High" value at the same time.
- If 2 bits are set to "High" at the same time, system will only recognize the first "High" bit threshold that is set.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		CONSTX6_1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Ch	R/W	--	--	X6	X5	X4	X3	X2	X1
Default	00h	0	0	0	0	0	0	0	0

D5 : X6 X6CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X6CNT is fixed to High. The LED A6's current setting is used.

D4 : X5 X5CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X5CNT is fixed to High. The LED A5's current setting is used.

D3 : X4 X4CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X4CNT is fixed to High. The LED A4's current setting is used.

D2 : X3 X3CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X3CNT is fixed to High. The LED A3's current setting is used.

D1 : X2 X2CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X2CNT is fixed to High. The LED A2's current setting is used.

D0 : X1 X1CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X1CNT is fixed to High. The LED A1's current setting is used.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		CONSTX10_7							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Dh	R/W	--	--	--	--	X10	X9	X8	X7
Default	00h	0	0	0	0	0	0	0	0

D3 : X10 X10CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X10CNT is fixed to High. The LED I1's current setting is used.

D2 : X9 X9CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X9CNT is fixed to High. The LED A9's current setting is used.

D1 : X8 X8CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X8CNT is fixed to High. The LED A8's current setting is used.

D0 : X7 X7CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix X7CNT is fixed to High. The LED A7's current setting is used.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		CONSTY6_1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Eh	R/W	--	--	Y6	Y5	Y4	Y3	Y2	Y1
Default	00h	0	0	0	0	0	0	0	0

D5 : Y6 Y6CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y6CNT is fixed to High.

D4 : Y5 Y5CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y5CNT is fixed to High.

D3 : Y4 Y4CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y4CNT is fixed to High.

D2 : Y3 Y3CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y3CNT is fixed to High.

D1 : Y2 Y2CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y2CNT is fixed to High.

D0 : Y1 Y1CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y1CNT is fixed to High.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		CONSTY9_7							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Fh	R/W	--	--	--	--	--	Y9	Y8	Y7
Default	00h	0	0	0	0	0	0	0	0

D2 : Y9 Y9CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y9CNT is fixed to High.

D1 : Y8 Y8CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y8CNT is fixed to High.

D0 : Y7 Y7CNT constant mode.
[0] : Normal matrix operation (default)
[1] : Matrix Y7CNT is fixed to High.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		MASKY6_1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
30h	R/W	--	--	Y6MSK	Y5MSK	Y4MSK	Y3MSK	Y2MSK	Y1MSK
Default	00h	0	0	0	0	0	0	0	0

D5 : Y6MSK Y6CNT is fixed to Low mode.
[0] : Y6CNT output (default)
[1] : Y6CNT is fixed to Low.

D4 : Y5MSK Y5CNT is fixed to Low mode.
[0] : Y5CNT output (default)
[1] : Y5CNT is fixed to Low.

D3 : Y4MSK Y4CNT is fixed to Low mode.
[0] : Y4CNT output (default)
[1] : Y4CNT is fixed to Low.

D2 : Y3MSK Y3CNT is fixed to Low mode.
[0] : Y3CNT output (default)
[1] : Y3CNT is fixed to Low.

D1 : Y2MSK Y2CNT is fixed to Low mode.
[0] : Y2CNT output (default)
[1] : Y2CNT is fixed to Low.

D0 : Y1MSK Y1CNT is fixed to Low mode.
[0] : Y1CNT output (default)
[1] : Y1CNT is fixed to Low.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		MASKY9_7							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
31h	R/W	--	--	--	--	--	Y9MSK	Y8MSK	Y7MSK
Default	00h	0	0	0	0	0	0	0	0

D2 : Y9MSK Y9CNT is fixed to Low mode.
[0] : Y9CNT output (default)
[1] : Y9CNT is fixed to Low.

D1 : Y8MSK Y8CNT is fixed to Low mode.
[0] : Y8CNT output (default)
[1] : Y8CNT is fixed to Low.

D0 : Y7MSK Y7CNT is fixed to Low mode.
[0] : Y7CNT output (default)
[1] : Y7CNT is fixed to Low.

Y*CNT fix mode priority (* == 1 to 9)

X*	Y*MSK	Y*	XCNT	YCNT
1	x	x	High	Low
0	1	x	X*CNT	Low
0	0	1	Low	High
0	0	0	X*CNT	Y*CNT

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

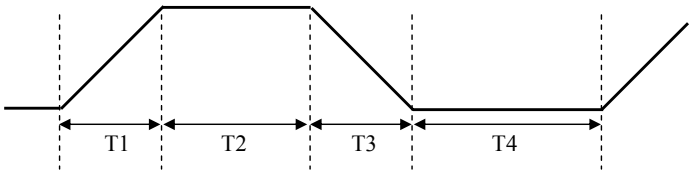
Register Name		SLPTIME							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
32h	R/W	--	--	--	FADTIM	SLOPEEXTL[1:0]		SLOPEEXTH[1:0]	
Default	00h	0	0	0	0	0	0	0	0

D4 : FADTIM Fade out time control.
[0] : T3 = T1 (default)
[1] : T3 = T1 × 2

- This bit also affect in PWM fade out mode. Fade out time becomes 2 times of fade in time when FADTIM = 1.

D3-2 : SLOPEEXTL T4 time extent control.
[00] : T4 = T1 (default)
[01] : T4 = T1 × 0.25
[10] : T4 = T1 × 0.5
[11] : T4 = T1 × 2

D1-0 : SLOPEEXTH T2 time extent control.
[00] : T2 = T1 (default)
[01] : T2 = T1 × 0.25
[10] : T2 = T1 × 0.5
[11] : T2 = T1 × 2



- T1 time is controlled by the register #91h to #E1h.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		MLDCOM							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
33h	R/W	--	--	--	--	--	MLDCOM[2:0]		
Default	03h	0	0	0	0	0	0	1	1

D2-0 : MLDCOM LED Turn on time compensation in melody mode
[000] : 0s
[001] : 1.94 µs
[010] : 3.87 µs
[011] : 5.8 µs (default)
[100] : 7.74 µs
[101] : 9.67 µs
[110] : 11.6 µs
[111] : 13.5 µs

Register Name		SCANSET							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
36h	R/W	--	--	--	--	SCANSET[3:0]			
Default	08h	0	0	0	0	1	0	0	0

D3-0 : SCANSET SCAN number control
[0000] : Only scan the first column.
[0001] : Only scan the first 2 column.
[0010] : Only scan the first 3 column.
[0011] : Only scan the first 4 column.
[0100] : Only scan the first 5 column.
[0101] : Only scan the first 6 column.
[0110] : Only scan the first 7 column.
[0111] : Only scan the first 8 column.
[1000] : Scan all column. (default)

- All other values will scan all column.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		DTA1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
40h	R/W	DTA1[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7-0 : DTA1 A1 PWM duty control.
[0000_0000] : 0%. (default)
[0000_0001] : 0.39%. (1/256)
[0000_0010] : 0.78%. (2/256)
[0000_0011] : 1.17%. (3/356)
…
[1111_1100] : 98.8%. (253/256)
[1111_1110] : 99.2%. (254/256)
[1111_1111] : 99.6%. (255/256)

- This duty setting is only effective when PWMA1 is High.
- The definition for register addresses #41h to #90h is the same as address #40h.

■ Technical Data (continued)

3. Register map Detailed Explanation (continued)

Register Name		A1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
91h	R/W	BRTA1[3:0]				--	SDTA1[2:0]		
Default	00h	0	0	0	0	0	0	0	0

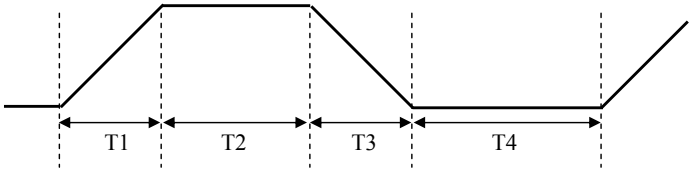
D7-4 : BRTA1 Luminance set up of LED A1 (in case of IMAX [2:0] == [011])

[0000] : 0 mA (default)
[0001] : 2 mA
[0010] : 4 mA
[0011] : 6 mA
[0100] : 8 mA
[0101] : 10 mA
…
[1010] : 20 mA
[1011] : 22 mA
[1100] : 24 mA
[1101] : 26 mA
[1110] : 28 mA
[1111] : 30 mA

D2-0 : SDTA1 (SCANSET == [11], default setting)

(1) Firefly Operation (PWMA1 == 0)

[000] : Constant current mode (default)
[001] : 0.248 s
[010] : 0.495 s
[011] : 0.99 s
[100] : 1.484 s
[101] : 1.979 s
[110] : 2.473 s
[111] : 2.968 s



(2) PWM Fade-in/out Operation (PWMA1 == 1)

[000] : Instant change mode (default)
[001] : 1.939 ms
[010] : 3.879 ms
[011] : 7.758 ms
[100] : 11.636 ms
[101] : 15.515 ms
[110] : 19.394 ms
[111] : 23.273 ms

- In case of PWM duty change from 0 to 255, the longest time is 255 × 23.273 ms = 5.957 s.
- T1 time is also controlled by SCANSET in register #36h. The calculation method is as follow:
  SCANSET == 0000 : T1 = 0.111 × T_default
  SCANSET == 0001 : T1 = 0.222 × T_default
  …
  SCANSET == 0111 : T1 = 0.888 × T_default
- The definition for register addresses #92h to #E1h is the same as address #91h.

■ Technical Data (continued)

4. Operation Mode priority

MTXON	X*	Y*MSK	Y*	PWM*	SDT*	Operation Mode
0	x	x	x	x	x	OFF
1	1	x	x	x	x	X*CNT constant mode
1	0	1	x	x	x	OFF
1	0	0	1	x	x	Turn on with all A1, A2, A3, A4
1	0	0	0	1	x	PWM mode
1	0	0	0	0	!=0	Blinking mode
1	0	0	0	0	0	Constant current mode

■ Technical Data (continued)

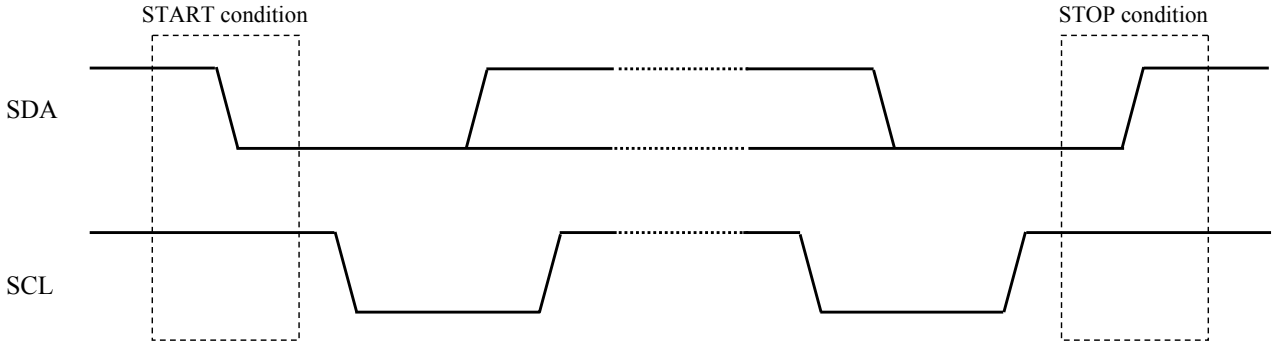
5. I²C Bus Interface

5.1 Basic Rules

- This IC, I²C-bus, is designed to correspond to the Standard-mode (100 kbps), Fast-mode(400 kbps) and Fast-mode plus (1 000 kbps) devices in the version 03 of NXP's specification. However, it does not correspond to the H_S-mode (to 3.4 Mbps).
- This IC will operate as a slave device in the I²C-bus system. This IC will not operate as a master device.
- The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm our company if it will be used in these mode systems.
- The I²C is the brand of NXP.

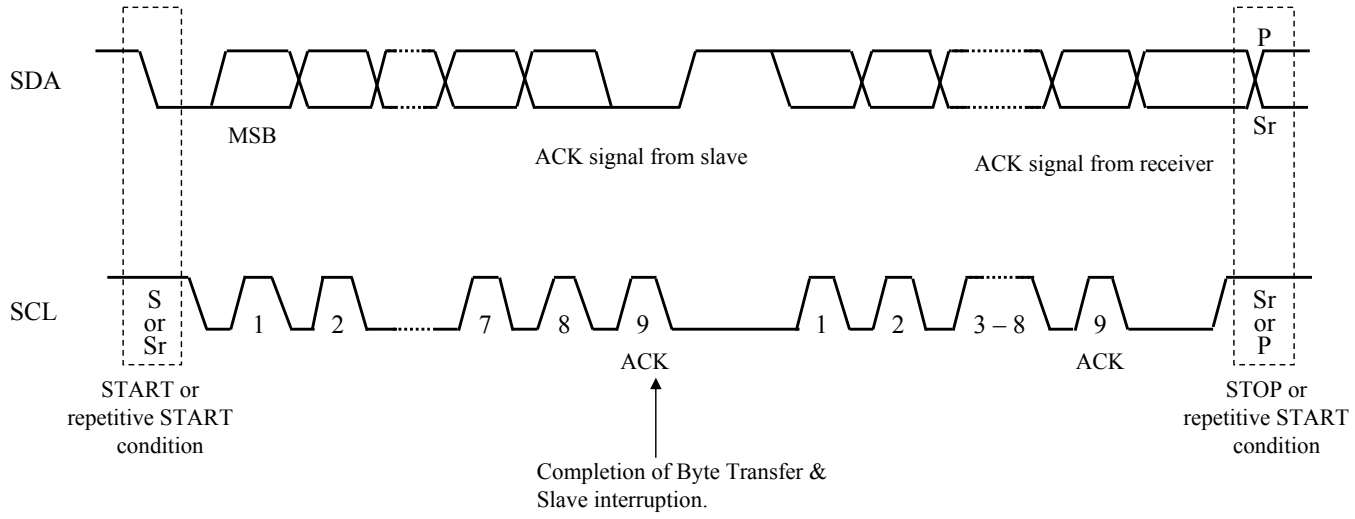
5.2 START and STOP conditions

When SDA signal changes from "High" to "Low" while SCL is "High" will trigger START condition. Whereas, STOP condition will be triggered when SDA signal changes from "Low" to "High" while SCL is "High".
START condition and STOP condition are always formed by the master. After the START condition occurs, the bus becomes busy state. After STOP condition occurs, the bus becomes free again.



5.3 Data Transfer

Length of each byte output to SDA line is always 8 bits. There is no limitation in the number of bytes that can be transmitted at 1 time. Many bytes can be sent. The acknowledge bit is necessary for each byte. Data is sequentially transmitted from most significant bit (MSB).



■ Technical Data (continued)

5. I²C Bus Interface (continued)

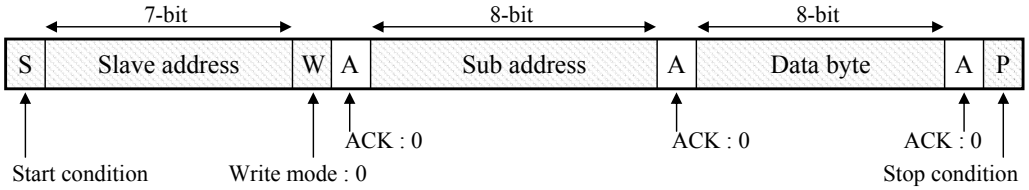
5.4 I²C Interface - Data Format

In this IC, 4 different Slave address can be changed by selecting SLAVSEL ("Low" or "High" or "SCL" or "SDI").
The slave addresses of this IC are as follow:

SLAVSEL	Slave address
Low	1011 100X
High	1011 101X
SCL	1011 110X
SDI	1011 111X

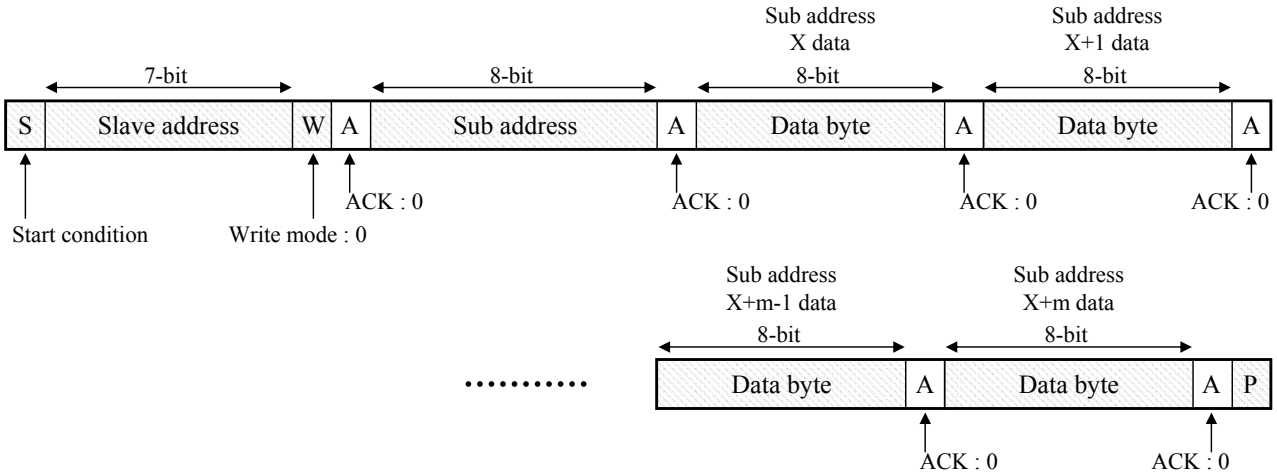
- Write mode

Sub address is not incremented automatically.
The next data byte is written in the same Sub address by transmitting data byte continuously.



- Write mode (Auto increment mode)

Data byte can be written in Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



: Data transmission from Master

: Data transmission from Slave

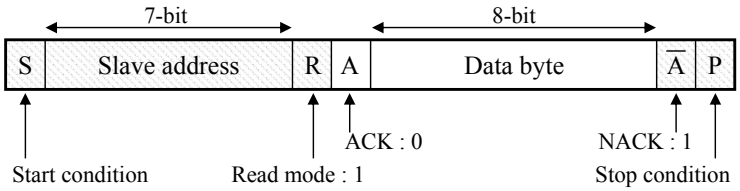
■ Technical Data (continued)

5. I²C Bus Interface (continued)

5.4 I²C Interface - Data Format (continued)

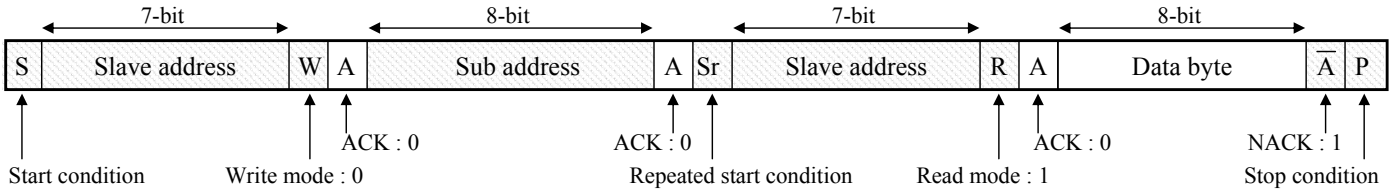
- Read mode (in case Sub address is not specified)

When Sub address 8 bit is not specified and data is read, this IC allows to read the value of adjacent Sub address specified in the last Write mode.
The next data byte reads the same Sub address by transmitting data byte continuously.



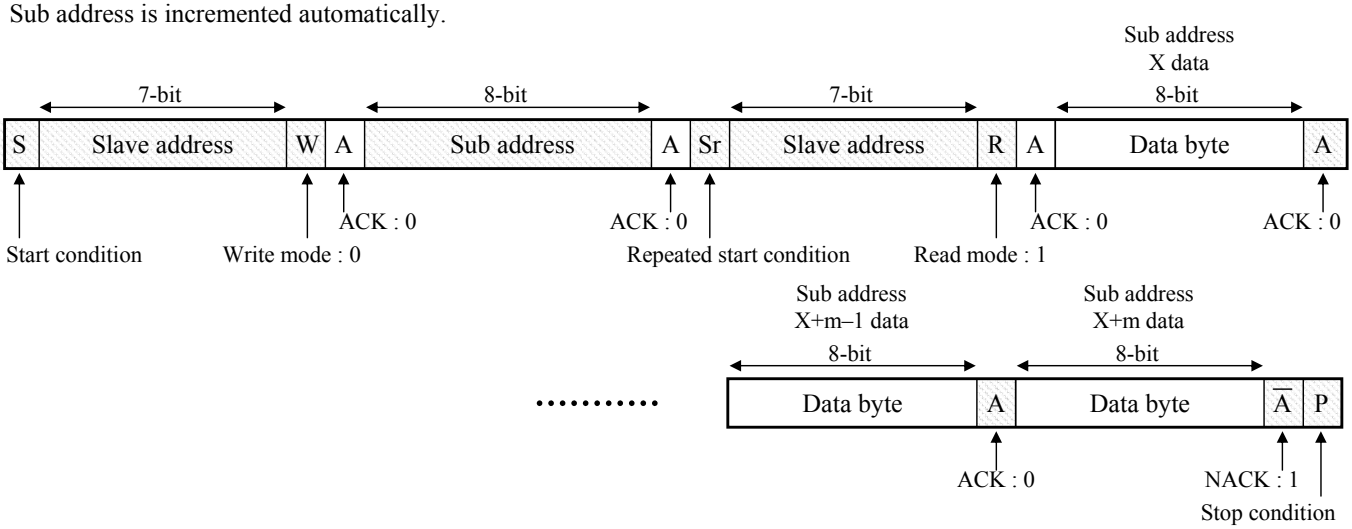
- Read mode (in case Sub address is specified)

Sub address is not incremented automatically.
The next data byte reads the same Sub address by transmitting data byte continuously.



- Read mode (Auto increment mode)

It is possible to read data byte in continuous Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



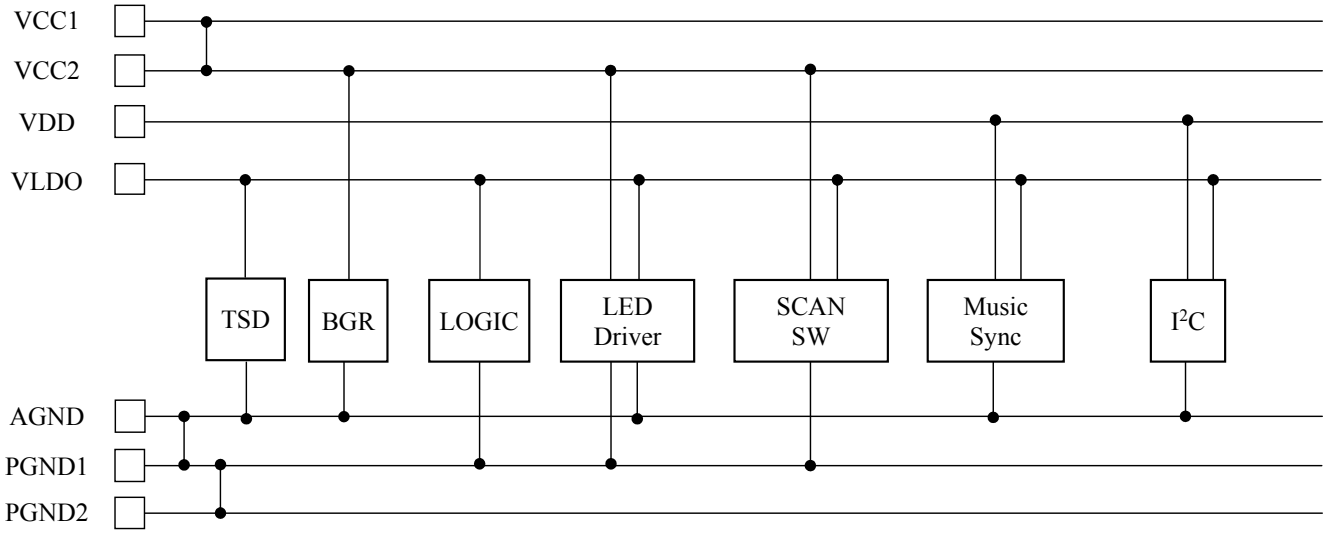
: Data transmission from Master

: Data transmission from Slave

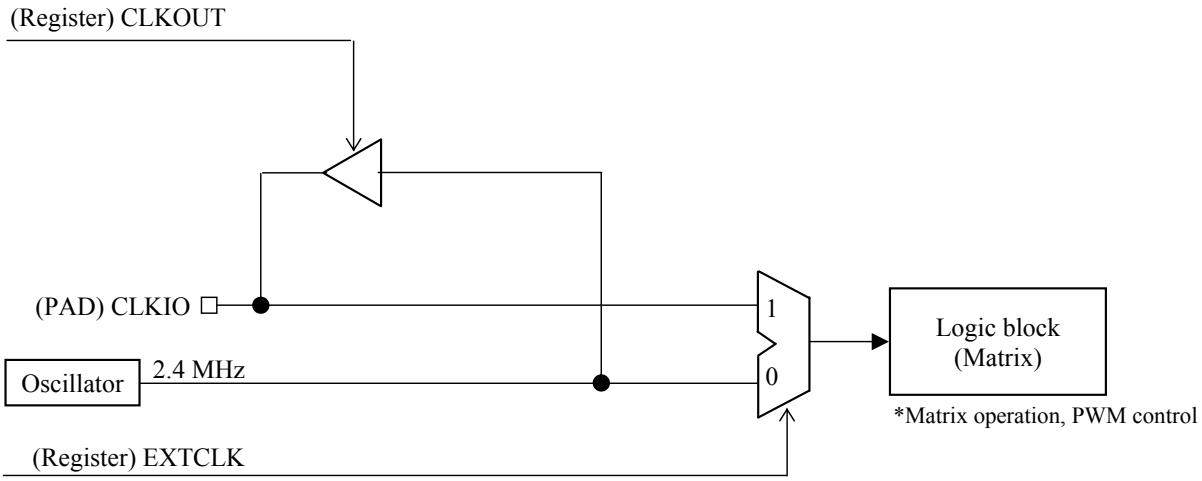
■ Technical Data (continued)

6. Signal distribution diagram

6.1 Distribution diagram of power supply



6.2 Distribution diagram of control / clock system

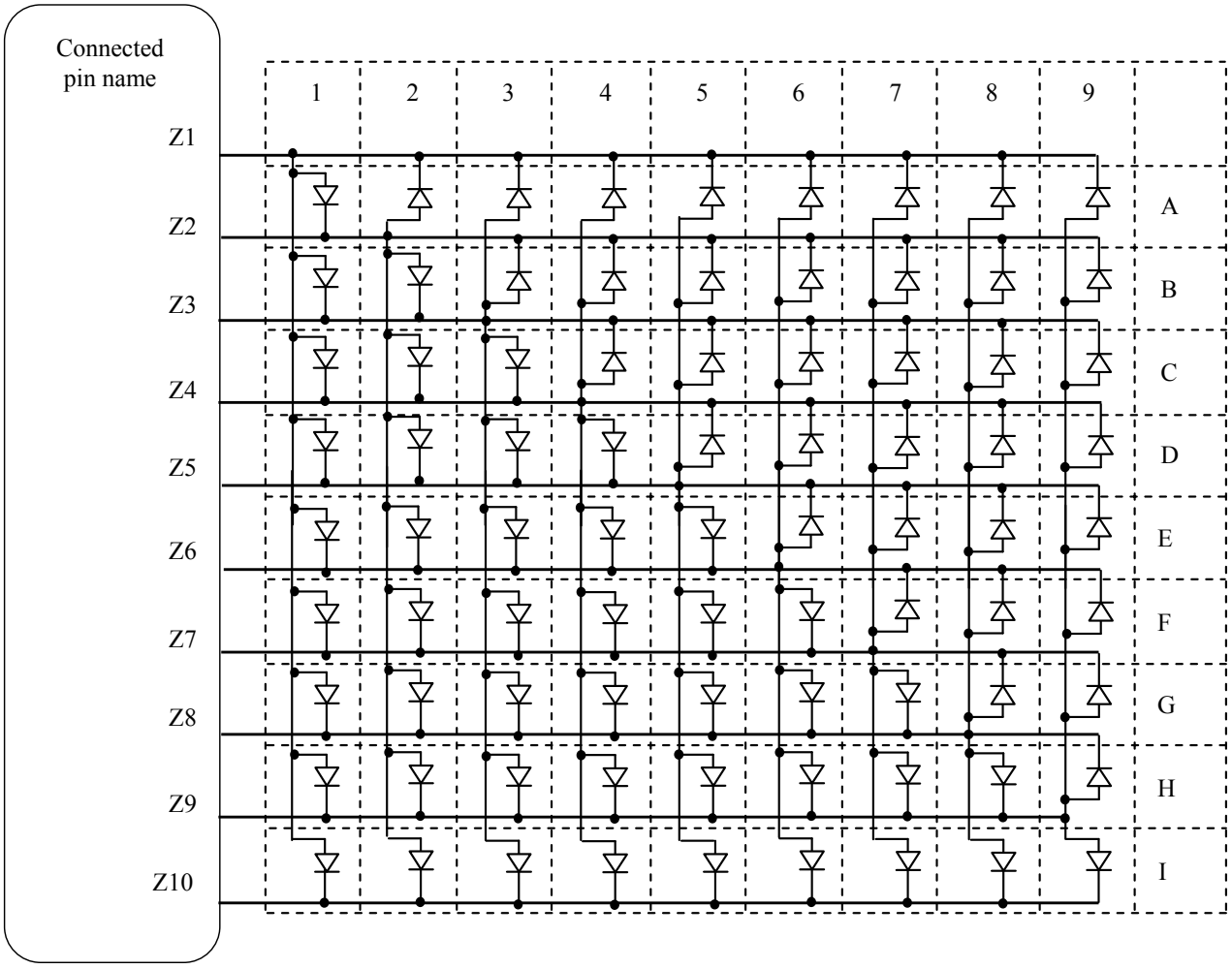


■ Technical Data (continued)

7. Block Configuration of Matrix LED

7.1 Matrix LED descriptions, Matrix LED's numbers

LED matrix driver circuit individually drives LED of 9 × 9 matrix. In total, the IC can drive and light up 81 LED.
In this specification, LED's number controlled by each pin corresponds as follows.
The internal logic circuit is operated by using an internal clock or the external clock input to the terminal CLKIO.

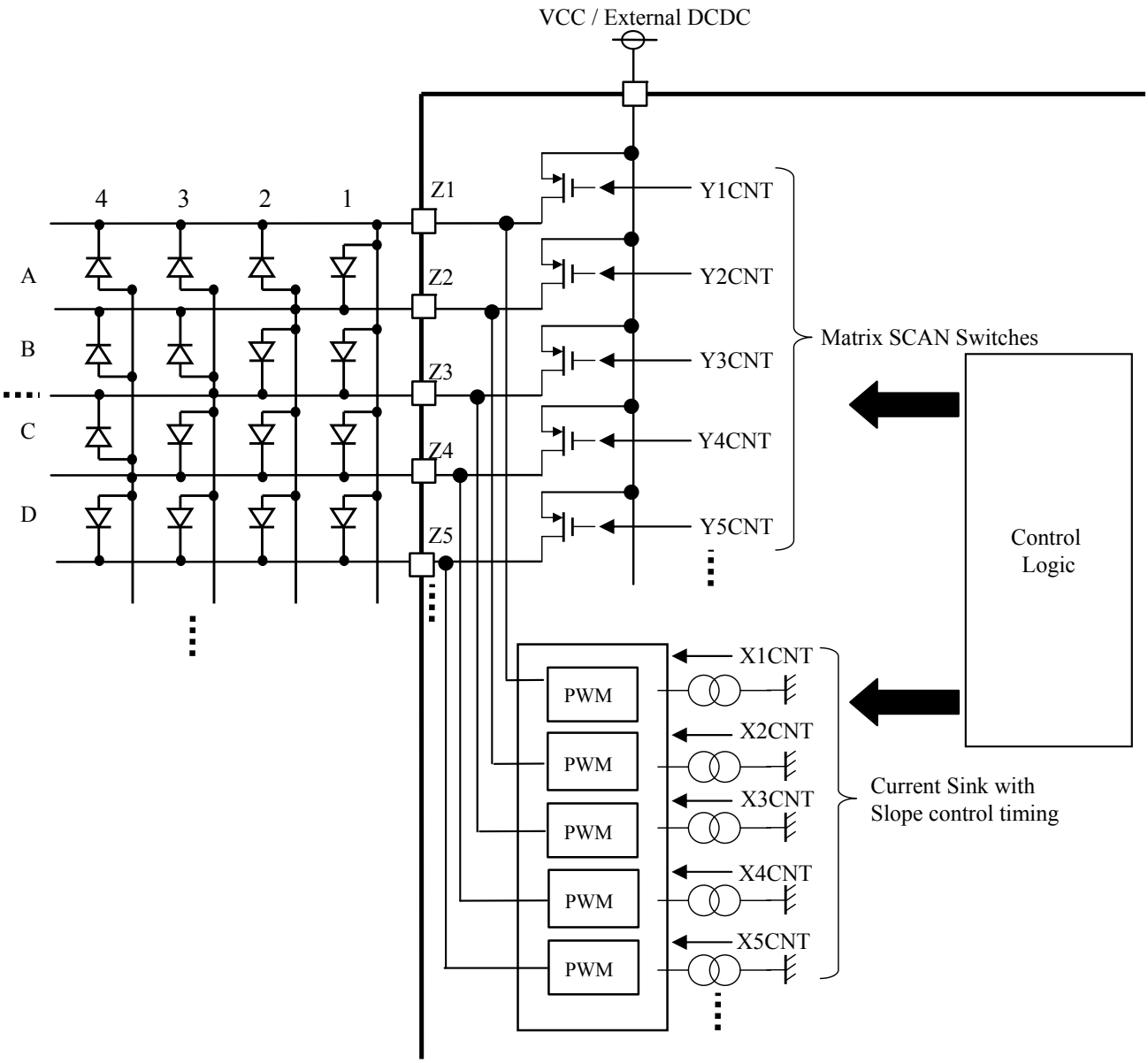


■ Technical Data (continued)

7. Block Configuration of Matrix LED (continued)

7.2 Driver Configuration

- Actual driver configuration is shown in the following figure.
- The anodes and cathode of each LED are connected to different Z pin as shown in figure below.
- Z10 pin consists of only Current Sink and Slope control timing driver. Thus, LED anode are not to be connected to Z10 pin.
- Please do not remove any of the LED inside the matrix if it is not used. If LED are to be removed, it is advice to remove the entire row (e.g: all LED in row A) instead of removing only 1 LED. If only one LED in the row is removed instead of the whole row, user needs to ensure that the reverse breakdown of LED is lower than the operating VCC level.
- Internal control logic according to user register settings is used to control Y1 to Y9CNT(PMOS ON/Off Scan Switches) as well as X1 to X10CNT (Current sink value as well as PWM/Slope timing for lighting effects)

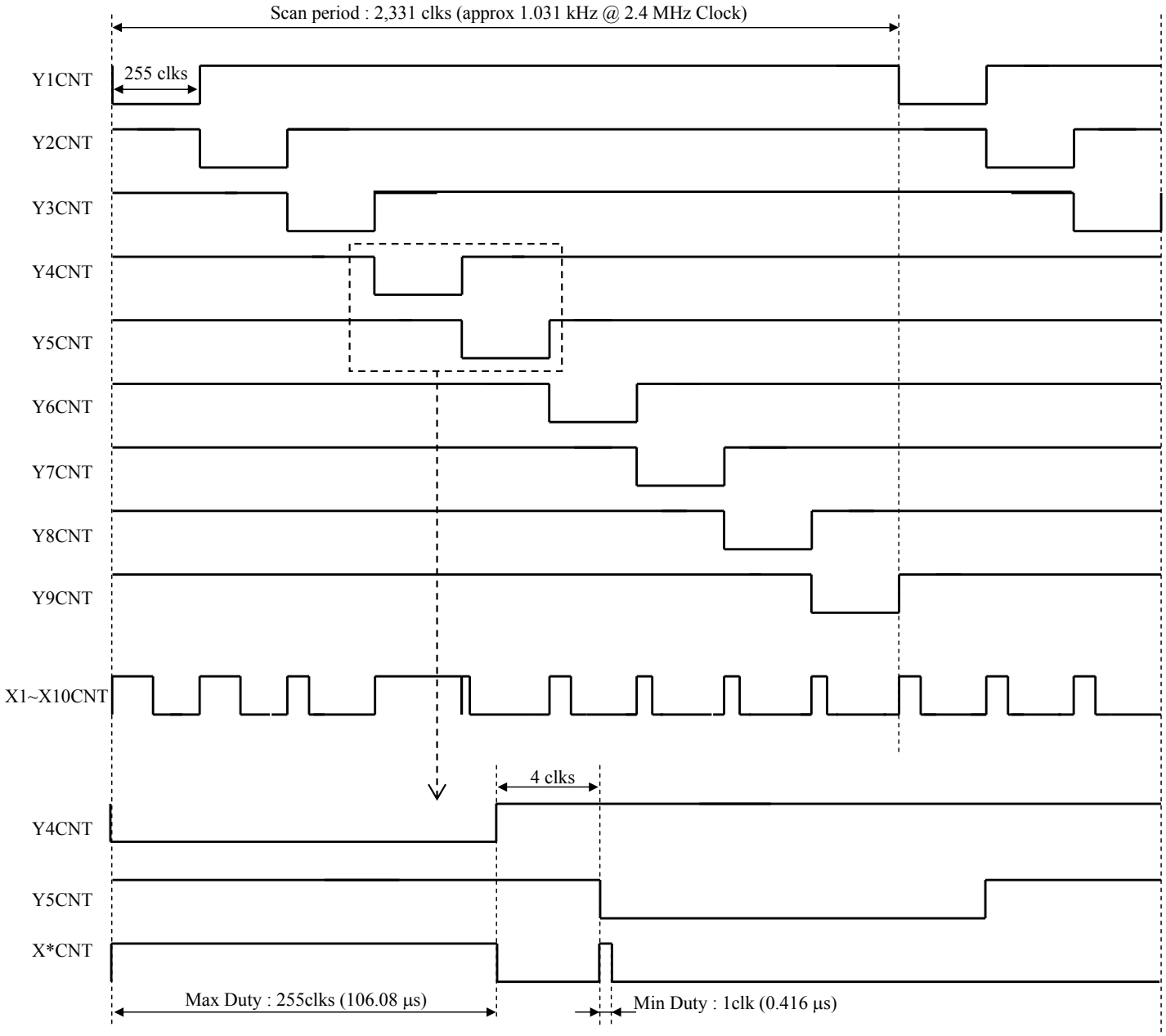


■ Technical Data (continued)

7. Block Configuration of Matrix LED (continued)

7.3 Timing Chart when in operation

- The figure below shows a timing chart when in operation.
- Timing can be controlled according to the external clock frequency input to CLKIO pin.
- In default condition, it is controlled by internal 2.4 MHz clock.
- Y1 to Y9CNT are scan timing which is turned on one at a time. The ON period of each pin is constant 255 clks (106.08 µs) and includes the interval of 4 clks (1.664 µs).
- 81 LED (9 × 9 matrix) are controlled by X1 to X10CNT according to below figure.
- When Yx = Xx = Low, the actual waveform of Zx is set to Hi-Z.



- Duty can be set using register DT*[7:0] from registers #40h to #90h. Additional brightness control is provided through register BRT*[3:0] (registers #91h to #E1h).

■ Technical Data (continued)

8. LED Driver Block Function

- Functions Table for LED Driver

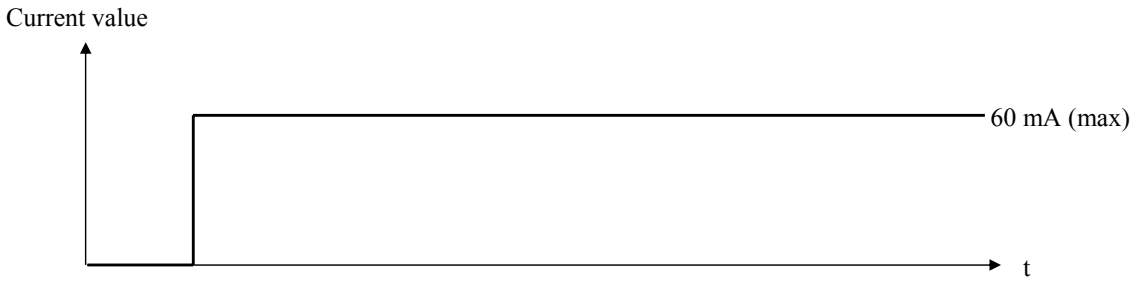
No.	Features	Setting Range
1	Constant current mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step
2	PWM mode and Fade-in/out mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Adjustable detention Time for each step : (1.939 ms to 23.273 ms / step)
3	Firefly mode	Fixed Current at 100% Duty IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Adjustable detention Time for each step : (0.248 s to 2.968 s / step)
4	Melody mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Each LED can synchronize with Music Input from CLKIO pin
5	Bar mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Group LED can synchronize with Music Input from CLKIO pin Bar mode has more priority than Melody mode.

8.1 Constant Current Mode

Maximum current setting value can be set up as 60mA using register IMAX[2:0] (register 05h). Brightness can be set through the register BRT*[3:0] (register #91h to #E1h) for individual LED. (please refer to page 25 for IMAX setting and page 39 for brightness setting).

Example)

E.g. If user sets register IMAX[2:0](#05h) = 011 and BRT*[3:0](#91h to #E1h) = 1111, the current will be 30 mA.
E.g. If user sets register IMAX[2:0](#05h) = 111 and BRT*[3:0](#91h to #E1h) = 1111, the current will be 60 mA.
E.g. If user sets register IMAX[2:0](#05h) = 111 and BRT*[3:0](#91h to #E1h) = 0111, the current will be 28 mA.



■ Technical Data (continued)

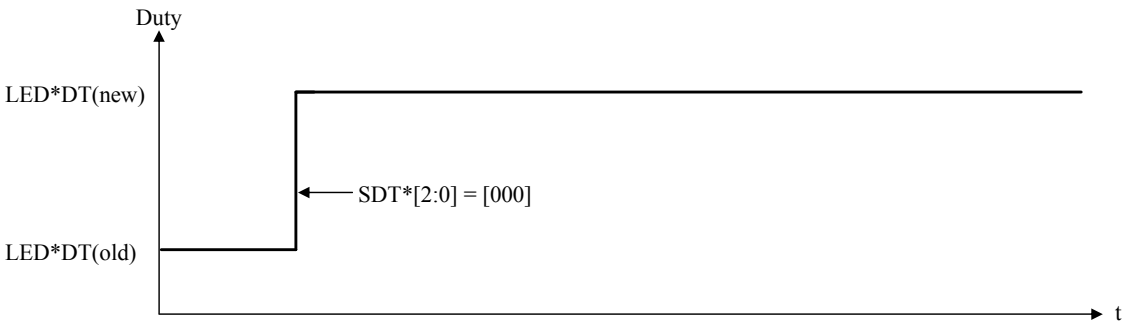
8. LED Driver Block Function (continued)

8.2 PWM Mode and Fade-in/out Mode

This operation is characterized by PWM signal having variable duty depending on register DT*[7:0] (registers #40h to #90h). However, any changes in duty is not instantaneous, but rather it will step to the new duty at time determined by register SDT*[2:0].

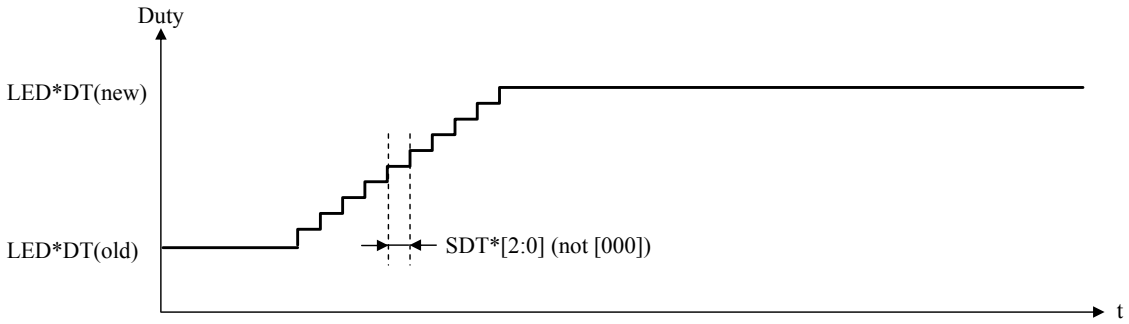
Example)

Case 1 : LED*DT(new) > LED*DT(old) (PWM Mode without Fade in/out control)



In Case 1, PWM duty has been changed from low to high duty. But the register SDT*[2:0] setting is [000] meaning there is no Fade in/out control. Therefore, PWM duty changes instantaneously. Users can see that LED becomes brighter instantaneously once PWM duty has been changed.

Case 2 : LED*DT(new) > LED*DT(old) (PWM Mode with Fade in control)



In Case 2, PWM duty has also been changed from low to high duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 2. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade in control. Users can see that LED becomes brighter slowly according to the timing set in register SDT*[2:0].

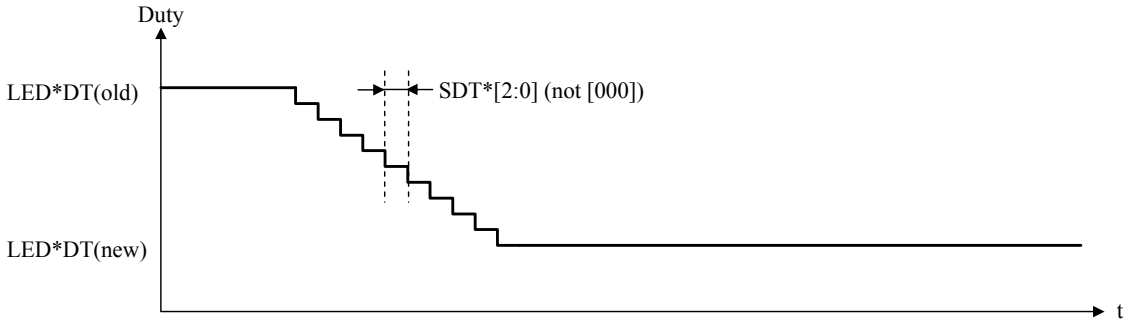
■ Technical Data (continued)

8. LED Driver Block Function (continued)

8.2 PWM Mode and Fade-in/out Mode (continued)

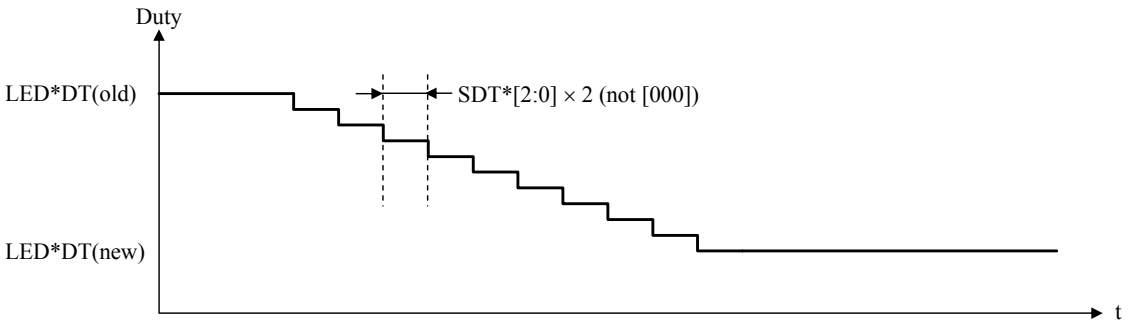
Example) (continued)

Case 3 : LED*DT(new) < LED*DT(old), FADTIM = 0 (PWM Mode with Fade out control)



In Case 3, PWM duty has been changed from high to low duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 3. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade out control. Users can see that LED becomes dimmer slowly according to the timing set in register SDT*[2:0].

Case 4 : LED*DT(new) < LED*DT(old), FADTIM = 1 (PWM Mode with Fade out control)



In Case 4, PWM duty has also been changed from high to low duty. Unlike in case 3, the register FADTIM is not [0]. Again, the register SDT*[2:0] setting is also not [000] in case 4. PWM duty has changed according to the register SDT*[2:0] setting. Users can see that LED becomes dimmer slowly. It is slower than Case3 as FADTIM register is high (2 times slower than Case 3 Fade out control).

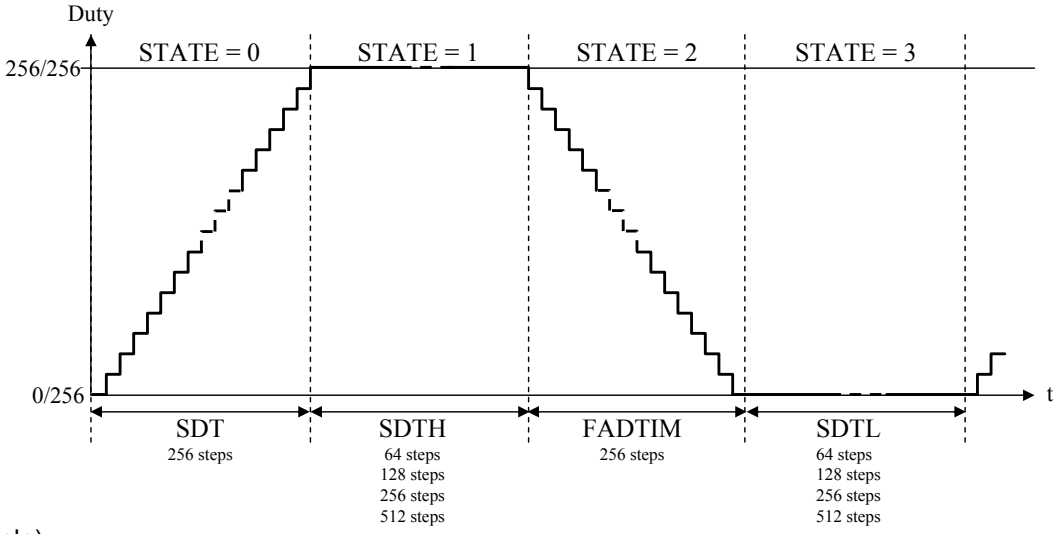
DT*[7:0] is set through register #40h to #90h. FADTIM is set through register #32h. SDT*[2:0] is set through register #91h to #E1h.

■ Technical Data (continued)

8. LED Driver Block Function (continued)

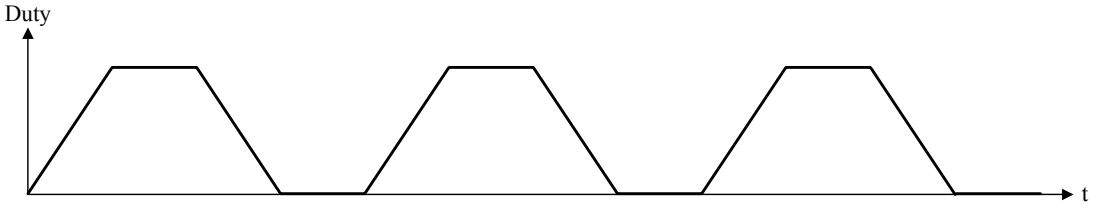
8.3 Firefly Control

This operation is characterized by PWM signal cycling from minimum to maximum duty and vice versa with auto repeat function at time step determined by register SDT*[2:0]. Unlike PWM Fade in/out mode, firefly is auto repetition of the sequence and thus creating LED blinking function effect.

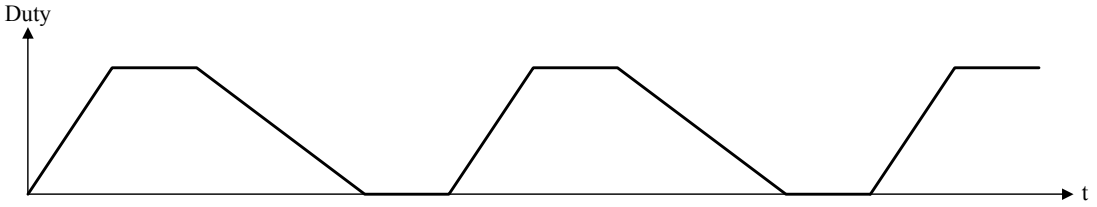


Example)

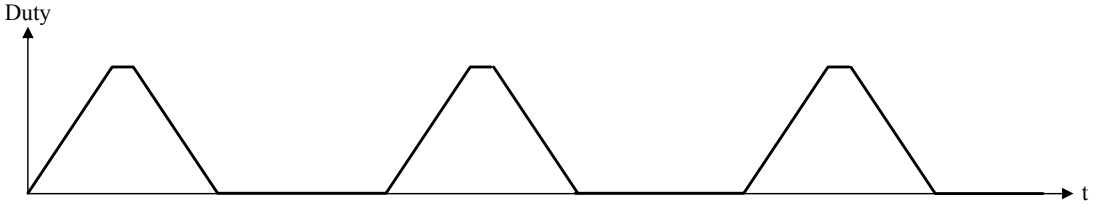
Example 1 : SDTH = 00 (SDT × 1), SDTL = 00 (SDT × 1), FADTIM = 0



Example 2 : SDTH = 00 (SDT × 1), SDTL = 00 (SDT × 1), FADTIM = 1 (SDT × 2)



Example 3 : SDTH = 01 (SDT × 0.25), SDTL = 11 (SDT × 2), FADTIM = 0



The SDTH is controlled by SLOPEEXTH[1:0] register, SDTL is controlled by SLOPEEXTL[1:0] register. All these register, SLOPEEXTH[1:0], SLOPEEXTL[1:0] and FADTIM can be set through register #32h. SDT*[2:0] registers are set individually through register #91h to #E1h. All other combinations of SDTH, SDTL and FADTIM is possible.

■ Technical Data (continued)

8. LED Driver Block Function (continued)

8.4 Melody Mode Explanation

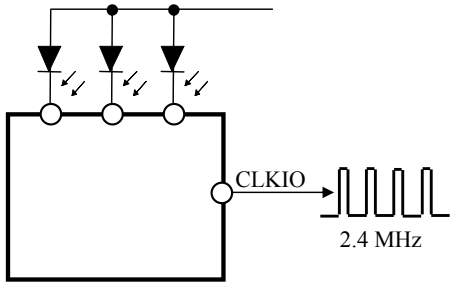
Melody mode is to synchronize LED to external music signal. Melody mode can be set through register MLDACT from register 04h. Each of the 81 LED matrix can be individually enabled for external music synchronization through register data (address #11h to #1Bh when register 04h is 04h).

External Music Signal can be injected from CLKIO pin. CLKIO pin serve as both input and output. CLKIO pin can output internal oscillator frequency by using CLKOUT register (register 04h).

CLKIO pin can be used as input for external signal by using EXTCLK register (register 04h). External clock frequency is typically 2.4 MHz. It is advisable to use external clock frequency from 1.2 MHz to 4.8 MHz (TBD).

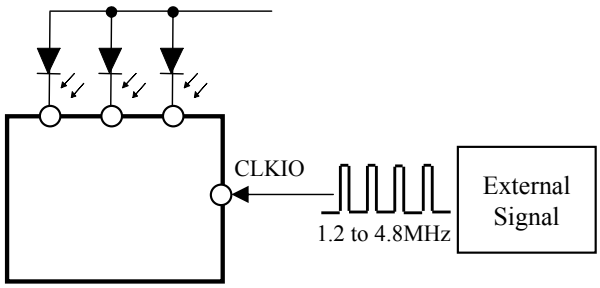
Please do not set MLDACT, EXTCLK and CLKOUT register to "High" at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Case 1 : CLKIO as output pin



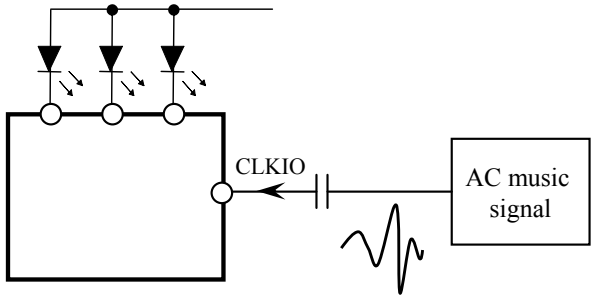
CLKIO output internal frequency by using CLKOUT register

Case 2 : CLKIO as input for external clock



CLKIO uses as external input by using EXTCLK register

Case 3 : CLKIO as input for music signal during melody mode



CLKIO uses as music input when melody mode is enabled by register MLDACT from register 04h.

Note : If input CLKIO voltage is higher than VDD, there will be back flow current to VDD. It can be calculated as below :

$$I_{BackFlow} = \frac{(V_{CLKIO} - 0.7\ V - VDD)}{393\ k\Omega}$$

■ Technical Data (continued)

8. LED Driver Block Function (continued)

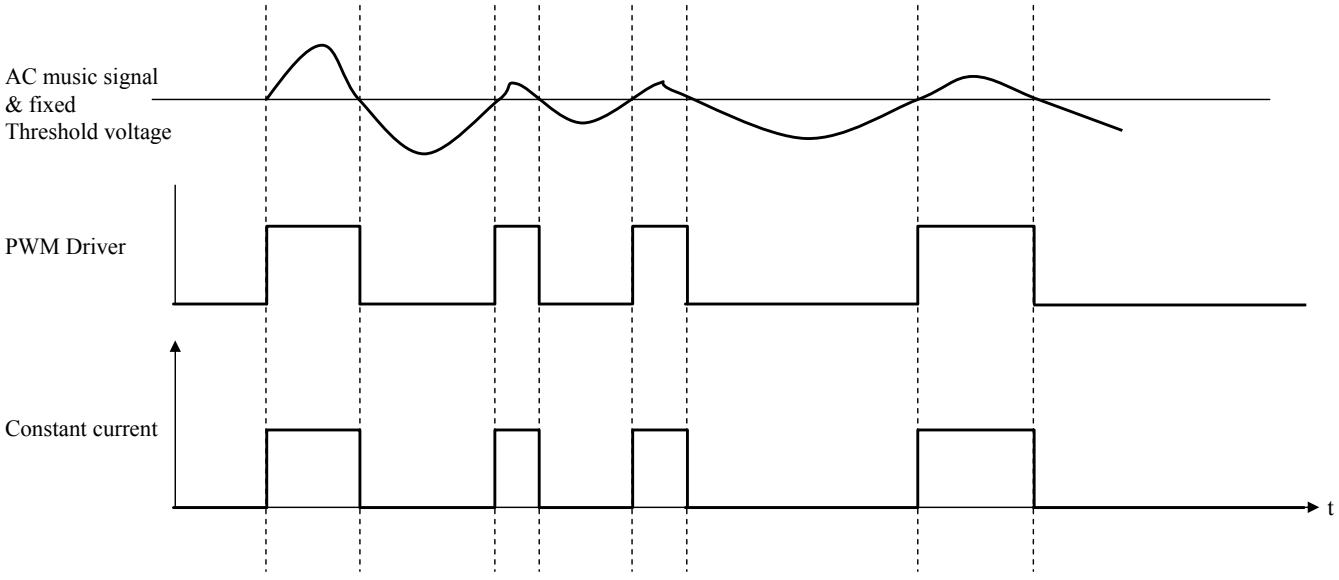
8.4 Melody Mode Explanation (continued)

AC music signal input from CLKIO pin will be compared with internal threshold setting. Based on the comparison of music signal and threshold voltage, PWM driver control will change and control the LED ON/OFF. Therefore, LED light on/off control will synchronize with music tempo while LED brightness will synchronize with music loudness.
There are two threshold mode, one is auto threshold and the other is fixed threshold mode.

There are 8 threshold voltage levels in this IC as defined in the register 2Bh (THOLD[7:0]). Auto threshold mode means that the 8 threshold voltages will be scanned automatically from the lowest to highest threshold voltages at a fixed frequency higher than audio frequency. Input music signal will be compared with these scanning threshold voltages to control PWM Driver in order to have music synchronization effects. This mode allows user to easily use music synchronize function without having the trouble of manually setting the detection threshold. When melody mode is enabled, auto threshold mode will be the default mode.

Fixed threshold mode means that the threshold voltage is fixed at one threshold level. It can be set using register 2Bh (THOLD[7:0]). Input music signal will be compared with this fixed threshold voltage set by the user. During fixed threshold mode, do not set more than 1 register bit to logic "High" value at the same time. If user set more register bits to logic "High" after setting 1 register bit to “High”, system will only recognise the first "High" bit threshold that is set. In this mode, user can have the flexibility to configure different threshold voltage levels to achieve the desired LED music synchronizing visual effect according to the system music input level.

It is also advised that AC music signal peak to peak voltage to be at least 0.35 V and not more than 2.8 V.



Example of Fixed threshold mode

- Brightness Compensation in Melody Mode

Additional brightness compensation in melody mode can be achieved by increasing or decreasing the turning on period of LED. Using brightness compensation register MLDCOM[2:0] (#33h), LED turning on period can be controlled and LED can become brighter or dimmer.

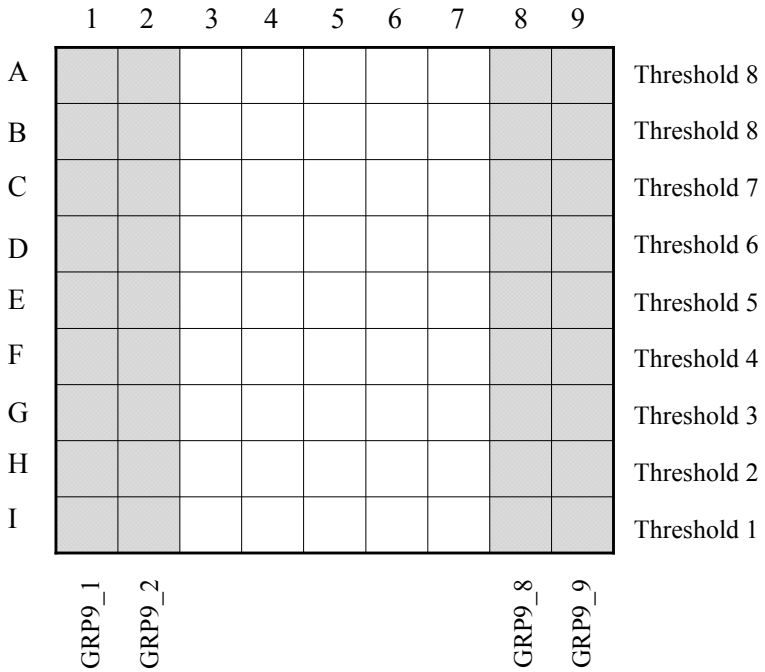
This additional brightness compensation will be effective only in auto threshold mode. If fixed threshold mode is used, this register will not be able to control LED brightness.

■ Technical Data (continued)

8. LED Driver Block Function (continued)

8.5 Bar Mode Explanation

Bar Mode operation is another method of external melody mode wherein a group of LEDs are used instead of individual LED. Bar Mode has higher priority than individual LED melody mode.



In the above diagram, column 1 = group1, column 2 = group2, column 8 = group8 and column 9 = group9. Each group can be enabled through register GRP9_1, 9_2, 9_8, 9_9 (address #2Ah). The LED in the all groups will be synchronized to threshold signals as follow:

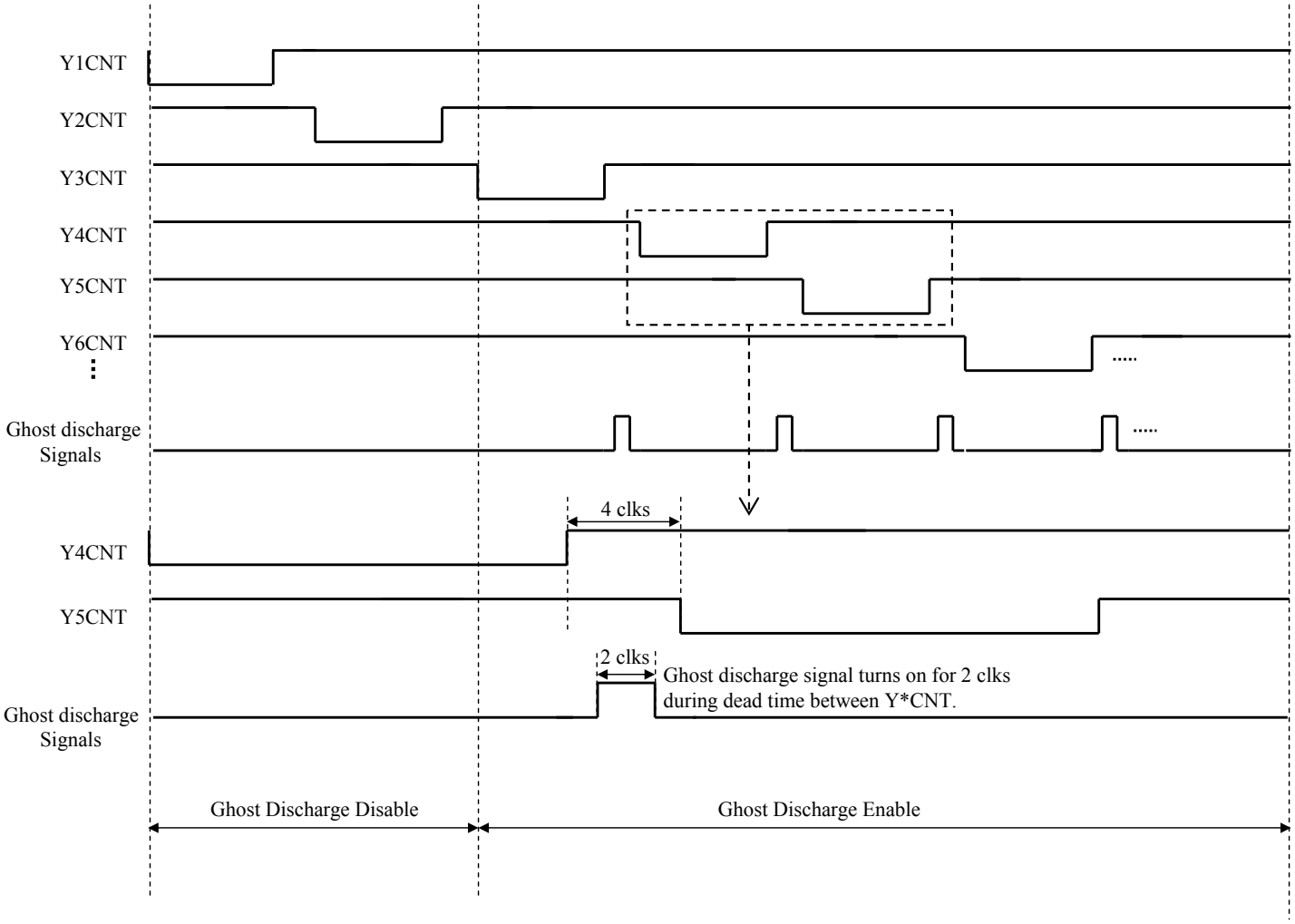
Threshold Signal	Bar Mode Group LED ON	
Threshold 1	Row's	I
Threshold 2	Row's	H, I
Threshold 3	Row's	G, H, I
Threshold 4	Row's	F, G, H, I
Threshold 5	Row's	E, F, G, H, I
Threshold 6	Row's	D, E, F, G, H, I
Threshold 7	Row's	C, D, E, F, G, H, I
Threshold 8	Row's	A, B, C, D, E, F, G, H, I

All other LEDs not in bar mode can operate in individual external melody mode or other modes.
During bar mode, auto threshold detection should be used. This IC does not support bar mode with fixed threshold setting. It is also recommended not to use other modes together with bar mode of LED in group 1, 2, 8 & 9 (i.e. LED A to I1, 2, 8, 9)

■ Technical Data (continued)

9. Ghost Image Prevention Function

Ghost images sometimes appear during LED matrix mode operation. Very dim light can appear in some LED even during OFF condition. This is called Ghost Image. In this IC, Ghost Image Prevention Function is included to reduce Ghost Image effect. Ghost Image Prevention Function can be enable through register ZPDEN (register 04h).

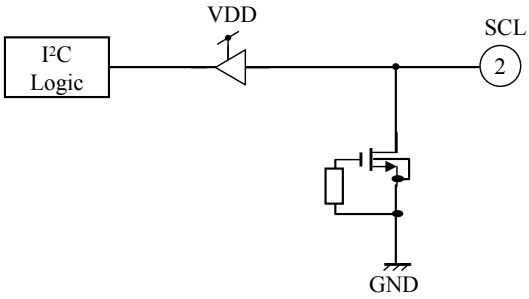
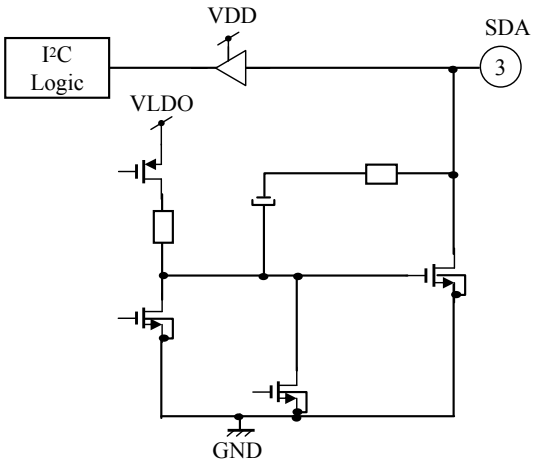
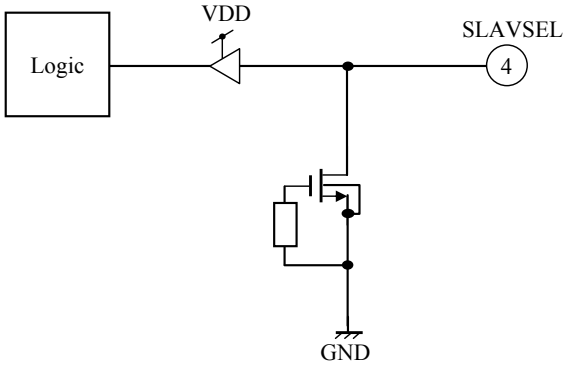


During normal operation, ghost discharge signal will be always low. When ghost image prevention function is enable through register 04h, ghost discharge signal will turn on for 2 clks cycle during 4 clks dead time between each YCNT. During on period of 2 clks cycle, output Z pin will be forced to half of VCC.

■ Technical Data (continued)

10. I/O block circuit diagrams and pin function descriptions

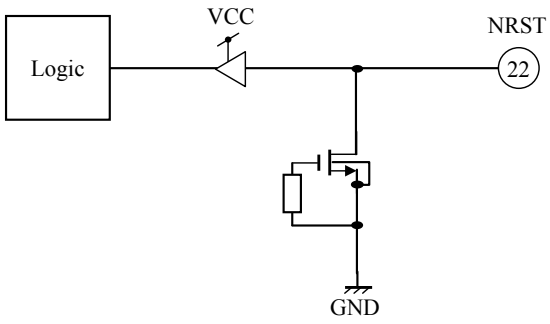
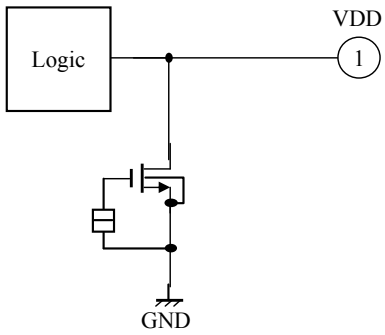
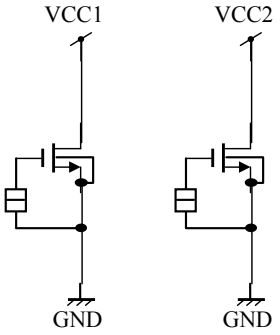
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
2	Logic Input VDD Level		High Impedance	SCL
3	Logic Input VDD Level Open Drain Output		High Impedance	SDA
4	Logic Input 0 V to VDD Level		High Impedance	SLAVSEL

■ Technical Data (continued)

10. I/O block circuit diagrams and pin function descriptions (continued)

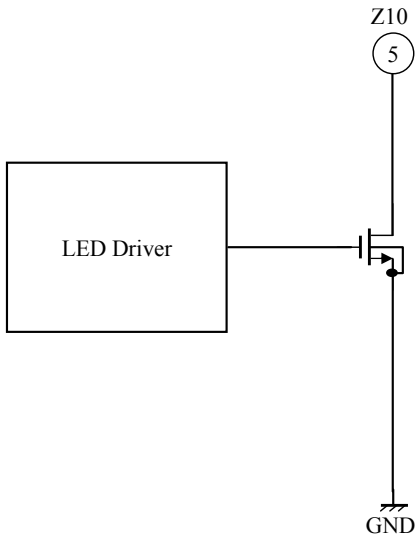
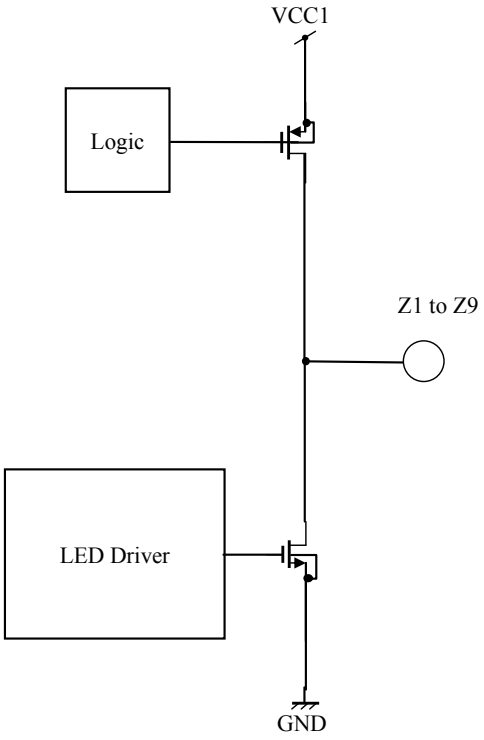
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
22	Logic Input 0 V to VCC Level		High Impedance	NRST
1	Logic Circuit Power Supply Input		—	VDD
17 7	VCC Power Supply Input		—	VCC1 VCC2

■ Technical Data (continued)

10. I/O block circuit diagrams and pin function descriptions (continued)

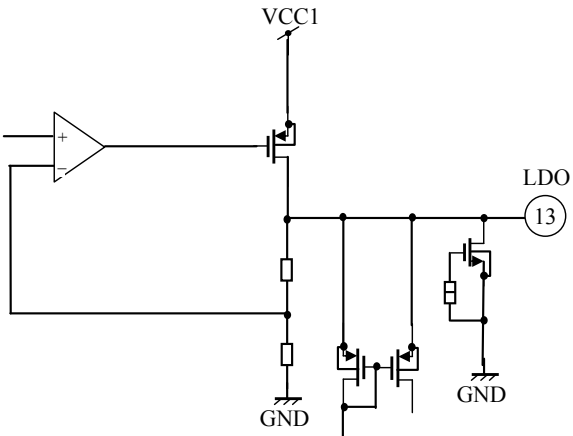
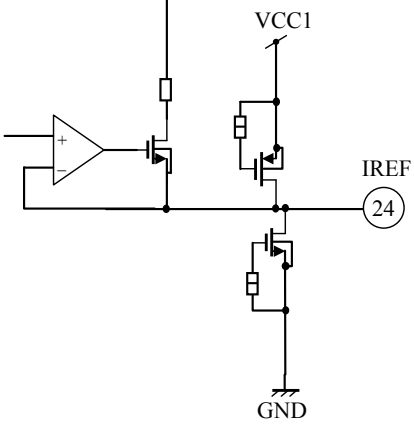
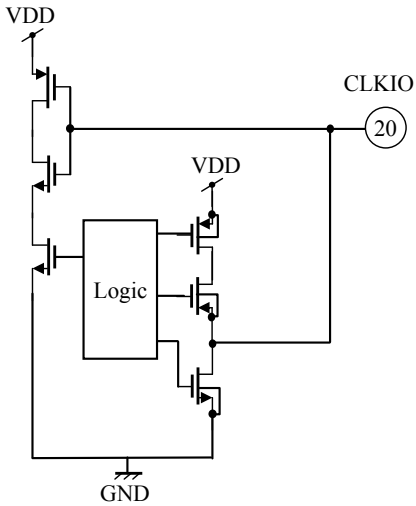
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
5	Constant current output or PWM output		High Impedance	Z10
19 18 16 14 12 11 10 8 6	Constant current output, PWM output, control switch		High Impedance	Z1 Z2 Z3 Z4 Z5 Z6 Z7 Z8 Z9

■ Technical Data (continued)

10. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

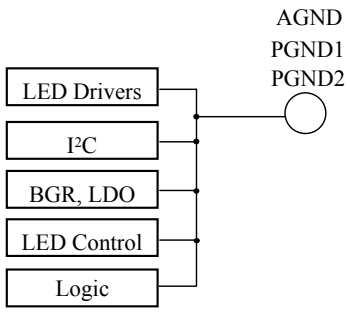
Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
13	2.85 V Voltage		716.5 kΩ	LDO
24	Standard current About GND potential or 0.5 V		GND Potential (Depends on external resistor)	IREF*
20	Logic or AC Input VDD Level Logic Output VDD Level		200 kΩ	CLKIO

Notes) *:To ensure the accuracy of the constant current of each LED, place the external resistor as close as possible to IC and parasitic capacitor of not more than 20 pF at IREF pin.

■ Technical Data (continued)

10. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
23 15 9	GND		—	AGND PGND1 PGND2

■ Usage Notes

- Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [Mobile phones].
   Consult our sales staff in advance for information on the following applications:
   - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   - Any applications other than the standard applications intended.
     (1) Space appliance (such as artificial satellite, and rocket)
     (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
     (3) Medical equipment for life support
     (4) Submarine transponder
     (5) Control equipment for power plant
     (6) Disaster prevention and security device
     (7) Weapon
     (8) Others : Applications of which reliability equivalent to (1) to (7) is required

   It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the IC described in this book for any special application, unless our company agrees to your using the IC in this book for any special application.
2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_{CC} short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
7. When using the LSI for new models, verify the safety including the long-term reliability for each product.
8. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.