July 2014

FAN6224
Synchronous Rectification Controller for Flyback and Forward Freewheeling Rectification

Features

- mWSaver™ Technology:
  - Internal Green Mode to Stop SR Switching for Lower No-Load Power Consumption
  - 300 μA Ultra-Low Green Mode Operating Current
- Synchronous Rectification Controller
- Suited for High-Side and Low-Side of Flyback Converters in QR, DCM, and CCM Operation
- Suited for Forward Freewheeling Rectification
- PWM Frequency Tracking with Secondary-Side Winding Voltage Detection
- 140 kHz Maximum Operation Frequency
- V_{DD} Pin Over-Voltage Protection (OVP)
- LPC Pin Open/Short Protection
- RES Pin Open/Short Protection
- RP Pin Open/Short Protection
- Internal Over-Temperature Protection (OTP)
- SOP-8 Package Available

Applications

- AC-DC NB Adapters
- Open-Frame SMPS

Description

FAN6224 is a secondary-side Synchronous Rectification (SR) controller to drive SR MOSFET for improved efficiency. The IC is suitable for flyback converters and forward freewheeling rectification.

FAN6224 can be applied in Continuous or Discontinuous Conduction Mode (CCM and DCM) and Quasi-Resonant (QR) flyback converters based on a proprietary linear-predict timing-control technique. The benefits of this technique include a simple control method without current-sense circuitry to accomplish noise immunity.

With PWM frequency tracking and secondary-side winding voltage detection, FAN6224 can operate in both fixed- and variable-frequency systems up to 140kHz.

FAN6224 detects output load condition and determines adjustable loading levels for Green Mode. In Green Mode, the SR controller stops all SR switching operation to reduce the operating current. Power consumption is maintained at a minimum level in light-load condition.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6224M	-40°C to +105°C	8-Lead, Small Outline Package (SOP-8)	Tape & Reel

Typical Application Diagrams

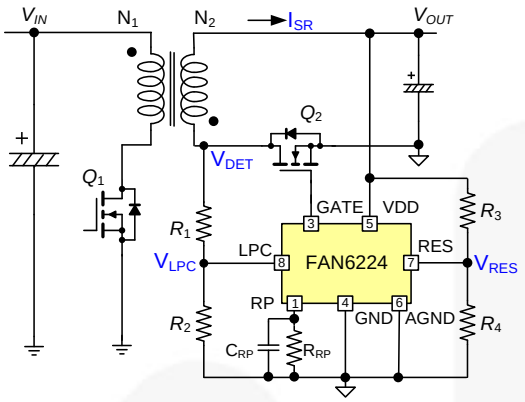


Figure 1. Flyback Low-Side SR

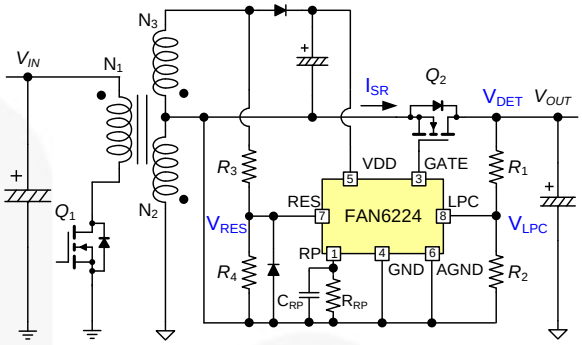


Figure 2. Flyback High-Side SR

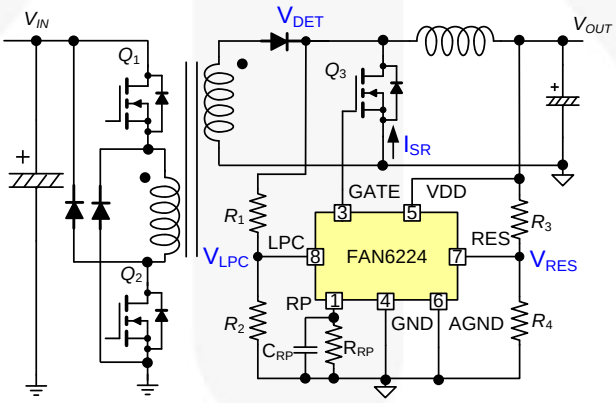


Figure 3. Forward Freewheeling Rectification

Internal Block Diagram

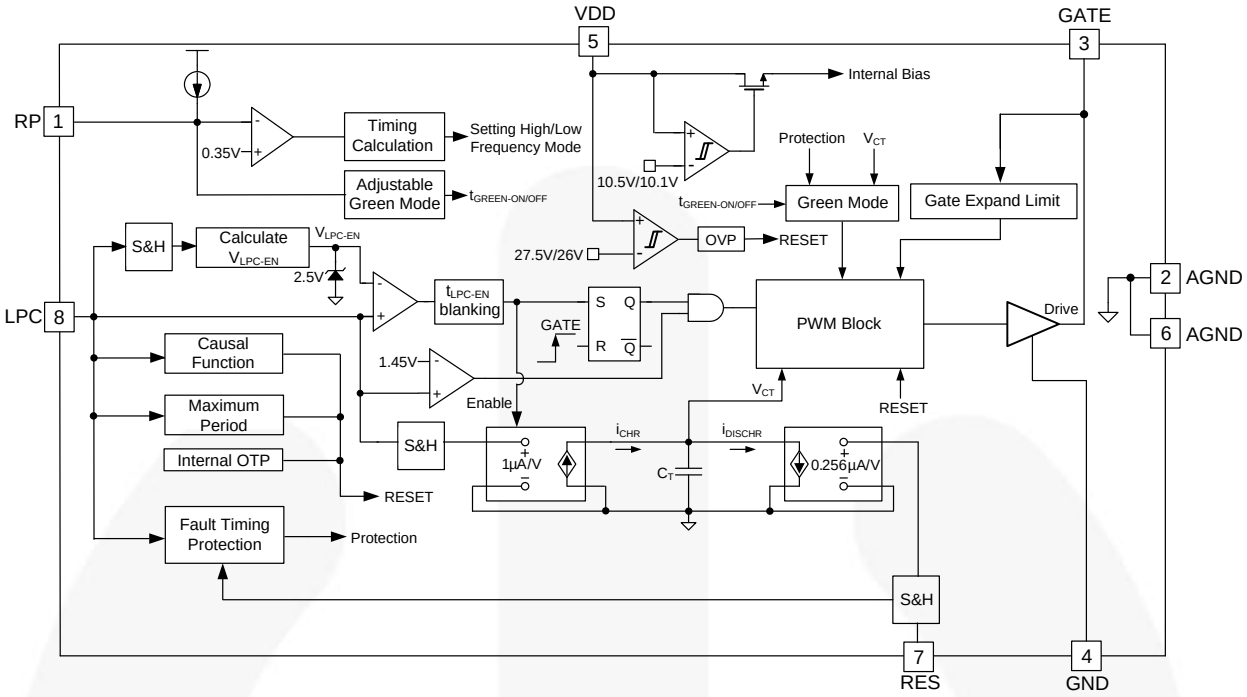
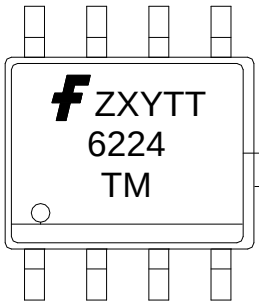


Figure 4. Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: Package Type (M = SOP)
M: Manufacturing Flow Code

Figure 5. Top Mark

Pin Configuration

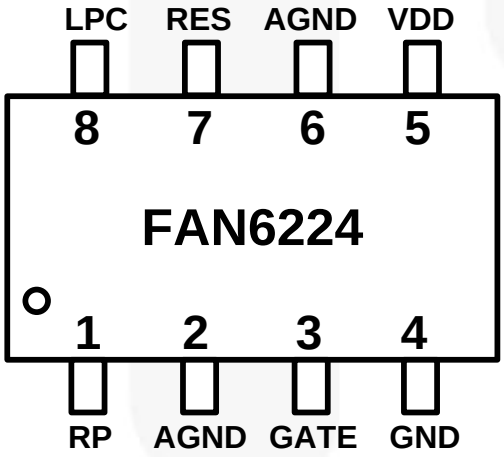


Figure 6. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	RP	**Programmable**. A resistor paralleled with a capacitor is connected to RP pin and reference ground externally. The timing to enter / exit Green Mode is programmable by the resistor, while the range of operating frequency is programmable by the capacitor.
2, 6	AGND	**Signal Ground**.
3	GATE	**Driver Output**. The totem-pole output driver for driving the power MOSFET.
4	GND	**Ground**. MOSFET source connection.
5	VDD	**Power Supply**. The threshold voltages for startup and turn-off are 10.5 V and 10.1 V, respectively.
7	RES	**Reset Control of Linear Predict**. RES pin is used to detect output voltage level through a voltage divider. An internal current source, I_{DISCHR}, is modulated by this voltage level on the RES pin.
8	LPC	**Winding Detection**. This pin is used to detect the voltage on the winding during the on-time period of the primary GATE.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage			30	V
V_{LPC}	Voltage on LPC Pin (T_A=25°C)		-0.3	7.0	V
V_{RES}	Voltage on RES Pin (Continuously in -0.5 V) (T_A=25°C)		-1.5	7.0	V
V_{RP}	Voltage on RP Pin (T_A=25°C)		-0.3	7.0	V
P_D	Power Dissipation (T_A=25°C)			0.8	W
Θ_{JA}	Thermal Resistance (Junction-to-Air)			151	°C/W
Θ_{JC}	Thermal Resistance (Junction-to-Case)			58	°C/W
T_{STG}	Storage Temperature Range		-55	150	°C
T_L	Lead Temperature (Soldering) 10s			260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		5500	V
		Charged Device Model, JESD22-C101		2000	

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{LPC}	Voltage on LPC Pin	Continuous Operation		4.8	V
V_{RES}	Voltage on RES Pin			4.8	V
V_{RP}	Voltage on RP Pin		0.5	2.5	V

Electrical Characteristics

V_{DD}=15 V and T_A=25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OP}	Continuously Operating Voltage		V_{DD-OFF}		V_{DD-OVP}	V
V_{DD-ON}	Turn-On Threshold Voltage		9.5	10.5	11.5	V
V_{DD-OFF}	Turn-Off Threshold Voltage		9.1	10.1	11.1	V
$V_{DD-HYST}$	Hysteresis Voltage for Turn-On / Turn-Off Threshold		0.1		0.7	V
I_{DD-OP}	Operating Current	V_{DD}=15 V, LPC=65 kHz, C_L=6000 pF		7	8	mA
$I_{DD-GREEN}$	Operating Current in Green Mode	V_{DD}=15 V		300	400	µA
V_{DD-OVP}	V_{DD} Over-Voltage Protection		26.0	27.5	29.0	V
$V_{DD-OVP-HYST}$	Hysteresis Voltage for V_{DD} OVP		1.1	1.5	1.9	V
$t_{VDD-OVP}$	V_{DD} OVP Debounce Time(3)			100		µs
Output Driver for internal SR Mosfet Section						
V_Z	Output Voltage Maximum (Clamp)		10	12	14	V
V_{OL}	Output Voltage LOW	V_{DD}=12 V, I_O=50 mA			0.5	V
V_{OH}	Output Voltage HIGH	V_{DD}=12 V, I_O=50 mA	9			V
t_R	Rising Time	V_{DD}=12 V, C_L=6 nF, GATE=2 V~9 V	30	70	120	ns
t_F	Falling Time	V_{DD}=12 V, C_L=6 nF, GATE=9 V~2 V	20	50	100	ns
$t_{PD\_HIGH\_LPC}$	Propagation Delay to GATE HIGH (LPC Trigger)	t_R:0%~10%, V_{DD}=12 V		150	250	ns
$t_{PD\_LOW\_LPC}$	Propagation Delay to GATE LOW (LPC Trigger(3)	t_F:100%~90%,V_{DD}=12 V		150		ns
$t_{MAX-PERIOD}$	Limitation between LPC Rising Edge to Gate Falling Edge	f_S=65 kHz	24.0	29.5	35.0	µs
		f_S=140 kHz	12.5	15.5	18.5	
LPC Section						
t_{BNK}	Blanking Time for Charging C_T(3)			150		ns
$t_{LPC-SMP}$	LPC Sampling Timing of Previous Cycle	f_S=65 kHz, R_{RP}=75 kΩ~200 kΩ, C_{RP}=100 nF	0.9	1.1	1.3	µs
		f_S=140 kHz, R_{RP}=75 kΩ~200 kΩ, C_{RP}=1 nF	0.5	0.6	0.7	µs
$V_{LPC-SOURCE}$	Lower Clamp Voltage	Source I_{LPC}=10 µA	0	0.1	0.2	V
$V_{LPC-HIGH-EN}$	Threshold Voltage for LPC to Enable SR	$V_{LPC-HIGH}$>$V_{LPC-HIGH-EN}$, SR Enable	1.38	1.45	1.54	V
$V_{EN-CLAMP}$	SR Enable Threshold Clamp Voltage(3)	V_{LPC-EN}=2.5 V at $V_{LPC-HIGH}$ >3 V		2.5		V
$V_{LPC-TH-HIGH}$	Threshold Voltage on LPC Rising Edge(3)			1.22		V
$V_{LPC-CLAMP-H}$	V_{LPC} High Clamping Voltage	V_{LPC}>$V_{LPC-CLAMP-H}$	5.7	6.2	6.7	V
$V_{LPC-DIS}$	Threshold Voltage of V_{LPC} to Disable SR Gate Switching	V_{LPC}>$V_{LPC-DIS}$	4.8		5.5	V

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Electrical Characteristics (Continued)

V_{DD}=15 V and T_A=25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RES Section						
$t_{RES-SMP}$	V_{RES} Sampling Time(3)	t_{SR_gate}=5 µs		2.5		µs
V_{RES-EN}	Threshold Voltage of V_{RES} to Enable SR Gate Switching	V_{RES}>V_{RES-EN}	1.3	1.6	2.0	V
$V_{RES-CLAMP-H}$	V_{RES} High Clamping Voltage	V_{RES}>$V_{RES-CLAMP-H}$	5.7	6.2	6.7	V
$K_{RES-DROP}$	V_{RES} Drop Protection Ratio(3)	V_{RES}[n+1]<V_{RES}[n] x $K_{RES-DROP}$		85		%
$V_{RES-SOURCE}$	V_{RES} Low Clamping Voltage	I_{RES}=10 µA, V_{DD}=15 V	0	0.2	0.4	V
Linear Prediction Section						
$Ratio_{LPC}$	Transfer Ratio of V_{LPC} to I_{LPC}(3)			1		µA/V
$Ratio_{RES}$	Transfer Ratio of V_{RES} to I_{RES}(3)			0.256		µA/V
$Ratio_{LPC-RES}$	$Ratio_{LPC}$/$Ratio_{RES}$	V_{RES}=3 V,V_{LPC}=3 V C_{RP}=100 nF	3.65	3.90	4.15	
t_{LPC-EN}	Debounce Time for V_{LPC}>V_{LPC-EN}=0.875 x $V_{LPC-HIGH}$	f_s=65 kHz, R_{RP}=75 kΩ~200 kΩ, C_{RP}=100 nF	0.9	1.1	1.3	µs
		f_s=140 kHz, R_{RP}=75 kΩ~200 kΩ, C_{RP}=1 nF	0.5	0.6	0.7	
$Ratio_{SR-LMT}$	Maximum Ratio of SR Gate On Time(3)	$Ratio_{SR-LMT}$ < t_{ON-SR}[n+1]/ t_{ON-SR}[n]		120		%
$t_{LPC-EXP-LMT}$	LPC Pulse Width Expansion Limit	$t_{LPC-EXP-LMT}$ < t_{LPC}[n+1]- t_{LPC}[n]	0.5	0.7	0.9	µs
$t_{LPC-SRK-LMT}$	LPC Pulse Width Shrink Limit	$t_{LPC-SRK-LMT}$ < t_{LPC}[n]- t_{LPC}[n+1]	0.6	0.8	1.0	µs
Green Mode Section						
$t_{GREEN-OFF}$	SR Gate On Time to Exit Green Mode	R_{RP}=200 kΩ, C_{RP}=100 nF	5.5	5.9	6.3	µs
		R_{RP}=75 kΩ,C_{RP}=1 nF	3.0	3.3	3.6	
$t_{GREEN-ON}$	SR Gate On time to Enter Green Mode	R_{RP}=200 kΩ, C_{RP}=100 nF	4.0	4.4	4.8	µs
		R_{RP}=75 kΩ,C_{RP}=1 nF	1.6	1.9	2.2	
$t_{GREEN-HYST(65kHz)}$	Hysteresis Voltage for $t_{GREEN-On}$/$t_{GREEN-Off}$ Threshold(3)	R_{RP}=200 kΩ, C_{RP}=100 nF		1.5		µs
$t_{GREEN-HYST(140kHz)}$	Hysteresis Voltage for $t_{GREEN-On}$/$t_{GREEN-Off}$ Threshold(3)	R_{RP}=75 kΩ,C_{RP}=1 nF		1.4		µs
$n_{GREEN-OFF}$	Number of Switching Cycles to Exit Green Mode(3)	SR Gate On Time > $t_{GREEN-OFF}$		15		times
$n_{GREEN-ON}$	Number of Switching Cycles to Enter Green Mode(3)	SR Gate On Time < $t_{GREEN-ON}$		3		times
$V_{RP-OPEN}$	Threshold Voltage for RP Pin Pull High Protection		3.0	3.5	4.0	V
$V_{RP-SHORT}$	Threshold Voltage for RP Pin Pull Low Protection		0.30	0.35	0.40	V

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Electrical Characteristics

V_{DD}=15 V and T_A=25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operation Frequency Setting Section						
V_{CRP-TH}	Threshold Voltage for High / Low Frequency Determination(3)	Set V_{RP}> V_{CRP-th} for Higher Operating Frequency		0.35		V
t_{CRP-TH}	Debounce Time for High / Low Frequency Determination(3)			170		µs
$I_{RP-SOURCE}$	RP Pin Source Current		8.5	9.5	10.5	µA
Casual Function Section						
$t_{DEAD-CAUSAL}$	SR Turn-Off Dead Time by Causal Function	f_S=65 kHz, (R_{RP}=75 kΩ~200 kΩ, C_{RP}=100 nF)	480	680	880	ns
		f_S=140 kHz, (R_{RP}=75 kΩ~200 kΩ, C_{RP}=1 nF)	350	500	650	ns
$t_{CAUSAL-FAULT}$	If $t_{S-PWM}(n+1) > t_{CAUSAL} x\ t_{S-PWM}(n)$, SR Stops Switching & Enters Green Mode	f_S=65 kHz to 140 kHz	130	150	170	%
t_{CAUSAL_LEAVE}	(Assume SR Triggers Fault Causal Protection) If LPC Rises Twice during t_{CAUSAL_LEAVE} and Previous On-Time of $V_{LPC-HIGH}$ is Longer than t_{LPC-EN}, then SR Leaves Fault Causal Protection(3)			5.3		µs
$t_{DEAD-CFR}$	Once CFR is Triggered, SR Terminates & Forces SR to Enter Green Mode (The Last Time from SR Gate Falling to LPC Rising)(3)	Causal Function Regulator (CFR)		70		ns
Internal Over-Temperature Protection for OTP						
T_{OTP}	Internal Threshold Temperature for OTP(3)			140		°C
$T_{OTP-HYST}$	Hysteresis Temperature for Internal OTP(3)			20		°C

Note:

3. Guarantee by Design

Typical Performance Characteristics

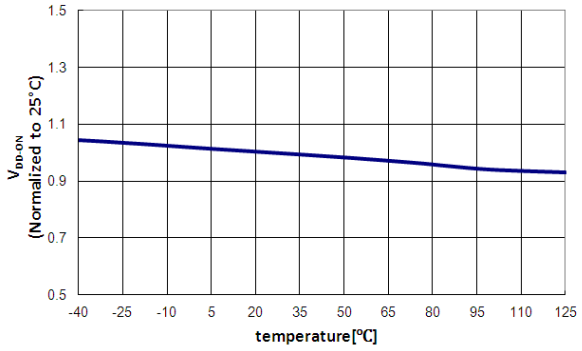


Figure 7. V_{DD-ON} vs. Temperature

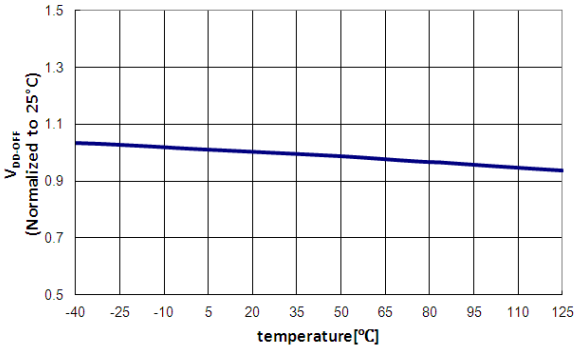


Figure 8. V_{DD-OFF} vs. Temperature

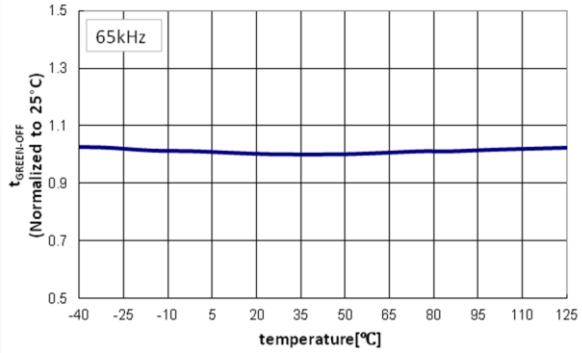


Figure 9. $t_{GREEN-OFF}$ vs. Temperature

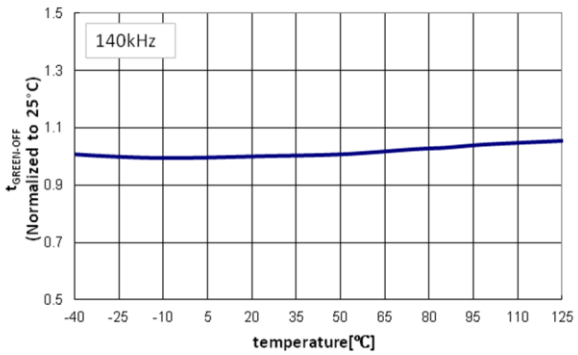


Figure 10. $t_{GREEN-OFF}$ vs. Temperature

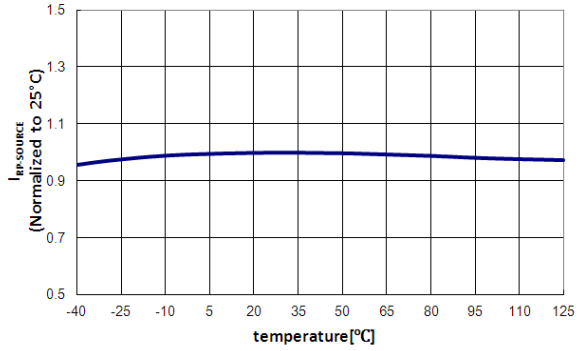


Figure 11. $I_{RP-SOURCE}$ vs. Temperature

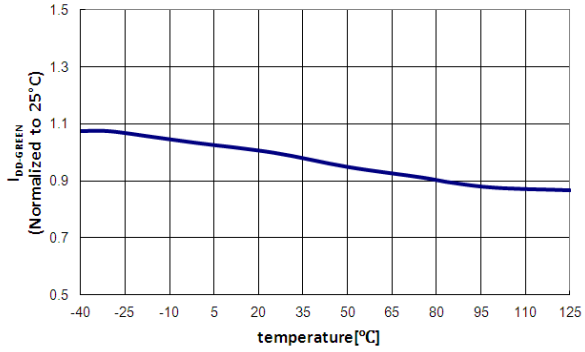


Figure 12. $I_{DD-GREEN}$ vs. Temperature

Typical Performance Characteristics (Continued)

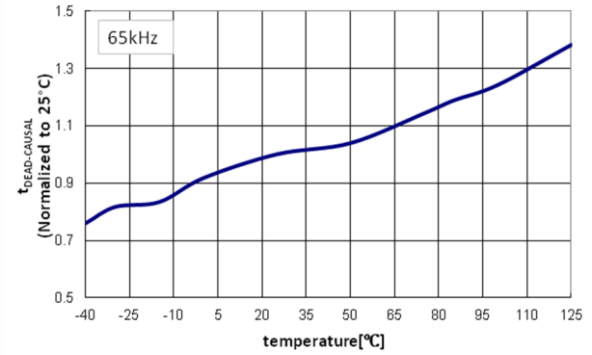


Figure 13. $t_{DEAD-CAUSAL}$ vs. Temperature

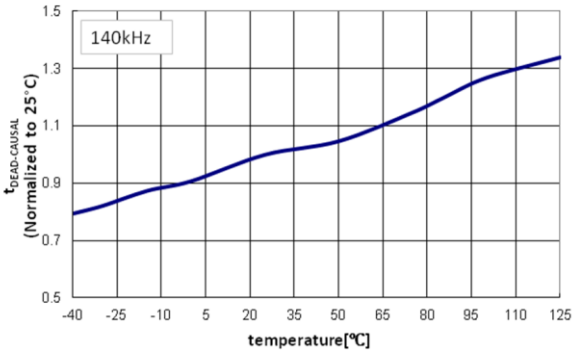


Figure 14. $t_{DEAD-CAUSAL}$ vs. Temperature

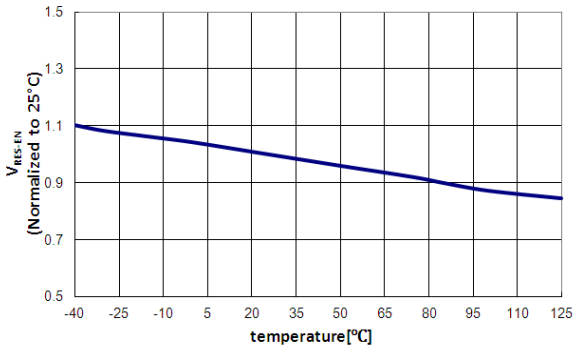


Figure 15. V_{RES-EN} vs. Temperature

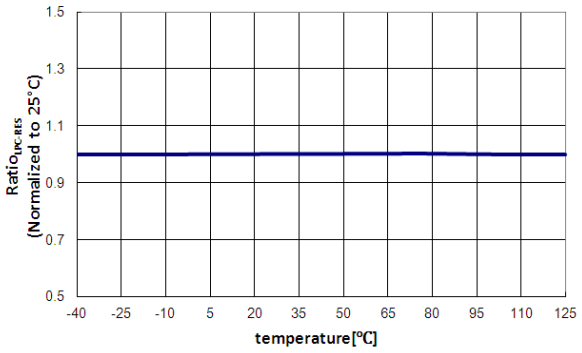


Figure 16. $Ratio_{LPC-RES}$ vs. Temperature

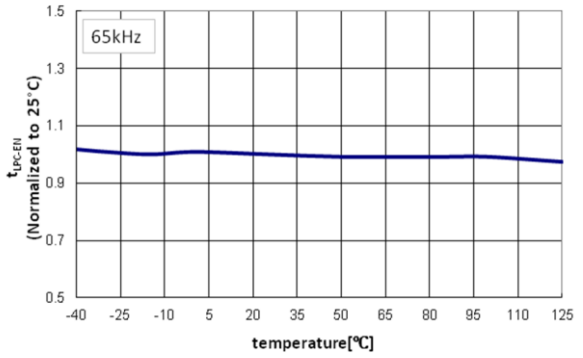


Figure 17. t_{LPC-EN} vs. Temperature

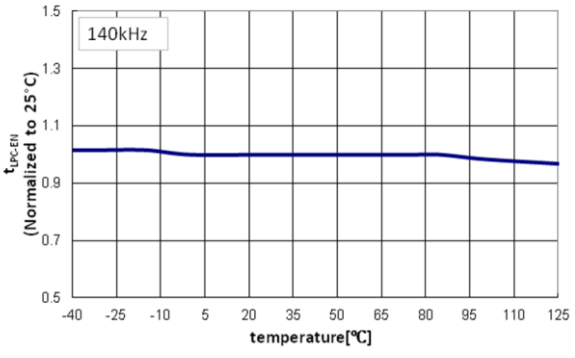


Figure 18. t_{LPC-EN} vs. Temperature

Typical Performance Characteristics (Continued)

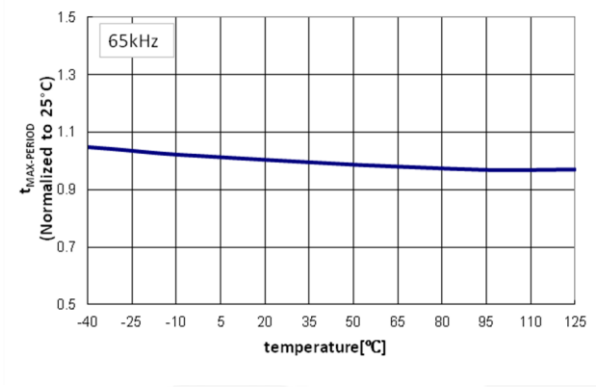


Figure 19. $t_{MAX-PERIOD}$ vs. Temperature

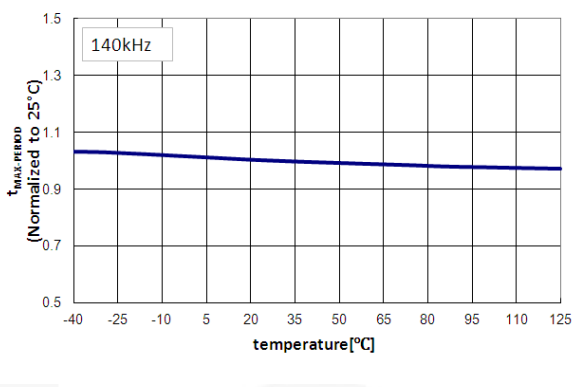


Figure 20. $t_{MAX-PERIOD}$ vs. Temperature

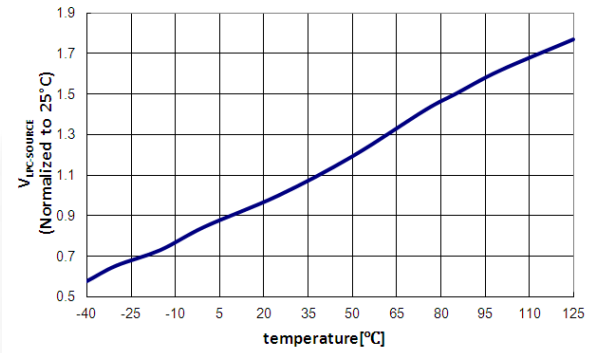


Figure 21. $V_{LPC-SOURCE}$ vs. Temperature

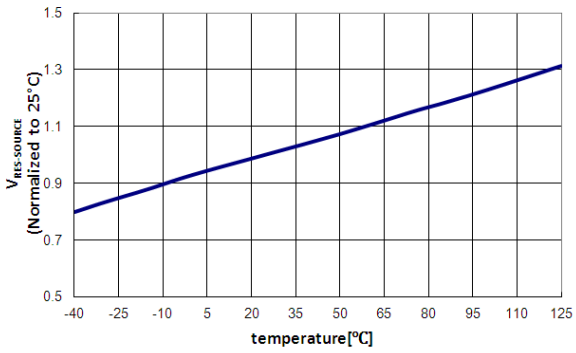


Figure 22. $V_{RES-SOURCE}$ vs. Temperature

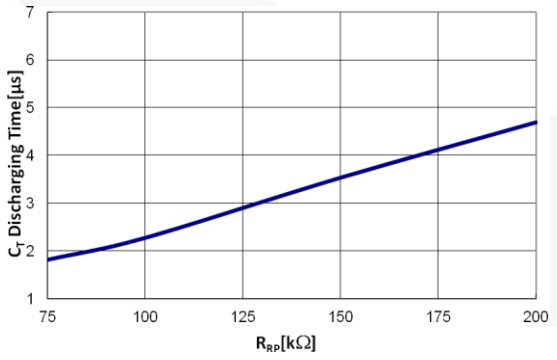


Figure 23. $t_{GREEN-ON}$ vs. R_{RP}

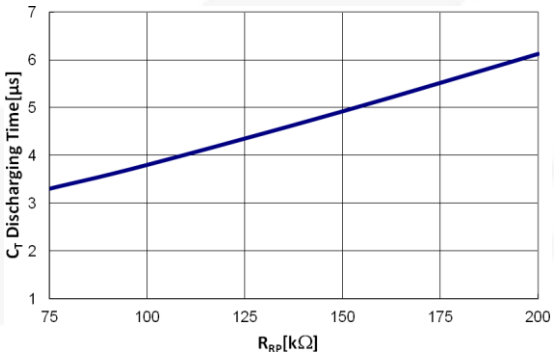


Figure 24. $t_{GREEN-OFF}$ vs. R_{RP}

Functional Description

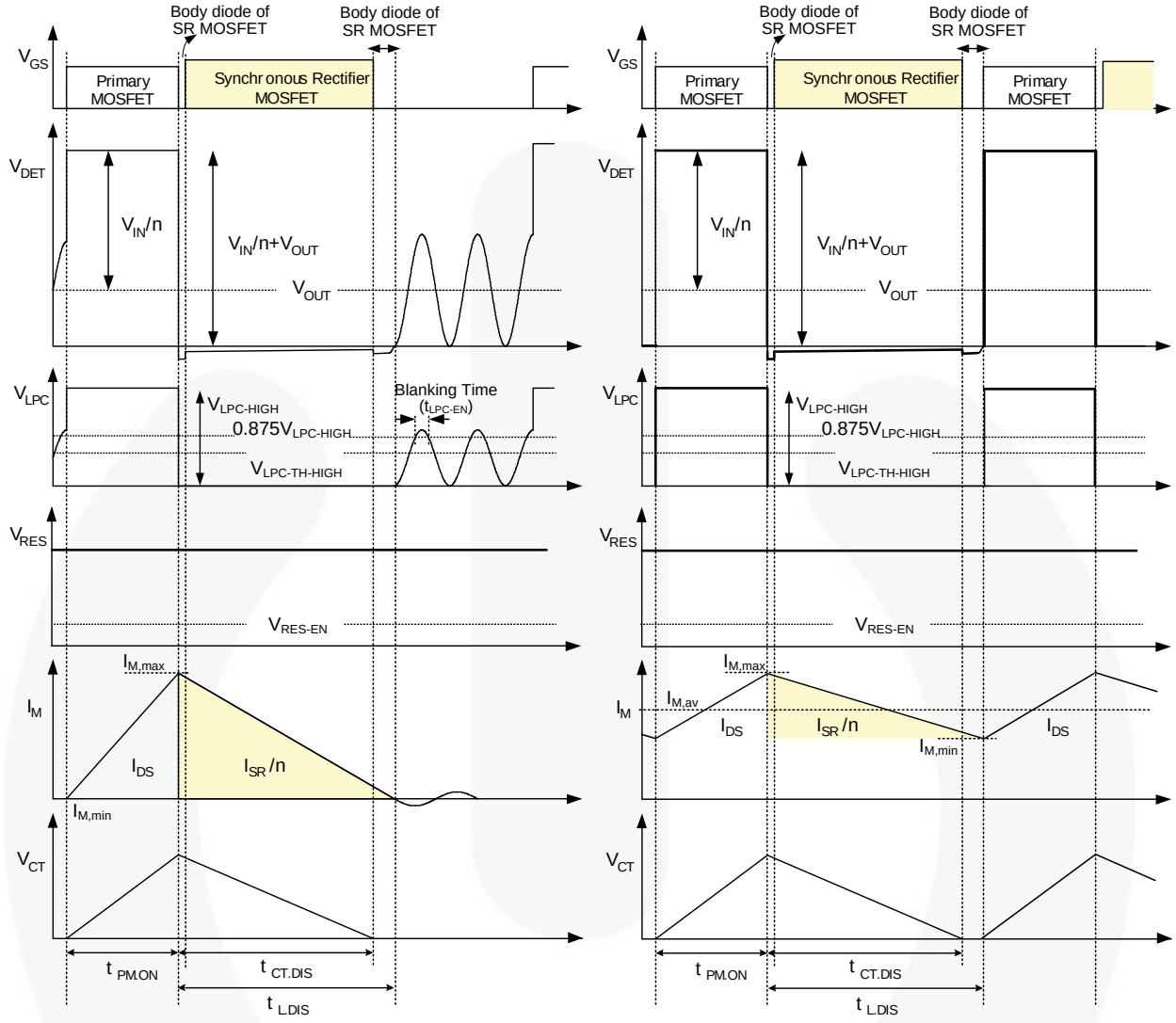


Figure 25. Waveforms of Linear-Predict Timing Control in CCM and DCM / QR Flyback for Low-Side Application

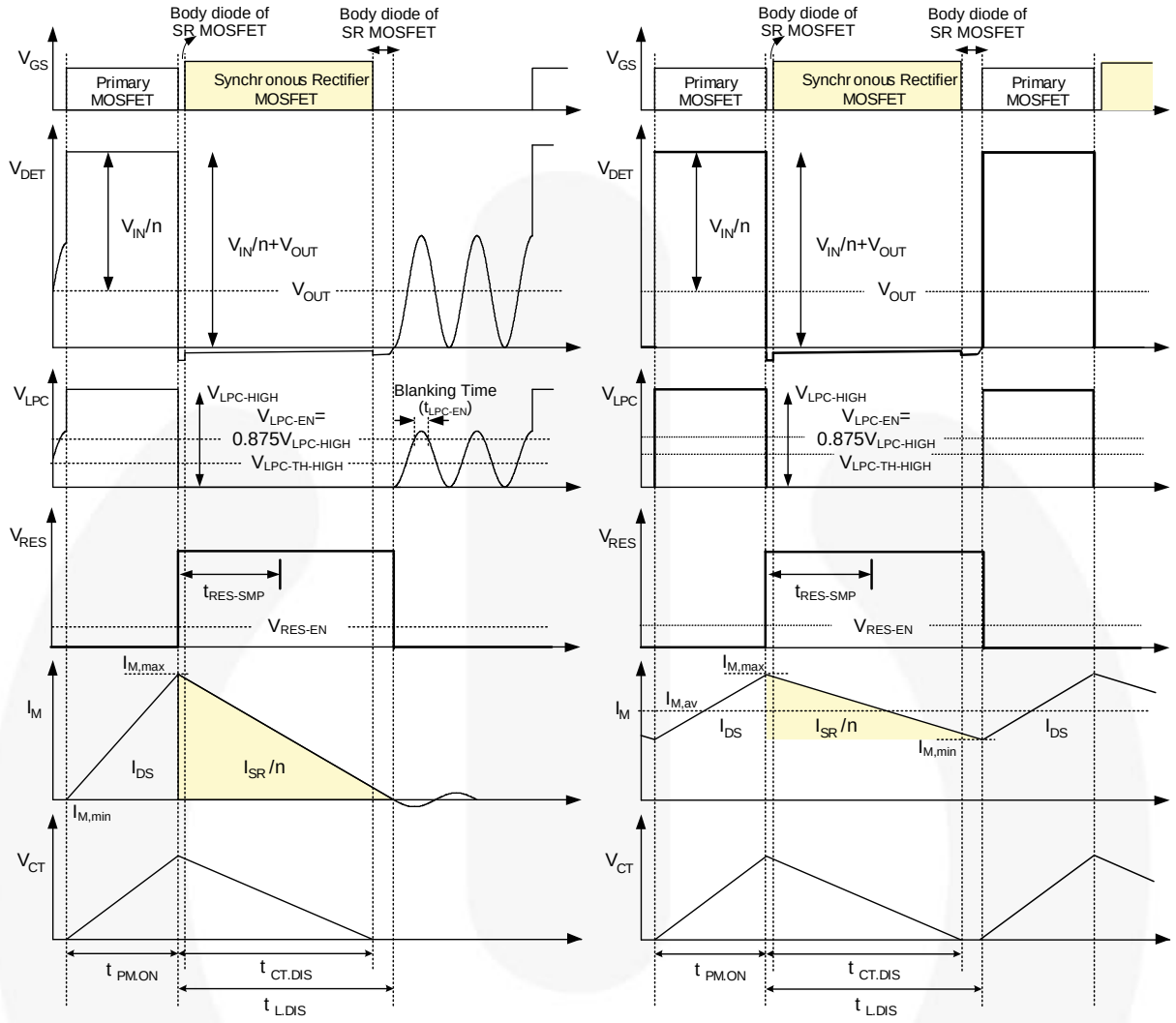


Figure 26. Waveforms of Linear-Predict Timing Control in CCM and DCM / QR Flyback for High-Side Application

Linear Predict Timing Control

The SR MOSFET turn-off timing is determined by linear-predict timing control and the operation principle is based on the volt-second balance theorem, which states: the inductor average voltage is zero during a switching period in steady state, so the charge voltage and charge time product is equal to the discharge voltage and discharge time product. In flyback converters, the charge voltage on the magnetizing inductor is input voltage (V_{IN}), while the discharge voltage is reflected output voltage (nV_{OUT}), as the typical waveforms show in Figure 25. The following equation can be drawn:

$$V_{IN} \cdot t_{PM.ON} = n \cdot V_{OUT} \cdot t_{L.DIS} \quad (1)$$

where $t_{PM,ON}$ is inductor charge time; $t_{L,DIS}$ is inductor discharge time; and n is turn ratio of primary windings (N_1) to secondary windings (N_2).

FAN6224 uses the LPC and RES pins with two sets of voltage dividers to sense DET voltage (V_{DET}) and output voltage (V_{OUT}), respectively; so V_{IN}/n, $t_{PM.ON}$, and V_{OUT} can be obtained. As a result, $t_{L,DIS}$, which is the on-time of SR MOSFET, can be predicted by Equation 1. As shown in Figure 25, the SR MOSFET is turned on when the SR MOSFET body diode starts conducting and DET voltage drops to zero. The SR MOSFET is turned off by linear-predict timing control.

Circuit Realization

The linear-predict timing-control circuit generates a replica (V_{CT}) of the magnetizing current of the flyback transformer using an internal timing capacitor (C_T), as shown in Figure 27. Using the internal capacitor voltage, the inductor discharge time ($t_{L,DIS}$) can be detected indirectly, as shown in Figure 25. When C_T is discharged to zero, the SR controller turns off the SR MOSFET.

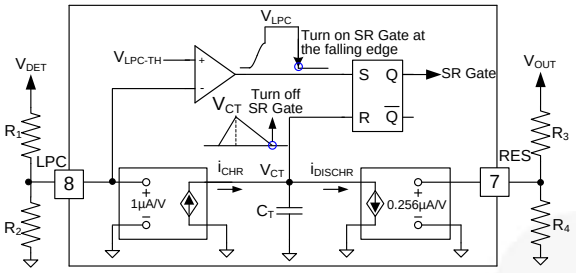


Figure 27. Simplified Linear-Predict Block

The voltage-second balance equation for the primary-side inductance of the flyback converter is given in Equation (1). Inductor current discharge time is given as:

$$t_{L.DIS} = \frac{V_{IN} \cdot t_{PM.ON}}{n \cdot V_{OUT}} \quad (2)$$

The voltage scale-down ratio between RES and LPC is defined as K below:

$$K = \frac{R_4 / (R_3 + R_4)}{R_2 / (R_1 + R_2)} \quad (3)$$

During $t_{PM.ON}$, the charge current of C_T is i_{CHR}-i_{DICHR}, while during $t_{L.DIS}$, the discharge current is i_{DICHR}. As a result, the current-second balance equation for internal timing capacitor (C_T) can be derived from:

$$(\frac{3.9}{K} \cdot (\frac{V_{IN}}{n} + V_{OUT}) - V_{OUT}) \cdot t_{PM.ON} = V_{OUT} \cdot t_{CT.DIS} \quad (4)$$

Therefore, the discharge time of C_T is given as:

$$t_{CT.DIS} = \frac{(\frac{3.9}{K} \cdot (\frac{V_{IN}}{n} + V_{OUT}) - V_{OUT}) \cdot t_{PM.ON}}{V_{OUT}} \quad (5)$$

When the voltage scale-down ratio between LPC and RES (K) is 3.9, the discharge time of C_T ($t_{CT.DIS}$) is the same as inductor current discharge time ($t_{L.DIS}$). However, considering the tolerance of voltage divider resistors and internal circuit, the scale-down ratio (K) should be larger than 3.9 to guarantee that $t_{CT.DIS}$ is shorter than $t_{L.DIS}$. It is typical to set K around 4.0~4.5.

Referring to Figure 25, when LPC voltage is higher than V_{LPC-EN} over a period of blanking time (t_{LPC-EN}) and lower than $V_{LPC-TH-HIGH}$ (1.22 V), then SR MOSFET can be triggered. Therefore, V_{LPC-EN} must be lager than $V_{LPC-TH-HIGH}$ or the SR MOSFET cannot be turned on. As a result, when designing the voltage divider of the LPC, considering the tolerance, R_1 and R_2 should satisfy the equation:

$$\frac{R_2}{R_1 + R_2} \cdot (\frac{V_{IN.MIN}}{n} + V_{OUT}) > 1.54 \quad (6)$$

On the other hand, there is also a threshold voltage, V_{RES-EN}, for RES pin to enable SR switching, hence R_3 and R_4 must satisfy:

$$\frac{R_3}{R_3 + R_4} \cdot V_{OUT} > 2 \quad (7)$$

In addition, considering the linear operating range, LPC and RES voltage should be under 4.8 V, and therefore:

$$\frac{R_2}{R_1 + R_2} \cdot (\frac{V_{IN.MAX}}{n} + V_{OUT}) < 4.8 \quad (8)$$

$$\frac{R_4}{R_3 + R_4} \cdot V_{OUT} < 4.8 \quad (9)$$

For high-side applications, as shown in Figure 2, an extra auxiliary winding (N_3) is used to supply voltage for controller. To detect output voltage, the RES pin is connected to the auxiliary winding through a set of voltage dividers. As Figure 26 shows, V_{RES} is proportional to V_{OUT} when SR MOSFET or its body diode conducts. Therefore, information of V_{OUT} is sampled at $t_{RES-SMP}$ after the primary-side MOSFET turns off. As a result, Equation (4) can be rewritten as:

$$(\frac{3.9}{K \cdot n'} \cdot (\frac{V_{IN}}{n} + V_{OUT}) - V_{OUT}) \cdot t_{PM.ON} = V_{OUT} \cdot t_{CT.DIS} \quad (10)$$

where n' is the turn ratio of auxiliary windings (N_3) to secondary windings (N_2).

The discharge time of C_T can be obtained as:

$$t_{CT.DIS} = \frac{(\frac{3.9}{K \cdot n'} \cdot (\frac{V_{IN}}{n} + V_{OUT}) - V_{OUT}) \cdot t_{PM.ON}}{V_{OUT}} \quad (11)$$

Therefore, when the voltage scale-down ratio (K) and turn ratio (n') product is 3.9; the discharge time, $t_{CT.DIS}$, is the same as inductor current discharge time, $t_{L.DIS}$. To guarantee $t_{CT.DIS}$ is shorter than $t_{L.DIS}$, the K and n' product should be larger than 3.9. It is typical to set the product around 4.0~4.5. When designing the voltage divider of LPC, the consideration is the same as that of low-side application, which means that the linear operating range, Equations (6) and (8) must be satisfied. However, when determining the voltage divider of RES, note that turn ratio n' must be taken into consideration and so that Equation (7) and (9) are modified as:

$$\frac{R_4}{R_3 + R_4} \cdot n' \cdot V_{OUT} > 2 \quad (12)$$

$$\frac{R_4}{R_3 + R_4} \cdot n' \cdot V_{OUT} < 4.8 \quad (13)$$

CCM Operation

The typical waveforms of CCM operation in steady state are shown as right side of Figure 25 and Figure 26. When the primary-side MOSFET is turned on, the energy is stored in L_m. During the on-time of the primary-side MOSFET ($t_{PM.ON}$), the magnetizing current (I_M) increases linearly from $I_{M,min}$ to $I_{M,max}$. Meanwhile, internal timing capacitor (C_T) is charged by current source (i_{CHR}-i_{DICHR}) proportional to V_{IN}, so V_{CT} also increases linearly.

When the primary-side MOSFET is turned off, the energy stored in L_m is released to the output. During the inductor discharge time ($t_{L.DIS}$), the magnetizing current (I_M) decreases linearly from $I_{M,max}$ to $I_{M,min}$. At the same time, the internal timing capacitor (C_T) is discharged by current source (i_{DISCHR}) proportional to V_{OUT}, so V_{CT} also decreases linearly. To guarantee the proper operation of SR, it is important to turn off the SR MOSFET just before SR current reaches $I_{M,min}$ so that the body diode of the SR MOSFET is naturally turned off.

DCM / QR Operation

In DCM / QR operation, when primary-side MOSFET is turned off, the energy stored in L_m is fully released to the output at the turn-off timing of primary-side MOSFET. Therefore, the DET voltage continues resonating until the primary-side MOSFET is turned on, as depicted in Figure 25. While DET voltage is resonating, DET voltage and LPC voltage drop to zero by resonance, which can trigger the turn-on of the SR MOSFET. To prevent fault triggering of the SR MOSFET in DCM operation, a blanking time is introduced to LPC voltage. The SR MOSFET is not turned on even when LPC voltage drops below $V_{LPC-TH-HIGH}$ unless LPC voltage stays above 0.875 $V_{LPC-HIGH}$ longer than the blanking time (t_{LPC-EN}). The turn-on timing of the SR MOFET is inhibited by gate inhibit time ($t_{INHIBIT}$), once the SR MOSFET turns off, to prevent fault triggering.

mWSaver™ Technology

Green-Mode Operation

To minimize the power consumption at light-load condition, the SR circuit is disabled when the load decreases. As illustrated in Figure 28, the discharge times of the inductor and internal timing capacitor decrease as load decreases. If the discharge time of the internal timing capacitor ($t_{CT.DIS}$) is shorter than $t_{GREEN-ON}$ for more than three cycles, then the SR circuit enters Green Mode. Once FAN6224 enters Green Mode, the SR MOSFET stops switching and the major internal block is shut down to further reduce the operating current of the SR controller. In Green Mode, the operating current reduces to 300 µA. This allows power supplies to meet stringent power conservation requirements. When the discharge time of the internal capacitor is longer than $t_{GREEN-OFF}$ for more than fifteen cycles, the SR circuit is enabled and resumes the normal operation, as shown in Figure 29.

To enhance flexibility of design, $t_{GREEN-ON}$ and $t_{GREEN-OFF}$ are adjustable by the external resistor of the RP pin within a certain range. As shown in Figure 30, larger R_{RP} resistance corresponds to longer $t_{GREEN-ON}$ and $t_{GREEN-OFF}$, and vice versa. Therefore, by setting different resistance of R_{RP}, the loading of entering and exiting Green Mode is adjustable.

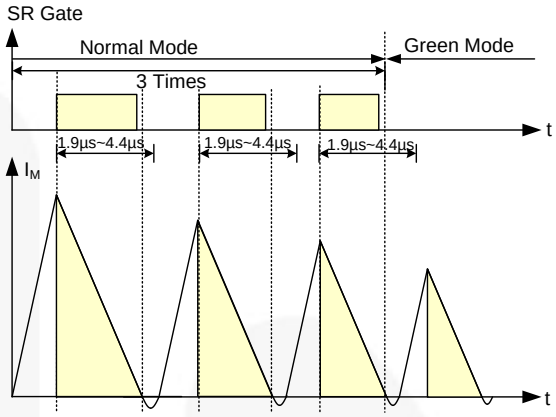


Figure 28. Entering Green Mode

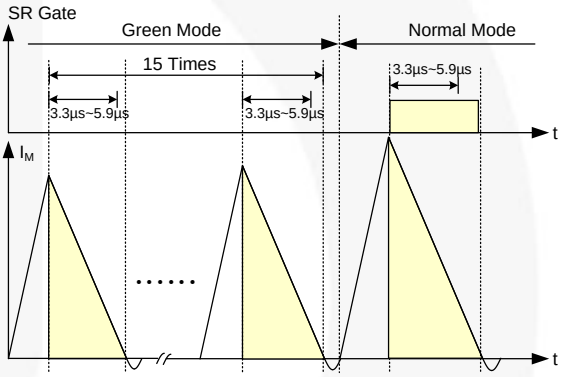


Figure 29. Resuming Normal Operation

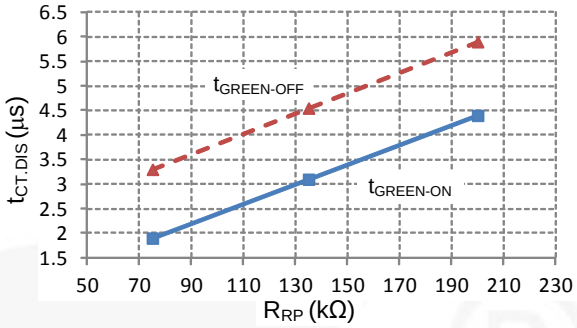


Figure 30. Adjustable $t_{GREEN-ON}$ and $t_{GREEN-OFF}$

Selection of Operating Frequency

For different operating frequency range, internal parameters of the SR controller should be different to optimize signal processing. The capacitor of the RP pin (C_{RP}) is used to determine the operating frequency range of the SR controller. For low switching frequency systems (<100 kHz), C_{RP} is recommended as 100 nF; for high switching frequency systems (100k~140 kHz), C_{RP} is recommended as 1nF.

Causal Function

Causal function is utilized to limit the time interval (t_{SR-MAX}) from the rising edge of V_{LPC} to the falling edge of the SR Gate. As shown in Figure 31, t_{SR-MAX} is limited to previous switching period (t_{S-PWM}) minus a dead time, say $t_{DEAD-CAUSAL}$. When the system operates at fixed frequency, whether voltage-second balance theorem can be applied or not, causal function can guarantee reliable operation.

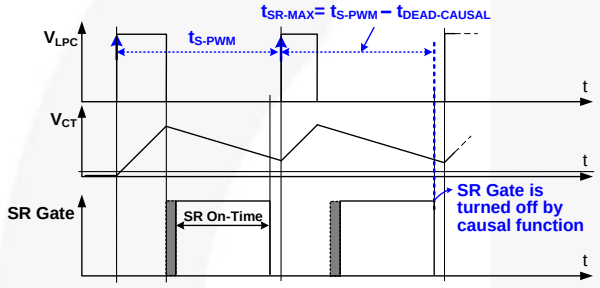


Figure 31. Causal Function Operation

Fault Causal Timing Protection

Fault causal timing protection is utilized to disable the SR Gate under some abnormal conditions. Once the switching period ($t_{S-PWM}[n]$) is longer than 150% of previous switching period ($t_{S-PWM}[n-1]$), the SR Gate is disabled and enters Green Mode, as shown in Figure 32. Since the rising edge of V_{LPC} among switching periods (t_{S-PWM}) is tracked for causal function, the accuracy of switching period is important. Therefore, if the detected switching period has a serious variation, the SR Gate is terminated to prevent fault trigger.

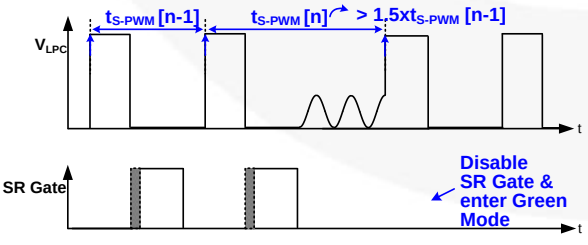


Figure 32. Fault Causal Timing Protection

Gate Expansion Limit Protection

Gate expansion limit protection controls the on-time expansion of the SR MOSFET. Once the discharge time of the internal timing capacitor ($t_{DIS.CT}$) is longer than 120% of the previous on-time of the SR MOSFET ($t_{on-SR}[n-1]$); $t_{on-SR}[n]$ is limited to 120% of $t_{on-SR}[n-1]$, as shown in Figure 33. When output load changes rapidly from light load to heavy load, voltage-second balance theorem may not be applied. In this transient state, gate expand limit protection is activated to prevent overlap between the SR Gate and the PWM gate.

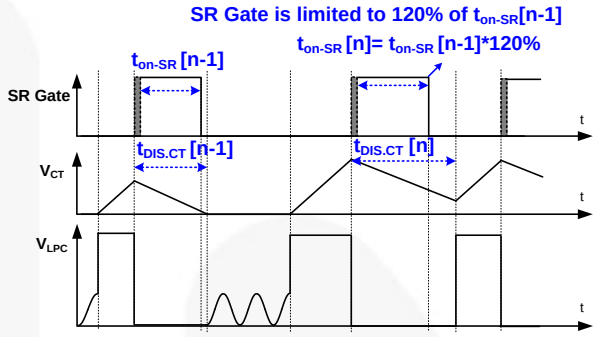


Figure 33. Gate Expand Limit Protection

RES Dropping Protection

RES dropping protection prevents V_{RES} dropping too much within a cycle. The V_{RES} is sampled as a reference voltage, V_{RES}', on V_{LPC} rising edge. Once V_{RES} drops below 85% of V_{RES}', the SR Gate is turned off immediately, as shown in Figure 34. When output voltage drops rapidly within a switching cycle, voltage-second balance may not be applied; RES dropping protection is activated to prevent overlap.

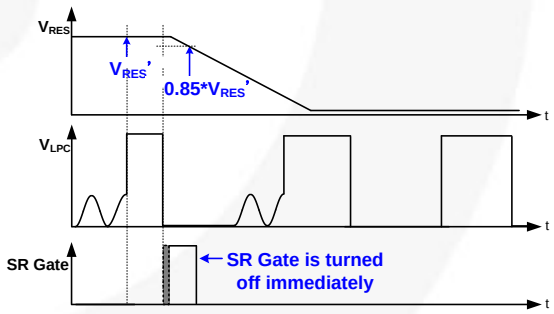


Figure 34. V_{RES} Dropping Protection

LPC Width Expansion / Shrink Protection

LPC width expansion and shrink protection is utilized to disable the SR MOSFET switching under some abnormal conditions. As Figure 35 shows, once the LPC pulse width ($t_{LPC}[n]$) is longer than that of previous cycle ($t_{LPC}[n-1]$) for $t_{LPC-EXP-LMT}$, the LPC width expansion protection is triggered and SR MOSFET switching is terminated immediately. Figure 36 shows the timing diagram of LPC width shrink protection. Once $t_{LPC}[n]$ is shorter than $t_{LPC}[n-1]$, the SR MOSFET switching also shuts down immediately.

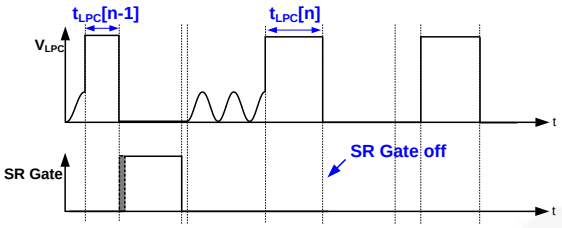


Figure 35. V_{LPC} Width Expand Protection

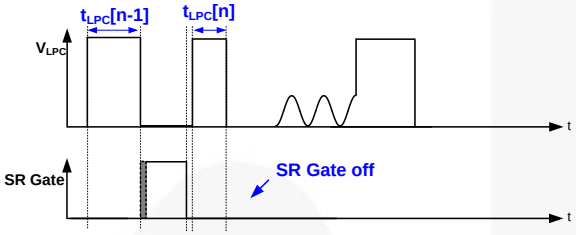


Figure 36. V_{LPC} Width Shrink Protection

LPC Pin Open / Short Protection

LPC-Open Protection: If V_{LPC} is higher than $V_{LPC-DIS}$ for longer than debounce time $t_{LPC-HIGH}$, FAN6224 stops switching immediately and enters Green Mode. V_{LPC} is clamped at 6.2 V to avoid LPC pin damage.

LPC-Short Protection: If V_{LPC} is pulled to ground and the charging current of timing capacitor (C_T) is near zero, SR Gate is not output.

RES Pin Open / Short Protection

RES-Open Protection: If V_{RES} is pulled to HIGH level, the gate signal is extremely small and FAN6224 enters Green Mode. In addition, V_{RES} is clamped at 6.2 V to avoid RES pin damage.

RES-Short Protection: If V_{RES} is lower than V_{RES-EN} (1.6 V), FAN6224 stops switching immediately and enters Green Mode.

Under-Voltage Lockout (UVLO)

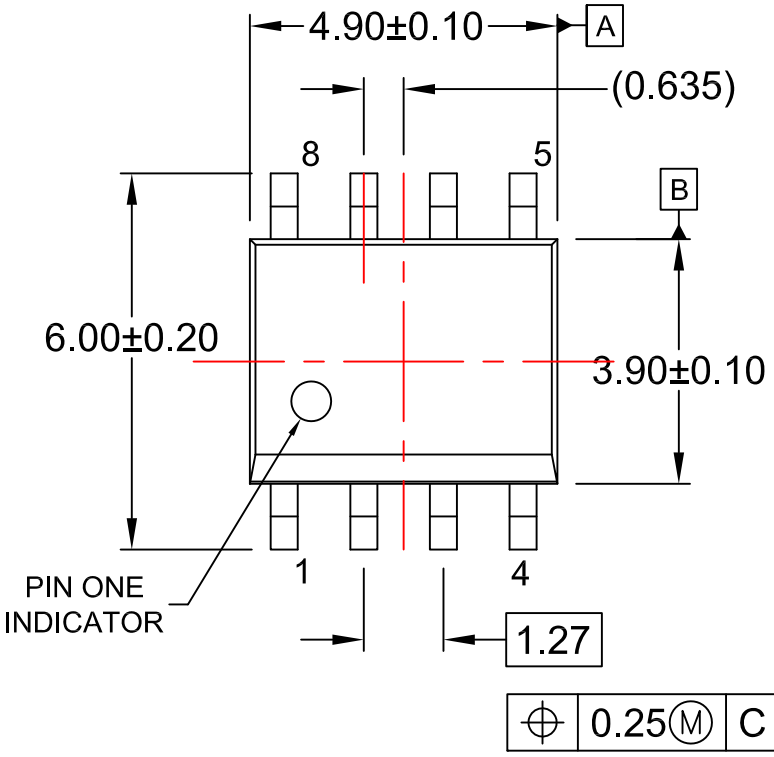
The power ON and OFF V_{DD} threshold voltages are fixed at 10.5 V and 10.1 V, respectively. The FAN6224 can be used in various output voltage applications.

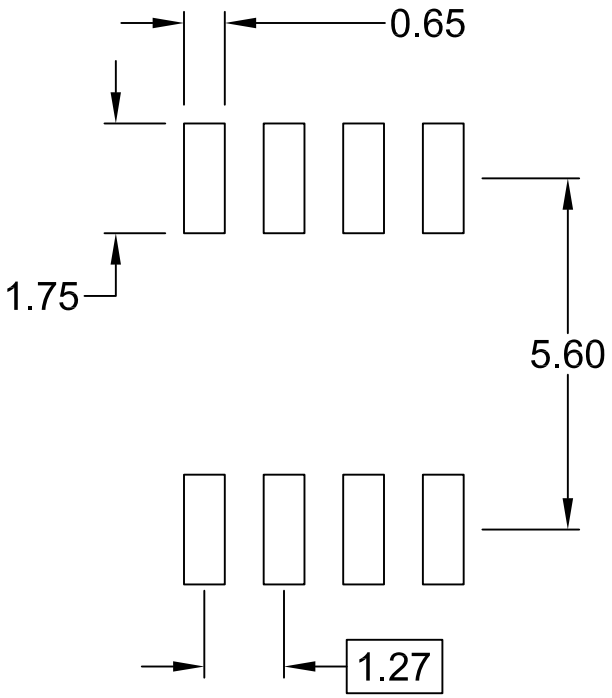
V_{DD} Pin Over-Voltage Protection (OVP)

Over-voltage conditions are usually caused by an open feedback loop. V_{DD} over-voltage protection prevents damage to the SR MOSFET. When the voltage on the VDD pin exceeds 27.5 V, the SR controller stops switching the SR MOSFET.

Over-Temperature Protection (OTP)

To prevent the SR Gate from fault triggering in high temperatures, internal over-temperature protection is integrated in FAN6224. If the temperature is over 140°C, the SR Gate is disabled until the temperature drops below 120°C.





LAND PATTERN RECOMMENDATION

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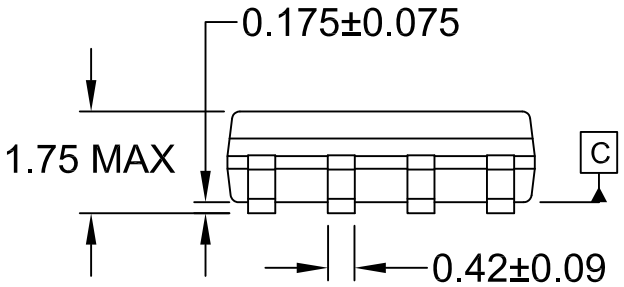
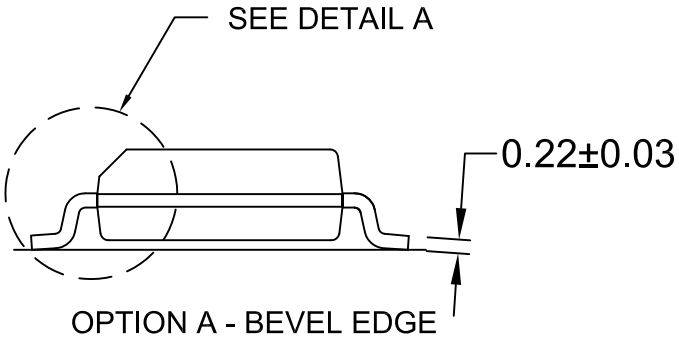
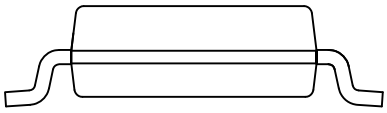


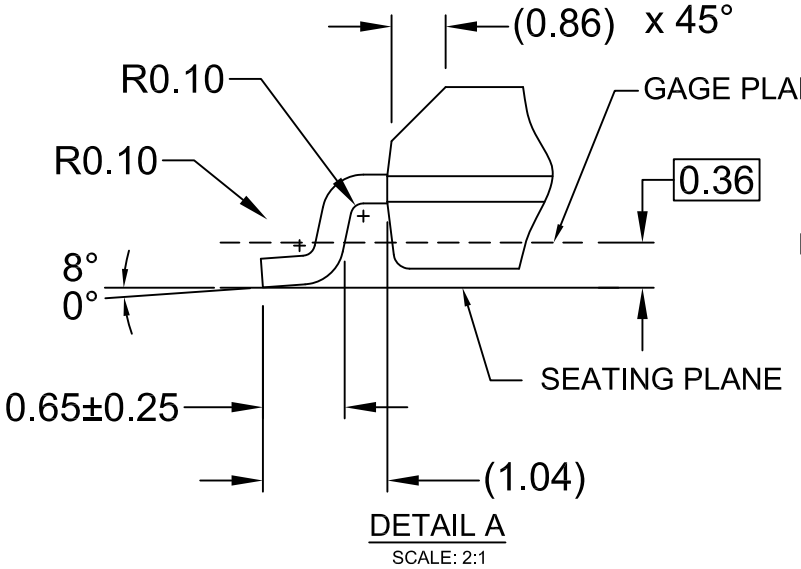
⌓	0.10



OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

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A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
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