GENERAL DESCRIPTION

The XRT86VL34 is a four-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy). The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VL34 provides protection from power failures and hot swapping.

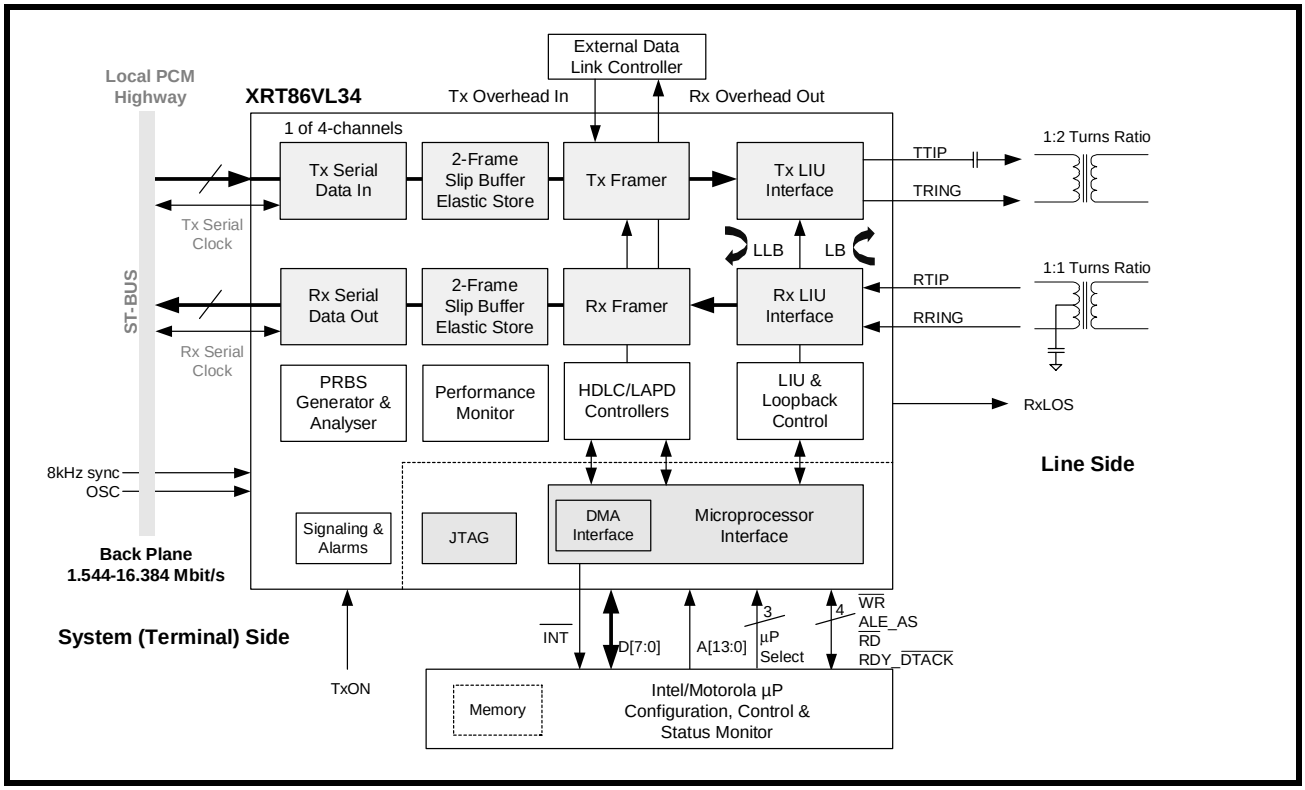
The XRT86VL34 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86VL34 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86VL34 4-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Four independent, full duplex DS1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers per channel for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.

- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core
- 3.3V CMOS operation with 5V tolerant inputs
- 225-pin PBGA package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL34IB	225 Plastic Ball Grid Array	-40°C to +85°C

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DESCRIPTION OF THE CONTROL REGISTERS - E1 MODE

All address on this register description is shown in HEX format, where n indicates channels 0-3 in the 4-channel device.

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Control Registers (0xn100 - 0xn1FF)		
Clock and Select Register	CSR	0xn100
Line Interface Control Register	LICR	0xn101
Reserved	-	0xn102 - 0xn106
Framing Select Register	FSR	0xn107
Alarm Generation Register	AGR	0xn108
Synchronization MUX Register	SMR	0xn109
Transmit Signaling and Data Link Select Register	TSDLSR	0xn10A
Framing Control Register	FCR	0xn10B
Receive Signaling & Data Link Select Register	RSDLSR	0xn10C
Receive Signaling Change Register 0	RSCR0	0xn10D
Receive Signaling Change Register 1	RSCR1	0xn10E
Receive Signaling Change Register 2	RSCR2	0xn10F
Receive Signaling Change Register 3	RSCR3	0xn110
Receive National Bits Register	RNBR	0xn111
Receive Extra Bits Register	REBR	0xn112
Data Link Control Register 1	DLCR1	0xn113
Transmit Data Link Byte Count Register 1	TDLBCR1	0xn114
Receive Data Link Byte Count Register 1	RDLBCR1	0xn115
Slip Buffer Control Register	SBCR	0xn116
FIFO Latency Register	FIFOLR	0xn117
DMA 0 (Write) Configuration Register	D0WCR	0xn118
DMA 1 (Read) Configuration Register	D1RCR	0xn119
Interrupt Control Register	ICR	0xn11A
LAPD Select Register	LAPDSR	0xn11B
Reserved - T1 mode only	-	0xn11C
Performance Report Control Register	PRCR	0xn11D
Gapped Clock Control Register	GCCR	0xn11E
Transmit Interface Control Register	TICR	0xn120
PRBS Control & Status Register 0	PRBSCSR0	0xn121

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Receive Interface Control Register	RICR	0xn122
PRBS Control & Status Register 1	PRBSCSR1	0xn123
For T1 mode only	-	0xn124 - 0xn127
Defect Detection Enable Register	DDER	0xn129
Transmit Sa Select Register	TSASR	0xn130
Transmit Sa Auto Control Register 1	TSACR1	0xn131
Transmit Sa Auto Control Register 2	TSACR2	0xn132
Transmit Sa4 Register	TSA4R	0xn133
Transmit Sa5 Register	TSA5R	0xn134
Transmit Sa6 Register	TSA6R	0xn135
Transmit Sa7 Register	TSA7R	0xn136
Transmit Sa8 Register	TSA8R	0xn137
Receive Sa4 Register	RSA4R	0xn13B
Receive Sa5 Register	RSA5R	0xn13C
Receive Sa6 Register	RSA6R	0xn13D
Receive Sa7 Register	RSA7R	0xn13E
Receive Sa8 Register	RSA8R	0xn13F
Reserved - T1 mode only	-	0xn142
Data Link Control Register 2	DLCR2	0xn143
Transmit Data Link Byte Count Register 2	TDLBCR2	0xn144
Receive Data Link Byte Count Register 2	RDLBCR2	0xn145
Data Link Control Register 3	DLCR3	0xn153
Transmit Data Link Byte Count Register 3	TDLBCR3	0xn154
Receive Data Link Byte Count Register 3	RDLBCR3	0xn155
Device ID Register	DEVID	0xn1FE
Revision Number Register	REVID	0xn1FF
Time Slot (payload) Control (0xn300 - 0xn3FF)		
Transmit Channel Control Register 0-31	TCCR 0-31	0xn300 - 0xn31F
User Code Register 0-31	TUCR 0-31	0xn320 - 0xn33F
Transmit Signaling Control Register 0 -31	TSCR 0-31	0xn340 - 0xn35F

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Receive Channel Control Register 0-31	RCCR 0-31	0xn360 - 0xn37F
Receive User Code Register 0-31	RUCR 0-31	0xn380 - 0xn39F
Receive Signaling Control Register 0-31	RSCR 0-31	0xn3A0 - 0xn3BF
Receive Substitution Signaling Register 0-31	RSSR 0-31	0xn3C0 - 0xn3DF
Receive Signaling Array (0xn500 - 0xn51F)		
Receive Signaling Array Register 0	RSAR0-31	0xn500 - 0xn51F
LAPDn Buffer 0		
LAPD Buffer 0 Control Register	LAPDBCR0	0xn600 - 0xn660
LAPDn Buffer 1		
LAPD Buffer 1 Control Register	LAPDBCR1	0xn700 - 0xn760
Performance Monitor		
Receive Line Code Violation Counter: MSB	RLCVCU	0xn900
Receive Line Code Violation Counter: LSB	RLCVCL	0xn901
Receive Frame Alignment Error Counter: MSB	RFAECU	0xn902
Receive Frame Alignment Error Counter: LSB	RFAECL	0xn903
Receive Severely Errored Frame Counter	RSEFC	0xn904
Receive Synchronization Bit (CRC-6 (T1) CRC-4 (E1) Block) Error Counter: MSB	RSBBECU	0xn905
Receive Synchronization Bit (CRC-6 (T1) CRC-4 (E1) Block) Error Counter: LSB	RSBBECL	0xn906
Receive Far-End Block Error Counter: MSB	RFEBECU	0xn907
Receive Far-End Block Error Counter: LSB	RFEBECL	0xn908
Receive Slip Counter	RSC	0xn909
Receive Loss of Frame Counter	RLFC	0xn90A
Receive Change of Frame Alignment Counter	RCFAC	0xn90B
LAPD Frame Check Sequence Error counter 1	LFCSEC1	0xn90C
PRBS bit Error Counter: MSB	PBECU	0xn90D
PRBS bit Error Counter: LSB	PBECL	0xn90E
Transmit Slip Counter	TSC	0xn90F

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Excessive Zero Violation Counter: MSB	EZVCU	0xn910
Excessive Zero Violation Counter: LSB	EZVCL	0xn911
LAPD Frame Check Sequence Error counter 2	LFCSEC2	0xn91C
LAPD Frame Check Sequence Error counter 3	LFCSEC3	0xn92C
Interrupt Generation/Enable Register Address Map (0xnB00 - 0xnB41)		
Block Interrupt Status Register	BISR	0xnB00
Block Interrupt Enable Register	BIER	0xnB01
Alarm & Error Interrupt Status Register	AEISR	0xnB02
Alarm & Error Interrupt Enable Register	AEIER	0xnB03
Framer Interrupt Status Register	FISR	0xnB04
Framer Interrupt Enable Register	FIER	0xnB05
Data Link Status Register 1	DLSR1	0xnB06
Data Link Interrupt Enable Register 1	DLIER1	0xnB07
Slip Buffer Interrupt Status Register	SBISR	0xnB08
Slip Buffer Interrupt Enable Register	SBIER	0xnB09
Receive Loopback code Interrupt and Status Register	RLCISR	0xnB0A
Receive Loopback code Interrupt Enable Register	RLCIER	0xnB0B
Receive SA (Sa6) Interrupt Status Register	RSAISR	0xnB0C
Receive SA (Sa6) Interrupt Enable Register	RSAIER	0xnB0D
Excessive Zero Status Register	EXZSR	0xnB0E
Excessive Zero Enable Register	EXZER	0xnB0F
Reserved - T1 mode only	-	0xnB10 - 0xnB11
RxLOS/CRC Interrupt Status Register	RLCISR	0xnB12
RxLOS/CRC Interrupt Enable Register	RLCIER	0xnB13
Data Link Status Register 2	DLSR2	0xnB16
Data Link Interrupt Enable Register 2	DLIER2	0xnB17
Reserved - T1 mode only	-	0xnB18 - 0xnB19
Data Link Status Register 3	DLSR3	0xnB26
Data Link Interrupt Enable Register 3	DLIER3	0xnB27
Reserved - T1 mode only	-	0xnB28 - 0xnB29
Reserved - T1 mode only	CIAIER	0xnB40 - 0xnB41
LIU Register Summary - Channel Control Registers		
LIU Channel Control Register 0	LIUCCR0	0x0Fn0

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
LIU Channel Control Register 1	LIUCCR1	0x0Fn1
LIU Channel Control Register 2	LIUCCR2	0x0Fn2
LIU Channel Control Register 3	LIUCCR3	0x0Fn3
LIU Channel Control Interrupt Enable Register	LIUCCIER	0x0Fn4
LIU Channel Control Status Register	LIUCCSR	0x0Fn5
LIU Channel Control Interrupt Status Register	LIUCCISR	0x0Fn6
LIU Channel Control Cable Loss Register	LIUCCCCR	0x0Fn7
LIU Channel Control Arbitrary Register 1	LIUCCAR1	0x0Fn8
LIU Channel Control Arbitrary Register 2	LIUCCAR2	0x0Fn9
LIU Channel Control Arbitrary Register 3	LIUCCAR3	0x0FnA
LIU Channel Control Arbitrary Register 4	LIUCCAR4	0x0FnB
LIU Channel Control Arbitrary Register 5	LIUCCAR5	0x0FnC
LIU Channel Control Arbitrary Register 6	LIUCCAR6	0x0FnD
LIU Channel Control Arbitrary Register 7	LIUCCAR7	0x0FnE
LIU Channel Control Arbitrary Register 8	LIUCCAR8	0x0FnF
Reserved	-	0x0F80 - 0x0FDF
LIU Register Summary - Global Control Registers		
LIU Global Control Register 0	LIUGCR0	0x0FE0
LIU Global Control Register 1	LIUGCR1	0x0FE1
LIU Global Control Register 2	LIUGCR2	0x0FE2
LIU Global Control Register 3	LIUGCR3	0x0FE4
LIU Global Control Register 4	LIUGCR4	0x0FE9
LIU Global Control Register 5	LIUGCR5	0x0FEA
Reserved	-	0x0FEB - 0x0FFF

1.0 REGISTER DESCRIPTIONS - E1 MODE

All address on this register description is shown in HEX format, where n indicates channels 0-3 in the 4-channel device.

TABLE 1: CLOCK SELECT REGISTER (CSR) **HEX ADDRESS: 0xn100**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LCV Insert	R/W	0	**Line Code Violation Insertion** This bit is used to force a Line Code Violation (LCV) on the transmit output of TTIP/TRING. A “0” to “1” transition on this bit will cause a single LCV to be inserted on the transmit output of TTIP/TRING.
6	Set T1 Mode	R/W	0	**T1/E1 Mode select** This bit is used to program the individual channel to operate in either T1 or E1 mode. 0 = Configures the selected channel to operate in E1 mode. 1 = Configures the selected channel to operate in T1 mode.
5	Sync All Transmit-ters to 8kHz	R/W	0	**Sync All Transmit Framers to 8kHz** This bit permits the user to configure each of the four (4) Transmit E1 Framer blocks to synchronize their “transmit output” frame alignment with the 8kHz signal that is derived from the MCLK PLL, as described below. 0 - Disables the “Sync all Transmit Framers to 8kHz” feature for all 4 channels. 1 - Enables the “Sync all Transmit Framers to 8kHz” feature for all 4 channels. ***NOTE:*** *Writing to this bit in register 0x0100 will enable this feature for all 4 channels.* ***NOTE:*** *This bit is only active if the MCLK PLL is used as the “Timing Source” for the Transmit E1 Framer” blocks. CSS[1:0] of this register allows users to select the transmit source of the framer.*
4	Clock Loss Detect	R/W	1	**Clock Loss Detect Enable/Disable Select** This bit enables a clock loss protection feature for the Framer whenever the recovered line clock is used as the timing source for the transmit section. If the LIU loses clock recovery, the Clock Distribution Block will detect this occurrence and automatically begin to use the internal clock derived from MCLK PLL as the Transmit source, until the LIU is able to regain clock recovery. 0 = Disables the clock loss protection feature. 1 = Enables the clock loss protection feature. ***NOTE:*** *This bit needs to be enabled in order to detect the clock loss detection interrupt status (address: 0xnB00, bit 5)*
3:2	Reserved	R/W	00	**Reserved**

TABLE 1: CLOCK SELECT REGISTER (CSR) **HEX ADDRESS: 0xn100**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1:0	CSS[1:0]	R/W	01	**Clock Source Select** These bits select the timing source for the Transmit E1 Framer block. These bits can also determine the direction of TxSERCLK, TxSYNC, and TxMSYNC in base rate operation mode (2.048MHz Clock mode). **In Base Rate (2.048MHz Clock Mode):**

CSS[1:0]	TRANSMIT SOURCE FOR THE TRANSMIT E1 FRAMER BLOCK	DIRECTION OF TXSERCLK
00/11	**Loop Timing Mode** The recovered line clock is chosen as the timing source.	Output
01	**External Timing Mode** The Transmit Serial Input Clock from the TxSERCLK_n input pin is chosen as the timing source.	Input
10	**Internal Timing Mode** The MCLK PLL is chosen as the timing source.	Output

NOTE: *TxSYNC/TxMSYNC can be programmed as input or output depending on the setting of SYNC INV bit in Register Address 0xn109, bit 4. Please see Register Description for the Synchronization Mux Register (SMR - 0xn109).*

NOTES: *In High-Speed or multiplexed modes, TxSERCLK, TxSYNC, and TxMSYNC are all configured as INPUTS only.*

TABLE 2: LINE INTERFACE CONTROL REGISTER (LICR) **HEX ADDRESS: 0XN101**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FORCE_LOS	R/W	0	**Force Transmit LOS (To the Line Side)** This bit permits the user to configure the transmit direction circuitry (within the channel) to transmit the LOS pattern to the remote terminal equipment, as described below. 0 - Configures the transmit direction circuitry to transmit “normal” traffic. 1 - Configures the transmit direction circuitry to transmit the LOS Pattern.
6	SR	R/W	0	**Single Rail Mode** This bit can only be set if the LIU Block is also set to single rail mode. See Register 0x0FE0, bit 7. 0 - Dual Rail 1 - Single Rail
5:4	LB[1:0]	R/W	00	**Framer Loopback Selection** These bits are used to select any of the following loop-back modes for the framer section. For LIU loopback modes, see the LIU configuration registers.

LB[1:0]	TYPES OF LOOPBACK SELECTED
00	Normal Mode (No LoopBack)
01	**Framer Local LoopBack:** When framer local loopback is enabled, the transmit PCM input data is looped back to the receive PCM output data. The receive input data at RTIP/RRING is ignored while an All Ones Signal is transmitted out to the line interface.
10	**Framer Far-End (Remote) Line LoopBack:** When framer remote loopback is enabled, the digital data enters the framer interface, however does not enter the framing blocks. The receive digital data from the LIU is allowed to pass through the LIU Decoder/ Encoder circuitry before returning to the line interface.
11	**Framer Payload LoopBack:** When framer payload loopback is enabled, the raw data within the receive time slots are looped back to the transmit framer block where the data is re-framed according to the transmit timing.

3:2	Reserved	R/W	0	**Reserved**

TABLE 2: LINE INTERFACE CONTROL REGISTER (LICR) **HEX ADDRESS: 0XN101**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	Encode B8ZS	R/W	0	**Encode AMI or B8ZS/HDB3 Line Code Select** This bit enables or disables the B8ZS/HDB3 encoder on the transmit path. 0 = Enables the B8ZS encoder. 1 = Disables the B8ZS encoder. ***NOTE:*** *When B8ZS encoder is disabled, AMI line code is used.*
0	Decode AMI/B8ZS	R/W	0	**Decode AMI or B8ZS/HDB3 Line Code Select** This bit enables or disables the B8ZS/HDB3 decoder on the receive path. 0 = Enables the B8ZS decoder. 1 = Disables the B8ZS decoder. ***NOTE:*** *When B8ZS decoder is disabled, AMI line code is received.*

TABLE 3: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	G.706 Annex B CRC-4 Calculation Enable	R/W	0	**G.706 Annex B CRC-4 Calculation Enable** This bit configures the E1 Receive Framer Block to be compliant with ITU-T G.706 Annex B for CRC-to-non-CRC interworking detection. If Annex B is enabled, G.706 Annex B CRC-4 multiframe alignment algorithm is implemented. If CRC-4 alignment is enabled and not achieved in 400msec while the basic frame alignment signal is present, it is assumed that the remote end is a non CRC-4 equipment. A CRC-to-Non-CRC interworking interrupt will be generated. The CRC-to-Non-CRC interworking interrupt Status can be read from Register Address 0xnB0A. 0 - Configures the Receive E1 Framer block to NOT support the “G.706 Annex B” CRC-4 Multiframe Alignment algorithm. 1 - Configures the Receive E1 Framer block to support the “G.706 Annex B” CRC-4 Multiframe Alignment algorithm.
6	Transmit CRC-4 Error	R/W	0	**Transmit CRC-4 Error** This bit is used to force a continuous errored CRC pattern in the outbound CRC multiframe to be sent on the transmission line. The Transmit E1 Framer Block will implement this error by inverting the value of CRC bit (C1). 0 = Disables the Transmit E1 Framer Block to transmit errored CRC bit. 1 = Forces the Transmit E1 Framer Block to transmit continuous errored CRC bit. ***NOTE:*** *This bit is ignored if CRC multi-Framing is disabled.*

TABLE 3: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5-4	CAS MF Align Sel[1:0]	R/W	00	**CAS Multiframe Alignment Declaration Algorithm Select[1:0]** These bits allow the user to select which CAS Multiframe Alignment Declaration algorithm the Receive E1 Framer block will employ, according to the table below. **CAS MF ALIGN SEL[1:0]** — **CAS MULTIFRAME ALIGNMENT DECLARATION ALGORITHM SELECTED** 00/11 — CAS Multiframe Alignment is Disabled 01 — **The "16-Frame" Algorithm** If this alignment algorithm is selected, then the Receive E1 Framer block will monitor the 16th timeslot of each incoming E1 frame and will declare CAS Multiframe alignment (e.g., clear the Loss of CAS Multiframe" defect) condition; anytime that it detects 15 consecutive E1 frames in which bits 1 - 4 (of timeslot 16) do not contain the "CAS Multiframe Alignment" pattern; which is immediately followed by an E1 frame that DOES contain the "CAS Multiframe Alignment" pattern. 10 — **The "2-Frame" (ITU-T G.732) Algorithm** If this alignment algorithm is selected, then the Receive E1 Framer block will monitor the 16th timeslot of each incoming E1 frame and will declare CAS Multiframe alignment (e.g., clear the Loss of CAS Multiframe" defect) condition; anytime that it detects a single E1 frame in which bits 1 - 4 (of timeslot 16) do not contain the "CAS Multiframe Alignment" pattern; which is immediately followed by an E1 frame that DOES contain the "CAS Multiframe Alignment" pattern. ***NOTE:*** *For information on the criteria that the Receive E1 Framer block uses in order to declare the "Loss of CAS Multiframe" defect condition, please see register description for the Framing Control Register (FCR - address 0xn10B)*

TABLE 3: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-2	CRC MF Align Sel[1:0]	R/W	00	**CRC Multiframe Alignment Declaration Criteria Select [1:0]** These two bits allow the user to select which CRC-Multiframe Alignment Declaration criteria the Receive E1 Framer block will employ. The Receive E1 Framer block will check for CRC Multiframe Alignment by checking the incoming E1 data-stream and determining whether the international bits (bit 1 of timeslot 0) of non-FAS frames match the CRC multiframe alignment pattern (0,0,1,0,1,1,E1,E2). The table below provides more details on the three different CRC Multiframe Alignment Declaration Criteria. **CRC MF ALIGN SEL [1:0]** — **CRC MULTIFRAME ALIGNMENT DECLARATION CRITERIA SELECTED** 00 — CRC Multiframe Alignment is Disabled 01 — CRC Multiframe Alignment is Enabled. Alignment is declared if at least 1 valid CRC multiframe alignment signal (0,0,1,0,1,1,E1,E2) is observed within 8ms. 10 — CRC Multiframe Alignment is Enabled. Alignment is declared if at least 2 valid CRC multiframe alignment signals (0,0,1,0,1,1,E1,E2) are observed within 8ms. 11 — CRC Multiframe Alignment is Enabled. Alignment is declared if at least 3 valid CRC multiframe alignment signals (0,0,1,0,1,1,E1,E2) are observed within 8ms. ***NOTE:*** *For information on the criteria that the Receive E1 Framer block uses to declare the "Loss of CRC Multiframe Alignment" defect condition, please see register description for the Framing Control Register (FCR - 0xn10B)*
1	Additional Frame Check Enable - FAS	R/W	0	**Additional Frame Check Enable - FAS Frame Alignment Declaration** This bit permits the user to configure the Receive E1 Framer block to perform some "additional FAS frame synchronization checking" prior to declaring "FAS Frame Alignment". If the user implements this feature, then the Receive E1 Framer block will perform some more testing on two additional E1 frames, prior to declaring the "FAS Frame Alignment" condition. 0 - Disables this additional FAS frame checking. 1 - Enables this additional FAS frame checking.

TABLE 3: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	FAS Frame Align Sel	R/W	0	**FAS Alignment Declaration Algorithm Select** This bit specifies which algorithm the Receive E1 Framer block uses in its search for the FAS Alignment. 0 = Selects the FAS Alignment Algorithm 1 1 = Selects the FAS Alignment Algorithm 2 **FAS Alignment Algorithm 1** If the Receive E1 Framer block has been configured to use “FAS Alignment Algorithm # 1", then it will acquire FAS alignment by performing the following three steps: **Step 1** - The Receive E1 Framer block begins by searching for the correct 7-bit FAS pattern. Go to Step 2 if found. **Step 2** - Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed timeslot 0 of the Non-FAS frame is a one. Go back to Step 1 if failed, otherwise, go to step 3. **Step 3** - Check if the FAS is present in the assumed timeslot 0 of the third frame. Go back to Step 1 if failed. After the first three steps (if they all passed), the Receive E1 Framer Block will declare FAS in SYNC if Frame Check Sequence (Bit 1 of this register) is disabled. If Frame Check Sequence (Bit 1 of this register) is enabled, then the Receive E1 Framer Block will need to verify the correct frame alignment for an additional two frames. **FAS Alignment Algorithm 2** If the Receive E1 Framer block has been configured to support “FAS Alignment Algorithm # 2, then it will perform the following 3 steps in order to acquire and declare FAS Frame Alignment with the incoming E1 data-stream. Algorithm 2 is similar to Algorithm 1 but adds a one-frame hold off time after the second step fails. After the second step fails, it waits for the next assumed FAS in the next frame before it begins the new search for the correct FAS pattern. **Step 1** - Algorithm 1 begins by searching for the correct 7-bit FAS pattern. Go to Step 2 if found. **Step 2** - Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed timeslot 0 of the Non-FAS frame is a one. Go back to Step 4 if failed, otherwise, go to step 3. **Step 3** - Check if the FAS is present in the assumed timeslot 0 of the third frame. Go back to Step 1 if failed, otherwise, proceed to check for Frame Check Sequence. **Step 4** - Wait for assumed FAS in the next frame, then go back to Step 1 After the first three steps (if they all passed), the Receive E1 Framer Block will declare FAS in SYNC if Frame Check Sequence (Bit 1 of this register) is disabled. If Frame Check Sequence (Bit 1 of this register) is enabled, then the Receive E1 Framer Block will need to verify the correct frame alignment for an additional two frames.

TABLE 4: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0xn108**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Transmit AUXP Pattern	R/W	0	**Transmit Auxiliary (AUXP) Pattern** This bit permits the user to command the Transmit E1 Framer block to transmit the AUXP Pattern to the remote terminal equipment, as depicted below. 0 - Configures the Transmit E1 Framer block to NOT transmit the AUXP Pattern (which is an unframed, repeating 1010... pattern). 1 - Configures the Transmit E1 Framer block to transmit the AUXP Pattern. The device also supports AUXP pattern detection, please read register (address 0xnB0A) for more detail.
6	Loss of Frame Declaration Criteria	R/W	0	**Loss of Frame Declaration Criteria** This bit permits the user to select the “Loss of Frame Declaration Criteria” for the Receive E1 Framer block, as depicted below. 0 = Loss of Frame is declared immediately if either CRC Multiframe Alignment or FAS Alignment is lost. 1 = Loss of Frame is declared immediately if FAS Alignment is lost. If CRC Multiframe Alignment is lost for more than 8ms, E1 receive framer will force a frame search.
5-4	Transmit YEL And Multi-YEL[1:0]	R/W	00	**Yellow Alarm and Multiframe Yellow Alarm Generation [1:0]** These bits activate or deactivate the transmission of yellow and multiframe yellow alarm. The Yellow alarm and multiframe Yellow alarm can be forced to transmit as’1’, or be inserted upon detection of loss of alignment. The decoding of these bits are explained as follows: **YEL[1:0]** — **YELLOW ALARM TRANSMITTED** 00/10 — **Yellow Alarm and Multiframe Yellow Alarm transmission is disabled.** 01 — **Automatic Transmission of Yellow and CAS Multiframe Yellow Alarms are enabled, as described below:** 1. Whenever the Receive E1 Framer block declares the LOF (Loss of FAS Framing) defect condition: The corresponding Transmit E1 Framer block will automatically transmit the Yellow Alarm indicator (by setting Bit 3 of Time-Slot 0, within the non-FAS frames) to 1" whenever (and for the duration that) the Receive E1 Framer block declares the LOF defect condition. 2. Whenever the Receive E1 Framer block declares the “Loss of CAS Multiframe Alignment” defect condition: The corresponding Transmit E1 Framer block will automatically transmit the CAS Multiframe Yellow Alarm indicator (by setting Bit 6 within “Frame 0" of Time-slot 16) to “1” whenever (and for the duration that) the Receive E1 Framer block declares the Loss of CAS Multiframe Defect condition. 11 — **Force Transmission of Yellow and Multiframe Yellow Alarm** Both Yellow and Multiframe Yellow Alarm are transmitted as ‘1’ when this is enabled.

TABLE 4: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0xn108**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>Transmit AIS Pattern Select[1:0]</td><td>R/W</td><td>00</td><td>
Types of AIS Pattern Generation Select
These bits permit the user to do the following.
a. To select the type of AIS Pattern that the Transmit E1 Framer block will transmit.
b. To force (via Software-control) the transmission of the “selected” AIS Pattern.
<table>
<tr><th>AISG[1:0]</th><th>TYPES OF AIS PATTERN TRANSMITTED</th></tr>
<tr><td>00</td><td>Transmission of AIS Indicator is Disabled
The Transmit E1 Framer block will transmit “normal” E1 traffic to the remote terminal equipment.</td></tr>
<tr><td>01</td><td>Unframed AIS alarm
Transmit E1 Framer block will transmit an Unframed All Ones Pattern, as an AIS Pattern.</td></tr>
<tr><td>10</td><td>The AIS-16 Pattern
In this case, Time-slot 16 (within each outbound E1 frame) will be set to an “All Ones” Pattern.</td></tr>
<tr><td>11</td><td>Framed AIS alarm
Transmit E1 Framer block will transmit a Framed All Ones Pattern, as an AIS Pattern.</td></tr>
</table>
NOTE: For “normal” operation, the user should set these bits to “[0, 0]”.
</td></tr>
<tr><td>1-0</td><td>AIS Defect Declaration Criteria[1:0]</td><td>R/W</td><td>00</td><td>
AIS Defect Declaration Criteria[1:0]:
These bits permit the user to specify the types of AIS Patterns that the Receive E1 Framer block must detect before it will declare the AIS defect condition.
<table>
<tr><th>AISD[1:0]</th><th>AIS Defect Declaration Criteria</th></tr>
<tr><td>00</td><td>AIS Defect Condition will NOT be declared.</td></tr>
<tr><td>01</td><td>Receive E1 Framer block will detect both Unframed and Framed AIS pattern</td></tr>
<tr><td>10</td><td>Receive E1 Framer block will detect AIS16 (Time Slot 16 AIS) pattern*.</td></tr>
<tr><td>11</td><td>Receive E1 Framer block will detect only Framed AIS pattern</td></tr>
</table>
NOTE: In revision C of XRT86VL34, Receive E1 framer will always monitor AIS16 condition and report the state and interrupt status without having to enable these two bits. AIS16 alarm state and interrupt status can be read from register 0xnB12, 0xnB13.
</td></tr>
</table>

TABLE 5: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0XN109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	E Bit Source Sel[1:0]	R/W	00	**Source for E bits [1:0]** These bits permit the user to specify the source of the E-bits, within each outbound E1 frame, as depicted below. **ESRC[1:0]** — **SOURCE FOR E-BITS** 00 — The corresponding Receive E1 Framer block: In this case, the E-bits will be used to indicate whether the Receive E1 Framer block has detected a CRC error within the most recently received Sub-Multiframe. The Receive E1 Framer will indicate a received errored sub-multiframe by setting the binary state of E bit from ‘1’ to ‘0’ for each errored sub-multi-frame. 01 — All E bits (within the outbound E1 data-stream) are set to “0”. 10 — All E bits (within the outbound E1 data-stream) are set to “1”. 11 — The outgoing E bits will be used to carry data link information. ***NOTE:*** *This bit is only active if the Transmit E1 Framer block has been configured to internally generate and insert the various Framing Alignment bits within the outbound E1 data-stream. In other words, whenever the “Framing Alignment Pattern Source Select” bit (within Bit 0 of this Register) is set to “0”.*
5	Reserved	-	-	**Reserved**

TABLE 5: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0xn109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	Transmit Frame Sync Select	R/W	0	**Transmit Frame Sync Select** This bit permits the user to configure the System-Side Terminal Equipment or the E1 Transmit Framer to dictate whenever the Transmit E1 Framer block will initiate its generation and transmission of the very next E1 frame. If the system side controls, then all of the following will be true. 1. The corresponding TxSync_n and TxMSync_n pins will function as input pins. 2. The Transmit E1 Framer block will initiate its generation of a new E1 frame whenever it samples the corresponding “TxSync_n” input pin “high” (via the TxSerClk_n input clock signal). 3. The Transmit E1 Framer block will initiate its generation of a new CRC Multiframe whenever it samples the corresponding “TxMSync_n” input pin “high”. This bit can also be used to select the direction of the transmit single frame boundary (TxSYNC) and multi-frame boundary (TxMSYNC) depending on whether TxSERCLK is chosen as the timing source for the transmit section of the framer. (CSS[1:0] = 01 in register 0xn100) **If TxSERCLK is chosen as the timing source:** 0 = Configures TxSYNC and TxMSYNC as inputs. (System Side Controls) 1 = Configures TxSYNC and TxMSYNC as outputs. (Chip Controls) **If either Recovered Line Clock, MCLK PLL is chosen as the timing source:** 0 = Configures TxSYNC and TxMSYNC as outputs. (Chip Controls) 1 = Configures TxSYNC and TxMSYNC as inputs. (System Side Controls) ***NOTE:*** *TxSERCLK is chosen as the transmit clock if CSS[1:0] of the Clock Select Register (Register Address: 0xn100) is set to b01. Recovered Clock is chosen as the transmit clock if CSS[1:0] is set to b00 or b11; Internal Clock is chosen as the transmit clock if CSS[1:0] is set to b10.*
3-2	Data Link Source Select [1:0]	R/W	00	**Data Link Source Select** These bits are used to specify the source of the Data Link bits that will be inserted in the outbound E1 frames. The table below describes the three different sources from which the Data Link bits can be inserted.

DLSRC[1:0]	SOURCE OF DATA LINK BITS
00/11	TxSER Input - The transmit serial input from the transmit payload data input block will be the source for data link bits
01	Transmit HDLC Controller - The Transmit HDLC Controller will generate either BOS (Bit Oriented Signaling) or MOS (Message Oriented Signaling) messages which will be inserted into the Data Link bits in the outbound E1frames.
10	TxOH Input - The Transmit Overhead data Input Port will be the source for the Data Link bits.

TABLE 5: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0XN109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	CRC-4 Bits Source Sel	R/W	0	**CRC-4 Bits Source Select** This bit permits the user to specify the source of the CRC-4 bits, within the outbound E1 data-stream, as depicted below. 0 - Configures the Transmit E1 Framer block to internally compute and insert the CRC-4 bits within the outbound E1 data-stream. 1 - Configures the Transmit E1 Framer block to externally accept data from the TxSer_n input pin, and to insert this data into the CRC-4 bits within the outbound E1 data-stream. ***NOTE:*** *This bit is ignored if CRC Multiframe Alignment is disabled*
0	Framing Alignment Pattern Source Select	R/W	0	**Framing Alignment Pattern Source Select** This bit permits the user to specify the source of the various "Framing Alignment" bits (which includes the FAS bits, the CRC Multiframe Alignment bits, the E and A bits). 0 - Configures the Transmit E1 Framer block to internally generate and insert these various framing alignment bits into the outbound E1 data-stream. 1 - Configures the Transmit E1 Framer block to externally accept data from the TxSer_n input pin, and to insert this data into the FAS, CRC Multiframe, E and A bits within the outbound E1 data-stream. ***NOTE:*** *Users can specify the source for E-bits in register bits 6-7 within this register if Transmit E1 Framer is configured to internally generate the various framing alignment bits (i.e. this bit set to'0').*

TABLE 6: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0xn10A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSa8ENB	R/W	0	**Transmit Sa8 Enable** This bit specifies if the Sa8 bits (bit 7 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa8 will NOT be used to transport Data Link Information. Sa8 bits will be set to "1" within the outbound E1 data-stream if the Sa8 bits are inserted from the transmit serial input. 1 = Sa8 WILL be used to transport Data Link Information. ***NOTE:*** *Sa8 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xn130) setting. The data link interface uses Sa8 bits for transmission only if Data Link source is from HDLC controller (DLSRC = b01 from Register 0xn109) and if Sa8 bits are inserted from the transmit serial input (TxSa8SEL = 0 from Register 0xn130).*
6	TxSa7ENB	R/W	0	**Transmit Sa7 Enable** This bit specifies if the Sa7 bits (bit 6 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa7 will NOT be used to transport Data Link Information. Sa7 bits will be set to "1" within the outbound E1 data-stream if the Sa7 bits are inserted from the transmit serial input. 1 = Sa7 WILL be used to transport Data Link Information. ***NOTE:*** *Sa7 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xn130) setting. The data link interface uses Sa8 bits for transmission only if Data Link source is from HDLC controller (DLSRC = b01 from Register 0xn109) and if Sa7 bits are inserted from the transmit serial input (TxSa7SEL = 0 from Register 0xn130).*
5	TxSa6ENB	R/W	0	**Transmit Sa6 Enable** This bit specifies if the Sa6 bits (bit 5 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa6 will NOT be used to transport Data Link Information. Sa6 bits will be set to "1" within the outbound E1 data-stream if the Sa6 bits are inserted from the transmit serial input. 1 = Sa6 WILL be used to transport Data Link Information. ***NOTE:*** *Sa6 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xn130) setting. The data link interface uses Sa6 bits for transmission only if Data Link source is from HDLC controller (DLSRC = b01 from Register 0xn109) and if Sa6 bits are inserted from the transmit serial input (TxSa6SEL = 0 from Register 0xn130).*
4	TxSa5ENB	R/W	0	**Transmit Sa5 Enable** This bit specifies if the Sa5 bits (bit 4 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa5 will NOT be used to transport Data Link Information. Sa5 bits will be set to "1" within the outbound E1 data-stream if the Sa5 bits are inserted from the transmit serial input. 1 = Sa5 WILL be used to transport Data Link Information. *Sa5 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xn130) setting. The data link interface uses Sa5 bits for transmission only if Data Link source is from HDLC controller (DLSRC = b01 from Register 0xn109) and if Sa5 bits are inserted from the transmit serial input (TxSa5SEL = 0 from Register 0xn130).*

TABLE 6: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0XN10A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	TxSa4ENB	R/W	0	**Transmit Sa4 Enable** This bit specifies if the Sa4 bits (bit 3 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa4 will NOT be used to transport Data Link Information. Sa4 bits will be set to "1" within the outbound E1 data-stream if the Sa4 bits are inserted from the transmit serial input. 1 = Sa4 WILL be used to transport Data Link Information. *Sa4 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xn130) setting. The data link interface uses Sa4 bits for transmission only if Data Link source is from HDLC controller (DLSRC = b01 from Register 0xn109) and if Sa4 bits are inserted from the transmit serial input (TxSa5SEL = 0 from Register 0xn130).*

TABLE 6: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0xn10A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2-0	TxSIGDL[2:0]	R/W	000	**Transmit Signaling and Data Link Select[2:0]:** These bits are used to specify the source for D/E channel, National Bits in timeslot 0 of the non-FAS frames, and Timeslot 16 of the outbound E1 frames. The table below presents the settings of these three bits in detail.

TxSIGDL [2:0]	SOURCE OF D/E CHANNEL	SOURCE OF NATIONAL BITS	SOURCE OF TIMESLOT 16
000	TxFrTD_n or TxSer_n input pin	Data link	TxSer_n input pin
001	TxFrTD_n or TxSer_n input pin	Data link	CAS signaling is enabled. Time Slot 16 can be inserted from any of the following: • TxSer_n input pin • TSCR Register (0xn340-0xn35F) • TxOH_n input pin on time slot 16 only • TxSIG_n input pin on every slot
010	TxFrTD_n or TxSer_n input pin	Forced to All Ones	TxSER_n input pin or TxSIG_n input pin on time slot 16 only
011	TxFrTD_n or TxSer_n input pin	Forced to All Ones	CAS signaling is enabled. Time Slot 16 can be inserted from any of the following: • TxSer_n input pin • TSCR Register (0xn340-0xn35F) • TxOH_n input pin on time slot 16 only • TxSIG_n input pin on every slot
100	TxSIG_n or TxSer_n input pin	Data link	TxSer_n input pin
101/ 110/	Not Used	Not Used	Not Used

TABLE 7: FRAMING CONTROL REGISTER (FCR) **HEX ADDRESS: 0xn10B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reframe	R/W	0	**Force Reframe** A ‘0’ to ‘1’ transition will force the Receive E1 Framer to restart the synchronization process. This bit field is automatically cleared (set to 0) after frame synchronization is reached.
6-5	Loss of CAS MF Align_Sel [1:0]	R/W	10	**Loss of CAS Multiframe Alignment Defect Declaration Criteria Select [1:0]** These two bits permit the user to select the “Loss of CAS Multiframe Alignment” defect declaration criteria. Loss of CAS Multiframe Alignment defect is declared based on the number of consecutive CAS multiframes with Multiframe Alignment signal received in error as indicated in the table below. **CASC[1:0]** — **LOSS OF CAS MULTIFRAME ALIGNMENT DECLARATION CRITERIA** 00 — 2 consecutive CAS Multiframes 01 — 3 consecutive CAS Multiframes 10 — 4 consecutive CAS Multiframes 11 — 8 consecutive CAS Multiframes ***NOTE:*** *These bits are active only if CAS Multiframe Alignment is enabled.*
4-3	Loss of CRC Multiframe Align_Sel[1:0]	R/W	00	**Loss of CRC-4 Multiframe Alignment Defect Declaration Criteria Select [1:0]** These two bits permit the user to select the “Loss of CRC-4 Multiframe Alignment” defect declaration criteria for the Channel. The following table presents the different CRC-4 Multiframe Algorithms in terms of the number of consecutive erred CRC-4 multiframe alignments that the E1 Receiver Framer will receive before it declares the “Loss of CRC-4 Multiframe Alignment” defect condition. **CRCC[1:0]** — **LOSS OF CRC-4 MULTIFRAME ALIGNMENT DECLARATION CRITERIA** 00 — 4 consecutive CRC-4 Multiframes Alignment 01 — 2 consecutive CRC-4 Multiframes Alignment 10 — 8 consecutive CRC-4 Multiframes Alignment 11 — **If TBR-4 Standard is Enabled*:** 4 consecutive CRC-4 Multiframe Alignment or 915 or more CRC-4 errors **If TBR-4 Standard is Disabled*:** 915 or more CRC-4 errors ***NOTE:*** *These bits are only active if CRC Multiframe Alignment is enabled. If CRC multiframe alignment is not found in 8ms, the E1 receive framer will restart the synchronization process.* ***NOTE:*** *TBR-4 standard is enabled by writing to 0xn112, bit 6.*

TABLE 7: FRAMING CONTROL REGISTER (FCR) **HEX ADDRESS: 0xn10B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2-0	FASC [2:0]	R/W	011	**Loss of FAS Alignment Defect Declaration Criteria Select [2:0]** These bits permit the user to specify the Loss of FAS Alignment defect declaration criteria. The following table presents the different FAS Alignment Algorithms in terms of the number of consecutive erred FAS patterns within a multiframe that the E1 Receiver Framer will receive before it declares the “Loss of FAS Alignment” defect conditions

FASC[2:0]	LOSS OF FAS ALIGNMENT DECLARATION CRITERIA
000	Setting these bits to ‘b000’ is illegal. Do not use this configuration.
001	1 FAS Alignment pattern
010	2 consecutive FAS Alignment patterns
011	3 consecutive FAS Alignment patterns
100	4 consecutive FAS Alignment patterns
101	5 consecutive FAS Alignment patterns
110	6 consecutive FAS Alignment patterns
111	7 consecutive FAS Alignment patterns

NOTE: *Loss of FAS alignment will force the E1 receive framer to declare the loss of CAS multiframe alignment and loss of CRC multiframe alignment.*

TABLE 8: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RSDLSR) **HEX ADDRESS: 0XN10C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RxSa8ENB	R/W	0	**Receive Sa8 Enable** This bit is used to specify whether or not Sa 8 (bit 7 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa8 is not used to receive data link information 1 = Sa8 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*
6	RxSa7ENB	R/W	0	**Receive Sa7 Enable** This bit is used to specify whether or not Sa 7 (bit 6 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa7 is not used to receive data link information 1 = Sa7 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*
5	RxSa6ENB	R/W	0	**Receive Sa6 Enable** This bit is used to specify whether or not Sa 6 (bit 5 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa6 is not used to receive data link information 1 = Sa6 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*
4	RxSa5ENB	R/W	0	**Receive Sa5 Enable** This bit is used to specify whether or not Sa 5 (bit 4 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa5 is not used to receive data link information 1 = Sa5 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*
3	RxSa4ENB	R/W	0	**Receive Sa4 Enable** This bit is used to specify whether or not Sa 4 (bit 3 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa4 is not used to receive data link information 1 = Sa4 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*

TABLE 8: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RSDLSR) **HEX ADDRESS: 0xn10C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2-0	RxSIGDL[2:0]	R/W	000	**Receive Signaling and Datalink Select[2:0]:** These bits specify the destination for the data that is to be extracted via D/E channel, National Bits in timeslot 0 of the non-FAS frames, and Timeslot 16 in the outbound frames. The table below presents the settings of these three RxSIGDL bits in detail.

RxSIGDL [2:0]	D/E CHANNEL	NATIONAL BITS	TIME SLOT 16
000	RxFrTD_n or the RxSer_n output pin	Data Link	RxSER_n output pin
001	RxFrTD_n or the RxSer_n output pin	Data Link	CAS signaling is enabled. Time Slot 16 can be extracted to any of the following: • RxSer_n output pin • RSAR Register (0xn500-0xn51F) • RxOH_n output pin on time slot 16 only • RxSIG_n output pin on every time slot
010	RxFrTD_n or the RxSer_n output pin	Data Link forced to All Ones	Time Slot 16 can be extracted to any of the following: • RxSer_n output pin • RSAR Register (0xn500-0xn51F) • RxOH_n output pin on time slot 16 only • RxSIG_n output pin on time slot 16 only
011	RxFrTD_n or the RxSer_n output pin	Data Link forced to All Ones	CAS signaling is enabled. Time Slot 16 can be extracted to any of the following: • RxSer_n output pin • RSAR Register (0xn500-0xn51F) • RxOH_n output pin on time slot 16 only RxSIG_n output pin on every time slot
100	RxSIG_n or the RxSer_n output pin	Data Link	RxSER_n output pin
101/110/111	Not Used	Not Used	Not Used

TABLE 9: RECEIVE SIGNALING CHANGE REGISTER 0 (RSCR 0) **HEX ADDRESS: 0XN10D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch. 0	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 0 through 7 within the incoming E1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 0 through 7) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 0 through 7) HAS changed since the last read of this register. ***NOTES:*** *1. Bit 7 (Time-Slot 0) is NOT active, since it carries the FAS and National Bits.* ***NOTE:*** *2. This register is only active if the incoming E1 data-stream is using Channel Associated Signaling.*
6	Ch. 1	RUR	0	
5	Ch.2	RUR	0	
4	Ch.3	RUR	0	
3	Ch.4	RUR	0	
2	Ch.5	RUR	0	
1	Ch.6	RUR	0	
0	Ch.7	RUR	0	

TABLE 10: RECEIVE SIGNALING CHANGE REGISTER 1 (RSCR 1) **HEX ADDRESS: 0XN10E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.8	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 8 through 15 within the incoming E1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 8 through 15) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 8 through 15) HAS changed since the last read of this register. ***NOTE:*** *This register is only active if the incoming E1 data-stream is using Channel Associated Signaling.*
6	Ch.9	RUR	0	
5	Ch.10	RUR	0	
4	Ch.11	RUR	0	
3	Ch.12	RUR	0	
2	Ch.13	RUR	0	
1	Ch.14	RUR	0	
0	Ch.15	RUR	0	

TABLE 11: RECEIVE SIGNALING CHANGE REGISTER 2 (RSCR 2) **HEX ADDRESS: 0XN10F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.16	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 16 through 23 within the incoming E1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 16 through 23) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 16 through 23) HAS changed since the last read of this register. ***NOTE:*** *This register is only active if the incoming E1 data-stream is using Channel Associated Signaling.*
6	Ch.17	RUR	0	
5	Ch.18	RUR	0	
4	Ch.19	RUR	0	
3	Ch.20	RUR	0	
2	Ch.21	RUR	0	
1	Ch.22	RUR	0	
0	Ch.23	RUR	0	

TABLE 12: RECEIVE SIGNALING CHANGE REGISTER 3 (RSCR 3) **HEX ADDRESS: 0XN110**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.24	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 24 through 31 within the incoming E1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 24 through 31) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 24 through 31) HAS changed since the last read of this register. ***NOTE:*** *This register is only active if the incoming E1 data-stream is using Channel Associated Signaling.*
6	Ch.25	RUR	0	
5	Ch.26	RUR	0	
4	Ch.27	RUR	0	
3	Ch.28	RUR	0	
2	Ch.29	RUR	0	
1	Ch.30	RUR	0	
0	Ch.31	RUR	0	

TABLE 13: RECEIVE NATIONAL BITS REGISTER (RNBR) **HEX ADDRESS: 0xn111**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Si_FAS	RO	x	**Received International Bit - FAS Frame** This Read Only bit contains the value of the International Bit (e.g., the Si bit) in the most recently received FAS frame.
6	Si_nonFAS	RO	x	**Received International Bit - Non FAS Frame** This Read Only bit contains the value of the International Bit (e.g., the Si bit) in the most recently received non-FAS frame
5	R_ALARM	RO	x	**Received A bit - Non FAS Frame** This Read Only bit contains the value in the Remote Alarm Indication bit (A bit, or bit 3 of non-FAS frame) within the most recently received non-FAS frame.
4	Sa4	RO	x	**Received National Bits** These Read Only bits contain the values of the National bits (Sa4-Sa8) within the most recently received non-FAS frame.
3	Sa5	RO	x	
2	Sa6	RO	x	
1	Sa7	RO	x	
0	Sa8	RO	x	

TABLE 14: RECEIVE EXTRA BITS REGISTER (REBR) **HEX ADDRESS: 0XN112**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	In-Frame	RO	0	**In Frame State:** This READ-ONLY bit indicates whether the Receive E1 Framer block is currently declaring the “In-Frame” condition with the incoming E1 data-stream. 0 - Indicates that the Receive E1 Framer block is currently declaring the LOF (Loss of Frame) Defect condition. 1 - Indicates that the Receive E1 Framer block is currently declaring itself to be in the “In-Frame” condition.
6	TBR4_Std	R/W	0	**TBR4 Standard** Setting this bit will force the XRT86VL34 to be compliant with the TBR-4 standard for “Loss of CRC-4 Multiframe Alignment Criteria”. 0 - Backward compatible with XRT86L38 for Loss of CRC-4 Multiframe Criteria. When CRCC[1:0] (from register 0xn10B) is set to’11’, Loss of CRC-4 Multiframe Alignment will declare if 915 or more CRC-4 errors have been detected in 1 second. 1 - “TBR-4 Compliant” Loss of CRC-4 Multiframe Alignment Criteria - When CRCC[1:0] (from register 0xn10B) is set to’11’, Loss of CRC-4 Multiframe Alignment will declare if 4 consecutive CRC-4 Multiframe Alignment have been received in error OR if 915 or more CRC-4 errors have been detected in 1 second.
5-4	Reserved	-	-	**Reserved**
3	EX1	RO	x	**Extra Bit 1** This READ ONLY bit field indicates the value of the most recently received Extra Bit value (bit 5 within timeslot 16 of frame 0 of the signaling multiframe). ***NOTE:*** *This bit only has meaning if the framer is using Channel Associated Signaling.*
2	ALARMFE	RO	x	**CAS Multi-Frame Yellow Alarm** This READ ONLY bit field indicates the value of the most recently received CAS Multiframe Yellow Alarm Bit (bit 6 within timeslot 16 of frame 0 of the signaling multiframe). 0 = Indicates that the E1 receive framer block is NOT receiving the CAS Multiframe Yellow Alarm. 1 = Indicates that the E1 receive framer block is currently receiving the CAS Multiframe Yellow Alarm. ***NOTE:*** *This bit only has meaning if the framer is using Channel Associated Signaling.*

TABLE 14: RECEIVE EXTRA BITS REGISTER (REBR) **HEX ADDRESS: 0XN112**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	EX2	RO	x	**Extra Bit 2** This READ ONLY bit field indicates the value of the most recently received Extra Bit value (bit 7 within timeslot 16 of frame 0 of the signaling multiframe). ***NOTE:*** *This bit only has meaning if the framer is using Channel Associated Signaling.*
0	EX3	RO	x	**Extra Bit 3** This READ ONLY bit field indicates the value of the most recently received Extra Bit value (bit 8 within timeslot 16 of frame 0 of the signaling multiframe). ***NOTE:*** *This bit only has meaning if the framer is using Channel Associated Signaling.*

TABLE 15: DATA LINK CONTROL REGISTER (DLCR1) **HEX ADDRESS: 0XN113**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	Reserved. Please set this bit to'0' for normal operation.
6	MOS ABORT Disable	R/W	0	**MOS ABORT Disable:** This bit permits the user to either enable or disable the "Automatic MOS ABORT" feature within Transmit HDLC Controller # 1. If the user enables this feature, then Transmit HDLC Controller block # 1 will automatically transmit the ABORT Sequence (e.g., a zero followed by a string of 7 consecutive "1s") whenever it abruptly transitions from transmitting a MOS type of message, to transmitting a BOS type of message. If the user disables this feature, then the Transmit HDLC Controller Block # 1 will NOT transmit the ABORT sequence, whenever it abruptly transitions from transmitting a MOS-type of message to transmitting a BOS-type of message. 0 - Enables the "Automatic MOS Abort" feature 1 - Disables the "Automatic MOS Abort" feature
5	Rx_FCS_DIS	R/W	0	**Receive Frame Check Sequence (FCS) Verification Enable/Disable** This bit permits the user to configure the Receive HDLC Controller Block # 1 to compute and verify the FCS value within each incoming LAPD message frame. 0 - Enables FCS Verification 1 - Disables FCS Verification
4	AutoRx	R/W	0	**Auto Receive LAPD Message** This bit configures the Receive HDLC Controller Block #1 to discard any incoming BOS or LAPD Message frame that exactly match which is currently stored in the Receive HDLC1 buffer. 0 = Disables this "AUTO DISCARD" feature 1 = Enables this "AUTO DISCARD" feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** This bit configures the Transmit HDLC Controller Block #1 to transmit an ABORT sequence (string of 7 or more consecutive 1's) to the Remote terminal. 0 - Configures the Transmit HDLC Controller Block # 1 to function normally (e.g., not transmit the ABORT sequence). 1 - Configures the Transmit HDLC Controller block # 1 to transmit the ABORT Sequence.

TABLE 15: DATA LINK CONTROL REGISTER (DLCR1) **HEX ADDRESS: 0XN113**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** This bit configures the Transmit HDLC Controller Block #1 to unconditionally transmit a repeating string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. In normal conditions, the Transmit HDLC Controller block will repeatedly transmit the Flag Sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this “Transmit Idle Sequence” feature, then the Transmit HDLC Controller block will UNCONDITIONALLY transmit a repeating stream of the Flag Sequence octet (thereby overwriting all outbound MOS data-link messages). 0 - Configures the Transmit HDLC Controller Block # 1 to transmit data-link information in a “normal” manner. 1 - Configures the Transmit HDLC Controller block # 1 to transmit a repeating string of Flag Sequence Octets (0x7E). ***NOTE:*** *This bit is ignored if the* Transmit *HDLC1 controller is operating in the BOS Mode - bit 0 (MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with Frame Check Sequence (FCS)** This bit permits the user to configure the Transmit HDLC Controller block # 1 to compute and append FCS octets to the “back-end” of each outbound MOS data-link message. 0 - Configures the Transmit HDLC Controller block # 1 to NOT compute and append the FCS octets to the back-end of each outbound MOS data-link message. 1 - Configures the Transmit HDLC Controller block # 1 TO COMPUTE and append the FCS octets to the back-end of each outbound MOS data-link message. ***NOTE:*** *This bit is ignored if the transmit HDLC1 controller has been configured to operate in the BOS mode - bit 0 (MOS/BOS) within this register is set to 0.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Send** This bit permits the user to enable LAPD transmission through HDLC Controller Block # 1 using either BOS (Bit-Oriented Signaling) or MOS (Message-Oriented Signaling) frames. 0 - Transmit HDLC Controller block # 1 BOS message Send. 1 - Transmit HDLC Controller block # 1 MOS message Send. ***NOTE:*** *This is not an Enable bit. This bit must be set to "0" each time a BOS is to be sent.*

TABLE 16: TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR1) **HEX ADDRESS: 0XN114**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxHDLC1 BUFAvail/ BUFSel	R/W	0	**Transmit HDLC1 Buffer Available/Buffer Select** This bit has different functions, depending upon whether the user is writing to or reading from this register, as depicted below. **If the user is writing data into this register bit:** 0 - Configures the Transmit HDLC1 Controller to read out and transmit the data, residing within “Transmit HDLC1 Buffer # 0", via the Data Link channel to the remote terminal equipment. 1 - Configures the Transmit HDLC1 Controller to read out and transmit the data, residing within the “Transmit HDLC1 Buffer #1”, via the Data Link channel to the remote terminal equipment. **If the user is reading data from this register bit:** 0 - Indicates that “Transmit HDLC1 Buffer # 0" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC1 Message Buffer, he/she should proceed to write this message into “Transmit HDLC1 Buffer # 0" - Address location: 0xn600. 1 - Indicates that “Transmit HDLC1 Buffer # 1" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC1 Message Buffer, he/she should proceed to write this message into “Transmit HDLC1 Buffer # 1" - Address location: 0xn700. ***NOTE:*** *If one of these Transmit HDLC1 buffers contain a message which has yet to be completely read-in and processed for transmission by the Transmit HDLC1 controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in-use buffer is not permitted.*
6-0	TDLBC[6:0]	R/W	0000000	**Transmit HDLC1 Message - Byte Count** The exact function of these bits depends on whether the Transmit HDLC 1 Controller is configured to transmit MOS or BOS messages to the Remote Terminal Equipment. **In BOS MODE:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Transmit HDLC1 controller generates the Transmit End of Transfer (TxEOT) interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. **In MOS MODE:** These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, Control field, however, it does not include the FCS bytes.

TABLE 17: RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR1) **HEX ADDRESS: 0XN115**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC1 Buffer-Pointer** This bit Identifies which Receive HDLC1 buffer contains the most recently received HDLC1 message. 0 - Indicates that Receive HDLC1 Buffer # 0 contains the contents of the most recently received HDLC message. 1 - Indicates that Receive HDLC1 Buffer # 1 contains the contents of the most recently received HDLC message.
6-0	RDLBC[6:0]	R/W	0000000	**Receive HDLC Message - byte count** The exact function of these bits depends on whether the Receive HDLC Controller Block #1 is configured to receive MOS or BOS messages. **In BOS Mode:** These seven bits contain the number of repetitions the BOS message must be received before the Receive HDLC1 controller generates the Receive End of Transfer (RxEOT) interrupt. If these bits are set to “0000000”, the message will be received indefinitely and no Receive End of Transfer (RxEOT) interrupt will be generated. **In MOS Mode:** These seven bits contain the size in bytes of the HDLC1 message that has been received and written into the Receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control field, AND the FCS bytes.

TABLE 18: SLIP BUFFER CONTROL REGISTER (SBCR) **HEX ADDRESS: 0XN116**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSB_ISFIFO	R/W	0	**Transmit Slip Buffer Mode** This bit permits the user to configure the Transmit Slip Buffer to function as either “Slip-Buffer” Mode, or as a “FIFO”, as depicted below. 0 - Configures the Transmit Slip Buffer to function as a “Slip-Buffer”. 1 - Configures the Transmit Slip Buffer to function as a “FIFO”. ***NOTE:*** *Transmit slip buffer is only used in high-speed or multiplexed mode where TxSERCLKn must be configured as inputs only. Users must make sure that the “Transmit Direction” timing (i.e. TxMSYNC) and the TxSerClk input clock signal are synchronous to prevent any transmit slips from occurring.* ***NOTE:*** *The data latency is dictated by FIFO Latency in the FIFO Latency Register (register 0xn117).*
6-5	Reserved	-	-	**Reserved**
4	SB_FORCESF	R/W	0	**Force Signaling Freeze** This bit permits the user to freeze any signaling update on the RxSIGn output pin as well as the Receive Signaling Array Register -RSAR (0xn500-0xn51F) until this bit is cleared. 0 = Signaling on RxSIG and RSAR is updated immediately. 1 = Signaling on RxSIG and RSAR is not updated until this bit is set to ‘0’.
3	SB_SFENB	R/W	0	**Signal Freeze Enable Upon Buffer Slips** This bit enables signaling freeze for one multiframe after the receive buffer slips. If signaling freeze is enabled, then the “Receive Channel” will freeze all signaling updates on RxSIG pin and RSAR (0xn500-0xn51F) for at least “one-multiframe” period, after a “slip-event” has been detected within the “Receive Slip Buffer”. 0 = Disables signaling freeze for one multi-frame after receive buffer slips. 1 = Enables signaling freeze for one multi-frame after receive buffer slips.
2	SB_SDIR	R/W	1	**Slip Buffer (RxSync) Direction Select** This bit permits user to select the direction of the receive frame boundary (RxSYNC) signal if the receive buffer is enabled. (i.e. SB_ENB[1:0] = 01 or 10). If slip buffer is bypassed, RxSYNC is always an output pin. 0 = Selects the RxSync signal as an output 1 = Selects the RxSync signal as an input

TABLE 18: SLIP BUFFER CONTROL REGISTER (SBCR) **HEX ADDRESS: 0XN116**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1-0	SB_ENB[1:0]	R/W	01	**Receive Slip Buffer Mode Select** These bits select modes of operation for the receive slip buffer. These two bits also select the direction of RxSERCLK and RxSYNC in base clock rate (2.048MHz). The following table shows the corresponding slip buffer modes as well as the direction of the RxSYNC/RxSERCLK according to the setting of these two bits.

SB_ENB [1:0]	RECEIVE SLIP BUFFER MODE SELECT	DIRECTION OF RXSERCLK	DIRECTION OF RXSYNC
00/11	Receive Slip Buffer is bypassed	Output	Output
01	Slip Buffer Mode	Input	Depends on the setting of SB_SDIR (bit 2 of this register) **If SB_SDIR = 0:** RxSYNC = Output **If SB_SDIR = 1:** RxSYNC = Input
10	FIFO Mode. FIFO data latency can be programmed by the 'FIFO Latency Register' (Address = 0xn117).	Input	Depends on the setting of SB_SDIR (bit 2 of this register) **If SB_SDIR = 0:** RxSYNC = Output **If SB_SDIR = 1:** RxSYNC = Input

NOTE: *If the user configures the Receive Slip Buffer to operate in the "FIFO Mode", then the user must make sure that the RxSerClk input pin is synchronized to the Recovered Clock signal for this particular channel.*

TABLE 19: FIFO LATENCY REGISTER (FFOLR) **HEX ADDRESS: 0XN117**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Reserved	-	-	**Reserved**
4-0	Rx Slip Buffer FIFO Latency[4:0]	R/W	00100	**Receive Slip Buffer FIFO Latency[4:0]:** These bits permit the user to specify the "Receive Data" Latency (in terms of RxSerClk_n clock periods), whenever the Receive Slip Buffer has been configured to operate in the "FIFO" Mode. ***NOTE:*** *These bits are only active if the Receive Slip Buffer has been configured to operate in the FIFO Mode.*

TABLE 20: DMA 0 (WRITE) CONFIGURATION REGISTER (D0WCR) **HEX ADDRESS: 0XN118**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	DMA0 RST	R/W	0	**DMA_0 Reset** This bit resets the transmit DMA (Write) channel 0. 0 = Normal operation. 1 = A zero to one transition resets the transmit DMA (Write) channel 0.
6	DMA0 ENB	R/W	0	**DMA_0 Enable** This bit enables the transmit DMA_0 (Write) interface. After a transmit DMA is enabled, DMA transfers are only requested when the transmit buffer status bits indicate that there is space for a complete message or cell. The DMA write channel is used by the external DMA controller to transfer data from the external memory to the HDLC buffers within the E1 Framer. The DMA Write cycle starts by E1 Framer asserting the DMA Request ($\overline{REQ0}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{ACK0}$) 'low' to indicate that it is ready to start the transfer. The external DMA controller should place new data on the Microprocessor data bus each time the Write Signal is Strobed low if the $\overline{WR}$ is configured as a Write Strobe. If $\overline{WR}$ is configured as a direction signal, then the external DMA controller would place new data on the Microprocessor data bus each time the Read Signal ($\overline{RD}$) is Strobed low. 0 = Disables the transmit DMA_0 (Write) interface 1 = Enables the transmit DMA_0 (Write) interface
5	WR TYPE	R/W	0	**Write Type Select** This bit selects the function of the $\overline{WR}$ signal. 0 = $\overline{WR}$ functions as a direction signal (indicates whether the current bus cycle is a read or write operation) and $\overline{RD}$ functions as a data strobe signal. 1 =$\overline{WR}$ functions as a write strobe signal
4 - 3	Reserved	-	-	**Reserved**
2	DMA0_CHAN(2)	R/W	0	**Channel Select** These three bits select which T/E1 channel within the XRT86VL34 uses the Transmit DMA_0 (Write) interface. 000 = Channel 0 001 = Channel 1 001 = Channel 2 011 = Channel 3 1xx = Reserved
1	DMA0_CHAN(1)	R/W	0	
0	DMA0_CHAN(0)	R/W	0	

TABLE 21: DMA 1 (READ) CONFIGURATION REGISTER (D1RCR) **HEX ADDRESS: 0XN119**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	Reserved	-	-	**Reserved**
7	DMA1 RST	R/W	0	**DMA_1 Reset** This bit resets the Receive DMA (Read) Channel 1 0 = Normal operation. 1 = A zero to one transition resets the Receive DMA (Read) channel 1.
6	DMA1 ENB	R/W	0	**DMA1_ENB** This bit enables the Receive DMA_1 (Read) interface. After a receive DMA is enabled, DMA transfers are only requested when the receive cell buffer contains a complete message or cell. The DMA read channel is used by the E1 Framer to transfer data from the HDLC buffers within the E1 Framer to external memory. The DMA Read cycle starts by E1 Framer asserting the DMA Request ($\overline{REQ1}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{ACK1}$) 'low' to indicate that it is ready to receive the data. The E1 Framer should place new data on the Microprocessor data bus each time the Read Signal is Strobed low if the $\overline{RD}$ is configured as a Read Strobe. If $\overline{RD}$ is configured as a direction signal, then the E1 Framer would place new data on the Microprocessor data bus each time the Write Signal ($\overline{WR}$) is Strobed low. 0 = Disables the DMA_1 (Read) interface 1 = Enables the DMA_1 (Read) interface
5	RD TYPE	R/W	0	**READ Type Select** This bit selects the function of the $\overline{RD}$ signal. 0 = $\overline{RD}$ functions as a Read Strobe signal 1 = $\overline{RD}$ acts as a direction signal (indicates whether the current bus cycle is a read or write operation), and $\overline{WR}$ works as a data strobe.
4 - 3	Reserved	-	-	**Reserved**
2	DMA1_CHAN(2)	R/W	0	**Channel Select** These three bits select which T/E1 channel within the chip uses the Receive DMA_1 (Read) interface. 000 = Channel 0 001 = Channel 1 001 = Channel 2 011 = Channel 3 1xx = Reserved
1	DMA1_CHAN(1)	R/W	0	
0	DMA1_CHAN(0)	R/W	0	

TABLE 22: INTERRUPT CONTROL REGISTER (ICR) **HEX ADDRESS: 0XN11A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3	Reserved	-	-	**Reserved**
2	INT_WC_RUR	R/W	0	**Interrupt Write-to-Clear or Reset-upon-Read Select** This bit configures all Interrupt Status bits to be either Reset Upon Read or Write-to-Clear 0 = Configures all Interrupt Status bits to be Reset Upon Read (RUR). 1= Configures all Interrupt Status bits to be Write-to-Clear (WC).
1	ENBCLR	R/W	0	**Interrupt Enable Auto Clear** This bit configures all interrupt enable bits to clear or not clear after reading the interrupt status bit. 0= Configures all Interrupt Enable bits to not cleared after reading the interrupt status bit. The corresponding Interrupt Enable bit will stay 'high' after reading the interrupt status bit. 1= Configures all interrupt Enable bits to clear after reading the interrupt status bit. The corresponding interrupt enable bit will be set to 'low' after reading the interrupt status bit.
0	INTRUP_ENB	R/W	0	**Interrupt Enable for Framer_n** This bit enables the entire E1 Framer Block for Interrupt Generation. 0 = Disables the E1 framer block for Interrupt Generation 1 = Enables the E1 framer block for Interrupt Generation

TABLE 23: LAPD SELECT REGISTER (LAPDSR) **HEX ADDRESS: 0xn11B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:2]	Reserved	-	-	**Reserved**
[1:0]	HDLC Controller Select[1:0]	R/W	0	**HDLC Controller Select[1:0]:** These bits permit the user to select any of the three (3) HDLC Controllers that he/she will use within this particular channel, as depicted below. 00 & 11 - Selects HDLC Controller # 1 01 - Selects HDLC Controller # 2 10 - Selects HDLC Controller # 3

TABLE 24: PERFORMANCE REPORT CONTROL REGISTER (PRCR) **HEX ADDRESS: 0xn11D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**For T1 mode only**
6	RLOS_OUT_ENB	R/W	1	**RLOS Output Enable:** This bit is used to enable or disable the Receive LOS (RLOS_n) output pins. 0 - Disables the RLOS output pin. 1 - Enables the RLOS output pin.
5-0	Reserved	-	-	**Reserved.**

TABLE 25: GAPPED CLOCK CONTROL REGISTER (GCCR) **HEX ADDRESS: 0XN11E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FrOutclk	R/W	0	**Framer Output Clock Reference** This bit is used to enable or disable high-speed T1/E1 rate on the T1OSCCLK and the E1OSCCLK output pins. By default, the output clock reference on T1OSCCLK and E1OSCCLK output pins is 1.544MHz/2.048MHz respectively. By setting this bit to a “1”, the output clock reference on the T1OSCLK and the E1OSCCLK is 49.408MHz/65.536MHz for T1/E1 respectively. 0 = Disables high-speed rate to be output on the T1OSCCLK and E1OSCCLK output pins. Standard T1/E1 Rate - 1.544MHz/2.048Mhz will be output to the T1OSCCLK and E1OSCCLK output pins respectively. 1 = Enables high-speed rate to be output on the T1OSCCLK and E1OSCCLK output pins.
6-0	Reserved	-	-	**Reserved**

TABLE 26: TRANSMIT INTERFACE CONTROL REGISTER (TICR) **HEX ADDRESS:0xn120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSyncFrD	R/W	0	**Transmit Synchronous fraction data interface** This bit selects whether TxCHCLK or TxSERCLK will be used for fractional data input if the transmit fractional interface is enabled. If TxSERCLK is selected to clock in fractional data input, TxCHCLK will be used as an enable signal 0 = Fractional data Is clocked into the chip using TxChCLK if the transmit fractional data interface is enabled. 1 = Fractional data is clocked into the chip using TxSerClk if the transmit fractional data interface is enabled. TxChClk is used as fractional data enable. ***NOTE:*** *The Time Slot Identifier Pins (TxChn[4:0]) still indicates the time slot number if the transmit fractional data interface is not enabled. Fractional Interface can be enabled by setting TxFr2048 to 1*
6	Reserved	-	-	**Reserved**
5	TxPLClkEnb	R/W	0	**Transmit payload clock enable** This bit configures the E1 framer to output a regular clock or a payload clock on the transmit serial clock (TxSERCLK) pin when TxSERCLK is configured to be an output. 0 = Configures the framer to output a 2.048MHz clock on the TxSERCLK pin when TxSERCLK is configured as an output. 1 = Configures the framer to output a 2.048MHz clock on the TxSERCLK pin when transmitting payload bits. There will be gaps on the TxSERCLK output pin when transmitting overhead bits.
4	TxFr2048	R/W	0	**Transmit Fractional/Signaling Interface Enabled** This bit is used to enable or disable the transmit fractional data interface, signaling input, as well as the 32MHz transmit clock and the transmit overhead Signal output. This bit only functions when the device is configured in non-high speed or multiplexed modes of operations. **If the device is configured in base rate:** 0 = Configures the 5 time slot identifier pins (TxChn[4:0]) to output the channel number as usual. 1 = Configures the 5 time slot identifier pins (TxChn[4:0]) into the following different functions: TxChn[0] becomes the Transmit Serial SIgnaling pin (TxSIG_n) for signaling inputs. Signaling data can now be input from the TxSIG pin if configured appropriately. TxChn[1] becomes the Transmit Fractional Data Input pin (TxFrTD_n) for fractional data input. Fractional data can now be input from the TxFrTD pin if configured appropriately. TxChn[2] becomes the 32 MHz transmit clock output TxChn[3] becomes the Transmit Overhead Signal which pulses high on the first bit of each multi-frame. ***NOTE:*** *This bit has no function in the high speed or multiplexed modes of operation. In high-speed or multiplexed modes, TxCHN[0] functions as TxSIGn for signaling input.*

TABLE 26: TRANSMIT INTERFACE CONTROL REGISTER (TICR) **HEX ADDRESS:0XN120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	TxICLKINV	R/W	0	**Transmit Clock Inversion (Backplane Interface)** This bit selects whether data transition will happen on the rising or falling edge of the transmit clock. 0 = Selects data transition happen on the rising edge of the transmit clocks. 1 = Selects data transition happen on the falling edge of the transmit clocks. ***NOTE:*** *This feature is only available for base rate configuration (i.e. non-highspeed, or non-multiplexed modes).*
2	TxMUXEN	R/W	0	**Transmit Multiplexed Mode Enable** This bit enables or disables the multiplexed mode on the transmit side. When multiplexed mode is enable, four-channel data from the backplane interface are multiplexed onto one serial stream and output to the line side. The backplane speed will be running at 16.384MHz once multiplexed mode is enabled. 0 = Disables the multiplexed mode. 1 = Enables the multiplexed mode.

TABLE 26: TRANSMIT INTERFACE CONTROL REGISTER (TICR) **HEX ADDRESS:0xn120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	TxIMODE[1]	R/W	0	**Transmit Interface Mode selection** This bit determines the transmit interface speed. The exact function of these two bits depends on whether Multiplexed mode is enabled or disabled. Table 27 and Table 28shows the functions of these bits for non-multiplexed and multiplexed modes.: **TABLE 27: TRANSMIT INTERFACE SPEED WHEN MULTIPLEXED MODE IS DISABLED (TXMUXEN = 0)**
0	TxIMODE[0]	R/W	0	

TxIMODE[1:0]	TRANSMIT INTERFACE SPEED
00	**2.048Mbit/s. (Base Rate)** Transmit Backplane interface signals include: TxSERCLK is an input or output clock at 2.048MHz TxMSYNC is the superframe boundary at 2ms TxSYNC is the single frame boundary at 125 us TxSER is the base-rate data input
01	**2.048Mbit/ (High-speed MVIP Mode)** Transmit Backplane interface signals include: TxSERCLK is an input clock at 2.048MHz TxMSYNC will become the high speed input clock at 2.048MHz to input high-speed data TxSYNC indicates the single frame boundary TxSER is the high-speed data input
10	**4.096Mbit/s High-speed mode:** Transmit Backplane interface signals include: TxSERCLK is an input clock at 2.048MHz TxMSYNC will become the high speed input clock at 4.096MHz to input high-speed data TxSYNC indicates the single frame boundary TxSER is the high-speed data input
11	**8.192Mbit/s High-speed mode:** Transmit Backplane interface signals include: TxSERCLK is an input clock at 2.048MHz TxMSYNC will become the high speed input clock at 8.192MHz to input high-speed data TxSYNC indicates the single frame boundary TxSER is the high-speed data input

TABLE 26: TRANSMIT INTERFACE CONTROL REGISTER (TICR) **HEX ADDRESS:0XN120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1-0	TxIMODE[1:0]	R/W	0	**(Continued)**: **TABLE 28: TRANSMIT INTERFACE SPEED WHEN MULTIPLEXED MODE IS ENABLED (TXMUXEN = 1)** **TxIMODE[1:0]** — **TRANSMIT INTERFACE SPEED** 00 — Reserved 01 — **16.384MHz Bit Multiplexed Mode:** The transmit interface is taking four-channel multiplexed data at a rate of 16.384Mbit/s from channel 0 and bit-demultiplexing the serial data into 4 channels and output to the line on channels 0 through 3. The TxSYNC signal pulses “High” during the first bit of each E1 frame. 10 — **HMVIP High-Speed Multiplexed Mode Enabled:** Transmit interface is taking four-channel multiplexed data at a rate of 16.384Mbit/s from channel 0 and byte-demultiplexing the serial data into 4 channels and output to the line on channels 0 through 3. The TxSYNC signal pulses “High” during the last two bits of the previous E1 frame and the first two bits of the current E1 frame. 11 — **H.100 High-Speed Multiplexed Mode Enabled**: Transmit interface is taking four-channel multiplexed data at a rate of 16.384Mbit/s from channel 0 and byte-demultiplexing the serial data into 4 channels and output to the line on channels 0 through 3. The TxSYNC signal pulses “High” during the last bit of the previous E1 frame and the first bit of the current E1 frame. **Transmit Backplane interface signals include:** TxSERCLK is an input clock at 2.048MHz TxMSYNC will become the high speed input clock at 16.384MHz to input high-speed multiplexed data on the back-plane interface TxSYNC is the single multiplexed frame boundary TxSER is the high-speed data input ***NOTE:*** *In high speed mode, transmit data is sampled on the rising edge of the 16MHz clock edge.*

TABLE 29: PRBS CONTROL AND STATUS REGISTER 0 (PRBSCSR0) **HEX ADDRESS: 0XN121**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	PRBS_Switch	R/W	0	**PRBS Switch** This bit enables or disables the PRBS switch function within the XRT86VL34 device. By enabling the PRBS switch function, PRBS functionality will be switched between the receive and transmit framer. E1 Receive framer will generate the PRBS pattern and insert it onto the receive backplane interface, and E1 Transmit Framer will be monitoring the transmit backplane interface for PRBS pattern and declare PRBS LOCK if PRBS has locked onto the input pattern. If PRBS switch is disabled, E1 Transmit framer will generate the PRBS pattern to the line interface and the receive framer will be monitoring the line for PRBS/QRTS pattern and declare PRBS LOCK if PRBS has locked onto the input pattern. 0 = Disables the PRBS Switch Feature. 1 = Enables the PRBS Switch Feature.
2	BER[1]	R/W	0	**Bit Error Rate** This bit is used to insert PRBS bit error at the rates presented at the table below. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 within this register). If the PRBS switch function is disabled, bit error will be inserted by the E1 transmit framer out to the line interface if this bit is enabled. If the PRBS switch function is enabled, bit error will be inserted by the E1 receive framer out to the receive backplane interface if this bit is enabled.
1	BER[0]	R/W	0	

BER[1:0]	BIT ERROR RATE
00	Disable Bit Error insertion to the transmit output or receive backplane interface
01	Bit Error is inserted to the transmit output or receive backplane interface at a rate of 1/1000 (one out of one Thousand)
10	Bit Error is inserted to the transmit output or receive backplane interface at a rate of 1/ 1,000,000 (one out of one million)
11	Disable Bit Error insertion to the transmit output or receive backplane interface

TABLE 29: PRBS CONTROL AND STATUS REGISTER 0 (PRBSCSR0) **HEX ADDRESS: 0XN121**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	UnFramedPRBS	R/W	0	**Unframed PRBS Pattern** This bit enables or disables unframed PRBS/QRTS pattern generation (i.e. All timeslots and framing bits are all PRBS/QRTS data). The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 within this register). If PRBS switch function is disabled, E1 Transmit Framer will generate an unframed PRBS 15 or QRTS pattern to the line side if this bit is enabled. If PRBS switch function is enabled, E1 Receive Framer will generate an unframed PRBS 15 or QRTS pattern to the receive backplane interface if this bit is enabled. 0 - Enables an unframed PRBS/QRTS pattern generation to the line interface or to the receive backplane interface 1 - Disables an unframed PRBS/QRTS pattern generation to the line interface or to the receive backplane interface

TABLE 30: RECEIVE INTERFACE CONTROL REGISTER (RICR) **HEX ADDRESS: 0XN122**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RxSyncFrD	R/W	0	**Receive Synchronous fraction data interface** This bit selects whether RxCHCLK or RxSERCLK will be used for fractional data output if receive fractional interface is enabled. If RxSERCLK is selected to clock out fractional data, RxCHCLK will be used as an enable signal 0 = Fractional data Is clocked out of the chip using RxChCLK if the receive fractional interface is enabled. 1 = Fractional data is clocked out of the chip using RxSerClk if the receive fractional interface is enabled. RxChClk is used as fractional data enable. ***NOTE:*** *The Time Slot Identifier Pins (RxChn[4:0]) still indicates the time slot number if the receive fractional data interface is not enabled. Fractional Interface can be enabled by setting RxFr2048 to 1*
6	Reserved	-	-	**Reserved**
5	RxPLClkEnb	R/W	0	**Receive payload clock enable** This bit configures the E1 framer to either output a regular clock or a payload clock on the receive serial clock (RxSERCLK) pin when RxSERCLK is configured to be an output. 0 = Configures the framer to output a 2.048MHz clock on the RxSERCLK pin when RxSERCLK is configured as an output. 1 = Configures the framer to output a 2.048MHz clock on the RxSERCLK pin when receiving payload bits. There will be gaps on the RxSERCLK output pin when receiving overhead bits.
4	RxFr2048	R/W	0	**Receive Fractional/Signaling Interface Enabled** This bit is used to enable or disable the receive fractional output interface, receive signaling output, the serial channel number output, as well as the 8kHz and the received recovered clock output. This bit only functions when the device is configured in non-high speed or multiplexed modes of operations. If the device is configured in base rate: 0 = configure the 5 time slot identifier pins (RxChn[4:0]) to output the channel number in parallel as usual. 1 = configure the 5 time slot identifier pins (RxChn[4:0]) into the following different functions: RxChn[0] becomes the Receive Serial SIgnaling output pin (RxSIG_n) for signaling outputs. Signaling data can now be output to the RxSIG pin if configured appropriately. RxChn[1] becomes the Receive Fractional Data Output pin (RxFrTD_n) for fractional data output. Fractional data can now be output to the RxFrTD pin if configured appropriately. RxChn[2] outputs the serial channel number RxChn[3] outputs an 8kHz clock signal. RxCHN[4] outputs the received recovered clock signal (2.048MHz for E1) ***NOTE:*** *This bit has no function in the high speed or multiplexed modes of operation. In high-speed or multiplexed modes, RxCHN[0] outputs the Signaling data and RxCHN[4] outputs the recovered clock.*

TABLE 30: RECEIVE INTERFACE CONTROL REGISTER (RICR) **HEX ADDRESS: 0XN122**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxICLKINV	N/A	0	**Receive Clock Inversion (Backplane Interface)** This bit selects whether data transition will happen on the rising or falling edge of the receive clock. 0 = Selects data transition happen on the rising edge of the receive clocks. 1 = Selects data transition happen on the falling edge of the receive clocks. ***NOTE:*** *This feature is only available for base rate configuration (i.e. non-highspeed, or non-multiplexed modes).*
2	RxMUXEN	R/W	0	**Receive Multiplexed Mode Enable** This bit enables or disables the multiplexed mode on the receive side. When multiplexed mode is enable, four channels data from the line side are multi-plexed onto one serial stream and output to the back-plane interface on RxSER. The backplane speed will become 16.384MHz once multiplexed mode is enabled. 0 = Disables the multiplexed mode. 1 = Enables the multiplexed mode.

TABLE 30: RECEIVE INTERFACE CONTROL REGISTER (RICR) **HEX ADDRESS: 0XN122**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxIMODE[1]	R/W	0	**Receive Interface Mode Selection** This bit determines the receive interface speed. The exact function of these two bits depends on whether Receive Multiplexed mode is enabled or disabled. Table 31 and Table 32 shows the functions of these two bits for non-multiplexed and multiplexed modes.:
0	RxIMODE[0]	R/W	0	

TABLE 31: RECEIVE INTERFACE SPEED WHEN MULTIPLEXED MODE IS DISABLED (TXMUXEN = 0)

RxIMODE[1:0]	RECEIVE INTERFACE SPEED
00	**2.048Mbit/s. (Base Rate Mode)** Receive backplane interface signals include: RxSERCLK is an input or output clock at 2.048MHz RxSYNC is an input or output signal which indicates the receive singe frame boundary RxSER is the base-rate data output
01	**2.048Mbit/s (High-speed MVIP Mode)** Receive Backplane Interface signals include: RxSERCLK is an input clock at 2.048MHz RxSYNC is an input signal which indicates the receive singe frame boundary RxSER is the high-speed data output
10	**4.096Mbit/s High-speed Mode:** Receive Backplane Interface signals include: RxSERCLK is an input clock at 4.096MHz RxSYNC is an input signal which indicates the receive singe frame boundary RxSER is the high-speed data output
11	**8.192Mbit/s High-speed Mode:** Receive Backplane Interface signals include: RxSERCLK is an input clock at 8.192MHz RxSYNC is an input signal which indicates the receive singe frame boundary RxSER is the high-speed data output

TABLE 30: RECEIVE INTERFACE CONTROL REGISTER (RICR) **HEX ADDRESS: 0XN122**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1-0	RxIMODE	R/W	0	**(Continued):** **TABLE 32: RECEIVE INTERFACE SPEED WHEN MULTIPLEXED MODE IS ENABLED (TXMUXEN = 1)** **TXIMODE[1:0]** — **TRANSMIT INTERFACE SPEED** 00 — Reserved 01 — **16.384MHz Bit-Multiplexed Mode** Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing the four-channel data into one 16.384MHz serial stream and output to channel 0 of the Receive Serial Output (RxSER). The RxSYNC signal pulses “High” during the framing bit of each E1 frame. 10 — **HMVIP High-Speed Multiplexed Mode**: Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing the four-channel data into one 16.384MHz serial stream and output to channel 0 of the Receive Serial Output (RxSER). The RxSYNC signal pulses “High” during the last two bits of the previous E1 frame and the first two bits of the current E1 frame. 11 — **H.100 High-Speed Multiplexed Mode**: Receive interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing the four-channel data into one 16.384MHz serial stream and output to channel 0 of the Receive Serial Output (RxSER). The RxSYNC signal pulses “High” during the last bit of the previous E1 frame and the first bit of the current E1 frame. **Receive Backplane Interface signals include:** RxSERCLK is an input clock at 16.384MHz RxSYNC is an input signal which indicates the multiplexed frame boundary. The length of RxSYNC depends on the multiplexed mode selected. RxSER is the high-speed data output ***NOTE:*** *In high speed mode, receive data is clocked out on the rising edge of the 16MHz clock edge.*

TABLE 33: PRBS CONTROL AND STATUS REGISTER 1 (PRBSCSR1) **HEX ADDRESS: 0XN123**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSTyp	R/W	0	**PRBS Pattern Type** This bit selects the type of PRBS pattern that the E1 Transmit/ Receive framer will generate or detect. PRBS 15 ($X^{15} + X^{14} +1$) Polynomial or QRTS (Quasi-Random Test Signal) Pattern can be generated by the transmit or receive framer depending on whether PRBS switch function is enabled or not (bit 3 in register 0xn121). If the PRBS Switch function is disabled, E1 transmit framer will generate either PRBS 15 or QRTS pattern and output to the line interface. PRBS 15 or QRTS pattern depends on the setting of this bit. If the PRBS Switch function is enabled, E1 receive framer will generate either PRBS 15 or QRTS pattern and output to the receive back plane interface. PRBS 15 or QRTS pattern depends on the setting of this bit. 0 = Enables the PRBS 15 ($X^{15} + X^{14} +1$) Polynomial generation. 1 = Enables the QRTS (Quasi-Random Test Signal) pattern generation.
6	ERRORIns	R/W	0	**Error Insertion** This bit is used to insert a single PRBS/QRTS error to the transmit or receive output depending on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If the PRBS Switch function is disabled, E1 transmit framer will insert a single PRBS/QRTS error and output to the line interface if this bit is enabled. If the PRBS Switch function is enabled, E1 receive framer will insert a single PRBS/QRTS error and output to the receive back plane interface if this bit is enabled. A ‘0’ to ‘1’ transition will cause one output bit inverted in the PRBS/ QRTS stream. This bit only works if PRBS generation is enabled.
5	DATAInv	R/W	0	**PRBS Data Invert:** This bit inverts the Transmit PRBS/QRTS output data and the Receive PRBS/QRTS input data. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If the PRBS Switch function is disabled and if this bit is enabled, E1 transmit framer will invert the PRBS/QRTS data before it outputs to the line interface, and the E1 receive framer will invert the incoming PRBS/QRTS data before it receives it. If the PRBS Switch function and this bit are both enabled, E1 receive framer will invert the PRBS/QRTS data before it outputs to the line interface, and the E1 transmit framer will invert the incoming PRBS/QRTS data before it receives it. 0 - Transmit and Receive Framer will not invert the Transmit PRBS/ QRTS and Receive PRBS data. 1 - Transmit and Receive Framer will invert the Transmit PRBS/ QRTS and Receive PRBS data.

TABLE 33: PRBS CONTROL AND STATUS REGISTER 1 (PRBSCSR1) **HEX ADDRESS: 0XN123**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	RxPRBSLock	RO	0	**Lock Status** This READ ONLY bit field indicates whether or not the Receive or Transmit PRBS lock has obtained. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If the PRBS Switch function is disabled, E1 receive framer will declare LOCK if PRBS/QRTS has locked onto the input pattern. If the PRBS Switch function is disabled, E1 transmit framer will declare LOCK if PRBS/QRTS has locked onto the input pattern. 0 = Indicates the Receive PRBS/QRTS has not Locked onto the input patterns. 1 = Indicates the Receive PRBS/QRTS has locked onto the input patterns.
3	RxPRBSEnb	R/W	0	**Receive PRBS Detection/Generation Enable** This bit enables or disables the receive PRBS/QRTS pattern detection or generation. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If the PRBS switch function is disabled and if this bit is enabled, E1 Receive Framer will detect the incoming PRBS/QRTS pattern from the line side and declare PRBS/QRTS lock if incoming data locks onto the PRBS/QRTS pattern. If the PRBS switch function and this bit are both enabled, E1 Transmit Framer will detect the incoming PRBS/QRTS pattern from the transmit backplane interface and declare PRBS/QRTS lock if incoming data locks onto the PRBS/QRTS pattern. 0 = Disables the Receive PRBS/QRTS pattern detection. 1 - Enables the Receive PRBS/QRTS pattern detection.
2	TxPRBSEnb	R/W	0	**Transmit PRBS Generation Enable** This bit enables or disables the Transmit PRBS pattern generator. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If PRBS switch function is disabled, E1 Transmit Framer will generate the PRBS 15 or QRTS pattern to the line side if this bit is enabled. If PRBS switch function is enabled, E1 Receive Framer will generate the PRBS 15 or QRTS pattern to the receive backplane interface if this bit is enabled. 0 = Disables the Transmit PRBS/QRTS pattern generator. 1 - Enables the Transmit PRBS/QRTS pattern generator.
1	RxBypass	R/W	0	**Receive Framer Bypass** This bit enables or disables the Receive E1 Framer bypass. 0 = Disables the Receive E1 framer Bypass. 1 - Enables the Receive E1 Framer Bypass
0	TxBypass	R/W	0	**Transmit Framer Bypass** This bit enables or disables the Transmit E1 Framer bypass. 0 = Disables the Transmit E1 framer Bypass. 1 - Enables the Transmit E1 Framer Bypass

TABLE 34: LOOPBACK CODE CONTROL REGISTER (LCCR) **HEX ADDRESS: 0XN124**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Reserved	-	-	**For T1 mode only**

TABLE 35: TRANSMIT LOOPBACK CODER REGISTER (TLCR) **HEX ADDRESS: 0XN125**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Reserved	-	-	**For T1 mode only**

TABLE 36: RECEIVE LOOPBACK ACTIVATION CODE REGISTER (RLACR) **HEX ADDRESS: 0XN126**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Reserved			**For T1 mode only**

TABLE 37: RECEIVE LOOPBACK DEACTIVATION CODE REGISTER (RLDCR) **HEX ADDRESS: 0XN127**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Reserved			**For T1 mode only**

TABLE 38: DEFECT DETECTION ENABLE REGISTER (DDER) **HEX ADDRESS: 0XN129**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	DEFDET	R/W	1	For defect detection per ANSI T1.231-1997 and T1.403-1999, user should leave this bit set to ‘1’.

TABLE 39: TRANSMIT Sa SELECT REGISTER (TSASR) **HEX ADDRESS: 0XN130**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSa8SEL	R/W	0	**Transmit Sa8 bit select** This bit determines whether National Bit (Sa8) is inserted from the transmit serial input (TxSER_n) pin or from the Transmit Sa8 register (Register address = 0xn137). 0 = Selects Sa 8 to be inserted from the Transmit Serial input (TxSER_n) input pin. 1 = Selects Sa 8 to be inserted from the Transmit Sa8 Register (Register address = 0xn137)
6	TxSa7SEL	R/W	0	**Transmit Sa7 bit select** This bit determines whether National Bit (Sa7) is inserted from the transmit serial input (TxSER_n) pin or from the Transmit Sa7 register (Register address = 0xn136). 0 = Selects Sa 7 to be inserted from the Transmit Serial input (TxSER_n) input pin. 1 = Selects Sa 7 to be inserted from the Transmit Sa7 Register (Register address = 0xn136)
5	TxSa6SEL	R/W	0	**Transmit Sa6 bit select** This bit determines whether National Bit (Sa6) is inserted from the transmit serial input (TxSER_n) pin or from the Transmit Sa6 register (Register address = 0xn135). 0 = Selects Sa 6 to be inserted from the Transmit Serial input (TxSER_n) input pin. 1 = Selects Sa 6 to be inserted from the Transmit Sa6 Register (Register address = 0xn135)
4	TxSa5SEL	R/W	0	**Transmit Sa5bit select** This bit determines whether National Bit (Sa5) is inserted from the transmit serial input (TxSER_n) pin or from the Transmit Sa5 register (Register address = 0xn134). 0 = Selects Sa 5 to be inserted from the Transmit Serial input (TxSER_n) input pin. 1 = Selects Sa 5 to be inserted from the Transmit Sa5 Register (Register address = 0xn134)
3	TxSa4SEL	R/W	0	**Transmit Sa4 bit select** This bit determines whether National Bit (Sa4) is inserted from the transmit serial input (TxSER_n) pin or from the Transmit Sa4 register (Register address = 0xn133). 0 = Selects Sa 4 to be inserted from the Transmit Serial input (TxSER_n) input pin. 1 = Selects Sa 4 to be inserted from the Transmit Sa4 Register (Register address = 0xn133)

TABLE 39: TRANSMIT Sa SELECT REGISTER (TSASR) **HEX ADDRESS: 0XN130**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	LB1ENB	R/W	0	**Local Loopback 1 auto enable** This bit enables or disables local loopback mode when the National bits (Sa5, Sa6) and the A bit (remote alarm bit) received from the transmit backplane interface follows a specific pattern. Local loopback is activated when the National Bits (Sa5, Sa 6) and A bit (remote alarm bit) follow the following pattern from the transmit serial input. (TxSER_n pin) Sa5 = 00000000 occur for 8 consecutive times Sa6 = 11111111 occur for 8 consecutive times A = 11111111 occur for 8 consecutive times ***NOTE:*** *This feature only works if Sa bits are provided from the transmit serial input pin (TxSER_n)*
1	LB2ENB	R/W	0	**Local Loopback 2 auto enable** This bit enables or disables local loopback mode when the National bits (Sa5, Sa6) received from the transmit backplane interface follows a specific pattern. Local loopback is activated when the National Bits (Sa5, Sa 6) and A bit (remote alarm bit) follow the following pattern from the transmit serial input. (TxSER_n pin) Sa5 = 00000000 occur for 8 consecutive times, and Sa6 = 10101010 occur for 8 consecutive times, and A = 11111111 occur for 8 consecutive times ***NOTE:*** *This feature only works if Sa bits are provided from the transmit serial input pin (TxSER_n)*
0	LBRENB	R/W	0	**Local Loopback release enable** This bit releases the local loopback mode when the National bits (Sa5, Sa6) received from the transmit backplane interface follows a specific pattern. Local loopback is released when the National Bits (Sa5, Sa 6) follow the following pattern from the transmit serial input. (TxSER_n pin) Sa5 = 00000000 occur for 8 consecutive times Sa6 = 00000000 occur for 8 consecutive times ***NOTE:*** *This feature only works if Sa bits are provided from the transmit serial input pin (TxSER_n)*

TABLE 40: TRANSMIT Sa AUTO CONTROL REGISTER 1 (TSACR1) **HEX ADDRESS: 0XN131**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LOSLFA_1_ENB	R/W	0	**LOS/LFA 1 automatic transmission** This bit enables the automatic Sa-bit transmission upon detecting Loss of Signal (LOS) or Loss of frame alignment (LFA) condition. Upon detecting Loss of Signal or Loss of Frame alignment condition, E1 framer will transmit the Sa5 bit as '1', and Sa6 bit as '0' pattern. See Table 41 for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS or LFA conditions.
6	LOS_1_ENB	R/W	0	**LOS 1 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) condition. Upon detecting Loss of Signal condition, E1 framer will transmit the Alarm bit (A bit) as '1', Sa5 bit as '1', and Sa6 bit as '1110' pattern. See Table 41 for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS condition.
5	LOSLFA_2_ENB	R/W	0	**LOS/LFA 2 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) or Loss of frame alignment (LFA) condition. Upon detecting Loss of Signal or Loss of Frame alignment condition, E1 framer will transmit the Alarm bit (A bit) as '1', Sa5 bit as '0', and Sa6 bit as '0' pattern. See Table 41 for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS or LFA conditions.
4	LOSLFA_3_ENB	R/W	0	**LOS/LFA 3 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) or Loss of frame alignment (LFA) condition. Upon detecting Loss of Signal or Loss of Frame alignment condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', and Sa6 bit as '1100' pattern. See Table 41 for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS/LFA conditions.
3	LOSLFA_4_ENB	R/W	0	**LOS/LFA 4 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) or Loss of frame alignment (LFA) condition. Upon detecting Loss of Signal or Loss of Frame alignment condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', and Sa6 bit as '1110' pattern. See Table 41 for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS/LFA conditions.

TABLE 40: TRANSMIT Sa AUTO CONTROL REGISTER 1 (TSACR1) **HEX ADDRESS: 0XN131**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	NOP_ENB	R/W	0	**No power automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Power condition. The XRT86VL34 device recognizes the Loss of Power condition by monitoring the Loss of Power input pin (pin AB1). When the Loss of Power input pin is HIGH indicates a Loss of Power condition is occurring. When the Loss of Power input pin is LOW indicates no Loss of Power condition detected. Upon detecting Loss of Power condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', and Sa6 bit as '1000' pattern. See **Table 41** for the transmit Sa5, Sa6, and A bit pattern upon detecting Loss of Power condition.
1	NOP_LOSLFA_ENB	R/W	0	**No power and LOS/LFA automatic transmission** This bit enables the auto Sa-bit transmission upon detecting the following two conditions: **1.** Upon Loss of Power and Loss of Signal (LOS) or **2.** Upon Loss of Power and Loss of frame alignment (LFA) When the E1 framer detects any one of the above two conditions, E1 framer will transmit the Alarm bit (A bit) as '1', Sa5 bit as '1', Sa6 bit as '1000' pattern. See **Table 41** for the transmit Sa5, Sa6, and A bit format upon detecting loss of power and LOS/LFA conditions.
0	LOS_2_ENB	R/W	0	**LOS 3 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) condition. Upon detecting Loss of Signal condition, E1 framer will transmit the Sa5 and Sa6 bit as an Auxiliary (10101010...) pattern See **Table 41** for the transmit Sa5, Sa6, and A bit format upon detecting LOS condition.

The following table demonstrates the conditions on the receive side which trigger the Automatic Sa, and A bit transmission when TSACR1 bits are enabled.

TABLE 41: CONDITIONS ON RECEIVE SIDE WHEN TSACR1 BITS ARE ENABLED

CONDITIONS	ACTIONS - SENDING PATTERN			COMMENTS
	A	SA5	SA6	
LOSLFA_1_ENB: Loss of signal or Loss of frame alignment	X	1	0000	LOS/LFA at TE (FC2)
LOS_1_ENB: Loss of signal	1	1	1110	LOS (FC3)
LOSLFA_2_ENB: LOS or LFA	1	0	0000	LOS/LFA (FCL)
LOSLFA_3_ENB: LOS or LFA	0	1	1100	LOS/LFA (FC4)
LOSLFA_4_ENB: LOS or LFA	0	1	1110	LOS/LFA (FC3&FC4)
NOP_ENB: Loss of power	0	1	1000	Loss of power at NT1
NOP_LOSLFA_ENB: Loss of power and LOS or LFA	1	1	1000	Loss of power and LOS/LFA
LOS_2_ENB: LOS	AUXP pattern			LOS (FC1). Transmit AUXP pattern

TABLE 42: TRANSMIT Sa AUTO CONTROL REGISTER 2 (TSACR2) **HEX ADDRESS: 0XN132**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	AIS_1_ENB	R/W	0	**AIS reception** This bit enables the automatic Sa-bit transmission upon detecting AIS condition. Upon detecting the AIS condition, E1 framer will transmit the Alarm bit (A bit) as '1', Sa5 bit as '1', and Sa6 bit as '1'. See Table 43 for the transmit Sa5, Sa6, and A bit pattern upon detecting AIS condition.
6	AIS_2_ENB	R/W	0	**AIS reception** This bit enables the automatic Sa-bit transmission upon detecting AIS condition. Upon detecting the AIS condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', and Sa6 bit as '1'. See Table 43 for the transmit Sa5, Sa6, and A bit pattern upon detecting AIS condition.
5	Reserved	-	-	**Reserved**
4	Reserved	-	-	**Reserved**
3	CRCREP_ENB[1]	R/W	0	**CRC report** These two bits enable the automatic Sa-bit transmission upon detecting Far End Block Error (i.e. received E bit = 0). Upon detecting the Far End Block Error (FEBE) condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', Sa6 bit as '0000', and E bit as '0' pattern if these two bits are set to '01'. If these two bits are set to '10', E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '0', Sa6 bit as '0000', and E bit as '0' pattern upon detecting the Far End Block Error (FEBE). If these two bits are set to '11', E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', Sa6 bit as '0001', and E bit as '1' pattern upon detecting the Far End Block Error (FEBE). See Table 43 for the transmit Sa5, Sa6, E, and A bit pattern upon detecting FEBE condition.
2	CRCREP_ENB[0]	R/W	0	
1	CRCDET_ENB	R/W	0	**CRC detection** This bit enables the automatic Sa-bit transmission upon detecting CRC-4 error condition. Upon detecting CRC-4 error condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', Sa6 bit as '0010', and E bit as '1' pattern. See Table 43 for the transmit Sa5, Sa6, E, and A bit pattern upon detecting CRC-4 error condition.
0	CRCREC AND DET_ENB	R/W	0	**CRC report and detect** This bit enables automatic Sa-bit transmission upon detecting both Far End Block Error (FEBE) and CRC-4 error conditions. Upon detecting both Far End Block Error (FEBE) and CRC-4 error condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', Sa6 bit as '0011', and E bit as '1' pattern. See Table 43 for the transmit Sa5, Sa6, E, and A bit pattern upon detecting both FEBE and CRC-4 error conditions.

The following table demonstrates the conditions on receive side which trigger the Automatic Sa, E, and A bits transmission when TSACR2 bits are enabled.

TABLE 43: CONDITIONS ON RECEIVE SIDE WHEN TSACR2 BITS ENABLED

CONDITIONS	ACTIONS - SENDING PATTERN FOR			
	A	SA5	SA6	E
AIS_1_ENB	1	1	1111	X
AIS_2_ENB	0	1	1111	x
CRCREP_ENB = 01, CRC reported (E = 0)	0	1	0000	0
CRCREP_ENB = 10, CRC reported	0	0	0000	0
CRCREP_ENB = 11, CRC reported	0	1	0001	1
CRCDET_ENB	0	1	0010	1
CRCDET/REP_ENB	0	1	0011	1

TABLE 44: TRANSMIT Sa4 REGISTER (TSA4R) **HEX ADDRESS: 0XN133**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa4[7:0]	R/W	11111111	**Transmit Sa4 Sequence** The content of this register sources the transmit Sa4 bits if data link selects Sa 4 bit for transmission and if Sa4 is inserted from register. (i.e. TxSa4ENB bit in register 0xn10A = 1 and TxSa4SEL bit in register 0xn130 = 1). Bit 7 of this register is transmitted in the Sa4 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa4 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 45: TRANSMIT Sa5 REGISTER (TSA5R) **HEX ADDRESS: 0XN134**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa5[7:0]	R/W	11111111	**Transmit Sa5 Sequence** The content of this register sources the transmit Sa5 bits if data link selects Sa 5 bit for transmission and if Sa5 is inserted from register. (i.e. TxSa5ENB bit in register 0xn10A = 1 and TxSa5SEL bit in register 0xn130 = 1). Bit 7 of this register is transmitted in the Sa5 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa5 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 46: TRANSMIT Sa6 REGISTER (TSA6R) **HEX ADDRESS: 0XN135**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa6[7:0]	R/W	11111111	**Transmit Sa6 Sequence** The content of this register sources the transmit Sa6 bits if data link selects Sa 6 bit for transmission and if Sa6 is inserted from register. (i.e. TxSa6ENB bit in register 0xn10A = 1 and TxSa6SEL bit in register 0xn130 = 1). Bit 7 of this register is transmitted in the Sa6 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa6 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 47: TRANSMIT Sa7 REGISTER (TSA7R) **HEX ADDRESS: 0XN136**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa7[7:0]	R/W	11111111	**Transmit Sa7 Sequence** The content of this register sources the transmit Sa7 bits if data link selects Sa 7 bit for transmission and if Sa7 is inserted from register. (i.e. TxSa7ENB bit in register 0xn10A = 1 and TxSa7SEL bit in register 0xn130 = 1). Bit 7 of this register is transmitted in the Sa7 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa7 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 48: TRANSMIT Sa8 REGISTER (TSA8R) **HEX ADDRESS: 0XN137**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa8[7:0]	R/W	11111111	**Transmit Sa8 Sequence** The content of this register sources the transmit Sa8 bits when data link selects Sa 8 bit for transmission and if Sa8 is inserted from register. (i.e. TxSa8ENB bit in register 0xn10A = 1 and TxSa8SEL bit in register 0xn130 = 1). Bit 7 of this register is transmitted in the Sa8 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa8 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 49: RECEIVE SA4 REGISTER (RSA4R) **HEX ADDRESS: 0XN13B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa4[7:0]	RO	00000000	**Received Sa4 Sequence** The content of this register stores the Sa 4 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa4 bits if data link selects Sa4 bit for reception. (i.e.RxSa4ENB bit in register 0xn10Ch = 1). Bit 7 of this register indicates the received Sa4 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa4 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 50: RECEIVE SA5 REGISTER (RSA5R) **HEX ADDRESS: 0XN13C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa5[7:0]	RO	00000000	**Received Sa5 Sequence** The content of this register stores the Sa 5 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa5 bits if data link selects Sa5 bit for reception. (i.e.RxSa5ENB bit in register 0xn10Ch = 1). Bit 7 of this register indicates the received Sa5 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa5 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 51: RECEIVE SA6 REGISTER (RSA6R) **HEX ADDRESS: 0Xn13D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa6[7:0]	RO	00000000	**Received Sa6 Sequence** The content of this register stores the Sa 6 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa6 bits if data link selects Sa6 bit for reception. (i.e.RxSa6ENB bit in register 0xn10Ch = 1). Bit 7 of this register indicates the received Sa6 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa6 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 52: RECEIVE SA7 REGISTER (RSA7R) **HEX ADDRESS: 0XN13E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa7[7:0]	RO	00000000	**Received Sa7 Sequence** The content of this register stores the Sa 7 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa7 bits if data link selects Sa7 bit for reception. (i.e.RxSa7ENB bit in register 0xn10Ch = 1). Bit 7 of this register indicates the received Sa7 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa7 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 53: RECEIVE SA8 REGISTER (RSA8R) **HEX ADDRESS: 0XN13F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa8[7:0]	RO	00000000	**Received Sa8 Sequence** The content of this register stores the Sa 8 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa8 bits if data link selects Sa8 bit for reception. (i.e.RxSa8ENB bit in register 0xn10Ch = 1). Bit 7 of this register indicates the received Sa8 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa8 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 54: DATA LINK CONTROL REGISTER (DLCR2) **HEX ADDRESS: 0XN143**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	Reserved. Please set this bit to'0' for normal operation.
6	MOS ABORT Disable	R/W	0	**MOS ABORT Disable:** This bit permits the user to either enable or disable the "Automatic MOS ABORT" feature within Transmit HDLC Controller # 2. If the user enables this feature, then Transmit HDLC Controller block # 2 will automatically transmit the ABORT Sequence (e.g., a zero followed by a string of 7 consecutive "1s") whenever it abruptly transitions from transmitting a MOS type of message, to transmitting a BOS type of message. If the user disables this feature, then the Transmit HDLC Controller Block # 2 will NOT transmit the ABORT sequence, whenever it abruptly transitions from transmitting a MOS-type of message to transmitting a BOS-type of message. 0 - Enables the "Automatic MOS Abort" feature 1 - Disables the "Automatic MOS Abort" feature
5	Rx_FCS_DIS	R/W	0	**Receive Frame Check Sequence (FCS) Verification Enable/Disable** This bit permits the user to configure the Receive HDLC Controller Block # 2 to compute and verify the FCS value within each incoming LAPD message frame. 0 - Enables FCS Verification 1 - Disables FCS Verification
4	AutoRx	R/W	0	**Auto Receive LAPD Message** This bit configures the Receive HDLC Controller Block #2 to discard any incoming BOS or LAPD Message frame that exactly match which is currently stored in the Receive HDLC2 buffer. 0 = Disables this "AUTO DISCARD" feature 1 = Enables this "AUTO DISCARD" feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** This bit configures the Transmit HDLC Controller Block #2 to transmit an ABORT sequence (string of 7 or more consecutive 1's) to the Remote terminal. 0 - Configures the Transmit HDLC Controller Block # 2 to function normally (e.g., not transmit the ABORT sequence). 1 - Configures the Transmit HDLC Controller block # 2 to transmit the ABORT Sequence.

TABLE 54: DATA LINK CONTROL REGISTER (DLCR2) **HEX ADDRESS: 0XN143**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** This bit configures the Transmit HDLC Controller Block #2 to unconditionally transmit a repeating string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. In normal conditions, the Transmit HDLC Controller block will repeatedly transmit the Flag Sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this “Transmit Idle Sequence” feature, then the Transmit HDLC Controller block will UNCONDITIONALLY transmit a repeating stream of the Flag Sequence octet (thereby overwriting all outbound MOS data-link messages). 0 - Configures the Transmit HDLC Controller Block # 2 to transmit data-link information in a “normal” manner. 1 - Configures the Transmit HDLC Controller block # 2 to transmit a repeating string of Flag Sequence Octets (0x7E). ***NOTE:*** *This bit is ignored if the* Transmit *HDLC2 controller is operating in the BOS Mode - bit 0 (MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with Frame Check Sequence (FCS)** This bit permits the user to configure the Transmit HDLC Controller block # 2 to compute and append FCS octets to the “back-end” of each outbound MOS data-link message. 0 - Configures the Transmit HDLC Controller block # 2 to NOT compute and append the FCS octets to the back-end of each outbound MOS data-link message. 1 - Configures the Transmit HDLC Controller block # 2 TO COMPUTE and append the FCS octets to the back-end of each outbound MOS data-link message. ***NOTE:*** *This bit is ignored if the transmit HDLC2 controller has been configured to operate in the BOS mode - bit 0 (MOS/BOS) within this register is set to 0.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Send** This bit permits the user to enable LAPD transmission through HDLC Controller Block # 2 using either BOS (Bit-Oriented Signaling) or MOS (Message-Oriented Signaling) frames. 0 - Transmit HDLC Controller block # 2 BOS message Send. 1 - Transmit HDLC Controller block # 2 MOS message Send. ***NOTE:*** *This is not an Enable bit. This bit must be set to "0" each time a BOS is to be sent.*

TABLE 55: TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR2) **HEX ADDRESS: 0XN144**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxHDLC2 BUFAvail/ BUFSel	R/W	0	**Transmit HDLC2 Buffer Available/Buffer Select** This bit has different functions, depending upon whether the user is writing to or reading from this register, as depicted below. **If the user is writing data into this register bit:** 0 - Configures the Transmit HDLC2 Controller to read out and transmit the data, residing within “Transmit HDLC2 Buffer # 0", via the Data Link channel to the remote terminal equipment. 1 - Configures the Transmit HDLC2 Controller to read out and transmit the data, residing within the “Transmit HDLC2 Buffer #1”, via the Data Link channel to the remote terminal equipment. **If the user is reading data from this register bit:** 0 - Indicates that “Transmit HDLC2 Buffer # 0" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC2 Message Buffer, he/she should proceed to write this message into “Transmit HDLC2 Buffer # 0" - Address location: 0xn600. 1 - Indicates that “Transmit HDLC2 Buffer # 1" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC2 Message Buffer, he/she should proceed to write this message into “Transmit HDLC2 Buffer # 1" - Address location: 0xn700. ***NOTE:*** *If one of these Transmit HDLC2 buffers contain a message which has yet to be completely read-in and processed for transmission by the Transmit HDLC2 controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in-use buffer is not permitted.*
6-0	TDLBC[6:0]	R/W	0000000	**Transmit HDLC2 Message - Byte Count** The exact function of these bits depends on whether the Transmit HDLC 2 Controller is configured to transmit MOS or BOS messages to the Remote Terminal Equipment. **In BOS MODE:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Transmit HDLC2 controller generates the Transmit End of Transfer (TxEOT) interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. **In MOS MODE:** These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, Control field, however, it does not include the FCS bytes.

TABLE 56: RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR2) **HEX ADDRESS: 0XN145**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC2 Buffer-Pointer** This bit Identifies which Receive HDLC2 buffer contains the most recently received HDLC2 message. 0 - Indicates that Receive HDLC2 Buffer # 0 contains the contents of the most recently received HDLC message. 1 - Indicates that Receive HDLC2 Buffer # 1 contains the contents of the most recently received HDLC message.
6-0	RDLBC[6:0]	R/W	0000000	**Receive HDLC Message - byte count** The exact function of these bits depends on whether the Receive HDLC Controller Block #2 is configured to receive MOS or BOS messages. **In BOS Mode:** These seven bits contain the number of repetitions the BOS message must be received before the Receive HDLC2 controller generates the Receive End of Transfer (RxEOT) interrupt. If these bits are set to “0000000”, the message will be received indefinitely and no Receive End of Transfer (RxEOT) interrupt will be generated. **In MOS Mode:** These seven bits contain the size in bytes of the HDLC2 message that has been received and written into the Receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control field, AND the FCS bytes.

TABLE 57: DATA LINK CONTROL REGISTER (DLCR3) **HEX ADDRESS: 0XN153**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	Reserved. Please set this bit to'0' for normal operation.
6	MOS ABORT Disable	R/W	0	**MOS ABORT Disable:** This bit permits the user to either enable or disable the "Automatic MOS ABORT" feature within Transmit HDLC Controller # 3. If the user enables this feature, then Transmit HDLC Controller block # 3 will automatically transmit the ABORT Sequence (e.g., a zero followed by a string of 7 consecutive "1s") whenever it abruptly transitions from transmitting a MOS type of message, to transmitting a BOS type of message. If the user disables this feature, then the Transmit HDLC Controller Block # 3 will NOT transmit the ABORT sequence, whenever it abruptly transitions from transmitting a MOS-type of message to transmitting a BOS-type of message. 0 - Enables the "Automatic MOS Abort" feature 1 - Disables the "Automatic MOS Abort" feature
5	Rx_FCS_DIS	R/W	0	**Receive Frame Check Sequence (FCS) Verification Enable/Disable** This bit permits the user to configure the Receive HDLC Controller Block # 3 to compute and verify the FCS value within each incoming LAPD message frame. 0 - Enables FCS Verification 1 - Disables FCS Verification
4	AutoRx	R/W	0	**Auto Receive LAPD Message** This bit configures the Receive HDLC Controller Block #3 to discard any incoming BOS or LAPD Message frame that exactly match which is currently stored in the Receive HDLC1 buffer. 0 = Disables this "AUTO DISCARD" feature 1 = Enables this "AUTO DISCARD" feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** This bit configures the Transmit HDLC Controller Block #3 to transmit an ABORT sequence (string of 7 or more consecutive 1's) to the Remote terminal. 0 - Configures the Transmit HDLC Controller Block # 3 to function normally (e.g., not transmit the ABORT sequence). 1 - Configures the Transmit HDLC Controller block # 3 to transmit the ABORT Sequence.

TABLE 57: DATA LINK CONTROL REGISTER (DLCR3) **HEX ADDRESS: 0XN153**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** This bit configures the Transmit HDLC Controller Block #3 to unconditionally transmit a repeating string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. In normal conditions, the Transmit HDLC Controller block will repeatedly transmit the Flag Sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this “Transmit Idle Sequence” feature, then the Transmit HDLC Controller block will UNCONDITIONALLY transmit a repeating stream of the Flag Sequence octet (thereby overwriting all outbound MOS data-link messages). 0 - Configures the Transmit HDLC Controller Block # 3 to transmit data-link information in a “normal” manner. 1 - Configures the Transmit HDLC Controller block # 3 to transmit a repeating string of Flag Sequence Octets (0x7E). ***NOTE:*** *This bit is ignored if the* Transmit *HDLC3 controller is operating in the BOS Mode - bit 0 (MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with Frame Check Sequence (FCS)** This bit permits the user to configure the Transmit HDLC Controller block # 3 to compute and append FCS octets to the “back-end” of each outbound MOS data-link message. 0 - Configures the Transmit HDLC Controller block # 3 to NOT compute and append the FCS octets to the back-end of each outbound MOS data-link message. 1 - Configures the Transmit HDLC Controller block # 3 TO COMPUTE and append the FCS octets to the back-end of each outbound MOS data-link message. ***NOTE:*** *This bit is ignored if the transmit HDLC3 controller has been configured to operate in the BOS mode - bit 0 (MOS/BOS) within this register is set to 0.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Send** This bit permits the user to enable LAPD transmission through HDLC Controller Block # 3 using either BOS (Bit-Oriented Signaling) or MOS (Message-Oriented Signaling) frames. 0 - Transmit HDLC Controller block # 3 BOS message Send. 1 - Transmit HDLC Controller block # 3 MOS message Send. ***NOTE:*** *This is not an Enable bit. This bit must be set to "0" each time a BOS is to be sent.*

TABLE 58: TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR3) **HEX ADDRESS: 0XN154**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxHDLC3 BUFAvail/ BUFSel	R/W	0	**Transmit HDLC3 Buffer Available/Buffer Select** This bit has different functions, depending upon whether the user is writing to or reading from this register, as depicted below. **If the user is writing data into this register bit:** 0 - Configures the Transmit HDLC3 Controller to read out and transmit the data, residing within “Transmit HDLC3 Buffer # 0", via the Data Link channel to the remote terminal equipment. 1 - Configures the Transmit HDLC3 Controller to read out and transmit the data, residing within the “Transmit HDLC3 Buffer #1”, via the Data Link channel to the remote terminal equipment. **If the user is reading data from this register bit:** 0 - Indicates that “Transmit HDLC3 Buffer # 0" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC3 Message Buffer, he/she should proceed to write this message into “Transmit HDLC3 Buffer # 0" - Address location: 0xn600. 1 - Indicates that “Transmit HDLC3 Buffer # 1" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC3 Message Buffer, he/she should proceed to write this message into “Transmit HDLC3 Buffer # 1" - Address location: 0xn700. ***NOTE:*** *If one of these Transmit HDLC3 buffers contain a message which has yet to be completely read-in and processed for transmission by the Transmit HDLC3 controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in-use buffer is not permitted.*
6-0	TDLBC[6:0]	R/W	0000000	**Transmit HDLC3 Message - Byte Count** The exact function of these bits depends on whether the Transmit HDLC 3 Controller is configured to transmit MOS or BOS messages to the Remote Terminal Equipment. **In BOS MODE:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Transmit HDLC3 controller generates the Transmit End of Transfer (TxEOT) interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. **In MOS MODE:** These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, Control field, however, it does not include the FCS bytes.

TABLE 59: RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR3) **HEX ADDRESS: 0XN155**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC3 Buffer-Pointer** This bit Identifies which Receive HDLC3 buffer contains the most recently received HDLC1 message. 0 - Indicates that Receive HDLC3 Buffer # 0 contains the contents of the most recently received HDLC message. 1 - Indicates that Receive HDLC3 Buffer # 1 contains the contents of the most recently received HDLC message.
6-0	RDLBC[6:0]	R/W	0000000	**Receive HDLC Message - byte count** The exact function of these bits depends on whether the Receive HDLC Controller Block #3 is configured to receive MOS or BOS messages. **In BOS Mode:** These seven bits contain the number of repetitions the BOS message must be received before the Receive HDLC3 controller generates the Receive End of Transfer (RxEOT) interrupt. If these bits are set to “0000000”, the message will be received indefinitely and no Receive End of Transfer (RxEOT) interrupt will be generated. **In MOS Mode:** These seven bits contain the size in bytes of the HDLC3 message that has been received and written into the Receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control field, AND the FCS bytes.

TABLE 60: DEVICE ID REGISTER (DEVID) **HEX ADDRESS: 0XN1FE**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	DEVID[7:0]	RO	0x3A	**DEVID** This register is used to identify the XRT86VL34 Framer/LIU. The value of this register is 0x3Ah.

TABLE 61: REVISION ID REGISTER (REVID) **HEX ADDRESS: 0XN1FF**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	REVID[7:0]	RO	00000001	**REVID** This register is used to identify the revision number of the XRT86VL34. The value of this register for the first revision is A - 0x01h. ***NOTE:*** *The content of this register is subject to change when a newer revision of the device is issued.*

TABLE 62: TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) HEX ADDRESS: 0Xn300 TO 0xn31F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LAPDcntl[1]	R/W	1	**Transmit LAPD Control** These bits select which one of the three Transmit LAPD controller is configured to use D/E time slot (Octets 0-31) for transmitting LAPD messages. The following table presents the different settings of these two bits. **LAPDCNTL[1:0]** — **LAPD CONTROLLER SELECTED** 00 — Transmit LAPD Controller 1 01 — Transmit LAPD Controller 2 10 — The TxDE[1:0] bits in the Transmit Signaling and Data Link Select Register (TSDLSR - Register Address - 0xn10A, bit 3-2) determine the data source for D/E time slots. 11 — Transmit LAPD Controller 3 ***NOTE:*** *All three Transmit LAPD Controllers can use D/E timeslots for transmission. However, only Transmit LAPD Controller 1 can use datalink for transmission. Register 0xn300 represents D/E time slot 0, and 0xn31F represents D/E time slot 31.*
6	LAPDcntl[0]		0	
5-4	Reserved	-	-	Reserved (For T1 mode only)

TABLE 62: TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) **HEX ADDRESS: 0Xn300 TO 0xn31F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-0	TxCond(3:0)	R/W	0000	**Transmit Channel Conditioning for Timeslot 0 to 31** These bits allow the user to substitute the input PCM data (Octets 0-31) with internally generated Conditioning Codes prior to transmission to the remote terminal equipment on a per-channel basis. The table below presents the different conditioning codes based on the setting of these bits. ***NOTE:*** *Register address 0xn300 represents time slot 0, and address 0xn31F represents time slot 31.*

TXCOND[1:0]	CONDITIONING CODES
0x0 / 0xE	Contents of timeslot octet are unchanged.
0x1	All 8 bits of the selected timeslot octet are inverted (1's complement) OUTPUT = (TIME_SLOT_OCTET) XOR 0xFF
0x2	Even bits of the selected timeslot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0xAA
0x3	Odd bits of the selected time slot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0x55
0x4	Contents of the selected timeslot octet will be substituted with the 8 -bit value in the Transmit Programmable User Code Register (0xn320-0xn337),
0x5	Contents of the timeslot octet will be substituted with the value 0x7F (BUSY Code)
0x6	Contents of the timeslot octet will be substituted with the value 0xFF (VACANT Code)
0x7	Contents of the timeslot octet will be substituted with the BUSY time slot code (111#_####), where ##### is the Timeslot number
0x8	Contents of the timeslot octet will be substituted with the MOOF code (0x1A)
0x9	Contents of the timeslot octet will be substituted with the A-Law Digital Milliwatt pattern
0xA	Contents of the timeslot octet will be substituted with the μ-Law Digital Milliwatt pattern
0xB	The MSB (bit 1) of input data is inverted
0xC	All input data except MSB is inverted
0xD	Contents of the timeslot octet will be substituted with the PRBS $X^{15} + X^{14}$ + 1/QRTS pattern ***NOTE:*** *PRBS $X^{15} + X^{14}$ + 1 or QRTS pattern depends on PRBSType selected in the register 0xn123 - bit 7*
0xF	D/E time slot - The TxSIGDL[2:0] bits in the Transmit Signaling and Data Link Select Register (0xn10A) will determine the data source for D/E time slots.

TABLE 63: TRANSMIT USER CODE REGISTER 0 - 31 (TUCR 0-31) **HEX ADDRESS: 0XN320 TO 0XN33F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TUCR[7:0]	R/W	b00010111	**Transmit Programmable User code.** These eight bits allow users to program any code in this register to replace the input PCM data when the Transmit Channel Control Register (TCCR) is configured to replace timeslot octet with programmable user code. (i.e. if TCCR is set to '0x4') The default value of this register is an IDLE Code (b00010111).

TABLE 64: TRANSMIT SIGNALING CONTROL REGISTER 0-31 (TSCR 0-31) **HEX ADDRESS: 0XN340 TO 0XN35F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	A (x)	R/W	See Note	**Transmit Signaling bit A or x bit** This bit allows users to provide signaling Bit A for octets 0-31 if Channel Associated Signaling (CAS) is enabled and if signaling data is inserted from TSCR register (TxSIGSRC[1:0] = 01 in this register) ***NOTE:*** *Users must write to TSCR0 (Address 0xn340) the correct CAS alignment bits (0 bits) in order to get CAS SYNC at the remote terminal. The xyxx bits can be programmed by writing to TSCR16 (0xn350) and programming the TxSIGSRC[1:0] bits within this register to 'b11'.*
6	B (y)	R/W	See Note	**Transmit Signaling bit B or y bit** This bit allows users to provide signaling Bit B for octets 0-31 if Channel Associated Signaling (CAS) is enabled and if signaling data is inserted from TSCR register (TxSIGSRC[1:0] = 01 in this register) ***NOTE:*** *Users must write to TSCR0 (Address 0xn340) the correct CAS alignment bits (0 bits) in order to get CAS SYNC at the remote terminal. The xyxx bits can be programmed by writing to TSCR16 (0xn350) and programming the TxSIGSRC[1:0] bits within this register to 'b11'.*
5	C (x)	R/W	See Note	**Transmit Signaling bit C or x bit** This bit allows users to provide signaling Bit C for octets 0-31 if Channel Associated Signaling (CAS) is enabled and if signaling data is inserted from TSCR register (TxSIGSRC[1:0] = 01 in this register) ***NOTE:*** *Users must write to TSCR0 (Address 0xn340) the correct CAS alignment bits (0 bits) in order to get CAS SYNC at the remote terminal. The xyxx bits can be programmed by writing to TSCR16 (0xn350) and programming the TxSIGSRC[1:0] bits within this register to 'b11'.*
4	D (x)	R/W	See Note	**Transmit Signaling bit D or x bit** This bit allows users to provide signaling Bit D in for octets 0-31 if Channel Associated Signaling (CAS) is enabled and if signaling data is inserted from TSCR register (TxSIGSRC[1:0] = 01 in this register) ***NOTE:*** *Users must write to TSCR0 (Address 0xn340) the correct CAS alignment bits (0 bits) in order to get CAS SYNC at the remote terminal. The xyxx bits can be programmed by writing to TSCR16 (0xn350) and programming the TxSIGSRC[1:0] bits within this register to 'b11'.*
3	Reserved	-	See Note	**Reserved**
2	Reserved	-	See Note	**Reserved**

TABLE 64: TRANSMIT SIGNALING CONTROL REGISTER 0-31 (TSCR 0-31) **HEX ADDRESS: 0XN340 TO 0XN35F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	TxSIGSRC[1]	R/W	See Note	**Channel signaling control** These bits determine the source for signaling information. The table below presents the different sources for signaling information corresponding to different settings of these two bits.
0	TxSIGSRC[0]	R/W	See Note	

TXSIGSRC[1:0]	SIGNALING SOURCE SELECTED
00	Signaling data is inserted from input PCM data (TxSERn pin)
01	Signaling data is inserted from this register (TSCRs).
10	Signaling data is inserted from the transmit Overhead input pin (TxOH_n) if XRT86VL34 is configured in the base rate configuration and if the Transmit Signaling Interface bit is disabled. (i.e. TxMUXEN bit = 0, TxI-MODE[1:0] = 00, and TxFr2048 bit = 0 in the Transmit Interface Control Register (TICR) Register 0xn120). If the Transmit Signaling Interface bit is enabled (i.e. TxFr2048 bit = 1 in the Transmit Interface Control Register (TICR) Register 0xn120), signaling data will be inserted from the Transmit Signaling input pin (TxSIG_n)
11	No signaling data is inserted into the input PCM data. Setting these two bits to '11' will configure the xyxx bits only, where x bits are inserted from this register (TSCR) and y bit reflects the alarm condition.

NOTE: *The default value for register address 0xn340 = 0x01, 0xn341-0xn34F = 0xD0, 0xn350 = 0xB3, 0xn351-0xn35F = 0xD0*

TABLE 65: RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-31) **HEX ADDRESS: 0XN360 TO 0XN37F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LAPDcntl[1]	R/W	1	**Receive LAPD Control** These bits select which one of the three Receive LAPD controller will be configured to use D/E time slot (Octets 0-23) for receiving LAPD messages. **LAPDCNTL[1:0]** — **RECEIVE LAPD CONTROLLER SELECTED** 00 — Receive LAPD Controller 1 01 — Receive LAPD Controller 2 10 — The RxSIGDL[1:0] bits in the Receive Signaling and Data Link Select Register (RSDLSR - Address - 0xn10C) determine the data source for Receive D/E time slots. 11 — Receive LAPD Controller 3 ***NOTE:*** *All three LAPD Controller can use D/E timeslots for receiving LAPD messages. However, only LAPD Controller 1 can use datalink for reception.* ***NOTE:*** *Register 0xn360 represents D/E time slot 0, and 0xn37F represents D/E time slot 31.*
6	LAPDcntl[0]	R/W	0	
5-4	Reserved	-	-	**Reserved**

TABLE 65: RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-31) **HEX ADDRESS: 0XN360 TO 0XN37F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-0	RxCOND[3:0]	R/W	0000	**Receive Channel Conditioning for Timeslot 0 to 31** These bits allow the user to substitute the input line data (Octets 0-31) with internally generated Conditioning Codes prior to transmission to the back-plane interface on a per-channel basis. The table below presents the different conditioning codes based on the setting of these bits. ***NOTE:*** *Register address 0xn300 represents time slot 0, and address 0xn31F represents time slot 31.*

RXCOND[1:0]	CONDITIONING CODES
0x0 / 0xE	Contents of timeslot octet are unchanged.
0x1	All 8 bits of the selected timeslot octet are inverted (1's complement) OUTPUT = (TIME_SLOT_OCTET) XOR 0xFF
0x2	Even bits of the selected timeslot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0xAA
0x3	Odd bits of the selected time slot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0x55
0x4	Contents of the selected timeslot octet will be substituted with the 8 -bit value in the Receive Programmable User Code Register (0xn380-0xn397),
0x5	Contents of the timeslot octet will be substituted with the value 0x7F (BUSY Code)
0x6	Contents of the timeslot octet will be substituted with the value 0xFF (VACANT Code)
0x7	Contents of the timeslot octet will be substituted with the BUSY time slot code (111#_####), where ##### is the Timeslot number
0x8	Contents of the timeslot octet will be substituted with the MOOF code (0x1A)
0x9	Contents of the timeslot octet will be substituted with the A-Law Digital Milliwatt pattern
0xA	Contents of the timeslot octet will be substituted with the µ-Law Digital Milliwatt pattern
0xB	The MSB (bit 1) of input data is inverted
0xC	All input data except MSB is inverted
0xD	Contents of the timeslot octet will be substituted with the PRBS $X^{15} + X^{14}$ + 1/QRTS pattern ***NOTE:*** *PRBS $X^{15} + X^{14}$ + 1 or QRTS pattern depends on PRBSType selected in the register 0xn123 - bit 7*
0xF	D/E time slot - The RxSIGDL[2:0] bits in the Transmit Signaling and Data Link Select Register (0xn10C) will determine the data source for Receive D/E time slots.

TABLE 66: RECEIVE USER CODE REGISTER 0-31 (RUCR 0-31) **HEX ADDRESS: 0XN380 TO 0XN39F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxUSER[7:0]	R/W	11111111	**Receive Programmable User code.** These eight bits allow users to program any code in this register to replace the received data when the Receive Channel Control Register (RCCR) is configured to replace timeslot octet with the receive programmable user code. (i.e. if RCCR is set to '0x4')

TABLE 67: RECEIVE SIGNALING CONTROL REGISTER 0-31 (RSCR 0-31) **HEX ADDRESS: 0XN3A0 TO 0XN3BF**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	SIGC_ENB	R/W	0	**Signaling substitution enable** This bit enables or disables signaling substitution on the receive side on a per channel basis. Once signaling substitution is enabled, received signaling bits ABCD will be substituted with the ABCD values in the Receive Substitution Signaling Register (RSSR). Signaling substitution only occurs in the output PCM data (RxSERn). Receive Signaling Array Register (RSAR - Address 0xn500-0xn51F) and the external Signaling bus (RxSIG_n) output pin will not be affected. 0 = Disables signaling substitution on the receive side. 1 = Enables signaling substitution on the receive side.
5	OH_ENB	R/W	0	**Signaling OH interface output enable** This bit enables or disables signaling information to output via the Receive Overhead pin (RxOH_n) on a per channel basis. The signaling information in the receive signaling array registers (RSAR - Address 0xn500-0xn51F) is output to the receive overhead output pin (RxOH_n) if this bit is enabled. 0 = Disables signaling information to output via RxOH_n. 1 = Enables signaling information to output via RxOH_n.
4	DEB_ENB	R/W	0	**Per-channel debounce enable** This bit enables or disables the signaling debounce feature on a per channel basis. When this feature is enabled, the per-channel signaling state must be in the same state for 2 superframes before the Receive Framer updates signaling information on the Receive Signaling Array Register (RSAR) and the Signaling Pin (RxSIGn). If the signaling bits for two consecutive superframes are not the same, the current state of RSAR and RxSIG will not change. When this feature is disabled, RSAR and RxSIG will be updated as soon as the receive signaling bits have changed. 0 = Disables the Signaling Debounce feature. 1 = Enables the Signaling Debounce feature.

TABLE 67: RECEIVE SIGNALING CONTROL REGISTER 0-31 (RSCR 0-31) **HEX ADDRESS: 0XN3A0 TO 0XN3BF**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxSIGC[1]	R/W	0	**Signaling conditioning** These bits allow user to select the format of signaling substitution on a per-channel basis, as presented in the table below.
2	RxSIGC[0]	R/W	0	

RXSIGC[1:0]	SIGNALING SUBSTITUTION SCHEMES
00	**Substitutes all signaling bits with one.**
01	**Enables 16-code (A,B,C,D) signaling substitution.** Users must write to bits 3-0 in the Receive Signaling Substitution Register (RSSR) to provide the 16-code (A,B,C,D) signaling substitution values.
10	**Enables 4-code (A,B) signaling substitution.** Users must write to bits 4-5 in the Receive Signaling Substitution Register (RSSR) to provide the 4-code (A,B) signaling substitution values.
11	**Enables 2-code (A) signaling substitution.** Users must write to bit 6 in the Receive Signaling Substitution Register (RSSR) to provide the 2-code (A) signaling substitution values.

1	RxSIGE[1]	R/W	0	**Receive Signaling Extraction.** These bits control per-channel signaling extraction as presented in the table below. Signaling information can be extracted to the Receive Signaling Array Register (RSAR), the Receive Signaling Output pin (RxSIG_n) if the Receive SIgnaling Interface is enable, or the Receive Overhead Interface output (RxOH_n) if OH_ENB bit is enabled. (bit 5 of this register).
0	RxSIGE[0]	R/W	0	

RXSIGE[1:0]	SIGNALING EXTRACTION SCHEMES
00	No signaling information is extracted.
01	**Enables 16-code (A,B,C,D) signaling extraction.** All signaling bits A,B,C,D will be extracted.
10	**Enables 4-code (A,B) signaling extraction** Only signaling bits A,B will be extracted.
11	**Enables 2-code (A) signaling extraction** Only signaling bit A will be extracted.

TABLE 68: RECEIVE SUBSTITUTION SIGNALING REGISTER 0-31 (RSSR 0-31) HEX ADDRESS 0XN3C0 TO 0XN3DF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	SIG2-A	R/W	0	**2-code signaling A** This bit provides the value of signaling bit A to substitute the receive signaling bit A on a per channel basis when 2-code signaling substitution is enabled. Register address 0xn3C0 represents time slot 0, and 0xn3DF represents time slot 31.
5	SIG4-B	R/W	0	**4-code signaling B** This bit provides the value of signaling bit B to substitute the receive signaling bit B when 4-code signaling substitution is enabled. Register address 0xn3C0 represents time slot 0, and 0xn3DF represents time slot 31.
4	SIG4-A	R/W	0	**4-code signaling A** This bit provides the value of signaling bit A to substitute the receive signaling bit A when 4-code signaling substitution is enabled. Register address 0xn3C0 represents time slot 0, and 0xn3DF represents time slot 31.
3	SIG16-D	R/W	0	**16-code signaling D** This bit provides the value of signaling bit D to substitute the receive signaling bit D when 16-code signaling substitution is enabled. Register address 0xn3C0 represents time slot 0, and 0xn3DF represents time slot 31.
2	SIG16-C	R/W	0	**16-code signaling C** This bit provides the value of signaling bit C to substitute the receive signaling bit C when 16-code signaling substitution is enabled. Register address 0xn3C0 represents time slot 0, and 0xn3DF represents time slot 31.
1	SIG16-B	R/W	0	**16-code signaling B** This bit provides the value of signaling bit B to substitute the receive signaling bit B when 16-code signaling substitution is enabled. Register address 0xn3C0 represents time slot 0, and 0xn3DF represents time slot 31.
0	SIG16-A	R/W	0	**16-code signaling A** This bit provides the value of signaling bit A to substitute the receive signaling bit A when 16-code signaling substitution is enabled. Register address 0xn3C0 represents time slot 0, and 0xn3DF represents time slot 31.

TABLE 69: RECEIVE SIGNALING ARRAY REGISTER 0 - 31 (RSAR 0-31) **HEX ADDRESS: 0Xn500 TO 0Xn51F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	A	RO	0	These READ ONLY registers reflect the most recently received signaling value (A,B,C,D) associated with timeslot 0 to 31. If signaling debounce feature is enabled, the received signaling state must be the same for 2 superframes before this register is updated. If the signaling bits for two consecutive superframes are not the same, the current value of this register will not be changed. If the signaling debounce or sig feature is disabled, this register is updated as soon as the received signaling bits have changed. ***NOTE:*** *The content of this register only has meaning when the framer is using Channel Associated Signaling.*
2	B	RO	0	
1	C	RO	0	
0	D	RO	0	

TABLE 70: LAPD BUFFER 0 CONTROL REGISTER (LAPDBCR0) **HEX ADDRESS: 0xn600**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 0	R/W	0	**LAPD Buffer 0 (96-Bytes) Auto Incrementing** This register is used to transmit and receive LAPD messages within buffer 0 of the HDLC controller. Any one of the HDLC controller can be is chosen in the LAPD Select Register (0xn11B). Users should determine the next available buffer by reading the BUFAVAL bit (bit 7 of the Transmit Data Link Byte Count Register 1 (address 0xn114), Register 2 (0xn144) and Register 3 (0xn154) depending on which HDLC controller is selected. If buffer 0 is available, writing to buffer 0 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer cannot be retrieved. After detecting the Receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the Receive Data Link Byte Count Register 1 (address 0xn115), Register 2 (0xn145), or Register 3 (0xn155) depending on which HDLC controller is selected) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 0 is available to be read, reading buffer 0 (Register 0xn600) continuously will retrieve the entire received LAPD message. ***NOTE:*** *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 96 Byte LAPD message can be written into or read from buffer 0 (Register 0xn600) continuously.*

TABLE 71: LAPD BUFFER 1 CONTROL REGISTER (LAPDBCR1) **HEX ADDRESS: 0xn700**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 1	R/W	0	**LAPD Buffer 1 (96-Bytes) Auto Incrementing** This register is used to transmit and receive LAPD messages within buffer 1 of the HDLC controller. Any one of the HDLC controller can be is chosen in the LAPD Select Register (0xn11B). Users should determine the next available buffer by reading the BUFAVAL bit (bit 7 of the Transmit Data Link Byte Count Register 1 (address 0xn114), Register 2 (0xn144) and Register 3 (0xn154) depending on which HDLC controller is selected. If buffer 1 is available, writing to buffer 1 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer 1 cannot be retrieved. After detecting the Receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the Receive Data Link Byte Count Register 1 (address 0xn115), Register 2 (0xn145), or Register 3 (0xn155) depending on which HDLC controller is selected) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 1 is available to be read, reading buffer 1 (Register 0xn700) continuously will retrieve the entire received LAPD message. ***NOTE:*** *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 96 Byte LAPD message can be written into or read from buffer 0 (Register 0xn600) continuously.*

TABLE 72: PMON RECEIVE LINE CODE VIOLATION COUNTER MSB (RLCVCU) **HEX ADDRESS: 0XN900**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLCVC[15]	RUR	0	**Performance Monitor "Receive Line Code Violation" 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON Receive Line Code Violation Counter Register LSB combine to reflect the cumulative number of instances that Line Code Violation has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Line Code Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RLCVC[14]	RUR	0	
5	RLCVC[13]	RUR	0	
4	RLCVC[12]	RUR	0	
3	RLCVC[11]	RUR	0	
2	RLCVC[10]	RUR	0	
1	RLCVC[9]	RUR	0	
0	RLCVC[8]	RUR	0	

TABLE 73: PMON RECEIVE LINE CODE VIOLATION COUNTER LSB (RLCVCL) **HEX ADDRESS: 0XN901**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLCVC[7]	RUR	0	**Performance Monitor "Receive Line Code Violation" 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON Receive Line Code Violation Counter Register MSB combine to reflect the cumulative number of instances that Line Code Violation has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Line Code Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RLCVC[6]	RUR	0	
5	RLCVC[5]	RUR	0	
4	RLCVC[4]	RUR	0	
3	RLCVC[3]	RUR	0	
2	RLCVC[2]	RUR	0	
1	RLCVC[1]	RUR	0	
0	RLCVC[0]	RUR	0	

TABLE 74: PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER MSB (RFAECU) HEX ADDRESS: 0XN902

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFAEC[15]	RUR	0	**Performance Monitor "Receive Framing Alignment Error 16-Bit Counter" - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Framing Alignment Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Framing Alignment errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Framing Alignment Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFAEC[14]	RUR	0	
5	RFAEC[13]	RUR	0	
4	RFAEC[12]	RUR	0	
3	RFAEC[11]	RUR	0	
2	RFAEC[10]	RUR	0	
1	RFAEC[9]	RUR	0	
0	RFAEC[8]	RUR	0	

TABLE 75: PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER LSB (RFAECL) HEX ADDRESS: 0XN903

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFAEC[7]	RUR	0	**Performance Monitor "Receive Framing Alignment Error 16-Bit Counter" - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Framing Alignment Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Framing Alignment errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Framing Alignment Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFAEC[6]	RUR	0	
5	RFAEC[5]	RUR	0	
4	RFAEC[4]	RUR	0	
3	RFAEC[3]	RUR	0	
2	RFAEC[2]	RUR	0	
1	RFAEC[1]	RUR	0	
0	RFAEC[0]	RUR	0	

TABLE 76: PMON RECEIVE SEVERELY ERRORED FRAME COUNTER (RSEFC) **HEX ADDRESS: 0XN904**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSEFC[7]	RUR	0	**Performance Monitor - Receive Severely Errored frame Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Severely Errored Frames have been detected by the E1 Framer since the last read of this register. Severely Errored Frame is defined as the occurrence of two consecutive errored frame alignment signals without causing loss of frame condition.
6	RSEFC[6]	RUR	0	
5	RSEFC[5]	RUR	0	
4	RSEFC[4]	RUR	0	
3	RSEFC[3]	RUR	0	
2	RSEFC[2]	RUR	0	
1	RSEFC[1]	RUR	0	
0	RSEFC[0]	RUR	0	

TABLE 77: PMON RECEIVE CRC-4 BIT ERROR COUNTER - MSB (RSBBECU) **HEX ADDRESS: 0XN905**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSBBEC[15]	RUR	0	**Performance Monitor "Receive Synchronization Bit Error 16-Bit Counter" - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Synchronization Bit Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Synchronization Bit errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Synchronization Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RSBBEC[14]	RUR	0	
5	RSBBEC[13]	RUR	0	
4	RSBBEC[12]	RUR	0	
3	RSBBEC[11]	RUR	0	
2	RSBBEC[10]	RUR	0	
1	RSBBEC[9]	RUR	0	
0	RSBBEC[8]	RUR	0	

TABLE 78: PMON RECEIVE CRC-4 BLOCK ERROR COUNTER - LSB (RSBBECL) **HEX ADDRESS: 0XN906**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSBBEC[7]	RUR	0	**Performance Monitor "Receive Synchronization Bit Error 16-Bit Counter" - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Synchronization Bit Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Synchronization Bit errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Synchronization Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RSBBEC[6]	RUR	0	
5	RSBBEC[5]	RUR	0	
4	RSBBEC[4]	RUR	0	
3	RSBBEC[3]	RUR	0	
2	RSBBEC[2]	RUR	0	
1	RSBBEC[1]	RUR	0	
0	RSBBEC[0]	RUR	0	

TABLE 79: PMON RECEIVE FAR-END BLOCK ERROR COUNTER - MSB (RFEBECU) **HEX ADDRESS: 0XN907**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFEBEC[15]	RUR	0	**Performance Monitor - Receive Far-End Block Error 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Far-End Block Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Far-End Block errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Far-End Block Error counter. ***NOTE:*** *The Receive Far-End Block Error Counter will increment once each time the received E-bit is set to zero. This counter is disabled during loss of sync at either the FAS or CRC-4 level and it will continue to count if loss of multiframe sync occurs at the CAS level.* ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFEBEC[14]	RUR	0	
5	RFEBEC[13]	RUR	0	
4	RFEBEC[12]	RUR	0	
3	RFEBEC[11]	RUR	0	
2	RFEBEC[10]	RUR	0	
1	RFEBEC[9]	RUR	0	
0	RFEBEC[8]	RUR	0	

TABLE 80: PMON RECEIVE FAR END BLOCK ERROR COUNTER -LSB (RFEBECL) **HEX ADDRESS: 0XN908**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFEBEC[7]	RUR	0	**Performance Monitor - Receive Far-End Block Error 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Far-End Block Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Far-End Block errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Far-End Block Error counter. ***NOTE:*** *The Receive Far-End Block Error Counter will increment once each time the received E-bit is set to zero. This counter is disabled during loss of sync at either the FAS or CRC-4 level and it will continue to count if loss of multiframe sync occurs at the CAS level.* ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFEBEC[6]	RUR	0	
5	RFEBEC[5]	RUR	0	
4	RFEBEC[4]	RUR	0	
3	RFEBEC[3]	RUR	0	
2	RFEBEC[2]	RUR	0	
1	RFEBEC[1]	RUR	0	
0	RFEBEC[0]	RUR	0	

TABLE 81: PMON RECEIVE SLIP COUNTER (RSC) **HEX ADDRESS: 0XN909**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSC[7]	RUR	0	**Performance Monitor - Receive Slip Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Slip events have been detected by the E1 Framer since the last read of this register. ***NOTE:*** *A slip event is defined as a replication or deletion of a E1 frame by the receive slip buffer.*
6	RSC[6]	RUR	0	
5	RSC[5]	RUR	0	
4	RSC[4]	RUR	0	
3	RSC[3]	RUR	0	
2	RSC[2]	RUR	0	
1	RSC[1]	RUR	0	
0	RSC[0]	RUR	0	

TABLE 82: PMON RECEIVE LOSS OF FRAME COUNTER (RLFC) **HEX ADDRESS: 0XN90A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLFC[7]	RUR	0	**Performance Monitor - Receive Loss of Frame Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Loss of Frame condition have been detected by the E1 Framer since the last read of this register. ***NOTE:*** *This counter counts once every time the Loss of Frame condition is declared. This counter provides the capability to measure an accumulation of short failure events.*
6	RLFC[6]	RUR	0	
5	RLFC[5]	RUR	0	
4	RLFC[4]	RUR	0	
3	RLFC[3]	RUR	0	
2	RLFC[2]	RUR	0	
1	RLFC[1]	RUR	0	
0	RLFC[0]	RUR	0	

TABLE 83: PMON RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER (RCFAC) **HEX ADDRESS: 0XN90B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RCFAC[7]	RUR	0	**Performance Monitor - Receive Change of Frame Alignment Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Change of Framing Alignment have been detected by the E1 Framer since the last read of this register. ***NOTE:*** *Change of Framing Alignment (COFA) is declared when the newly-locked framing pattern is different from the one offered by off-line framer.*
6	RCFAC[6]	RUR	0	
5	RCFAC[5]	RUR	0	
4	RCFAC[4]	RUR	0	
3	RCFAC[3]	RUR	0	
2	RCFAC[2]	RUR	0	
1	RCFAC[1]	RUR	0	
0	RCFAC[0]	RUR	0	

TABLE 84: PMON LAPD FRAME CHECK SEQUENCE ERROR COUNTER 1 (LFCSEC1) **HEX ADDRESS: 0XN90C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FCSEC1[7]	RUR	0	**Performance Monitor - LAPD 1 Frame Check Sequence Error Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Frame Check Sequence Error have been detected by the LAPD Controller 1 since the last read of this register.
6	FCSEC1[6]	RUR	0	
5	FCSEC1[5]	RUR	0	
4	FCSEC1[4]	RUR	0	
3	FCSEC1[3]	RUR	0	
2	FCSEC1[2]	RUR	0	
1	FCSEC1[1]	RUR	0	
0	FCSEC1[0]	RUR	0	

TABLE 85: PMON PRBS BIT ERROR COUNTER MSB (PBECU) **HEX ADDRESS: 0XN90D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[15]	RUR	0	**Performance Monitor - E1 PRBS Bit Error 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON E1 PRBS Bit Error Counter Register LSB" combine to reflect the cumulative number of instances that the ReceiveE1 PRBS Bit errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive E1 PRBS Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	PRBSE[14]	RUR	0	
5	PRBSE[13]	RUR	0	
4	PRBSE[12]	RUR	0	
3	PRBSE[11]	RUR	0	
2	PRBSE[10]	RUR	0	
1	PRBSE[9]	RUR	0	
0	PRBSE[8]	RUR	0	

TABLE 86: PMON PRBS BIT ERROR COUNTER LSB (PBECL) **HEX ADDRESS: 0XN90E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[7]	RUR	0	**Performance Monitor - E1 PRBS Bit Error 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON E1 PRBS Bit Error Counter Register MSB" combine to reflect the cumulative number of instances that the ReceiveE1 PRBS Bit errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive E1 PRBS Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	PRBSE[6]	RUR	0	
5	PRBSE[5]	RUR	0	
4	PRBSE[4]	RUR	0	
3	PRBSE[3]	RUR	0	
2	PRBSE[2]	RUR	0	
1	PRBSE[1]	RUR	0	
0	PRBSE[0]	RUR	0	

TABLE 87: PMON TRANSMIT SLIP COUNTER (TSC) **HEX ADDRESS: 0XN90F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSLIP[7]	RUR	0	**Performance Monitor - Transmit Slip Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Transmit Slip events have been detected by the E1 Framer since the last read of this register. ***NOTE:*** *A slip event is defined as a replication or deletion of a E1 frame by the transmit slip buffer.*
6	TxSLIP[6]	RUR	0	
5	TxSLIP[5]	RUR	0	
4	TxSLIP[4]	RUR	0	
3	TxSLIP[3]	RUR	0	
2	TxSLIP[2]	RUR	0	
1	TxSLIP[1]	RUR	0	
0	TxSLIP[0]	RUR	0	

TABLE 88: PMON EXCESSIVE ZERO VIOLATION COUNTER MSB (EZVCU) **HEX ADDRESS: 0XN910**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EZVC[15]	RUR	0	**Performance Monitor - E1 Excessive Zero Violation 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the “PMON E1 Excessive Zero Violation Counter Register LSB” combine to reflect the cumulative number of instances that the ReceiveE1 Excessive Zero Violation has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive E1 Excessive Zero Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	EZVC[14]	RUR	0	
5	EZVC[13]	RUR	0	
4	EZVC[12]	RUR	0	
3	EZVC[11]	RUR	0	
2	EZVC[10]	RUR	0	
1	EZVC[9]	RUR	0	
0	EZVC[8]	RUR	0	

TABLE 89: PMON EXCESSIVE ZERO VIOLATION COUNTER LSB (EZVCL) **HEX ADDRESS: 0XN911**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EZVC[7]	RUR	0	**Performance Monitor - E1 Excessive Zero Violation 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the “PMON E1 Excessive Zero Violation Counter Register MSB” combine to reflect the cumulative number of instances that the ReceiveE1 Excessive Zero Violation has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive E1 Excessive Zero Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	EZVC[6]	RUR	0	
5	EZVC[5]	RUR	0	
4	EZVC[4]	RUR	0	
3	EZVC[3]	RUR	0	
2	EZVC[2]	RUR	0	
1	EZVC[1]	RUR	0	
0	EZVC[0]	RUR	0	

TABLE 90: PMON FRAME CHECK SEQUENCE ERROR COUNTER 2 (LFCSEC2) **HEX ADDRESS: 0XN91C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FCSEC2[7]	RUR	0	**Performance Monitor - LAPD 2 Frame Check Sequence Error Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Frame Check Sequence Error have been detected by the LAPD Controller 2 since the last read of this register.
6	FCSEC2[6]	RUR	0	
5	FCSEC2[5]	RUR	0	
4	FCSEC2[4]	RUR	0	
3	FCSEC2[3]	RUR	0	
2	FCSEC2[2]	RUR	0	
1	FCSEC2[1]	RUR	0	
0	FCSEC2[0]	RUR	0	

TABLE 91: PMON FRAME CHECK SEQUENCE ERROR COUNTER 3 (LFCSEC3) **HEX ADDRESS: 0XN92C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FCSEC3[7]	RUR	0	**Performance Monitor - LAPD 3 Frame Check Sequence Error Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Frame Check Sequence Error have been detected by the LAPD Controller 3 since the last read of this register.
6	FCSEC3[6]	RUR	0	
5	FCSEC3[5]	RUR	0	
4	FCSEC3[4]	RUR	0	
3	FCSEC3[3]	RUR	0	
2	FCSEC3[2]	RUR	0	
1	FCSEC3[1]	RUR	0	
0	FCSEC3[0]	RUR	0	

TABLE 92: BLOCK INTERRUPT STATUS REGISTER (BISR) **HEX ADDRESS: 0XNB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Sa6	RO	0	**Sa6 Block Interrupt Status** This bit Indicates whether or not the SA 6 block has an interrupt request awaiting service. 0 - Indicates no outstanding SA 6 block interrupt request is awaiting service 1 - Indicates the SA 6 block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the SA6 block Interrupt Status register (address 0xnB0C) to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the SA6 Interrupt Status Register*
6	Reserved			**For T1 mode only**
5	RxClkLOS	RO	0	**Loss of Recovered Clock Interrupt Status** This bit indicates whether or not the E1 receive framer is currently declaring the "Loss of Recovered Clock" interrupt. 0 = Indicates that the E1 Receive Framer Block is NOT currently declaring the "Loss of Recovered Clock" interrupt. 1 = Indicates that the E1 Receive Framer Block is currently declaring the "Loss of Recovered Clock" interrupt. ***NOTE:*** *This bit is only active if the clock loss detection feature is enabled (Register - 0xn100)*
4	ONESEC	RO	0	**One Second Interrupt Status** This bit indicates whether or not the E1 receive framer block is currently declaring the "One Second" interrupt. 0 = Indicates that the E1 Receive Framer Block is NOT currently declaring the "One Second" interrupt. 1 = Indicates that the E1 Receive Framer Block is currently declaring the "One Second" interrupt.
3	HDLC	RO	0	**HDLC Block Interrupt Status** This bit indicates whether or not the HDLC block has any interrupt request awaiting service. 0 = Indicates no outstanding HDLC block interrupt request is awaiting service 1 = Indicates HDLC Block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the corresponding Data Link Status Registers (address 0xnB06, 0xnB16, 0xnB26, 0xnB10, 0xnB18, 0xnB28) to clear the interrupt. ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the corresponding Data Link Status Registers that generated the interrupt.*

TABLE 92: BLOCK INTERRUPT STATUS REGISTER (BISR) **HEX ADDRESS: 0XNB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	SLIP	RO	0	**Slip Buffer Block Interrupt Status** This bit indicates whether or not the Slip Buffer block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding Slip Buffer Block interrupt request is awaiting service 1 = Indicates Slip Buffer block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the Slip Buffer Interrupt Status register (address 0xnB08) to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the Slip Buffer Interrupt Status Register.*
1	ALARM	RO	0	**Alarm & Error Block Interrupt Status** This bit indicates whether or not the Alarm & Error Block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding interrupt request is awaiting service 1 = Indicates the Alarm & Error Block has an interrupt request awaiting service. Interrupt service routine should branch to the interrupt source and read the corresponding alarm and error status registers (address 0xnB02, 0xnB0E, 0xnB40) to clear the interrupt. ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the corresponding Alarm & Error Interrupt Status register that generated the interrupt.*
0	E1 FRAME	RO	0	**E1 Framer Block Interrupt Status** This bit indicates whether or not the E1 Framer block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding interrupt request is awaiting service. 1 = Indicates the E1 Framer Block has an interrupt request awaiting service. Interrupt service routine should branch to the interrupt source and read the E1 Framer status register (address 0xnB04) to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the E1 Framer Interrupt Status register.*

TABLE 93: BLOCK INTERRUPT ENABLE REGISTER (BIER) **HEX ADDRESS: 0XNB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_ENB	R/W	0	**SA6 Block interrupt enable** This bit permits the user to either enable or disable the SA 6 Block for interrupt generation. If the user writes a “0” to this register bit and disables the SA 6 Block for interrupt generation, then all SA 6 interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the SA6 Block interrupt at the “Block Level” will be enabled. However, the individual SA 6 interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all SA6 Block interrupt within the device. 1 - Enables the SA6 interrupt at the “Block-Level”.
6	Reserved			**For T1 mode only**
5	RXCLKLOSS	R/W	0	**Loss of Recovered Clock Interrupt Enable** This bit permits the user to either enable or disable the Loss of Recovered Clock Interrupt for interrupt generation. 0 - Disables the Loss of Recovered Clock Interrupt within the device. 1 - Enables the Loss of Recovered Clock interrupt at the “Source-Level”.
4	ONESEC_ENB	R/W	0	**One Second Interrupt Enable** This bit permits the user to either enable or disable the One Second Interrupt for interrupt generation. 0 - Disables the One Second Interrupt within the device. 1 - Enables the One Second interrupt at the “Source-Level”.
3	HDLC_ENB	R/W	0	**HDLC Block Interrupt Enable** This bit permits the user to either enable or disable the HDLC Block for interrupt generation. If the user writes a “0” to this register bit and disables the HDLC Block for interrupt generation, then all HDLC interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the HDLC Block interrupt at the “Block Level” will be enabled. However, the individual HDLC interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all SA6 Block interrupt within the device. 1 - Enables the SA6 interrupt at the “Block-Level”.
2	SLIP_ENB	R/W	0	**Slip Buffer Block Interrupt Enable** This bit permits the user to either enable or disable the Slip Buffer Block for interrupt generation. If the user writes a “0” to this register bit and disables the Slip Buffer Block for interrupt generation, then all Slip Buffer interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Slip Buffer Block interrupt at the “Block Level” will be enabled. However, the individual Slip Buffer interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Slip Buffer Block interrupt within the device. 1 - Enables the Slip Buffer interrupt at the “Block-Level”.

TABLE 93: BLOCK INTERRUPT ENABLE REGISTER (BIER) **HEX ADDRESS: 0XNB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	ALARM_ENB	R/W	0	**Alarm & Error Block Interrupt Enable** This bit permits the user to either enable or disable the Alarm & Error Block for interrupt generation. If the user writes a “0” to this register bit and disables the Alarm & Error Block for interrupt generation, then all Alarm & Error interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Alarm & Error Block interrupt at the “Block Level” will be enabled. However, the individual Alarm & Error interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Alarm & Error Block interrupt within the device. 1 - Enables the Alarm & Error interrupt at the “Block-Level”.
0	E1FRAME_ENB	R/W	0	**E1 Framer Block Enable** This bit permits the user to either enable or disable the E1 Framer Block for interrupt generation. If the user writes a “0” to this register bit and disables the E1 Framer Block for interrupt generation, then all E1 Framer interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the E1 Framer Block interrupt at the “Block Level” will be enabled. However, the individual E1 Framer interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all E1 Framer Block interrupt within the device. 1 - Enables the E1 Framer interrupt at the “Block-Level”.

TABLE 94: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0XNB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx OOF State	RO	0	**Receive Out of Frame Defect State** This READ-ONLY bit indicates whether or not the Receive E1 Framer block is currently declaring the “Out of Frame” defect condition within the incoming E1 data-stream, as described below. Out of Frame defect condition is declared when “FASC” number of consecutive errored FAS patterns are detected, where “FASC” indicates the Loss of FAS Alignment Criteria in the Framing Control Register (0xn10B), bit 2-0. 0 – The Receive E1 Framer block is NOT currently declaring the “Out of Frame” defect condition. 1 – The Receive E1 Framer block is currently declaring the “Out of Frame” defect condition.
6	RxAIS State	RO	0	**Receive Alarm Indication Status Defect State** This READ-ONLY bit indicates whether or not the Receive E1 Framer block is currently declaring the AIS defect condition within the incoming E1 data-stream, as described below. AIS defect is declared when AIS condition persists for 250 microseconds (2 frames). AIS defect is cleared when more than 2 zeros are detected in two consecutive frames (250us) 0 – The Receive E1 Framer block is NOT currently declaring the AIS defect condition. 1 – The Receive E1 Framer block is currently declaring the AIS defect condition.
5	RxMYEL Status	RUR/ WC	0	**Change of CAS Multiframe Yellow Alarm Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the CAS multiframe yellow alarm interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the CAS Multiframe Yellow Alarm. **2.** Whenever the Receive E1 Framer block clears the CAS Multiframe Yellow Alarm CAS Multiframe Yellow Alarm is declared whenever the received ‘y’ bit in Time Slot 16 of Frame 0 is set to ‘1’. 0 = Indicates that the “Change of CAS Multiframe Yellow Alarm” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change of CAS Multiframe Yellow Alarm” interrupt has occurred since the last read of this register.
4	LOS State	RO	0	**Framer Receive Loss of Signal (LOS) State** This READ-ONLY bit indicates whether or not the Receive E1 framer is currently declaring the Loss of Signal (LOS) condition within the incoming DS1 data-stream, as described below LOS defect is declared when LOS condition persists for 175 consecutive bits. LOS defect is cleared when LOS condition is absent or when the received signal reaches a 12.5% ones density for 175 consecutive bits. 0 = The Receive DS1 Framer block is NOT currently declaring the Loss of Signal (LOS) condition. 1 = The Receive DS1 Framer block is currently declaring the Loss of Signal (LOS) condition.

TABLE 94: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0XNB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	LCV Int Status	RUR/ WC	0	**Line Code Violation Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the Receive E1 LIU block has detected a Line Code Violation interrupt since the last read of this register. 0 = Indicates that the Line Code Violation interrupt has not occurred since the last read of this register. 1 = Indicates that the Line Code Violation interrupt has occurred since the last read of this register.
2	Rx OOF State Change	RUR/ WC	0	**Change in Out of Frame Defect Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Out of Frame Defect Condition” interrupt has occurred since the last read of this register. Out of Frame defect condition is declared when “FASC” number of consecutive errored FAS patterns are detected, where “FASC” indicates the Loss of FAS Alignment Criteria in the Framing Control Register (0xn10B), bit 2-0. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the Out of Frame defect condition. **2.** Whenever the Receive E1 Framer block clears the Out of Frame defect condition 0 = Indicates that the “Change in Receive Out of Frame defect condition” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Out of Frame defect condition” interrupt has occurred since the last read of this register
1	RxAIS State Change	RUR/ WC	0	**Change in Receive AIS Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the “Change in Receive AIS Condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the AIS condition. **2.** Whenever the Receive E1 Framer block clears the AIS condition 0 = Indicates that the “Change in Receive AIS condition” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive AIS condition” interrupt has occurred since the last read of this register

TABLE 94: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0XNB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	RxYEL State Change	RUR/ WC	0	**Change in Receive Yellow Alarm Interrupt Status.** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Yellow Alarm Condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the Yellow Alarm condition. **2.** Whenever the Receive E1 Framer block clears the Yellow Alarm condition 0 = Indicates that the “Change in Receive Yellow Alarm condition” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Yellow Alarm condition” interrupt has occurred since the last read of this register

TABLE 95: ALARM & ERROR INTERRUPT ENABLE REGISTER (AEIER) **HEX ADDRESS: 0XNB03**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx_YEL_STATE	RO	0	**Receive Yellow Alarm State** This READ-ONLY bit indicates whether or not the Receive E1 Framer block is currently declaring the Yellow Alarm condition within the incoming E1 data-stream, as described below. Yellow alarm or Remote Alarm Indication (RAI) is declared when the 'A' bit of two consecutive non-FAS frames is set to '1', which is equivalent to taking 375us to declare a RAI condition. Yellow alarm is cleared when the 'A' bit of two consecutive non-FAS frames is set to 0, which is equivalent to taking 375us to clear a RAI condition. 0 – The Receive E1 Framer block is NOT currently declaring the Yellow Alarm condition. 1 – The Receive E1 Framer block is currently declaring the Yellow Alarm condition.
6	Reserved	-	-	**Reserved**
5	RxMYEL ENB	R/W	0	**Change of CAS Multiframe Yellow Alarm Interrupt Enable**. This bit permits the user to either enable or disable the "Change in CAS Multiframe Yellow Alarm" Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares CAS Multiframe Yellow Alarm. **2.** The instant that the Receive E1 Framer block clears the CAS Multiframe Yellow Alarm. 0 – Disables the "Change in CAS Multiframe Yellow Alarm" Interrupt. 1 – Enables the "Change in CAS Multiframe Yellow Alarm" Interrupt.
4	-	R/W	0	**This bit should be set to'0' for proper operation.**
3	LCV ENB	R/W	0	**Line Code violation interrupt enable** This bit permits the user to either enable or disable the "Line Code Violation" interrupt within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when Line Code Violation is detected. 0 = Disables the interrupt generation when Line Code Violation is detected. 1 = Enables the interrupt generation when Line Code Violation is detected.
2	RxOOF ENB	R/W	0	**Change in Out of Frame Defect Condition Interrupt enable** This bit permits the user to either enable or disable the "Change in Out of Frame Defect Condition" Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the Out of Frame defect condition. **2.** The instant that the Receive E1 Framer block clears the Out of Frame defect condition. 0 – Disables the "Change in Out of Frame Defect Condition" Interrupt. 1 – Enables the "Change in Out of Frame Defect Condition" Interrupt.

TABLE 95: ALARM & ERROR INTERRUPT ENABLE REGISTER (AEIER) **HEX ADDRESS: 0XNB03**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxAIS ENB	R/W	0	**Change in AIS Condition interrupt enable** This bit permits the user to either enable or disable the “Change in AIS Condition” Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the AIS condition. **2.** The instant that the Receive E1 Framer block clears the AIS condition. 0 – Disables the “Change in AIS Condition” Interrupt. 1 – Enables the “Change in AIS Condition” Interrupt.
0	RxYEL ENB	R/W	0	**Change in Yellow alarm Condition interrupt enable** This bit permits the user to either enable or disable the “Change in Yellow Alarm Condition” Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the Yellow Alarm condition. **2.** The instant that the Receive E1 Framer block clears the Yellow Alarm condition. 0 – Disables the “Change in Yellow Alarm Condition” Interrupt. 1 – Enables the “Change in Yellow Alarm Condition” Interrupt.

TABLE 96: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	COMFA Status	RUR/ WC	0	**Change of CAS Multiframe Alignment Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change of CAS multiframe alignment” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the “Loss of CAS Multiframe Alignment”. **2.** Whenever the Receive E1 Framer block clears the “Loss of CAS Multiframe Alignment” Loss CAS Multiframe Alignment is declared when the “CASC” number of consecutive CAS Multiframe Alignment signals have been received in error, where CASC sets the criteria for Loss of CAS multiframe. CASC can ben programmed through Framing Control Register (FCR - address 0xn10B, bit 6-5) 0 = Indicates that the “Change of CAS Multiframe Alignment” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change of CAS Multiframe Alignment” interrupt has occurred since the last read of this register. ***NOTES:*** *This bit only has meaning when Channel Associated Signaling (CAS) is enabled.*
6	NBIT Status	RUR/ WC	0	**Change in National Bits Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in National Bits” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever any one of the National Bits (Sa4-Sa8) within the incoming non-FAS E1 frames has changed. 0 = Indicates that the “Change in National Bits” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in National Bits” interrupt has occurred since the last read of this register.
5	SIG Status	RUR/ WC	0	**Change in CAS Signaling Bits Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in CAS Signaling Bits” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever any one of the four signaling bits values (A,B,C,D) has changed in any one of the 30 channels within the incoming E1 frames. Users can read the signaling change registers (address 0xn10D-0xn110) to determine which signalling channel has changed. 0 = Indicates that the “Change in CAS Signaling Bits” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in CAS Signaling Bits” interrupt has occurred since the last read of this register. ***NOTE:*** *This bit only has meaning when Channel Associated Signaling (CAS) is enabled.*

TABLE 96: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	COFA Status	RUR/ WC	0	**Change of FAS Framing Alignment (COFA) Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change of FAS Framing Alignment” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever the Receive E1 Framer block detects a Change of FAS Framing Alignment Signal (e.g., the FAS bits have appeared to move to a different location within the incoming E1 data stream). 0 = Indicates that the “Change of FAS Framing Alignment (COFA)” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change of FAS Framing Alignment (COFA)” interrupt has occurred since the last read of this register.
3	OOF Status	RUR/ WC	0	**Change in Out of Frame Defect Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Out of Frame Defect Condition” interrupt has occurred since the last read of this register. Out of Frame defect condition is declared when “FASC” number of consecutive errored FAS patterns are detected, where “FASC” indicates the Loss of FAS Alignment Criteria in the Framing Control Register (0xn10B), bit 2-0. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the Out of Frame defect condition. **2.** Whenever the Receive E1 Framer block clears the Out of Frame defect condition 0 = Indicates that the “Change in Receive Out of Frame defect condition” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Out of Frame defect condition” interrupt has occurred since the last read of this register
2	FMD Status	RUR/ WC	0	**Frame Mimic Detection Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Frame Mimic Detection” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever the Receive E1 Framer block detects the presence of Frame Mimic bits (i.e., the Payload bits have appeared to mimic the Framing pattern within the incoming E1 data stream). 0 = Indicates that the “Frame Mimic Detection” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Frame Mimic Detection” interrupt has occurred since the last read of this register.

TABLE 96: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0xnB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	Sync Error Status	RUR/ WC	0	**CRC-4 Error Interrupt Status.** This Reset-Upon-Read bit field indicates whether or not the “CRC-4 Error” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever the Receive E1 Framer block detects a CRC-4 Error within the incoming E1 sub-multiframe. 0 = Indicates that the “CRC-4 Error” interrupt has not occurred since the last read of this register. 1 = Indicates that the “CRC-4 Error” interrupt has occurred since the last read of this register.
0	Framing Error Sta-tus	RUR/ WC	0	**Framing Error Interrupt Status** This Reset-Upon-Read bit field indicates whether or not a “Framing Error” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever the Receive E1 Framer block detects one or more Framing Alignment Bit Error within the incoming E1 data stream. 0 = Indicates that the “Framing Error” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Framing Error” interrupt has occurred since the last read of this register. ***NOTE:*** *This bit doesn't not necessarily indicate that synchronization has been lost.*

TABLE 97: FRAMER INTERRUPT ENABLE REGISTER (FIER) **HEX ADDRESS: 0XNB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	COMFA ENB	R/W	0	**Change in CAS Multiframe Alignment Interrupt Enable** This bit permits the user to either enable or disable the "Change in CAS Multiframe Alignment" Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the Loss of CAS Multiframe Alignment condition. **2.** The instant that the Receive E1 Framer block clears the Loss of CAS Multiframe Alignment condition. 0 – Disables the "Change in CAS Multiframe Alignment" Interrupt. 1 – Enables the "Change in CAS Multiframe Alignment" Interrupt.
6	NBIT ENB	R/W	0	**Change in National Bits Interrupt Enable** This bit permits the user to either enable or disable the "Change in National Bits" Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects a change in the National Bits (Sa4-Sa8) within the channel. 0 = Disables the Change in National Bits Interrupt 1 - Enables the Change in National Bits Interrupt
5	SIG ENB	R/W	0	**Change in CAS Signaling Bits Interrupt Enable** This bit permits the user to either enable or disable the "Change in CAS Signaling Bits" Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects a change in the any four signaling bits (A,B,C,D) in any one of the 30 signaling channels. Users can read the signaling change registers (address 0xn10D-0xn110) to determine which signalling channel has changed state. 0 = Disables the Change in Signaling Bits Interrupt 1 - Enables the Change in Signaling Bits Interrupt ***NOTE:*** *This bit has no meaning when Channel Associated Signaling is disabled.*
4	COFA ENB	R/W	0	**Change of FAS Framing Alignment (COFA) Interrupt Enable** This bit permits the user to either enable or disable the "Change in FAS Framing Alignment (COFA)" Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects a Change of FAS Framing Alignment Signal (e.g., the FAS bits have appeared to move to a different location within the incoming E1 data stream). 0 – Disables the "Change of FAS Framing Alignment (COFA)" Interrupt. 1 – Enables the "Change of FAS Framing Alignment (COFA)" Interrupt.

TABLE 97: FRAMER INTERRUPT ENABLE REGISTER (FIER) **HEX ADDRESS: 0XNB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	OOF ENB	R/W	0	**Change in Out of Frame Defect Condition interrupt enable** This bit permits the user to either enable or disable the “Change in Out of Frame Defect Condition” Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the Out of Frame defect condition. **2.** The instant that the Receive E1 Framer block clears the Out of Frame defect condition. 0 – Disables the “Change in Out of Frame Defect Condition” Interrupt. 1 – Enables the “Change in Out of Frame Defect Condition” Interrupt.
2	FMD ENB	R/W	0	**Frame Mimic Detection Interrupt Enable** This bit permits the user to either enable or disable the “Frame Mimic Detection” Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects the presence of Frame mimic bits (i.e., the payload bits have appeared to mimic the framing bit pattern within the incoming E1 data stream). 0 – Disables the “Frame Mimic Detection” Interrupt. 1 – Enables the “Frame Mimic Detection” Interrupt.
1	SE_ENB	R/W	0	**Synchronization Bit (CRC-4) Error Interrupt Enable** This bit permits the user to either enable or disable the “CRC-4 Error Detection” Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects a CRC-4 error within the incoming E1 sub-multiframe. 0 – disable the “CRC-4 Error Detection” Interrupt. 1 – enable the “CRC-4 Error Detection” Interrupt.
0	FE_ENB	R/W	0	**Framing Bit Error Interrupt Enable** This bit permits the user to either enable or disable the “Framing Alignment Bit Error Detection” Interrupt, within the XRT86VL34 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects one or more Framing Alignment Bit error within the incoming E1 data stream. 0 – disable the “Framing Alignment Bit Error Detection” Interrupt. 1 – enable the “Framing Alignment Bit Error Detection” Interrupt. ***NOTE:*** *Detecting Framing Alignment Bit Error doesn't not necessarily indicate that synchronization has been lost.*

TABLE 98: DATA LINK STATUS REGISTER 1 (DLSR1) **HEX ADDRESS: 0XNB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RO	0	**HDLC1 Message Type Identifier** This READ ONLY bit indicates the type of data link message received by Receive HDLC 1 Controller. Two types of data link messages are supported within the XRT86VL34 device: Message Oriented Signaling (MOS) or Bit-Oriented Signalling (BOS). 0 = Indicates Bit-Oriented Signaling (BOS) type data link message is received 1 = Indicates Message Oriented Signaling (MOS) type data link message is received
6	TxSOT	RUR/ WC	0	**Transmit HDLC1 Controller Start of Transmission (TxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the “Transmit HDLC1 Controller Start of Transmission (TxSOT) “Interrupt has occurred since the last read of this register. Transmit HDLC1 Controller will declare this interrupt when it has started to transmit a data link message. For sending large HDLC messages, start loading the next available buffer once this interrupt is detected. 0 = Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC1 Controller Start of Transmission interrupt (TxSOT) has occurred since the last read of this register.
5	RxSOT	RUR/ WC	0	**Receive HDLC1 Controller Start of Reception (RxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register
4	TxEOT	RUR/ WC	0	**Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt has occurred since the last read of this register. Transmit HDLC1 Controller will declare this interrupt when it has completed its transmission of a data link message. For sending large HDLC messages, it is critical to load the next available buffer before this interrupt occurs. 0 = Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt has occurred since the last read of this register

TABLE 98: DATA LINK STATUS REGISTER 1 (DLSR1) **HEX ADDRESS: 0XNB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxEOT	RUR/ WC	0	**Receive HDLC1 Controller End of Reception (RxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC1 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt once it has completely received a full data link message, or once the buffer is full. 0 = Receive HDLC1 Controller End of Reception (RxEOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC1 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register
2	FCS Error	RUR/ WC	0	**FCS Error Interrupt Status** This Reset-Upon-Read bit indicates whether or not the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt when it has detected the FCS error in the most recently received data link message. 0 = FCS Error interrupt has not occurred since the last read of this register 1 = FCS Error interrupt has occurred since the last read of this register
1	Rx ABORT	RUR/ WC	0	**Receipt of Abort Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Abort Sequence interrupt has occurred since last read of this register. Receive HDLC1 Controller will declare this interrupt if it detects the Abort Sequence (i.e. a string of seven (7) consecutive 1's) in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register
0	RxIDLE	RUR/ WC	0	**Receipt of Idle Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC1 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. If RxIDLE "AND" RxEOT occur together, then the entire HDLC message has been received. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 99: DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1) **HEX ADDRESS: 0XNB07**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC1 Controller Start of Transmission (TxSOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC1 Controller Start of Transmission (TxSOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Transmit HDLC1 Controller will generate an interrupt when it has started to transmit a data link message. 0 = Disables the Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt. 1 = Enables the Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt.
5	RxSOT ENB	R/W	0	**Receive HDLC1 Controller Start of Reception (RxSOT) Interrupt Enable** This bit enables or disables the “Receive HDLC1 Controller Start of Reception (RxSOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has started to receive a data link message. 0 = Disables the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt. 1 = Enables the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt.
4	TxEOT ENB	R/W	0	**Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC1 Controller End of Transmission (TxEOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Transmit HDLC1 Controller will generate an interrupt when it has finished transmitting a data link message. 0 = Disables the Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt. 1 = Enables the Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt.
3	RxEOT ENB	R/W	0	**Receive HDLC1 Controller End of Reception (RxEOT) Interrupt Enable** This bit enables or disables the “Receive HDLC1 Controller End of Reception (RxEOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has finished receiving a complete data link message. 0 = Disables the Receive HDLC1 Controller End of Reception (RxEOT) interrupt. 1 = Enables the Receive HDLC1 Controller End of Reception (RxEOT) interrupt.

TABLE 99: DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1) **HEX ADDRESS: 0XNB07**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** This bit enables or disables the “Received FCS Error “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the FCS error within the incoming data link message. 0 = Disables the “Receive FCS Error” interrupt. 1 = Enables the “Receive FCS Error” interrupt.
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** This bit enables or disables the “Receipt of Abort Sequence“ Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the Abort Sequence (i.e. a string of seven (7) consecutive 1’s) within the incoming data link channel. 0 = Disables the “Receipt of Abort Sequence” interrupt. 1 = Enables the “Receipt of Abort Sequence” interrupt.
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** This bit enables or disables the “Receipt of Idle Sequence“ Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the Idle Sequence Octet (i.e. 0x7E) within the incoming data link channel. 0 = Disables the “Receipt of Idle Sequence” interrupt. 1 = Enables the “Receipt of Idle Sequence” interrupt.

TABLE 100: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSB_FULL	RUR/ WC	0	**Transmit Slip buffer Full Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Full interrupt has occurred since the last read of this register. The transmit Slip Buffer Full interrupt is declared when the transmit slip buffer is filled. If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Full interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Full interrupt has occurred since the last read of this register.
6	TxSB_EMPT	RUR/ WC	0	**Transmit Slip buffer Empty Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Empty interrupt has occurred since the last read of this register. The transmit Slip Buffer Empty interrupt is declared when the transmit slip buffer is emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Empty interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Empty interrupt has occurred since the last read of this register.
5	TxSB_SLIP	RUR/ WC	0	**Transmit Slip Buffer Slips Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Slips interrupt has occurred since the last read of this register. The transmit Slip Buffer Slips interrupt is declared when the transmit slip buffer is either filled or emptied. This interrupt bit will be set to '1' in either one of these two conditions: **1.** If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Slips interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Slips interrupt has occurred since the last read of this register. ***NOTE:*** *Users still need to read the Transmit Slip Buffer Empty Interrupt (bit 6 of this register) or the Transmit Slip Buffer Full Interrupts (bit 7 of this register) to determine whether transmit slip buffer empties or fills.*

TABLE 100: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0xnB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	CAS SYNC	RO	0	**CAS Multiframe Alignment is in SYNC** This READ ONLY bit field indicates whether or not the E1 Receive Framer Block is declaring CAS Multiframe Alignment LOCK status. The E1 Receive Framer Block will declare the CAS Multiframe Alignment LOCK status according to the CAS Multiframe Alignment Algorithm as described in the Framing Select Register (FSR - address 0xn107). The E1 Receive Framer Block will declare the CAS Multiframe Alignment LOSS OF LOCK status when CASC number of consecutive CAS Multi-frame Alignment Signals have been received in error, where CASC sets the Loss of CAS Multiframe Alignment Criteria, as described in the Fram-ing Control Register (FCR - address 0xn10B). 0 = Indicates that the E1 Receive Framer Block is currently declaring CAS Multiframe LOSS OF LOCK status 1 = Indicates that the E1 Receive Framer Block is currently declaring CAS Multiframe LOCK status ***NOTE:*** *In E1 mode, this bit has no meaning if Channel Associated Signaling is disabled.*
3	CRCMLOCK	RO	0	**CRC Multiframe is in SYNC** This READ ONLY bit field indicates whether or not the E1 Receive Framer Block is declaring the E1 CRC Multiframe Alignment LOCK status. The E1 Receive Framer declares the CRC Multiframe Alignment LOCK status according to the CRC Multiframe Alignment Declaration Criteria which can be selected in the Framing Select Register (FSR - address 0xn107) The E1 Receive Framer declares the CRC Multiframe Alignment LOSS OF LOCK status according to the Loss CRC Multiframe Alignment Criteria selected in the Framing Control Register (FCR - address 0xn10B) 0 = Indicates that the E1 Receive Framer is currently declaring E1 CRC Multiframe Alignment LOSS OF LOCK status 0 = Indicates that the E1 Receive Framer is currently declaring E1 Multi-frame Alignment LOCK status ***NOTE:*** *In E1 mode, this bit has no meaning if CRC Multiframe Alignment is disabled.*
2	RxSB_FULL	RUR/ WC	0	**Receive Slip buffer Full Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Full interrupt has occurred since the last read of this register. The Receive Slip Buffer Full interrupt is declared when the receive slip buffer is filled. If the receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to ‘1’. 0 = Indicates that the Receive Slip Buffer Full interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Full interrupt has occurred since the last read of this register.

TABLE 100: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxSB_EMPT	RUR/ WC	0	**Receive Slip buffer Empty Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Empty interrupt has occurred since the last read of this register. The Receive Slip Buffer Empty interrupt is declared when the receive slip buffer is emptied. If the receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. 0 = Indicates that the Receive Slip Buffer Empty interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Empty interrupt has occurred since the last read of this register.
0	RxSB_SLIP	RUR/ WC	0	**Receive Slip Buffer Slips Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Slips interrupt has occurred since the last read of this register. The Receive Slip Buffer Slips interrupt is declared when the receive slip buffer is either filled or emptied. This interrupt bit will be set to '1' in either one of these two conditions: **1.** If the receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Receive Slip Buffer Slips interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Slips interrupt has occurred since the last read of this register. ***NOTE:*** *Users still need to read the Receive Slip Buffer Empty Interrupt (bit 1 of this register) or the Receive Slip Buffer Full Interrupts (bit 2 of this register) to determine whether transmit slip buffer empties or fills.*

TABLE 101: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER) **HEX ADDRESS: 0XNB09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxFULL_ENB	R/W	0	**Transmit Slip Buffer Full Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Full interrupt within the XRT86VL34 device. Once this interrupt is enabled, the transmit Slip Buffer Full interrupt is declared when the transmit slip buffer is filled. If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and the interrupt status bit will be set to '1'. 0 = Disables the Transmit Slip Buffer Full interrupt when the Transmit Slip Buffer fills 1 - Enables the Transmit Slip Buffer Full interrupt when the Transmit Slip Buffer fills.
6	TxEMPT_ENB	R/W	0	**Transmit Slip Buffer Empty Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Empty interrupt within the XRT86VL34 device. Once this interrupt is enabled, the transmit Slip Buffer Empty interrupt is declared when the transmit slip buffer is emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. 0 = Disables the Transmit Slip Buffer Empty interrupt when the Transmit Slip Buffer empties 1 - Enables the Transmit Slip Buffer Empty interrupt when the Transmit Slip Buffer empties.
5	TxSLIP_ENB	R/W	0	**Transmit Slip Buffer Slips Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Slips interrupt within the XRT86VL34 device. Once this interrupt is enabled, the transmit Slip Buffer Slips interrupt is declared when either the transmit slip buffer is filled or emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. The interrupt status bit will be set to '1' in either one of these two conditions: **1.** If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Disables the Transmit Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills 1 - Enables the Transmit Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills.
4-3	Reserved	-	-	**Reserved**

TABLE 101: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER) **HEX ADDRESS: 0XNB09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	RxFULL_ENB	R/W	0	**Receive Slip Buffer Full Interrupt Enable** This bit enables or disables the Receive Slip Buffer Full interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive Slip Buffer Full interrupt is declared when the receive slip buffer is filled. If the Receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and the interrupt status bit will be set to ‘1’. 0 = Disables the Receive Slip Buffer Full interrupt when the Transmit Slip Buffer fills 1 - Enables the Receive Slip Buffer Full interrupt when the Transmit Slip Buffer fills.
1	RxEMPT_ENB	R/W	0	**Receive Slip buffer Empty Interrupt Enable** This bit enables or disables the Receives Slip Buffer Empty interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive Slip Buffer Empty interrupt is declared when the Receive slip buffer is emptied. If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to ‘1’. 0 = Disables the Receive Slip Buffer Empty interrupt when the Transmit Slip Buffer empties 1 - Enables the Receive Slip Buffer Empty interrupt when the Transmit Slip Buffer empties.
0	RxSLIP_ENB	R/W	0	**Receive Slip buffer Slips Interrupt Enable** This bit enables or disables the Receive Slip Buffer Slips interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive Slip Buffer Slips interrupt is declared when either the Receive slip buffer is filled or emptied. If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to ‘1’. The interrupt status bit will be set to ‘1’ in either one of these two conditions: **1.** If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to ‘1’. **2.** If the Receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to ‘1’. 0 = Disables the Receive Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills 1 - Enables the Receive Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills.

TABLE 102: RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER (RLCISR) HEX ADDRESS: 0XNB0A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	AUXPSTAT	RO	0	**AUXP state** This READ ONLY bit indicates whether or not the Receive E1 Framer Block is currently detecting Auxiliary (101010....) pattern. 0 = Indicates that the Receive E1 Framer Block is NOT currently detecting the Auxiliary (101010....)Pattern. 1 = Indicates that the Receive E1 Framer Block is currently detecting the Auxiliary (101010....)Pattern.
6	AUXPINT	RUR/WC	0	**Change in Auxiliary Pattern interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Auxiliary Pattern" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Auxiliary Pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Auxiliary Pattern 0 = Indicates that the "Change in Auxiliary Pattern" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Auxiliary Pattern" interrupt has occurred since the last read of this register
5	NONCRCSTAT	RO	0	**CRC-4-to-non-CRC-4 interworking state** This READ ONLY bit indicates the status of CRC-4 interworking status when Annex B is enabled. (MODENB bit in register 0xn107) When Annex B is enabled, G.706 Annex B CRC-4 multiframe alignment algorithm is implemented. If CRC-4 alignment is enabled and not achieved in 400msec while the basic frame alignment signal is present, it is assumed that the remote end is a non CRC-4 equipment. Then, a CRC-to-Non-CRC interworking interrupt status will be generated. 0 = Indicates CRC-4 to non-CRC-4 interworking is NOT established. 1 = Indicates CRC-4 to non-CRC-4 interworking is established.

TABLE 102: RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER (RLCISR) HEX ADDRESS: 0XNB0A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	NONCRCINT	RUR/WC	0	**Change of CRC-4-to-non-CRC-4 interworking interrupt Status -** This Reset-Upon-Read bit field indicates whether or not the "Change in CRC-4 to Non-CRC-4 interworking" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the CRC-4 to non-CRC-4 interworking condition. **2.** Whenever the Receive E1 Framer block detects the non-CRC-4 to CRC-4 interworking condition. 0 = Indicates that the "Change in CRC-4 to non-CRC-4 interworking" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in CRC-4 to non-CRC-4 interworking" interrupt has occurred since the last read of this register
3-0				**For T1 mode only**

TABLE 103: RECEIVE LOOPBACK CODE INTERRUPT ENABLE REGISTER (RLCIER) **HEX ADDRESS: 0XNB0B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	AUXPINTENB	R/W	0	**Change in Auxiliary Pattern interrupt enable** This READ WRITE bit field enables or disables the “Change in Auxiliary Pattern” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Auxiliary Pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Auxiliary Pattern 0 = Disables the “Change in Auxiliary Pattern” interrupt within the E1 Receive Framer. 1 - Enables the “Change in Auxiliary Pattern” interrupt within the E1 Receive Framer.
5	Reserved	-	-	**Reserved**
4	NONCRCENB	R/W	0	**Change of CRC-4-to-non-CRC-4 interworking interrupt Enable** This bit enables or disables the “Change in CRC-4 to Non-CRC-4 interworking” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the CRC-4 to non-CRC-4 interworking condition. **2.** Whenever the Receive E1 Framer block detects the non-CRC-4 to CRC-4 interworking condition. 0 = Disables the “Change in CRC-4 to non-CRC-4 interworking” interrupt within the E1 Receive Framer. 1 - Enables the “Change in CRC-4 to non-CRC-4 interworking” interrupt within the E1 Receive Framer.
3-2	Reserved	-	-	**Reserved**
1-0	Reserved			**For T1 mode only**

TABLE 104: RECEIVE SA INTERRUPT STATUS REGISTER (RSAISR) **HEX ADDRESS: 0XNB0C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_1111	RUR/ WC	0	**Change in Debounced Sa6 = 1111 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1111" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1111 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1111 pattern. 0 = Indicates that the "Change in Debounced Sa6=1111" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1111" interrupt has occurred since the last read of this register
6	SA6_1110	RUR/ WC	0	**Change in Debounced Sa6 = 1110 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1110" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1110 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1110 pattern. 0 = Indicates that the "Change in Debounced Sa6=1110" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1110" interrupt has occurred since the last read of this register
5	SA6_1100	RUR/ WC	0	**Change in Debounced Sa6 = 1100 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1100" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1100 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1100 pattern. 0 = Indicates that the "Change in Debounced Sa6=1100" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1100" interrupt has occurred since the last read of this register

TABLE 104: RECEIVE SA INTERRUPT STATUS REGISTER (RSAISR) **HEX ADDRESS: 0XNB0C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	SA6_1010	RUR/ WC	0	**Change in Debounced Sa6 = 1010 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1010" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1010 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1010 pattern. 0 = Indicates that the "Change in Debounced Sa6=1010" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1010" interrupt has occurred since the last read of this register
3	SA6_1000	RUR/ WC	0	**Change in Debounced Sa6 = 1000 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1000" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1000 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1000 pattern. 0 = Indicates that the "Change in Debounced Sa6=1000" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1000" interrupt has occurred since the last read of this register
2	SA6_001x	RUR/ WC	0	**Change in Debounced Sa6 = 001x Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=001x" interrupt has occurred since the last read of this register, where x is don't care. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 001x pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 001x pattern. 0 = Indicates that the "Change in Debounced Sa6=001x" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=001x" interrupt has occurred since the last read of this register

TABLE 104: RECEIVE SA INTERRUPT STATUS REGISTER (RSAISR) **HEX ADDRESS: 0XNB0C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	SA6_other	RUR/ WC	0	**Debounced Sa6 = other Combination Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=other combination" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt when it detects the Debounced Sa 6 equals to any other combinations. 0 = Indicates that the "Debounced Sa6 = other combination" interrupt has not occurred since the last read of this register 1 = Indicates that the "Debounced Sa6 = other combination" interrupt has occurred since the last read of this register
0	SA6_0000	RUR/ WC	0	**Change in Debounced Sa6 = 0000 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=0000" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 0000 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 0000 pattern. 0 = Indicates that the "Change in Debounced Sa6=0000" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=0000" interrupt has occurred since the last read of this register

TABLE 105: RECEIVE SA INTERRUPT ENABLE REGISTER (RSAIER) **HEX ADDRESS: 0XNB0D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_1111_ENB	R/W	0	**Change in Debounced Sa6 = 1111 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=1111” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1111 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1111 pattern. 0 = Disables the “Change in Debounced Sa6=1111” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=1111” interrupt within the Receive E1 Framer Block
6	SA6_1110_ENB	R/W	0	**Change in Debounced Sa6 = 1110 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=1110” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1110 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1110 pattern. 0 = Disables the “Change in Debounced Sa6=1110” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=1110” interrupt within the Receive E1 Framer Block
5	SA6_1100_ENB	R/W	0	**Change in Debounced Sa6 = 1100 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=1100” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1100 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1100 pattern. 0 = Disables the “Change in Debounced Sa6=1100” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=1100” interrupt within the Receive E1 Framer Block

TABLE 105: RECEIVE SA INTERRUPT ENABLE REGISTER (RSAIER) **HEX ADDRESS: 0XNB0D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	SA6_1010_ENB	R/W	0	**Change in Debounced Sa6 = 1010 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=1010” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1010 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1010 pattern. 0 = Disables the “Change in Debounced Sa6=1010” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=1010” interrupt within the Receive E1 Framer Block
3	SA6_1000_ENB	R/W	0	**Change in Debounced Sa6 = 1000 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=1000” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1000 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1000 pattern. 0 = Disables the “Change in Debounced Sa6=1000” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=1000” interrupt within the Receive E1 Framer Block
2	SA6_001x_ENB	R/W	0	**Change in Debounced Sa6 = 001x Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=001x” interrupt within the E1 Receive Framer, where x is don’t care. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 001x pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 001x pattern. 0 = Disables the “Change in Debounced Sa6=001x” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=001x” interrupt within the Receive E1 Framer Block

TABLE 105: RECEIVE SA INTERRUPT ENABLE REGISTER (RSAIER) **HEX ADDRESS: 0XNB0D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	SA6_other_ENB	R/W	0	**Debounced Sa6 = Other Combination Interrupt enable** This bit enables or disables the “Debounced Sa6=other combination” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt when it detects the debounced Sa6 equals to any other combination. 0 = Disables the “Debounced Sa6=other combination” interrupt within the Receive E1 Framer Block 1 - Enables the “Debounced Sa6=other combination” interrupt within the Receive E1 Framer Block
0	SA6_0000_ENB	R/W	0	**Change in Debounced Sa6 = 0000 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=0000” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 0000 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 0000 pattern. 0 = Disables the “Change in Debounced Sa6=0000” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=0000” interrupt within the Receive E1 Framer Block

TABLE 106: EXCESSIVE ZERO STATUS REGISTER (EXZSR) **HEX ADDRESS: 0XNB0E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5	SA7_EQ_0_STAT	RO	0	**Received Sa7 Equals '0' State** This READ ONLY bit field indicates whether or not the Receive E1 Framer is currently declaring the "Sa7 Equals 0" status within the incoming E1 National Bits. The "Received Sa7 Equals 0" status will be set to '1' if the received Sa7 is 0 for at least 2 out of 3 times. 0 = Indicates the E1 Receive Framer is currently not declaring the "Received Sa7 Equals 0" status. 1 = Indicates the E1 Receive Framer is currently declaring the "Received Sa7 Equals 0" status.
4-2	Reserved	-	-	**Reserved**
1	SA7_EQ_0_INT	RUR/ WC	0	**Change in "Sa 7 Equals 0" Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Sa7 Equals 0" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Received Sa7 equals to 0 for at least 2 out of 3 times. **2.** Whenever the Receive E1 Framer block no longer detects the Received Sa7 equals to the 0. 0 = Indicates that the "Change in Sa7 Equals 0" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Sa7 Equals 0" interrupt has occurred since the last read of this register
0	EXZ_STATUS	RUR/ WC	0	**Change in Excessive Zero Condition Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Excessive Zero Condition" interrupt within the E1 Receive Framer Block has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Excessive Zero Condition. **2.** Whenever the Receive E1 Framer block clears the Excessive Zero Condition 0 = Indicates the "Change in Excessive Zero Condition" interrupt has NOT occurred since the last read of this register 1 = Indicates the "Change in Excessive Zero Condition" interrupt has occurred since the last read of this register

TABLE 107: EXCESSIVE ZERO ENABLE REGISTER (EXZER) **HEX ADDRESS: 0XNB0F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	SA7_EQ_0_ENB	R/W	0	**Change in "Sa 7 Equals 0" Interrupt Enable** This bit enables or disables the "Change in Sa7 Equals 0" interrupt within the Receive E1 Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Received Sa7 equals to 0 for at least 2 out of 3 times. **2.** Whenever the Receive E1 Framer block no longer detects the Received Sa7 equals to the 0. 0 = Disables the "Change in Sa7 Equals 0" interrupt within the E1 Receive Framer Block. 1 = Enables the "Change in Sa7 Equals 0" interrupt within the E1 Receive Framer Block.
0	EXZ_ENB	R/W	0	**Change in Excessive Zero Condition Interrupt Enable** This bit enables or disables the "Change in Excessive Zero Condition" interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Excessive Zero Condition. **2.** Whenever the Receive E1 Framer block clears the Excessive Zero Condition 0 = Disables the "Change in Excessive Zero Condition" interrupt within the Receive E1 Framer Block 1 - Enables the "Change in Excessive Zero Condition" interrupt within the Receive E1 Framer Block

TABLE 108: RXLOS/CRC INTERRUPT STATUS REGISTER (RLCISR) **HEX ADDRESS: 0XNB12**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	AIS16	RO	0	**AIS 16 State** This bit indicates whether or not the Receive E1 Framer is declaring AIS 16 (Time slot 16 = All Ones Signal) alarm condition. 0 - Indicates the Receive E1 Framer is currently NOT declaring the AIS16 alarm condition. 1 - Indicates the Receive E1 Framer is currently declaring the AIS16 alarm condition.
3	RxLOSINT	RUR/ WC	0	**Change in Receive LOS condition Interrupt Status** This bit indicates whether or not the "Change in Receive LOS condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the Receive LOS condition. **2.** Whenever the Receive E1 Framer block clears the Receive LOS condition. 0 = Indicates that the "Change in Receive LOS Condition" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change in Receive LOS Condition" interrupt has occurred since the last read of this register.
2	CRCLOCK_INT	RUR/ WC	0	**Change in CRC Multiframe Alignment In-Frame Interrupt Status** This bit indicates whether or not the E1 Receive Framer block has lost or gained CRC Multiframe Alignment since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares CRC Multiframe Alignment LOCK. **2.** Whenever the Receive E1 Framer block declares Loss of CRC Multiframe Alignment. 0 = Indicates that the "Change in CRC Multiframe Alignment In-Frame" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change in CRC Multiframe Alignment In-Frame" interrupt has occurred since the last read of this register.

TABLE 108: RXLOS/CRC INTERRUPT STATUS REGISTER (RLCISR) **HEX ADDRESS: 0XNB12**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	CASLOCK_INT	RUR/ WC	0	**Change in CAS Multiframe Alignment In-Frame Interrupt Status** This bit indicates whether or not the E1 Receive Framer block has lost or gained CAS Multiframe Alignments since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares CAS Multiframe Alignment LOCK. **2.** Whenever the Receive E1 Framer block declares Loss of CAS Multiframe Alignment. 0 = Indicates that the “Change in CAS Multiframe Alignment In-Frame” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in CAS Multiframe Alignment In-Frame” interrupt has occurred since the last read of this register.
0	AIS16_INT	RUR/ WC	0	**Change in AIS16 Alarm Condition Interrupt Status** This bit indicates whether or not the “Change in AIS16 Alarm Condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares AIS16 (TimeSlot 16 = All Ones) condition. **2.** Whenever the Receive E1 Framer block clears AIS16 (TimeSlot 16 = All Ones) condition. 0 = Indicates that the “Change in AIS16 Condition” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in AIS16 Condition” interrupt has occurred since the last read of this register.

TABLE 109: RXLOS/CRC INTERRUPT ENABLE REGISTER (RLCIER) **HEX ADDRESS: 0XNB13**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxLOS_ENB	R/W	0	**Change in Receive LOS Condition Interrupt Enable** This bit enables the “Change in Receive LOS Condition” interrupt. 0 = Enables “Change in Receive LOS Condition” Interrupt. 1 = Disables “Change in Receive LOS Condition” Interrupt.
2	CRCLOCK_ENB	R/W	0	**Change in CRC Multiframe Alignment In-Frame Interrupt Enable** This bit enables the “Change in CRC Multiframe Alignment In-Frame” interrupt. 0 = Enables “Change in CRC Multiframe Alignment In-Frame” Interrupt. 1 = Disables “Change in CRC Multiframe Alignment In-Frame” Interrupt.
1	CASLOCK_ENB	R/W	0	**Change in CAS Multiframe Alignment In-Frame Interrupt Enable** This bit enables the “Change in CAS Multiframe Alignment In-Frame” interrupt. 0 = Enables “Change in CAS Multiframe Alignment In-Frame” Interrupt. 1 = Disables “Change in CAS Multiframe Alignment In-Frame” Interrupt.
0	AIS16_ENB	R/W	0	**Change in AIS16 Condition Interrupt Enable** This bit enables the “Change in AIS16 (Time Slot 16 = All Ones) Condition” interrupt. 0 = Enables “Change in AIS 16 Condition” Interrupt. 1 = Disables “Change in AIS 16 Condition” Interrupt.

TABLE 110: DATA LINK STATUS REGISTER 2 (DLSR2) **HEX ADDRESS: 0XNB16**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RO	0	**HDLC2 Message Type Identifier** This READ ONLY bit indicates the type of data link message received by Receive HDLC 2 Controller. Two types of data link messages are supported within the XRT86VL34 device: Message Oriented Signaling (MOS) or Bit-Oriented Signalling (BOS). 0 = Indicates Bit-Oriented Signaling (BOS) type data link message is received 1 = Indicates Message Oriented Signaling (MOS) type data link message is received
6	TxSOT	RUR/ WC	0	**Transmit HDLC2 Controller Start of Transmission (TxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the “Transmit HDLC2 Controller Start of Transmission (TxSOT) “Interrupt has occurred since the last read of this register. Transmit HDLC2 Controller will declare this interrupt when it has started to transmit a data link message. For sending large HDLC messages, start loading the next available buffer once this interrupt is detected. 0 = Transmit HDLC2 Controller Start of Transmission (TxSOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC2 Controller Start of Transmission interrupt (TxSOT) has occurred since the last read of this register.
5	RxSOT	RUR/ WC	0	**Receive HDLC2 Controller Start of Reception (RxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC2 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC2 Controller Start of Reception (RxSOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC2 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register
4	TxEOT	RUR/ WC	0	**Transmit HDLC2 Controller End of Transmission (TxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit HDLC2 Controller End of Transmission (TxEOT) Interrupt has occurred since the last read of this register. Transmit HDLC2 Controller will declare this interrupt when it has completed its transmission of a data link message. For sending large HDLC messages, it is critical to load the next available buffer before this interrupt occurs. 0 = Transmit HDLC2 Controller End of Transmission (TxEOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC2 Controller End of Transmission (TxEOT) interrupt has occurred since the last read of this register

TABLE 110: DATA LINK STATUS REGISTER 2 (DLSR2) **HEX ADDRESS: 0XNB16**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxEOT	RUR/ WC	0	**Receive HDLC2 Controller End of Reception (RxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC2 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt once it has completely received a full data link message, or once the buffer is full. 0 = Receive HDLC2 Controller End of Reception (RxEOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC2 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register
2	FCS Error	RUR/ WC	0	**FCS Error Interrupt Status** This Reset-Upon-Read bit indicates whether or not the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt when it has detected the FCS error in the most recently received data link message. 0 = FCS Error interrupt has not occurred since the last read of this register 1 = FCS Error interrupt has occurred since the last read of this register
1	Rx ABORT	RUR/ WC	0	**Receipt of Abort Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Abort Sequence interrupt has occurred since last read of this register. Receive HDLC2 Controller will declare this interrupt if it detects the Abort Sequence (i.e. a string of seven (7) consecutive 1's) in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register
0	RxIDLE	RUR/ WC	0	**Receipt of Idle Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC2 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. If RxIDLE "AND" RxEOT occur together, then the entire HDLC message has been received. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 111: DATA LINK INTERRUPT ENABLE REGISTER 2 (DLIER2) **HEX ADDRESS: 0XNB17**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	Reserved
6	TxSOT ENB	R/W	0	**Transmit HDLC2 Controller Start of Transmission (TxSOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC2 Controller Start of Transmission (TxSOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Transmit HDLC2 Controller will generate an interrupt when it has started to transmit a data link message. 0 = Disables the Transmit HDLC2 Controller Start of Transmission (TxSOT) interrupt. 1 = Enables the Transmit HDLC2 Controller Start of Transmission (TxSOT) interrupt.
5	RxSOT ENB	R/W	0	**Receive HDLC2 Controller Start of Reception (RxSOT) Interrupt Enable** This bit enables or disables the “Receive HDLC2 Controller Start of Reception (RxSOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has started to receive a data link message. 0 = Disables the Receive HDLC2 Controller Start of Reception (RxSOT) interrupt. 1 = Enables the Receive HDLC2 Controller Start of Reception (RxSOT) interrupt.
4	TxEOT ENB	R/W	0	**Transmit HDLC2 Controller End of Transmission (TxEOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC2 Controller End of Transmission (TxEOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Transmit HDLC2 Controller will generate an interrupt when it has finished transmitting a data link message. 0 = Disables the Transmit HDLC2 Controller End of Transmission (TxEOT) interrupt. 1 = Enables the Transmit HDLC2 Controller End of Transmission (TxEOT) interrupt.
3	RxEOT ENB	R/W	0	**Receive HDLC2 Controller End of Reception (RxEOT) Interrupt Enable** This bit enables or disables the “Receive HDLC2 Controller End of Reception (RxEOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has finished receiving a complete data link message. 0 = Disables the Receive HDLC2 Controller End of Reception (RxEOT) interrupt. 1 = Enables the Receive HDLC2 Controller End of Reception (RxEOT) interrupt.

TABLE 111: DATA LINK INTERRUPT ENABLE REGISTER 2 (DLIER2) **HEX ADDRESS: 0XNB17**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** This bit enables or disables the “Received FCS Error “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has detected the FCS error within the incoming data link message. 0 = Disables the “Receive FCS Error” interrupt. 1 = Enables the “Receive FCS Error” interrupt.
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** This bit enables or disables the “Receipt of Abort Sequence“ Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has detected the Abort Sequence (i.e. a string of seven (7) consecutive 1’s) within the incoming data link channel. 0 = Disables the “Receipt of Abort Sequence” interrupt. 1 = Enables the “Receipt of Abort Sequence” interrupt.
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** This bit enables or disables the “Receipt of Idle Sequence“ Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has detected the Idle Sequence Octet (i.e. 0x7E) within the incoming data link channel. 0 = Disables the “Receipt of Idle Sequence” interrupt. 1 = Enables the “Receipt of Idle Sequence” interrupt.

TABLE 112: DATA LINK STATUS REGISTER 3 (DLSR3) **HEX ADDRESS: 0XNB26**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RUR/ WC	0	**HDLC3 Message Type Identifier** This READ ONLY bit indicates the type of data link message received by Receive HDLC 3 Controller. Two types of data link messages are supported within the XRT86VL34 device: Message Oriented Signaling (MOS) or Bit-Oriented Signalling (BOS). 0 = Indicates Bit-Oriented Signaling (BOS) type data link message is received 1 = Indicates Message Oriented Signaling (MOS) type data link message is received
6	TxSOT	RUR/ WC	0	**Transmit HDLC3 Controller Start of Transmission (TxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the “Transmit HDLC3 Controller Start of Transmission (TxSOT) “Interrupt has occurred since the last read of this register. Transmit HDLC3 Controller will declare this interrupt when it has started to transmit a data link message. For sending large HDLC messages, start loading the next available buffer once this interrupt is detected. 0 = Transmit HDLC3 Controller Start of Transmission (TxSOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC3 Controller Start of Transmission interrupt (TxSOT) has occurred since the last read of this register.
5	RxSOT	RUR/ WC	0	**Receive HDLC3 Controller Start of Reception (RxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC3 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC3 Controller Start of Reception (RxSOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC3 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register
4	TxEOT	RUR/ WC	0	**Transmit HDLC3 Controller End of Transmission (TxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit HDLC3 Controller End of Transmission (TxEOT) Interrupt has occurred since the last read of this register. Transmit HDLC3 Controller will declare this interrupt when it has completed its transmission of a data link message. For sending large HDLC messages, it is critical to load the next available buffer before this interrupt occurs. 0 = Transmit HDLC3 Controller End of Transmission (TxEOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC3 Controller End of Transmission (TxEOT) interrupt has occurred since the last read of this register

TABLE 112: DATA LINK STATUS REGISTER 3 (DLSR3) **HEX ADDRESS: 0XNB26**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxEOT	RUR/ WC	0	**Receive HDLC3 Controller End of Reception (RxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC3 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt once it has completely received a full data link message, or once the buffer is full. 0 = Receive HDLC3 Controller End of Reception (RxEOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC3 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register
2	FCS Error	RUR/ WC	0	**FCS Error Interrupt Status** This Reset-Upon-Read bit indicates whether or not the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt when it has detected the FCS error in the most recently received data link message. 0 = FCS Error interrupt has not occurred since the last read of this register 1 = FCS Error interrupt has occurred since the last read of this register
1	Rx ABORT	RUR/ WC	0	**Receipt of Abort Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Abort Sequence interrupt has occurred since last read of this register. Receive HDLC3 Controller will declare this interrupt if it detects the Abort Sequence (i.e. a string of seven (7) consecutive 1's) in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register
0	RxIDLE	RUR/ WC	0	**Receipt of Idle Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC3 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. If RxIDLE "AND" RxEOT occur together, then the entire HDLC message has been received. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 113: DATA LINK INTERRUPT ENABLE REGISTER 3 (DLIER3) **HEX ADDRESS: 0XNB27**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC3 Controller Start of Transmission (TxSOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC3 Controller Start of Transmission (TxSOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Transmit HDLC3 Controller will generate an interrupt when it has started to transmit a data link message. 0 = Disables the Transmit HDLC3 Controller Start of Transmission (TxSOT) interrupt. 1 = Enables the Transmit HDLC3 Controller Start of Transmission (TxSOT) interrupt.
5	RxSOT ENB	R/W	0	**Receive HDLC3 Controller Start of Reception (RxSOT) Interrupt Enable** This bit enables or disables the “Receive HDLC3 Controller Start of Reception (RxSOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has started to receive a data link message. 0 = Disables the Receive HDLC3 Controller Start of Reception (RxSOT) interrupt. 1 = Enables the Receive HDLC3 Controller Start of Reception (RxSOT) interrupt.
4	TxEOT ENB	R/W	0	**Transmit HDLC3 Controller End of Transmission (TxEOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC3 Controller End of Transmission (TxEOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Transmit HDLC3 Controller will generate an interrupt when it has finished transmitting a data link message. 0 = Disables the Transmit HDLC3 Controller End of Transmission (TxEOT) interrupt. 1 = Enables the Transmit HDLC3 Controller End of Transmission (TxEOT) interrupt.
3	RxEOT ENB	R/W	0	**Receive HDLC3 Controller End of Reception (RxEOT) Interrupt Enable** This bit enables or disables the “Receive HDLC3 Controller End of Reception (RxEOT) “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has finished receiving a complete data link message. 0 = Disables the Receive HDLC3 Controller End of Reception (RxEOT) interrupt. 1 = Enables the Receive HDLC3 Controller End of Reception (RxEOT) interrupt.

TABLE 113: DATA LINK INTERRUPT ENABLE REGISTER 3 (DLIER3) **HEX ADDRESS: 0XNB27**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** This bit enables or disables the “Received FCS Error “Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has detected the FCS error within the incoming data link message. 0 = Disables the “Receive FCS Error” interrupt. 1 = Enables the “Receive FCS Error” interrupt.
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** This bit enables or disables the “Receipt of Abort Sequence“ Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has detected the Abort Sequence (i.e. a string of seven (7) consecutive 1’s) within the incoming data link channel. 0 = Disables the “Receipt of Abort Sequence” interrupt. 1 = Enables the “Receipt of Abort Sequence” interrupt.
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** This bit enables or disables the “Receipt of Idle Sequence“ Interrupt within the XRT86VL34 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has detected the Idle Sequence Octet (i.e. 0x7E) within the incoming data link channel. 0 = Disables the “Receipt of Idle Sequence” interrupt. 1 = Enables the “Receipt of Idle Sequence” interrupt.

2.0 LINE INTERFACE UNIT (LIU SECTION) REGISTERS

TABLE 114: LIU CHANNEL CONTROL REGISTER 0 (LIUCCR0) **HEX ADDRESS: 0X0FN0**

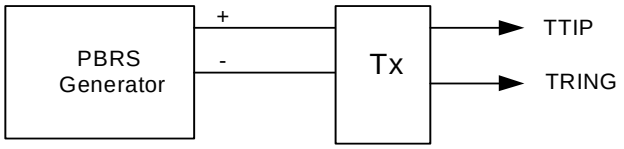
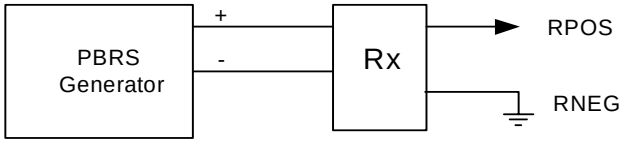
BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	QRSS_n/ PRBS_n	R/W	0	**QRSS/PRBS Select Bits** These bits are used to select between QRSS and PRBS. 0 = PRBS_n (2^{15} - 1) 1 = QRSS_n (2^{20} - 1)
6	PRBS_Rx_n/ PRBS_$\overline{Tx}$_n	R/W	0	**PRBS Receive/Transmit Select:** This bit is used to select where the output of the PRBS Generator is directed if PRBS generation is enabled. 0 = Normal Operation - PRBS generator is output on TTIP and TRING if PRBS generation is enabled. 1 = PRBS Generator is output on RPOS and RCLK. Bit 6 = "0"  Bit 6 = "1" 
5	RXON_n	R/W	0	**Receiver ON:** This bit permits the user to either turn on or turn off the Receive Section of XRT86VL34. If the user turns on the Receive Section, then XRT86VL34 will begin to receive the incoming data-stream via the RTIP and RRING input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section except the MCLKIN Phase Locked Loop (PLL) will be powered down. 0 = Shuts off the Receive Section of XRT86VL34. 1 = Turns on the Receive Section of XRT86VL34.

TABLE 114: LIU CHANNEL CONTROL REGISTER 0 (LIUCCR0) **HEX ADDRESS: 0X0FN0**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4-0	EQC[4:0]	R/W	00000	**Equalizer Control [4:0]:** These bits are used to control the transmit pulse shaping, transmit line build-out (LBO) and receive sensitivity level. The Transmit Pulse Shape can be controlled by adjusting the Transmit Line Build-Out Settings for different cable length in E1 mode. Transmit pulse shape can also be controlled by using the Arbitrary mode, where users can specify the amplitude of the pulse shape by using the 8 Arbitrary Pulse Segments provided in the LIU registers (0x0Fn8-0xnFnF), where n is the channel number. The XRT86VL34 device supports both long haul and short haul applications which can also be selected using the EQC[4:0] bits. Table 115 presents the corresponding Transmit Line Build Out and Receive Sensitivity settings using different combinations of these five EQC[4:0] bits.

TABLE 115: EQUALIZER CONTROL AND TRANSMIT LINE BUILD OUT

EQC[4:0]	T1 MODE/RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE
0x00h	T1 Long Haul/36dB	0dB	100Ω TP
0x01h	T1 Long Haul/36dB	-7.5dB	100Ω TP
0x02h	T1 Long Haul/36dB	-15dB	100Ω TP
0x03h	T1 Long Haul/36dB	-22.5dB	100Ω TP
0x04h	T1 Long Haul/45dB	0dB	100Ω TP
0x05h	T1 Long Haul/45dB	-7.5dB	100Ω TP
0x06h	T1 Long Haul/45dB	-15dB	100Ω TP
0x07h	T1 Long Haul/45dB	-22.5dB	100Ω TP
0x08h	T1 Short Haul/15dB	0 to 133 feet (0.6dB)	100Ω TP
0x09h	T1 Short Haul/15dB	133 to 266 feet (1.2dB)	100Ω TP
0x0Ah	T1 Short Haul/15dB	266 to 399 feet (1.8dB)	100Ω TP
0x0Bh	T1 Short Haul/15dB	399 to 533 feet (2.4dB)	100Ω TP
0x0Ch	T1 Short Haul/15dB	533 to 655 feet (3.0dB)	100Ω TP
0x0Dh	T1 Short Haul/15dB	Arbitrary Pulse	100Ω TP
0x0Eh	T1 Gain Mode/29dB	0 to 133 feet (0.6dB)	100Ω TP
0x0Fh	T1 Gain Mode/29dB	133 to 266 feet (1.2dB)	100Ω TP
0x10h	T1 Gain Mode/29dB	266 to 399 feet (1.8dB)	100Ω TP
0x11h	T1 Gain Mode/29dB	399 to 533 feet (2.4dB)	100Ω TP
0x12h	T1 Gain Mode/29dB	533 to 655 feet (3.0dB)	100Ω TP
0x13h	T1 Gain Mode/29dB	Arbitrary Pulse	100Ω TP
0x14h	T1 Gain Mode/29dB	0dB	100Ω TP
0x15h	T1 Gain Mode/29dB	-7.5dB	100Ω TP
0x16h	T1 Gain Mode/29dB	-15dB	100Ω TP
0x17h	T1 Gain Mode/29dB	-22.5dB	100Ω TP
0x18h	E1 Long Haul/36dB	ITU G.703	75Ω Coax
0x19h	E1 Long Haul/36dB	ITU G.703	120Ω TP
0x1Ah	E1 Long Haul/45dB	ITU G.703	75Ω Coax
0x1Bh	E1 Long Haul/45dB	ITU G.703	120Ω TP
0x1Ch	E1 Short Haul/15dB	ITU G.703	75Ω Coax
0x1Dh	E1 Short Haul/15dB	ITU G.703	120Ω TP
0x1Eh	E1 Gain Mode/29dB	ITU G.703	75Ω Coax
0x1Fh	E1 Gain Mode/29dB	ITU G.703	120Ω TP

TABLE 116: LIU CHANNEL CONTROL REGISTER 1 (LIUCCR1) **HEX ADDRESS: 0X0FN1**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RXTSEL_n	R/W	0	**Receiver Termination Select:** Upon power up, the receivers are in “High” impedance. The LIU provides an option for user to have either software or hardware control over receive termination. If RxTCNTL (bit 6 in Register 0x0FE2) is set to’0’, receive termination can be selected by programming this register bit. To switch control to the hardware pin (RxTSEL pin), RxTCNTL must be programmed to “1”. Once control has been granted to the hardware pin, RxTSEL must be pulled “High” to switch to internal termination. If RxTCNTL is set to’0’, receive termination can be selected by setting this bit according to the following table: **RXTSEL** / **RX Termination** **0** / **"High" Impedance** **1** / **Internal**
6	TXTSEL_n	R/W	0	**Transmit Termination Select:** This bit is used to select between internal termination or “High” impedance modes for the E1 transmitter according to the following table: **TXTSEL** / **TX Termination** **0** / **"High" Impedance** **1** / **Internal**
5-4	TERSEL[1:0]	R/W	00	**Termination Impedance Select [1:0]:** These bits are used to control the transmit and receive termination impedance when the LIU block is configured in Internal Termination Mode. In internal termination mode, (i.e., TXTSEL = “1” and RXTSEL = “1”), internal transmit and receive termination can be selected according to the following table: **TERSEL1** / **TERSEL0** / **Internal Transmit and Receive Termination** 0 / 0 / 100Ω 0 / 1 / 110Ω 1 / 0 / 75Ω 1 / 1 / 120Ω ***NOTE:*** *In the internal termination mode, the transmitter output should be AC coupled to the transformer.*

TABLE 116: LIU CHANNEL CONTROL REGISTER 1 (LIUCCR1) **HEX ADDRESS: 0X0FN1**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxJASEL_n	R/W	0	**Receive Jitter Attenuator Enable** This bit permits the user to enable or disable the Jitter Attenuator in the Receive Path within the XRT86VL34 device. 0 = Disables the Jitter Attenuator to operate in the Receive Path within the Receive E1 LIU Block. 1 = Enables the Jitter Attenuator to operate in the Receive Path within the Receive E1 LIU Block.
2	TxJASEL_n	R/W	0	**Transmit Jitter Attenuator Enable** This bit permits the user to enable or disable the Jitter Attenuator in the Transmit Path within the XRT86VL34 device. 0 = Disables the Jitter Attenuator to operate in the Transmit Path within the Transmit E1 LIU Block. 1 = Enables the Jitter Attenuator to operate in the Transmit Path within the Transmit E1 LIU Block.
1	JABW_n	R/W	0	**Jitter Attenuator Bandwidth Select:** In E1 mode, this bit is used to select the Jitter Attenuator Bandwidth as well as the FIFO size. 1 = Selects a 1.5Hz Bandwidth for the Jitter Attenuator. The FIFO length will be automatically set to 64 bits. 0 = Setting this bit to “0” will select 10Hz Bandwidth for the Jitter Attenuator. The FIFOS (bit D0 of this register) will be used to select the FIFO size. The table below presents the Jitter Attenuator and FIFO settings corresponding to the combinations of this JABW and FIFOS bits in both T1 and E1 mode.
0	FIFOS_n	R/W	0	**FIFO Size Select:** See table of bit D1 above for the function of this bit.

Mode	JABW bit D1	FIFOS_n bit D0	JA B-W Hz	FIFO Size
T1	0	0	3	32
T1	0	1	3	64
T1	1	0	3	32
T1	1	1	3	64
E1	0	0	10	32
E1	0	1	10	64
E1	1	0	1.5	64
E1	1	1	1.5	64

TABLE 117: LIU CHANNEL CONTROL REGISTER 2 (LIUCCR2) **HEX ADDRESS: 0X0FN2**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	INVQRSS_n	R/W	0	**Invert QRSS Pattern:** This bit inverts the output PRBS/QRSS pattern if the LIU Block is configured to transmit a PRBS/QRSS pattern. 0 = The LIU will NOT invert the output PRBS/QRSS pattern 1 = The LIU will invert the output PRBS/QRSS pattern
6-4	TXTEST[2:0]	R/W	000	**Transmit Test Pattern [2:0]**: These bits are used to configure the Transmit E1 LIU Block to generate and transmit test patterns according to the following table. Use of these bits automatically places the LIU section in Single Rail mode. When this happens, the Framer section must be placed in Single Rail mode in Reg 0xn101. **TXTEST2 / TXTEST1 / TXTEST0 / Test Pattern** 0 / X / X / No Pattern 1 / 0 / 0 / TDQRSS 1 / 0 / 1 / TAOS 1 / 1 / 0 / TLUC 1 / 1 / 1 / TLDC **TDQRSS (Transmit/Detect Quasi-Random Signal):** QRSS pattern is a 2^{15}-1 pseudo-random bit sequence (PRBS) pattern. **TAOS (Transmit All Ones):** Whenever the user implements this configuration setting, the Transmit E1 LIU Block will ignore the data that it is accepting from the Transmit E1 Framer block (as well as the upstream system-side terminal equipment) and overwrite this data with the All Ones Pattern. **TLUC (Transmit Network Loop-Up Code):** The Transmit E1 LIU Block will generate and transmit the Network Loop-Up Code of “00001” to the line for the selected channel number n. When Network Loop-Up code is being transmitted, the XRT86VL34 will ignore the “Automatic Loop-Code detection and Remote Loop-Back activation” (NLCDE1 =“1”, NLCDE0 =“1” of register 0x0Fn3) in order to avoid activating Remote Digital Loop-Back automatically when the remote terminal responds to the Loop-Back request. **TLDC (Transmit Network Loop-Down Code):** The Transmit E1 LIU Block will generate and transmit the Network Loop-Down Code of “001” to the line for the selected channel number n.

TABLE 117: LIU CHANNEL CONTROL REGISTER 2 (LIUCCR2) **HEX ADDRESS: 0X0FN2**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	TXON_n	R/W	0	**Transmitter ON:** This bit permits the user to either turn on or turn off the Transmit Driver of XRT86VL34. If the user turns on the Transmit Driver, then XRT86VL34 will begin to transmit DS1 data (on the line) via the TTIP and TRING output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP and TRING output pins will be tri-stated. 0 = Shuts off the Transmit Driver associated with the XRT86VL34 device and tri-states the TTIP and TRING output pins. 1 = Turns on the Transmit Driver associated with the XRT86VL34 device. ***NOTE:*** *If the user wishes to exercise software control over the state of the Transmit Driver of the XRT86VL34, then it is imperative that the user pull the TxON pin to a logic "HIGH" level.*
2-0	LOOP2_n	R/W	000	**Loop-Back control [2:0]:** These bits control the Loop-Back Modes of the LIU section, according to the table below.

LOOP2	LOOP1	LOOP0	Loop-Back Mode
0	X	X	No Loop-Back
1	0	0	Dual Loop-Back
1	0	1	Analog Loop-Back
1	1	0	Remote Loop-Back
1	1	1	Digital Loop-Back

TABLE 118: LIU CHANNEL CONTROL REGISTER 3 (LIUCCR3) **HEX ADDRESS: 0X0FN3**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	NLCDE[1:0]	R/W	00	**Network Loop Code Detection Enable [1:0]:** These bits are used to control the Loop-Code detection on the receive path of each channel, according to the table below. This part must be in Single Rail mode to detect. **NLCDE[1:0]** — **NETWORK LOOP CODE DETECTION ENABLE** 00 — Disables Loop Code Detection 01 — Enables Loop-Up Code Detection on the Receive Path. 10 — Enables Loop-Down Code Detection on the Receive Path. 11 — Enables Automatic Loop-Up Code Detection on the Receive Path and Remote Loop-Back Activation upon detecting Loop-Up Code. **Loop-Up Code Detection Enable:** The XRT86VL34 is configured to monitor the receive data for the Loop-Up code Pattern (i.e. a string of four ‘0’s followed by one ‘1’ pattern). When the presence of the “00001” pattern is detected for more than 5 seconds, the status of the NLCD bit (bit 3 of register 0x0Fn5) is set to “1” and if the NLCD interrupt is enabled (bit 3 of register 0x0Fn4), an interrupt will be generated. **Loop-Down Code Detection Enable:** The XRT86VL34 is configured to monitor the receive data for the Loop-Down code Pattern (i.e. a string of two ‘0’s followed by one ‘1’ pattern). When the presence of the “001” pattern is detected for more than 5 seconds, the status of the NLCD bit (bit 3 of register 0x0Fn5) is set to “1” and if the NLCD interrupt is enabled (bit 3 of register 0x0Fn4), an interrupt will be generated. **Automatic Loop-Up Code Detection and Remote Loop Back Activation Enable:** When this mode is enabled, the state of the NLCD bit (bit 3 of register 0x0Fn5) is reset to “0” and the XRT86VL34 is configured to monitor the receive data for the Loop-Up code. If the “00001” pattern is detected for longer than 5 seconds, then the NLCD bit (bit 3 of register 0x0Fn5) is set “1”, and Remote Loop-Back is activated. Once the remote loop-back is activated, the XRT86VL34 is automatically programmed to monitor the receive data for the Loop-Down code. The NLCD bit stays set even after the chip stops receiving the Loop-Up code. The Remote Loop-Back condition is removed only when the XRT86VL34 receives the Loop-Down code for more than 5 seconds or if the Automatic Loop-Code detection mode is terminated.
5-2	Reserved	R/W	0	This Bit Is Not Used

TABLE 118: LIU CHANNEL CONTROL REGISTER 3 (LIUCCR3) **HEX ADDRESS: 0X0FN3**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	INSBER_n	R/W	0	**Insert Bit Error:** This bit is used to insert a single bit error on the transmitter of the E1 LIU Block. When the E1 LIU Block is configured to transmit and detect the QRSS pattern, (i.e., TxTEST[2:0] bits set to ‘b100’), a “0” to “1” transition of this bit will insert a bit error in the transmitted QRSS pattern of the selected channel number n. The state of this bit is sampled on the rising edge of the respective TCLK_n. ***NOTE:*** *To ensure the insertion of bit error, a “0” should be written in this bit location before writing a “1”.*
0	Reserved	R/W	0	This Bit Is Not Used

TABLE 119: LIU CHANNEL CONTROL INTERRUPT ENABLE REGISTER (LIUCCIER) **HEX ADDRESS: 0X0FN4**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	RO	0	This Bit Is Not Used
6	DMOIE_n	R/W	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Enable:** This bit permits the user to either enable or disable the "Change of Transmit DMO Condition" Interrupt. If the user enables this interrupt, then the XRT86VL34 device will generate an interrupt any time when either one of the following events occur. **1.** Whenever the Transmit Section toggles the DMO Status bit (Bit 6 or Register 0x0Fn5) to "1". **2.** Whenever the Transmit Section toggles the DMO Status bit (Bit 6 or Register 0x0Fn5) to "0". 0 – Disables the "Change in the DMO Condition" Interrupt. 1 – Enables the "Change in the DMO Condition" Interrupt.
5	FLSIE_n	R/W	0	**FIFO Limit Status Interrupt Enable:** This bit permits the user to either enable or disable the "FIFO Limit Status" Interrupt. If the user enables this interrupt, then the XRT86VL34 device will generate an interrupt when the jitter attenuator Read/Write FIFO pointers are within +/- 3 bits. 0 = Disables the "FIFO Limit Status" Interrupt 1 = Enables the "FIFO Limit Status" Interrupt
4	Reserved	-	-	This bit is not used.
3	NLCDIE_n	R/W	0	**Change in Network Loop-Code Detection Interrupt Enable:** This bit permits the user to either enable or disable the "Change in Network Loop-Code Detection" Interrupt. If the user enables this interrupt, then the XRT86VL34 device will generate an interrupt any time when either one of the following events occur. **1.** Whenever the Receive Section (within XRT86VL34) detects the Network Loop-Code (Loop-Up or Loop-Down depending on which Loop-Code the Receive LIU is configured to detect). **2.** Whenever the Receive Section (within XRT86VL34) no longer detects the Network Loop-Code (Loop-Up or Loop-Down depending on which Loop-Code the Receive LIU is configured to detect). 0 – Disables the "Change in Network Loop-Code Detection" Interrupt. 1 – Enables the "Change in Network Loop-Code Detection" Interrupt.
2	Reserved	-	-	This bit is not used

TABLE 119: LIU CHANNEL CONTROL INTERRUPT ENABLE REGISTER (LIUCCIER) **HEX ADDRESS: 0X0FN4**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RLOSIE_n	R/W	0	**Change of the Receive LOS (Loss of Signal) Defect Condition Interrupt Enable:** This bit permits the user to either enable or disable the "Change of the Receive LOS Defect Condition" Interrupt. If the user enables this interrupt, then the XRT86VL34 device will generate an interrupt any time when either one of the following events occur. **1.** Whenever the Receive Section (within XRT86VL34) declares the LOS Defect Condition. **2.** Whenever the Receive Section (within XRT86VL34) clears the LOS Defect condition. 0 – Disables the "Change in the LOS Defect Condition" Interrupt. 1 – Enables the "Change in the LOS Defect Condition" Interrupt.
0	QRPDIE_n	R/W	0	**Change in QRSS Pattern Detection Interrupt Enable:** This bit permits the user to either enable or disable the "Change in QRSS Pattern Detection" Interrupt. If the user enables this interrupt, then the XRT86VL34 device will generate an interrupt any time when either one of the following events occur. **1.** Whenever the Receive Section (within XRT86VL34) detects the QRSS Pattern. **2.** Whenever the Receive Section (within XRT86VL34) no longer detects the QRSS Pattern. 0 – Disables the "Change in QRSS Pattern Detection" Interrupt. 1 – Enables the "Change in QRSS Pattern Detection" Interrupt.

NOTE: *Register 0x0FN4, 0x0FN5 and 0x0FN6 only work if the LIU is placed in Single Rail mode. If done so, the Framer block must also be placed in Single Rail mode in Register 0xn101.*

TABLE 120: LIU CHANNEL CONTROL STATUS REGISTER (LIUCCSR) **HEX ADDRESS: 0X0FN5**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	RO	0	
6	DMO_n	RO	0	**Driver Monitor Output (DMO) Status:** This READ-ONLY bit indicates whether or not the Transmit Section is currently declaring the DMO Alarm condition. The Transmit Section will check the Transmit Output E1 Line signal for bipolar pulses via the TTIP and TRING output signals. If the Transmit Section were to detect no bipolar signal for 128 consecutive bit-periods, then it will declare the Transmit DMO Alarm condition. This particular alarm can be used to check for fault conditions on the Transmit Output Line Signal path. The Transmit Section will clear the Transmit DMO Alarm condition the instant that it detects some bipolar activity on the Transmit Output Line signal. 0 = Indicates that the Transmit Section of XRT86VL34 is NOT currently declaring the Transmit DMO Alarm condition. 1 = Indicates that the Transmit Section of XRT86VL34 is currently declaring the Transmit DMO Alarm condition. ***NOTE:*** *If the DMO interrupt is enabled (DMOIE - bit D6 of register 0x0Fn4), any transition on this bit will generate an Interrupt.*
5	FLS_n	RO	0	**FIFO Limit Status:** This READ-ONLY bit indicates whether or not the XRT86VL34 is currently declaring the FIFO Limit Status. This bit is set to a “1” to indicate that the jitter attenuator Read/Write FIFO pointers are within +/- 3 bits. 0 = Indicates that the XRT86VL34 is NOT currently declaring the FIFO Limit Status. 1 = Indicates that the XRT86VL34 is currently declaring the FIFO Limit Status. ***NOTE:*** *If the FIFO Limit Status Interrupt is enabled, (FLSIE bit - bit D5 of register 0x0Fn4), any transition on this bit will generate an Interrupt.*
4	Reserved	-	0	This Bit Is Not Used

TABLE 120: LIU CHANNEL CONTROL STATUS REGISTER (LIUCCSR) **HEX ADDRESS: 0X0FN5**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	NLCD_n	RO	0	**Network Loop-Code Detection Status Bit:** This bit operates differently in the Manual or the Automatic Network Loop-Code detection modes. **Manual Loop-Up Code detection mode** (.i.e If NLCDE1 = “0” and NLCDE0 = “1”), this bit gets set to “1” as soon as the Loop-Up Code (“00001”) is detected in the receive data for longer than 5 seconds. This bit stays high as long as the Receive E1 LIU Block detects the presence of the Loop-Up code in the receive data and it is reset to “0” as soon as it stops receiving the Loop-Up Code. If the NLCD interrupt is enabled, the XRT86VL34 will initiate an interrupt on every transition of the NLCD status bit. **Manual Loop-Down Code detection mode** (i.e., If NLCDE1 = “1” and NLCDE0 = “0”), this bit gets set to “1” as soon as the Loop-Down Code (“001”) is detected in the receive data for longer than 5 seconds. This bit stays high as long as the Receive E1 LIU Block detects the presence of the Loop-Down code in the receive data and it is reset to “0” as soon as it stops receiving the Loop-Down Code. If the NLCD interrupt is enabled, the XRT86VL34 will initiate an interrupt on every transition of the NLCD status bit. **Automatic Loop-code detection mode** (i.e., If NLCDE1 = “1” and NLCDE0 =”1”), the state of the NLCD status bit is reset to “0” and the XRT86VL34 is programmed to monitor the receive input data for the Loop-Up code. This bit is set to a “1” to indicate that the Network Loop Code is detected for more than 5 seconds. Simultaneously the Remote Loop-Back condition is automatically activated and the XRT86VL34 is programmed to monitor the receive data for the Network Loop Down code. The NLCD bit stays ‘high’ as long as the Remote Loop-Back condition is in effect even if the chip stops receiving the Loop-Up code. Remote Loop-Back is removed only if the XRT86VL34 detects the Loop-Down Code “001” pattern for longer than 5 seconds in the receive data. Upon detecting the Loop-Down Code “001” pattern, the XRT86VL34 will reset the NLCD status bit and an interrupt will be generated if the NLCD interrupt enable bit is enabled. Users can monitor the state of this bit to determine if the Remote Loop-Back is activated.
2	Reserved	-	0	This Bit Is Not Used

TABLE 120: LIU CHANNEL CONTROL STATUS REGISTER (LIUCCSR) **HEX ADDRESS: 0X0FN5**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RLOS_n	RO	0	**Receive Loss of Signal Defect Condition Status:** This READ-ONLY bit indicates whether or not the Receive LIU Block is currently declaring the LOS defect condition. 0 = Indicates that the Receive Section is NOT currently declaring the LOS Defect Condition. 1 = Indicates that the Receive Section is currently declaring the LOS Defect condition. ***NOTE:*** *If the RLOSIE bit (bit D1 of Register 0x0Fn4) is enabled, any transition on this bit will generate an Interrupt.*
0	QRPD_n	RO	0	**Quasi-random Pattern Detection Status:** This READ-ONLY bit indicates whether or not the Receive LIU Block is currently declaring the QRSS Pattern LOCK status. 0 = Indicates that the XRT86VL34 is NOT currently declaring the QRSS Pattern LOCK. 1 = Indicates that the XRT86VL34 is currently declaring the QRSS Pattern LOCK. ***NOTE:*** *If the QRPDIE bit (bit D0 of register 0x0Fn4) is enabled, any transition on this bit will generate an Interrupt.*

NOTE: *Register 0x0FN4, 0x0FN5 and 0x0FN6 only work if the LIU is placed in Single Rail mode. If done so, the Framer block must also be placed in Single Rail mode in Register 0xn101.*

TABLE 121: LIU CHANNEL CONTROL INTERRUPT STATUS REGISTER (LIUCCISR) **HEX ADDRESS: 0X0FN6**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	RO	0	
6	DMOIS_n	RUR/ WC	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Status:** This RESET-upon-READ bit indicates whether or not the "Change of the Transmit DMO Condition" Interrupt has occurred since the last read of this register. 0 = Indicates that the "Change of the Transmit DMO Condition" Interrupt has NOT occurred since the last read of this register. 1 = Indicates that the "Change of the Transmit DMO Condition" Interrupt has occurred since the last read of this register. This bit is set to a "1" every time when DMO_n status bit (bit 6 of Register 0x0Fn5) has changed since the last read of this register. ***NOTE:*** *Users can determine the current state of the "Transmit DMO Condition" by reading out the content of bit 6 within Register 0x0Fn5*
5	FLSIS_n	RUR/ WC	0	**FIFO Limit Interrupt Status:** This RESET-upon-READ bit indicates whether or not the "FIFO Limit" Interrupt has occurred since the last read of this register. 0 = Indicates that the "FIFO Limit Status" Interrupt has NOT occurred since the last read of this register. 1 = Indicates that the "FIFO Limit Status" Interrupt has occurred since the last read of this register. This bit is set to a "1" every time when FIFO Limit Status bit (bit 5 of Register 0x0Fn5) has changed since the last read of this register. ***NOTE:*** *Users can determine the current state of the "FIFO Limit" by reading out the content of bit 5 within Register 0x0Fn5*
4	Reserved	-	-	This bit is not used
3	NLCDIS_n	RUR/ WC	0	**Change in Network Loop-Code Detection Interrupt Status:** This RESET-upon-READ bit indicates whether or not the "Change in Network Loop-Code Detection" Interrupt has occurred since the last read of this register. 0 = Indicates that the "Change in Network Loop-Code Detection" Interrupt has NOT occurred since the last read of this register. 1 = Indicates that the "Change in Network Loop-Code Detection" Interrupt has occurred since the last read of this register. This bit is set to a "1" every time when NLCD status bit (bit 3 of Register 0x0Fn5) has changed since the last read of this register. ***NOTE:*** *Users can determine the current state of the "Network Loop-Code Detection" by reading out the content of bit 3 within Register 0x0Fn5*
2	Reserved	-	-	This bit is not used

TABLE 121: LIU CHANNEL CONTROL INTERRUPT STATUS REGISTER (LIUCCISR) **HEX ADDRESS: 0X0FN6**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RLOSIS_n	RUR/ WC	0	**Change of Receive LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit indicates whether or not the "Change of the Receive LOS Defect Condition" Interrupt has occurred since the last read of this register. 0 = Indicates that the "Change of the Receive LOS Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Change of the Receive LOS Defect Condition" Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the "Receive LOS Defect condition" by reading out the contents of Bit 1 (Receive LOS Defect Condition Status) within Register 0xnFn5.*
0	QRPDIS_n	RUR/ WC	0	**Change in Quasi-Random Pattern Detection Interrupt Status:** This RESET-upon-READ bit indicates whether or not the "Change in QRSS Pattern Detection" Interrupt has occurred since the last read of this register. 0 = Indicates that the "Change in QRSS Pattern Detection" Interrupt has NOT occurred since the last read of this register. 1 = Indicates that the "Change in QRSS Pattern Detection" Interrupt has occurred since the last read of this register. This bit is set to a "1" every time when QRPD status bit (bit 0 of Register 0x0Fn5) has changed since the last read of this register. ***NOTE:*** *Users can determine the current state of the "QRSS Pattern Detection" by reading out the content of bit 0 within Register 0x0Fn5*

NOTE: *Register 0x0FN4, 0x0FN5 and 0x0FN6 only work if the LIU is placed in Single Rail mode. If done so, the Framer block must also be placed in Single Rail mode in Register 0xn101.*

TABLE 122: LIU CHANNEL CONTROL CABLE LOSS REGISTER (LIUCCCCR) **HEX ADDRESS: 0X0FN7**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	RO	0	
6	Reserved	RO	0	
5-0	CLOS[5:0]	RO	0	**Cable Loss [5:0]:** These bits represent the six bit receive selective equalizer setting which is also a binary word that represents the cable attenuation indication within ±1dB. CLOS5_n is the most significant bit (MSB) and CLOS0_n is the least significant bit (LSB).

TABLE 123: LIU CHANNEL CONTROL ARBITRARY REGISTER 1 (LIUCCAR1) **HEX ADDRESS: 0X0FN8**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_Seg1	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 1:** These seven bits form the first of the eight segments of the transmit shape pulse when the XRT86VL34 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). ***NOTE:*** *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 124: LIU CHANNEL CONTROL ARBITRARY REGISTER 2 (LIUCCAR2) **HEX ADDRESS: 0X0FN9**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_Seg2	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 2** These seven bits form the second of the eight segments of the transmit shape pulse when the XRT86VL34 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). ***NOTE:*** *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 125: LIU CHANNEL CONTROL ARBITRARY REGISTER 3 (LIUCCAR3) **HEX ADDRESS: 0X0FNA**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_seg3	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 3** These seven bits form the third of the eight segments of the transmit shape pulse when the XRT86VL34 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). ***NOTE:*** *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 126: LIU CHANNEL CONTROL ARBITRARY REGISTER 4 (LIUCCAR4) **HEX ADDRESS: 0X0FNB**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_seg4	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 4** These seven bits form the forth of the eight segments of the transmit shape pulse when the XRT86VL34 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 127: LIU CHANNEL CONTROL ARBITRARY REGISTER 5 (LIUCCAR5) **HEX ADDRESS: 0X0FNC**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_seg5	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 5** These seven bits form the fifth of the eight segments of the transmit shape pulse when the XRT86VL34 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 128: LIU CHANNEL CONTROL ARBITRARY REGISTER 6 (LIUCCAR6) **HEX ADDRESS: 0X0FND**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_seg6	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 6** These seven bits form the sixth of the eight segments of the transmit shape pulse when the XRT86VL34 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 129: LIU CHANNEL CONTROL ARBITRARY REGISTER 7 (LIUCCAR7) **HEX ADDRESS: 0X0FNE**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6	Arb_seg7	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 7** These seven bits form the seventh of the eight segments of the transmit shape pulse when the XRT86VL34 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 130: LIU CHANNEL CONTROL ARBITRARY REGISTER 8 (LIUCCAR8) **HEX ADDRESS: 0X0FNF**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6	Arb_seg8	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 8** These seven bits form the eight of the eight segments of the transmit shape pulse when the XRT86VL34 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 131: LIU GLOBAL CONTROL REGISTER 0 (LIUGCR0) **HEX ADDRESS: 0X0FE0**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SR	R/W	0	**Single Rail mode** This bit must set to "1" for Single Rail mode to use LIU diagnotic features. The Framer section must be programmed as well in Register 0xn101. 0 - Dual Rail 1 - Single Rail
6	ATAOS	R/W	0	**Automatic Transmit All Ones Upon RLOS:** This bit enables automatic transmission of All Ones Pattern upon detecting the Receive Loss of Signal (RLOS) condition. Once this bit is enabled, the Transmit E1 Framer Block will automatically transmit an All “Ones” data to the line for the channel that detects an RLOS condition. 0 = Disables the “Automatic Transmit All Ones” feature upon detecting RLOS 1 = Enables the “Automatic Transmit All Ones” feature upon detecting RLOS
5	RCLKE	R/W	0	**Receive Clock Data (Framer Bypass mode)** 0 = RPOS/RNEG data is updated on the rising edge of RCLK 1 = RPOS/RNEG data is updated on the falling edge of RCLK
4	TCLKE	R/W	0	**Transmit Clock Data (Framer Bypass mode)** 0 = TPOS/TNEG data is sampled on the falling edge of TCLK 1 = TPOS/TNEG data is sampled on the rising edge of TCLK
3	DATAP	R/W	0	**Data Polarity** 0 = Transmit input and receive output data is active “High” 1 = Transmit input and receive output data is active “Low”
2	Reserved			This Bit Is Not Used

TABLE 131: LIU GLOBAL CONTROL REGISTER 0 (LIUGCR0) **HEX ADDRESS: 0X0FE0**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	GIE	R/W	0	**Global Interrupt Enable:** This bit allows users to enable or disable the global interrupt generation for all channels within the E1 LIU Block. Once this global interrupt is disabled, no interrupt will be generated to the Microprocessor Interrupt Pin even when the individual "source" interrupt status bit pulses 'high'. If this global interrupt is enabled, users still need to enable the individual "source" interrupt in order for the E1 LIU Block to generate an interrupt to the Microprocessor pin. 0 - Disables the global interrupt generation for all channels within the E1 LIU Block. 1 - Enables the global interrupt generation for all channels within the E1 LIU Block.
0	SRESET	R/W	0	**Software Reset µP Registers:** This bit allows users to reset the XRT86VL34 device. Writing a "1" to this bit and keeping it at '1' for longer than 10µs initiates a device reset through the microprocessor interface. Once the XRT86VL34 is reset, all internal circuits are placed in the reset state except the microprocessor register bits. 0 = Disables software reset to the XRT86VL34 device. 1 = Enables software reset to the XRT86VL34 device.

TABLE 132: LIU GLOBAL CONTROL REGISTER 1 (LIUGCR1) **HEX ADDRESS: 0X0FE1**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6	Reserved	R/W	0	
5-4	Gauge [1:0]	R/W	00	**Wire Gauge Selector [1:0]:** This bit together with Guage0 bit (bit 4 within this register) are used to select the wire gauge size as shown in the table below. GAUGE1 / GAUGE0 / Wire Size 0 / 0 / 22 and 24 Gauge 0 / 1 / 22 Gauge 1 / 0 / 24 Gauge 1 / 1 / 26 Gauge

TABLE 132: LIU GLOBAL CONTROL REGISTER 1 (LIUGCR1) **HEX ADDRESS: 0X0FE1**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	E1 Arbitrary Enable			**E1 Arbitrary Mode Enable** This bit is used to enable the Arbitrary Pulse Generators for shaping the transmit pulse shape for E1 mode. If this bit is set to “1”, all 4 channels will be configured for the Arbitrary Mode. However, each channel’s pulse shape is individually controlled by programming the 8 transmit pulse shape segments (channel registers 0x0Fn8 through 0x0FnF) “0” = Disabled (Normal E1 Pulse Shape ITU G.703) “1” = Arbitrary Pulse Enabled
2	RXMUTE	R/W	0	**Receive Output Mute:** This bit permits the user to configure the Receive E1 Block to automatically pull its Recovered Data Output pins to GND anytime (and for the duration that) the Receive E1 LIU Block declares the LOS defect condition. In other words, if this feature is enabled, the Receive E1 LIU Block will automatically “mute” the Recovered data that is being routed to the Receive E1 Framer block anytime (and for the duration that) the Receive E1 LIU Block declares the LOS defect condition. 0 – Disables the “Muting upon LOS” feature. 1 – Enables the “Muting upon LOS” feature. ***NOTE:*** *The receive clock is not muted when this feature is enabled.*
1	EXLOS			**Extended LOS Enable:** This bit allows users to extend the number of zeros at the receive input of each channel before RLOS is declared. When Extended LOS is enabled, the Receive E1 LIU Block will declare RLOS condition when it receives 4096 number of consecutive zeros at the receive input. When Extended LOS is disabled, the Receive E1 LIU Block will declare RLOS condition when it receives 175 number of consecutive zeros at the receive input. 0 = Disables the Extended LOS Feature. 1 = Enables the Extended LOS Feature.
0	$\overline{\text{ICT}}$	R/W	0	**In-Circuit-Testing Enable:** This bit allows users to tristate the output pins of all channels for in-circuit testing purposes. When In-Circuit-Testing is enabled, all output pins of the XRT86VL34 are “Tri-stated”. When In-Circuit-Testing is disabled, all output pins will resume to normal condition. 0 = Disables the In-Circuit-Testing Feature. 1 = Enables the In-Circuit-Testing Feature.

TABLE 133: LIU GLOBAL CONTROL REGISTER 2 (LIUGCR2) **HEX ADDRESS: 0X0FE2**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Force to "0"	R/W	0	**Set to "0"**
6	RxTCNTL	R/W	0	**Receive Termination Select Control** This bit sets the LIU to control the RxTSEL function with either the individual channel register bit or the global hardware pin. 0 = Control of the receive termination is set to the register bits 1 = Control of the receive termination is set to the hardware pin
5-0	Reserved	R/W	0	This Bit Is Not Used

TABLE 134: LIU GLOBAL CONTROL REGISTER 3 (LIUGCR3) **HEX ADDRESS: 0X0FE4**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	MCLKnT1[1:0]	R/W	00	**Master T1 Output Clock Reference [1:0]** These two bits allow users to select the programmable output clock rates for the T1MCLKnOUT pin, according to the table below. **MCLKNT1[1:0]** — **CLOCK RATE OF THE T1MCLKNOUT OUTPUT PIN** 00 — 1.544MHz 01 — 3.088MHz 10 — 6.176MHz 11 — 12.352MHz
5-4	MCLKnE1[1:0]	R/W	00	**Master E1 Output Clock Reference [1:0]:** These two bits allow users to select the programmable output clock rates for the E1MCLKnOUT pin, according to the table below: **MCLKNE1[1:0]** — **CLOCK RATE OF THE E1MCLKNOUT OUTPUT PIN** 00 — 2.048MHz 01 — 4.096MHz 10 — 8.192MHz 11 — 16.384MHz
3-0	Reserved	R/W	0	This Bit Is Not Used.

TABLE 135: LIU GLOBAL CONTROL REGISTER 4 (LIUGCR4) **HEX ADDRESS: 0X0FE9**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	R/W	0	
3-0	CLKSEL[3:0]	R/W	1100	**Clock Select Input [3:0]** These four bits allow users to select the programmable input clock rates for the MCLKIN input pin, according to the table below.

CLKSEL[3:0]	CLOCK RATE OF THE MCLKIN INPUT PIN
0000	2.048MHz
0001	1.544MHz
0010	8kHz
0011	16kHz
0100	56kHz
0101	64kHz
0110	128kHz
0111	256kHz
1000	4.096MHz
1001	3.088MHz
1010	8.192MHz
1011	6.176MHz
1100	16.384MHz
1101	12.352MH
1110	2.048MHz
1111	1.544MHz

NOTE: *User must provide any one of the above clock frequencies to the MCLKIN input pin for the device to be functional.*

TABLE 136: LIU GLOBAL CONTROL REGISTER 5 (LIUGCR5) **HEX ADDRESS: 0X0FEA**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4-7	Reserved	-	0	**These bits are reserved**
3	GCHIS3	RUR/ WC	0	**Global Channel 3 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 3 within the XRT86VL34 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 3 within the XRT86VL34 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 3 within the XRT86VL34 device since the last read of this register.
2	GCHIS2	RUR/ WC	0	**Global Channel 2 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 2 within the XRT86VL34 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 2 within the XRT86VL34 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 2 within the XRT86VL34 device since the last read of this register.
1	GCHIS1	RUR/ WC	0	**Global Channel 1 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 1 within the XRT86VL34 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 1 within the XRT86VL34 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 1 within the XRT86VL34 device since the last read of this register.
0	GCHIS0	RUR/ WC	0	**Global Channel 0 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 0 within the XRT86VL34 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 0 within the XRT86VL34 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 0 within the XRT86VL34 device since the last read of this register.

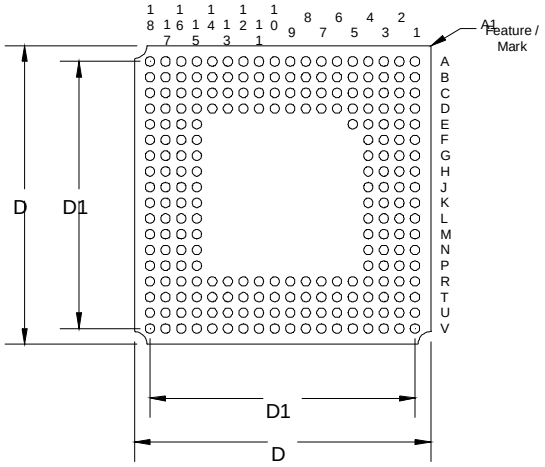
ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL34IB	225 LEAD PBGA	-40^0C to $+85^0$C

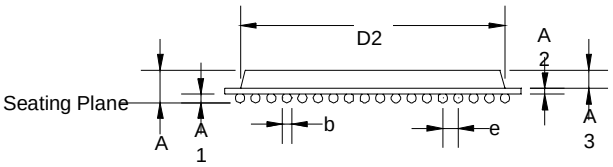
PACKAGE DIMENSIONS

225 Ball Plastic Ball Grid Array (19.0 mm x 19.0 mm, 1.0mm pitch PBGA)

Rev. 1.00



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.049	0.096	1.24	2.45
A1	0.016	0.024	0.40	0.60
A2	0.013	0.024	0.32	0.60
A3	0.020	0.048	0.52	1.22
D	0.740	0.756	18.80	19.20
D1	0.669 BSC		17.00 BSC	
D2	0.665	0.669	16.90	17.00
b	0.020	0.028	0.50	0.70
e	0.039 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
V1.2.0	January 25, 2007	Release to Production.

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