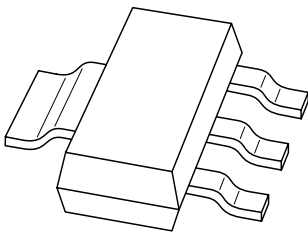


DATA SHEET



PBSS5350Z

50 V low V_{CEsat} PNP transistor

Product specification
Supersedes data of 2003 Jan 20

2003 May 13

50 V low V_{CEsat} PNP transistor

PBSS5350Z

FEATURES

- Low collector-emitter saturation voltage
- High collector current capability: I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- Higher efficiency leading to less heat generation
- Reduced PCB area requirements compared to DPAK.

APPLICATIONS

- Power management
 - DC/DC converters
 - Supply line switching
 - Battery charger
 - Linear voltage regulation (LDO).
- Peripheral drivers
 - Driver in low supply voltage applications, e.g. lamps, LEDs
 - Inductive load driver, e.g. relays, buzzers, motors.

DESCRIPTION

PNP low V_{CEsat} transistor in a SOT223 plastic package.
NPN complement: PBSS4350Z.

MARKING

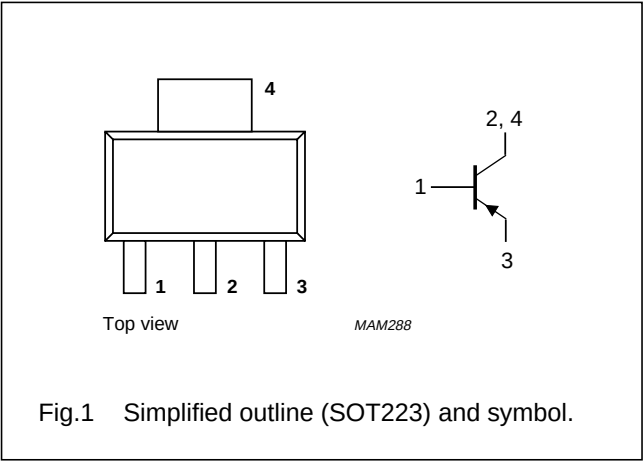
TYPE NUMBER	MARKING CODE
PBSS5350Z	PB5350

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	−50	V
I_C	collector current (DC)	−3	A
I_{CM}	peak collector current	−5	A
R_{CEsat}	equivalent on-resistance	<150	mΩ

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter
4	collector



50 V low V_{CEsat} PNP transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–60	V
V_{CEO}	collector-emitter voltage	open base	–	–50	V
V_{EBO}	emitter-base voltage	open collector	–	–6	V
I_C	collector current (DC)		–	–3	A
I_{CM}	peak collector current		–	–5	A
I_{BM}	peak base current		–	–1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; notes 1 and 3	–	1.35	W
		$T_{amb} \leq 25\text{ °C}$; notes 2 and 3	–	2	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm².
2. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 6 cm².
3. For other mounting conditions see “*Thermal considerations for SOT223 in the General Part of associated Handbook*”.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; notes 1 and 3	92	K/W
		in free air; notes 2 and 3	62.5	K/W

Notes

1. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm.
2. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 6 cm².
3. For other mounting conditions see “*Thermal considerations for SOT223 in the General Part of associated Handbook*”.

50 V low V_{CEsat} PNP transistor

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CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

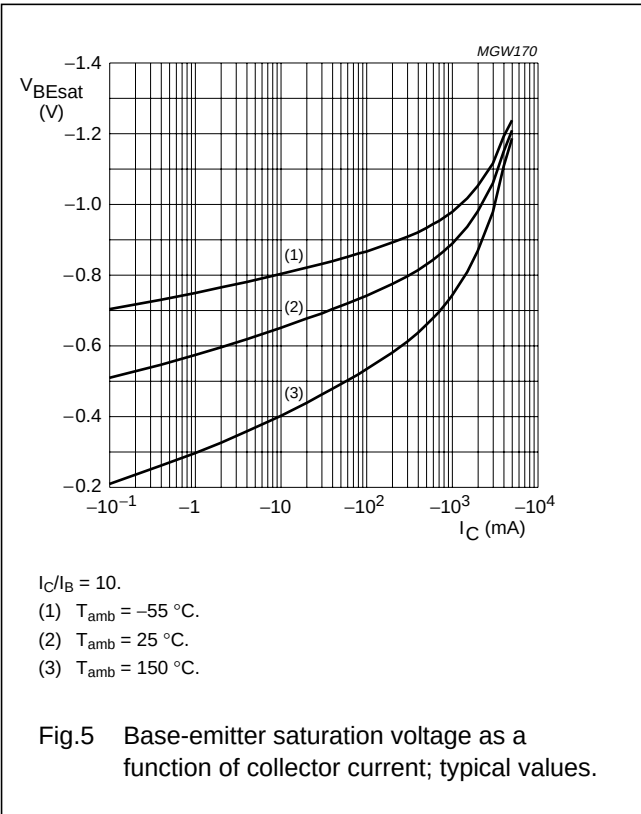
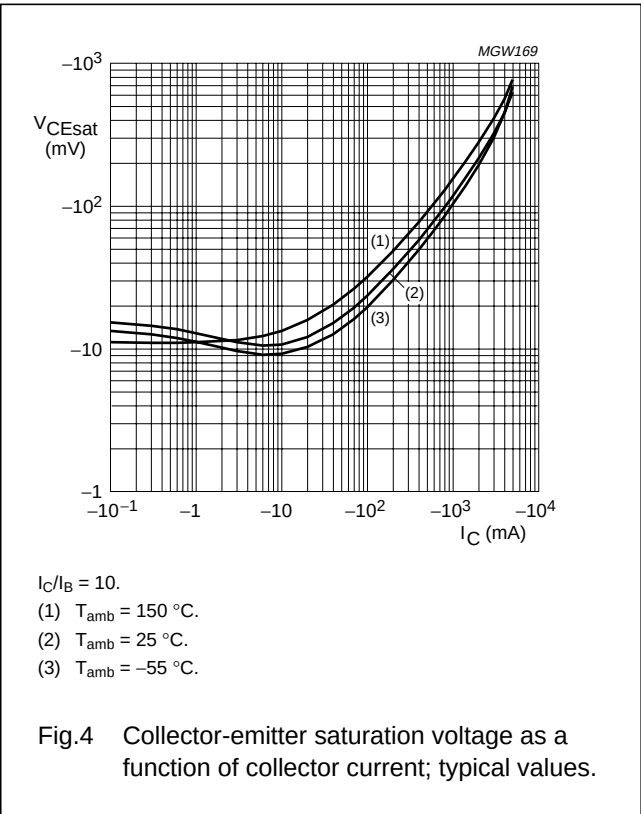
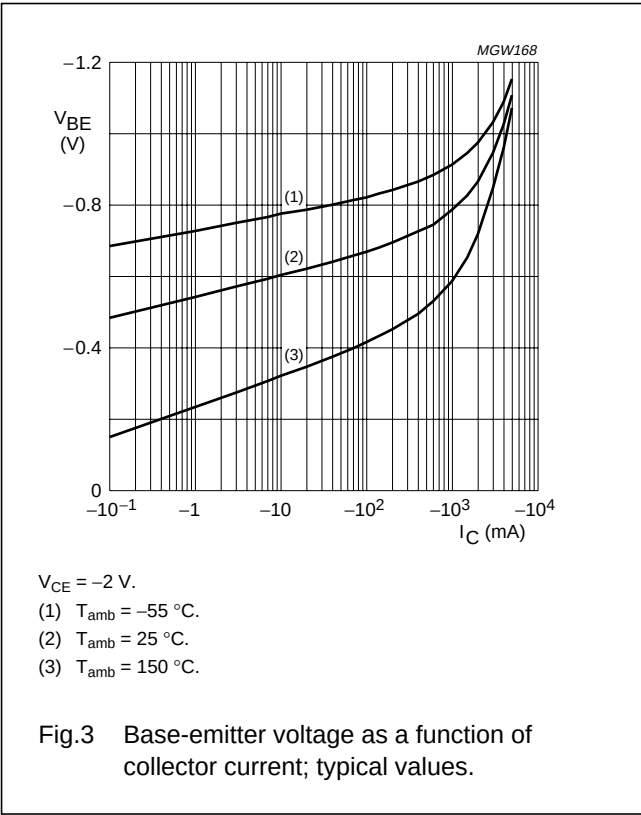
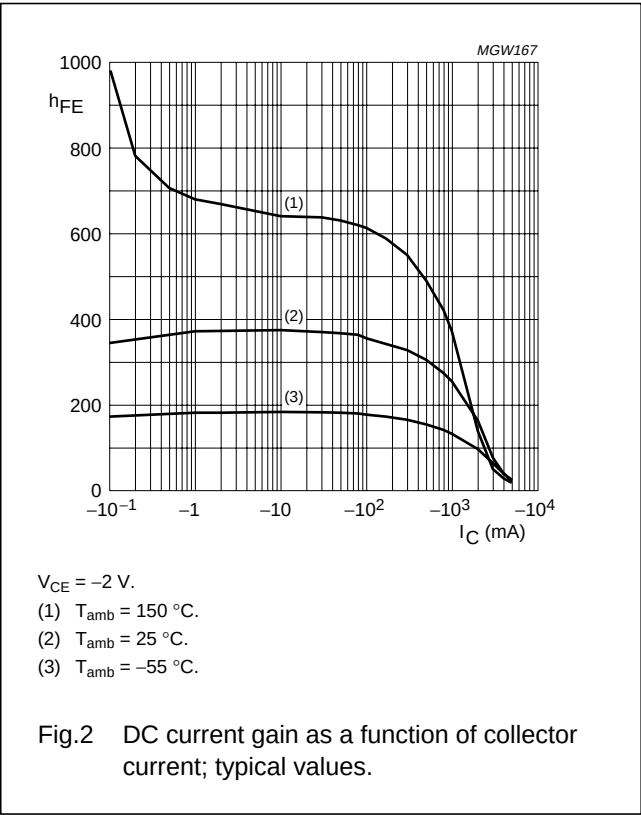
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -50\text{ V}; I_E = 0; T_j = 150\text{ }^{\circ}\text{C}$	–	–	–50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0$	–	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V};$ $I_C = -500\text{ mA}$	200	–	–	
		$I_C = -1\text{ A}; \text{note 1}$	200	–	–	
		$I_C = -2\text{ A}; \text{note 1}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–	–100	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–	–180	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–	–300	mV
R_{CEsat}	equivalent on-resistance	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	120	<150	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–	–1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	–	–	–1.1	V
f_T	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V};$ $f = 100\text{ MHz}$	100	–	–	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	–	40	pF

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.

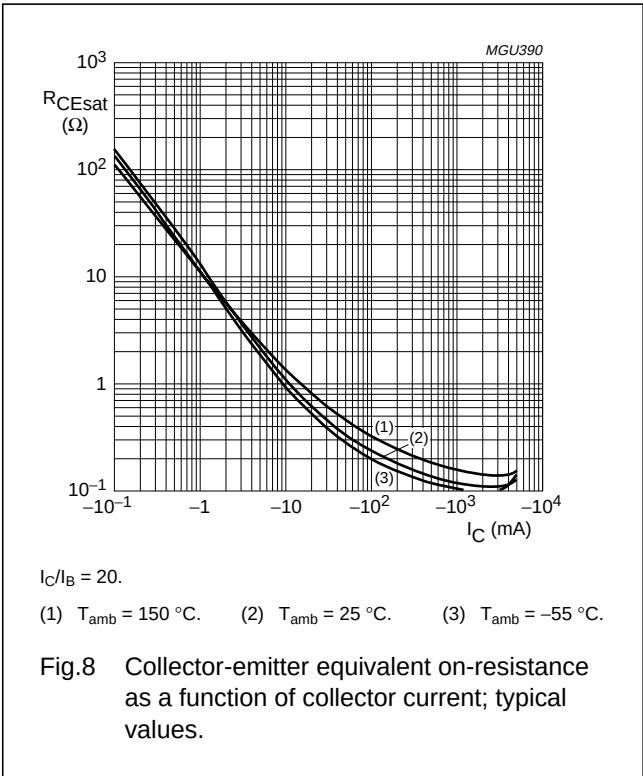
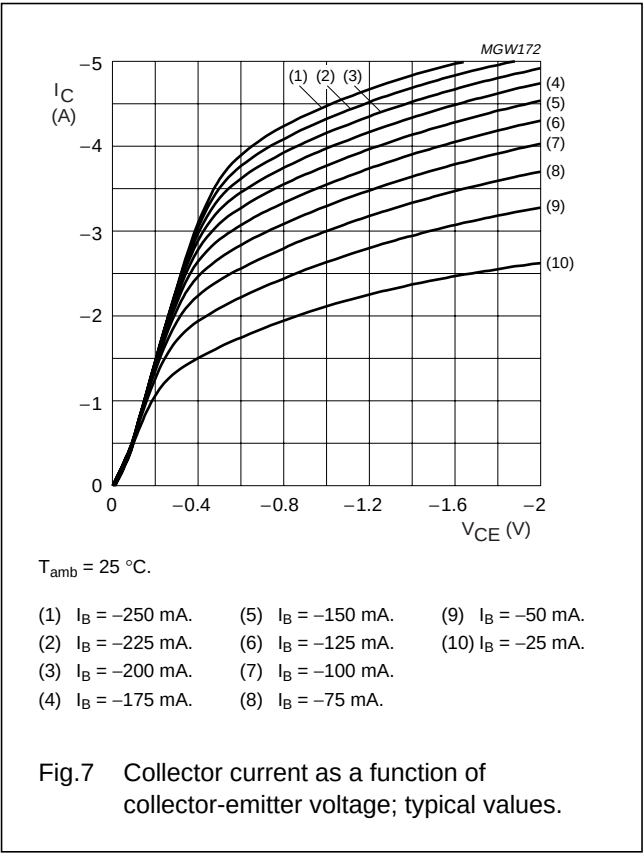
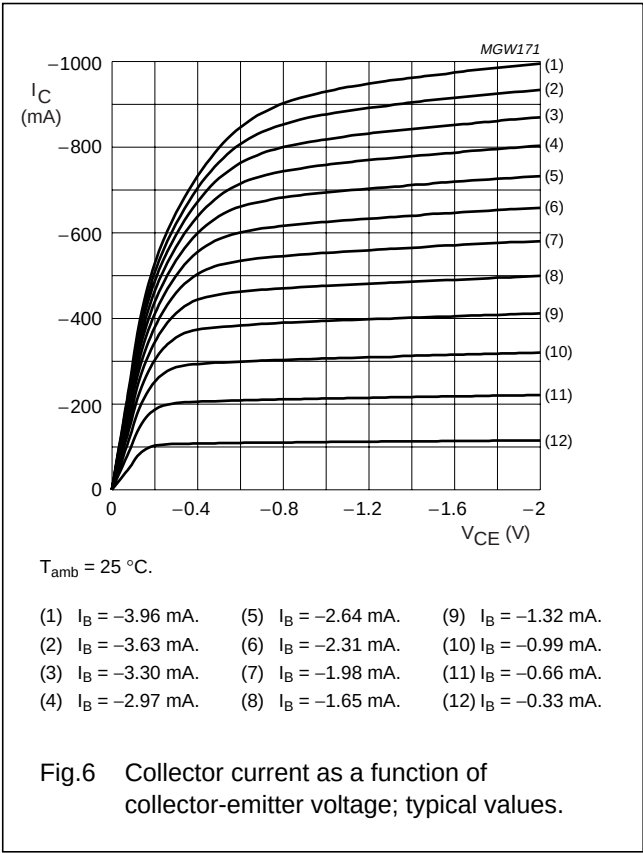
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PBSS5350Z



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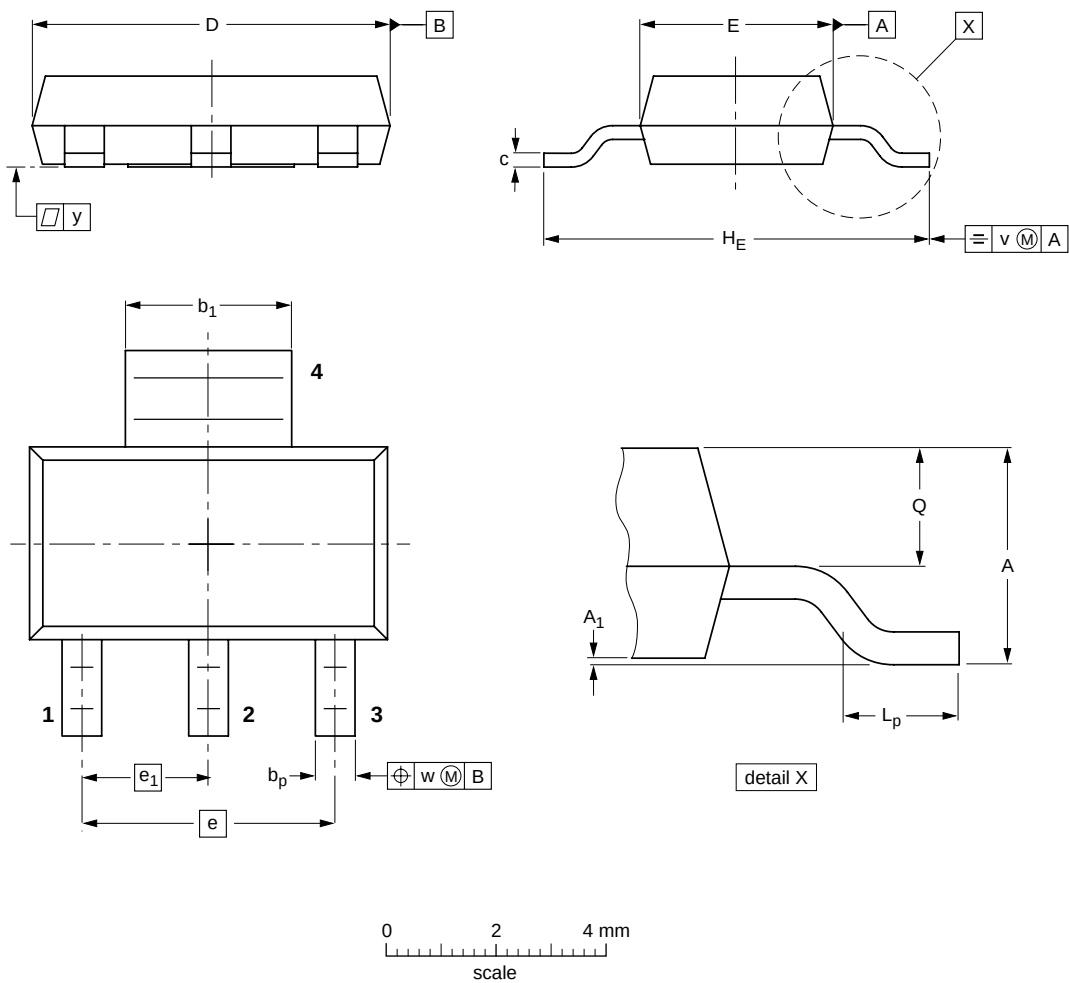
50 V low V_{CEsat} PNP transistor

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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223			SC-73			97-02-28 99-09-13

50 V low V_{CEsat} PNP transistor

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DATA SHEET STATUS

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I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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NOTES

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NOTES

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NOTES

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