USBUF01P6

IPAD™

EMI filter and line termination for USB upstream ports

Applications

EMI Filter and line termination for USB upstream ports on:

- USB Hubs
- PC peripherals

Features

- Monolithic device with recommended line termination for USB upstream ports
- Integrated Rt series termination and C_t bypassing capacitors.
- Integrated ESD protection
- Small package size

Description

The USB specification requires upstream ports to be terminated with pull-up resistors from the D+ and D- lines to Vbus. On the implementation of USB systems, the radiated and conducted EMI should be kept within the required levels as stated by the FCC regulations. In addition to the requirements of termination and EMC compatibility, the computing devices are required to be tested for ESD susceptibility.

The USBUF01P6 provides the recommended line termination while implementing a low pass filter to limit EMI levels and providing ESD protection which exceeds IEC 61000-4-2 level 4 standard. The device is packaged in a SOT-666 which is the smallest available lead frame package (45% smaller than the standard SOT323).

Benefits

- EMI / RFI noise suppression
- Required line termination for USB upstream ports
- ESD protection exceeding IEC 61000-4-2 level 4
- High flexibility in the design of high density boards
- Tailored to meet USB 2.0 standard (low speed and full speed data transmission)

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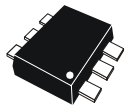
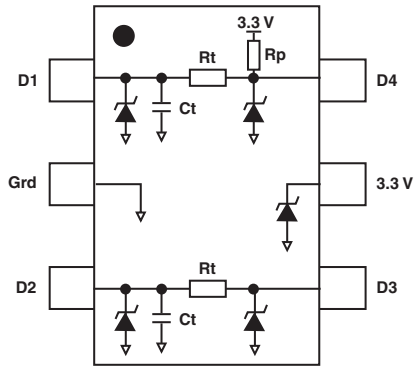


SOT-666IP
(Internal pad)

Functional diagram



Complies with the following standards:

IEC 61000-4-2 level4:

15 kV(air discharge)
8 kV(contact discharge)

MIL STD 883E-Method 3015-7:
Class 3 C = 100 pF R = 1500 Ω
3 positive strikes and 3 negative strikes (F = 1 Hz)

Order codes

Part Number	Marking
USBUF01P6	U

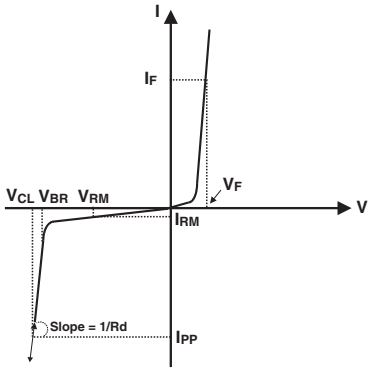
1 Characteristics

Table 1. Absolute maximum rating (T_{amb} = 25° C)

Symbol	Parameter		Value	Unit
V_{PP}	ESD discharge	IEC61000-4-2 air discharge IEC61000-4-2 contact discharge MIL STD 883E - Method 3015-7	± 16 ± 9 ± 25	kV
T_j	Junction temperature		150	° C
T_{stg}	Storage temperature range		-55 to +150	° C
T_L	Maximum lead temperature for soldering during 10 s at 5 mm for case		260	° C
T_{op}	Operating temperature range		-40 to + 85	° C

Table 2. Electrical characteristics (T_{amb} = 25° C)

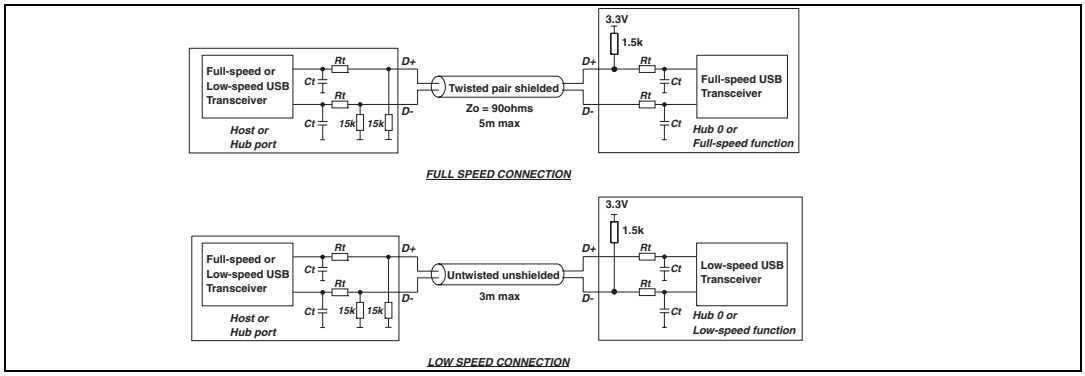
Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop
Rd	Dynamic resistance



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6		10	V
I_{RM}	V_{RM} = 3.3 V per line			500	nA
R_t	Tolerance ± 10%		33		Ω
R_p	Tolerance ± 10%		1.5		kΩ
C_t	Tolerance ± 20%		47		pF

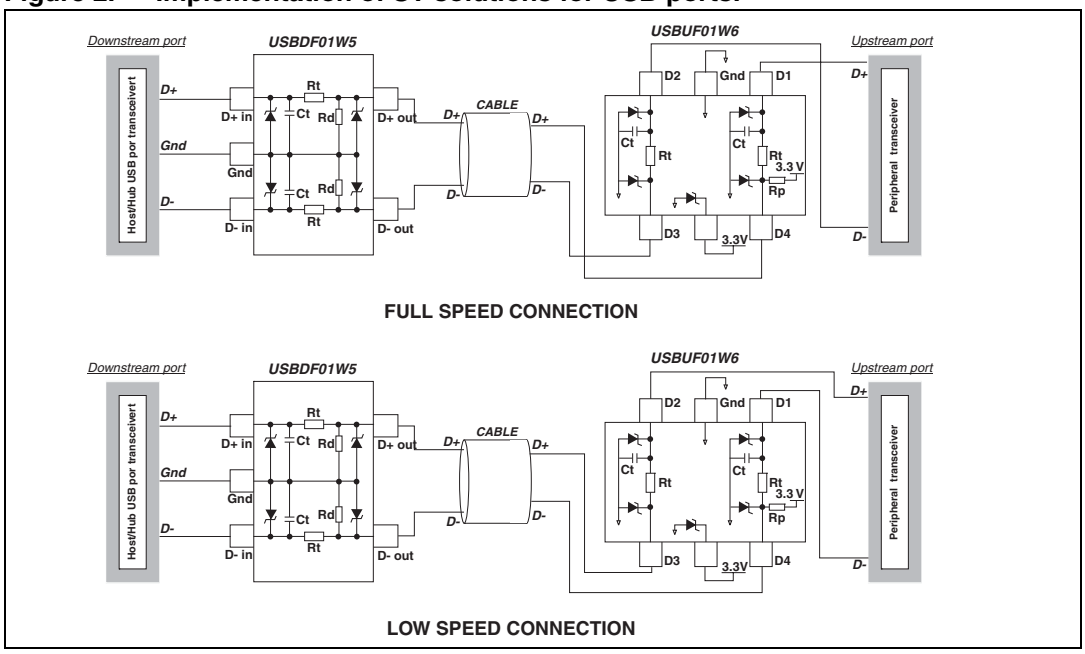
2 Technical information

Figure 1. USB Standard requirements.



2.1 Application example

Figure 2. Implementation of ST solutions for USB ports.



2.1.1 EMI filtering

Current FCC regulations requires that class B computing devices meet specified maximum levels for both radiated and conducted EMI.

- Radiated EMI covers the frequency range from 30 MHz to 1GHz.
- Conducted EMI covers the 450 kHz to 30 MHz range.

For the types of devices utilizing the USB, the most difficult test to pass is usually the radiated EMI test. For this reason the USBUF01P6 device is aiming to minimize radiated EMI.

The differential signal (D+ and D-) of the USB does not contribute significantly to radiated or conducted EMI because the magnetic field of both conductors cancels each other.

The inside of the PC environment is very noisy and designers must minimize noise coupling from the different sources. D+ and D- must not be routed near high speed lines (clocks spikes).

Induced common mode noise can be minimized by running pairs of USB signals parallel to each other and running grounded guard trace on each side of the signal pair from the USB controller to the USBUF device.

If possible, locate the USBUF device physically near the USB connectors. Distance between the USB controller and the USB connector must be minimized.

The 47 pF (C_t) capacitors are used to bypass high frequency energy to ground and for edge control, and are placed between the driver chip and the series termination resistors (R_t). Both C_t and R_t should be placed as close to the driver chip as is practicable.

The USBUF01P6 ensures a filtering protection against electro-magnetic and radio frequency Interference thanks to its low-pass filter structure. This filter is characterized by the following parameters:

- cut-off frequency
- insertion loss
- high frequency rejection.

Figure 3. USBUF01P6 typical attenuation curve.

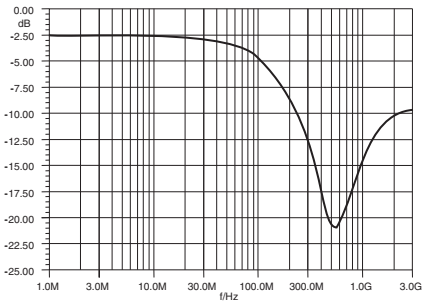
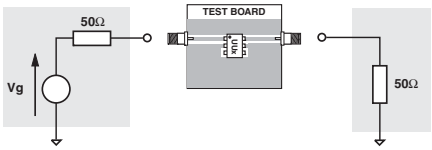


Figure 4. Measurement configuration.



2.1.2 ESD protection

In addition to the requirements of termination and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test is described in the IEC 61000-4-2 and is already in place in Europe. This test requires that a device tolerates ESD events and remains operational without user intervention.

The USBUF01P6 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at:

$$V_{CL} = V_{BR} + R_d \cdot I_{PP}$$

This protection function is splitted in 2 stages. As shown in *Figure 5.* the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R_t. Such a configuration makes the output voltage very low at the output.

Figure 5. USBUF01P6 ESD clamping behavior.

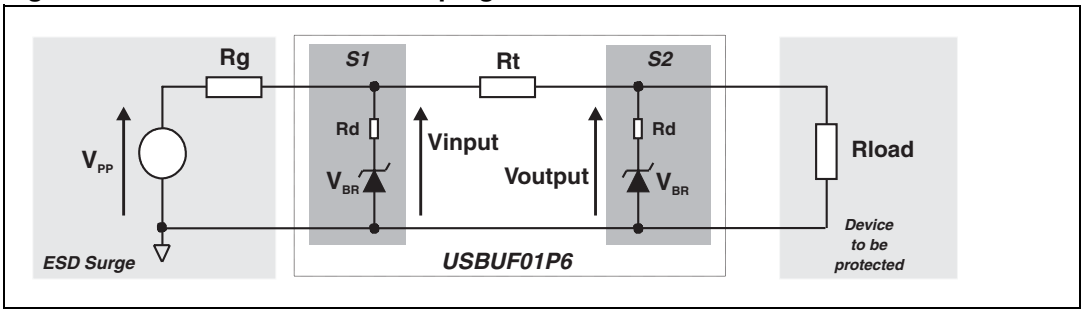
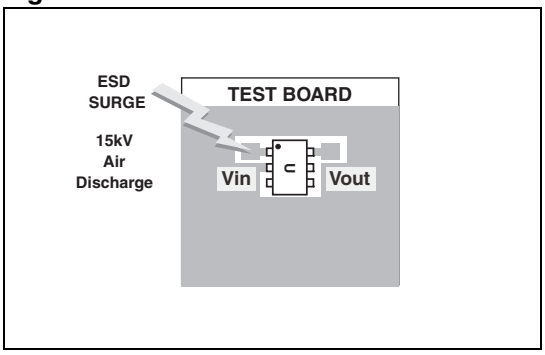


Figure 6. Measurement board.



To have a good approximation of the remaining voltages at both Vin and Vout stages, we give the typical dynamical resistance value R_d. By taking into account these following hypothesis : $R_t > R_d$, $R_g > R_d$ and $R_{load} > R_d$, it gives these formulas:

$$Vinput = \frac{R_g \cdot V_{BR} + R_d \cdot V_g}{R_g}$$

$$Voutput = \frac{R_t \cdot V_{BR} + R_d \cdot Vinput}{R_t}$$

The results of the calculation done for $V_g = 8$ kV, $R_g = 330\ \Omega$ (IEC 61000-4-2 standard), $V_{BR} = 7$ V (typ.) and $R_d = 2\ \Omega$ (typ.) give:

Vinput = 55.48 V

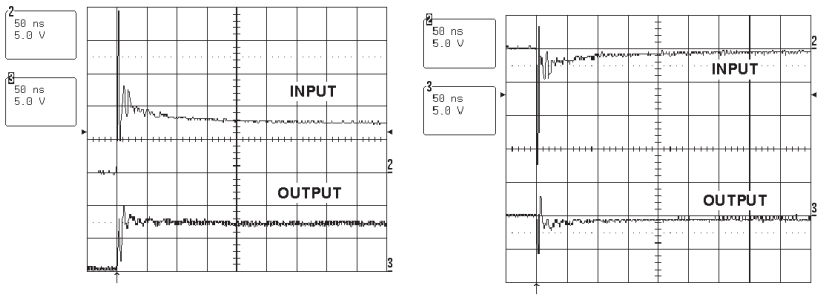
Voutput = 10.36 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the V_{input} side. This parasitic effect is not present at the V_{output} side due the low current involved after the resistance R_t.

The measurements done hereafter show very clearly (*Figure 7.a*) the high efficiency of the ESD protection:

- no influence of the parasitic inductances on Voutput stage
- V_{output} clamping voltage very close to V_{BR} (breakdown voltage) in the positive way and $-V_F$ (forward voltage) in the negative way

Figure 7. Remaining voltage at both stages S1 (V_{input}) and S2 (V_{output}) during ESD surge.



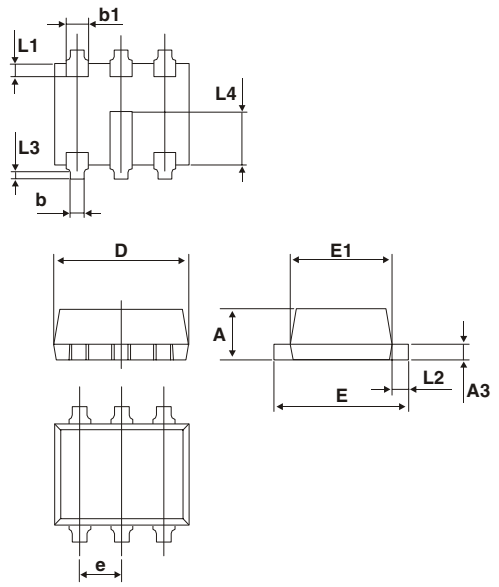
a: Positive surge

b: Negative surge

Please note that the USBUF01P6 is not only acting for positive ESD surges but also for negative ones. For these kinds of disturbances it clamps close to ground voltage as shown in *Figure 7.b.*

3 Package information

Table 3. SOT-666 internal pad dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45		0.60	0.018		0.024
A3	0.08		0.18	0.003		0.007
b	0.17		0.34	0.007		0.013
b1	0.19	0.27	0.34	0.007	0.011	0.013
D	1.50		1.70	0.059		0.067
E	1.50		1.70	0.059		0.067
E1	1.10		1.30	0.043		0.051
e		0.50			0.020	
L1		0.19			0.007	
L2	0.10		0.30	0.004		0.012
L3		0.10			0.004	
L4		0.60			0.024	

Figure 8. SOT-666 internal pad footprint (dimensions in mm)

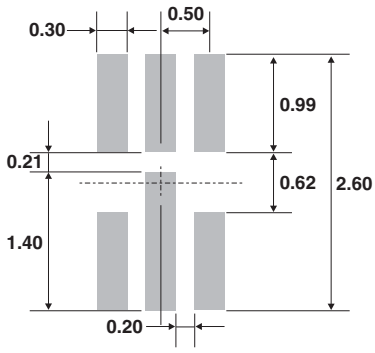


Table 4. Mechanical specifications

Lead plating	Tin-lead
Lead plating thickness	5 µm min 25 µm max
Lead material	Sn (100% Sn)
Lead coplanarity	10 µm max
Body material	Molded epoxy
Flammability	UL94V-0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
USBUF01P6	U	SOT-666IP	2.9 mg	3000	Tape and reel

5 Revision history

Date	Revision	Description of Changes
September-2003	1	First issue.
01-Jun-2004	2	SOT-666 Internal Pad version package change.
08-Jun-2005	3	Minor format changes; no content changed.
10-Mar-2006	4	Footprint and dimension graphic improved in packaging information. Ecopack statement added. Reformatted to current standard.
16-Aug-2006	5	Updated SOT-666IP package dimensions in Table 3.
29-Aug-2006	6	Typing error in table 2 on page 2: change W and kW unit to Ω and kΩ unit.

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