

VIN = 5 to 25 V, 1-channel DC-DC Step down Regulator integrated N-channel Power MOSFET for USB

FEATURES

- 1-channel DC-DC Step Down Regulator Circuit that employs Voltage Mode Switching Control System
- Current Feedback Function compensates output voltage drop due to external USB cable loss
- Internal reference voltage is within ±1.5% accuracy
- Input Voltage Range : PVCC , VCC: 5 V ~ 25 V
- Adjustable Switching Frequency with external Resistor : 200 kHz ~ 1 MHz
- Standby mode consumes less than 1 μA current
- Output over voltage protection function
- Output ground short protection function
- Over current protection with adjustable threshold.
- Under voltage lockout function (VREG)
- Thermal Shut Down function
- Adjustable soft-start function
- SSOP024-P-0300F
(Size : 7.8 mm X 8.1 mm, 0.65 mm pitch),
24pin Plastic Shrink Small Outline Package (SSOP Type)

DESCRIPTION

AN33014UA is 1-channel DC-DC Step down Regulator integrated N-channel Power MOSFET and employs the voltage mode switching control system.

This IC can be operated with wide input voltage range and is build in several protection functions, so this IC can provide high reliability power supply system.

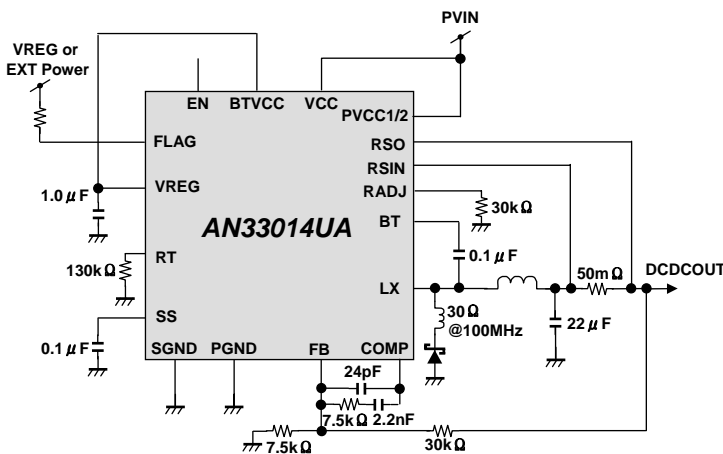
For USB applications, this IC can controlled USB supplied voltage level with external resistor for USB load current monitor (Current Feedback Function), and it can provide suitable power supply system for external USB with no voltage drop due to USB cable loss.

Maximum current is 1.5 A.

APPLICATIONS

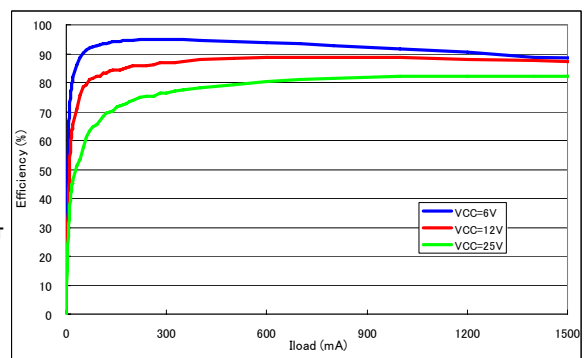
- High Input Voltage Power Systems for USB such as
- Car-Audio system
 - Car-Navigation system
 - OA Equipment
 - Home Appliances etc.

SIMPLIFIED APPLICATION



Notes) This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

EFFICIENCY CURVE



Condition)
 Vin = 6 , 12 , 25 V, Vout = 5 V,
 Lo = 10 μH, Co = 22 μF, Frequency = 490 kHz
 RSENSE=50mΩ

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	Vcc	40	V	*1
Operating free-air temperature	T _{opr}	- 40 to + 85	°C	*2
Operating junction temperature	T _j	- 40 to + 150	°C	*2
Storage temperature	T _{stg}	- 55 to + 150	°C	*2
Input Voltage Range	BT	-0.3 to (Vcc+VREG)	V	*1 *3
Input Voltage Range	RSIN,RSO	-0.3 to 10	V	*1
Input Voltage Range	EN	-0.3 to (Vcc+0.3)	V	*1 *4
Input Voltage Range	FB,BTVCC,SYNC	-0.3 to 5.5	V	*1
Output Voltage Range	FLAG	-0.3 to 5.5	V	*1
	LX	- 0.3 to (Vcc + 0.3)	V	*1 *4
ESD	HBM (Human Body Model)	2	kV	—
	MM (Machine Model)	200	V	—

Notes) Do not apply external currents and voltages to any pin not specifically mentioned.

This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating.

This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

Vcc is voltage for VCC, PVCC1 and PVCC2. VCC = PVCC1 = PVCC2.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C.

*3:(Vcc + VREG) V must not be exceeded 40 V

*4:(Vcc + 0.3) V must not be exceeded 40 V

POWER DISSIPATION RATING

PACKAGE	θ _{JA}	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Notes
24 Pin Plastic Shrink Small Outline Package (SSOP Type)	135.1 °C / W	0.925 W	0.481 W	*1

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1:Glass Epoxy Substrate(4 Layers) [Glass-Epoxy: 50 X 50 X 0.8(mm)]



CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	VCC	5	12	25	V	*1
	PVCC1					
	PVCC2					
Input Voltage Range	BT	-0.3	—	V _{cc} + VREG	V	*1 *2
Input Voltage Range	RSIN	-0.3	—	10	V	*1
	RSO					
Input Voltage Range	EN	-0.3	—	V _{cc} + 0.3	V	*1 *3
Output Voltage Range	LX	-0.3	—	V _{cc} + 0.3	V	*1 *3
Input Voltage Range	FB	-0.3	—	5.5	V	*1
	BTVCC					
	SYNC					
Output Voltage Range	FLAG	-0.3	—	5.5	V	*1

Note) Do not apply external currents and voltages to any pin not specifically mentioned.

Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for SGND, PGND. SGND = PGND

V_{cc} is voltage for VCC, PVCC1 and PVCC2. VCC = PVCC1 = PVCC2.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : (V_{cc} + VREG) V must not be exceeded 40 V

*3 : (V_{cc} + 0.3) V must not be exceeded 40 V

ELECTRICAL CHARACTERISTICS

Co = 22 μF, Lo = 10 μH, VOUT Setting = 5.0 V, VCC = 12 V, RT = 130 kΩ, RADJ = 30 kΩ, Rsense = 50 mΩ,
RS2 : MPZ1608S300A, Ta = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Quiescent current	I _{CQ}	No switching FB = 1.1 V EN = High (3.3 V)	—	1.0	1.4	mA	—
Standby current	I _{STBY}	EN = Low	—	0.01	1	μA	—
BGR							
Feedback voltage	V _{REF}	FB connected to COMP with gain of 1.5 times	0.985	1.0	1.015	V	—
Enable (EN)							
Low input threshold	V _{IL1}	—	—	—	0.4	V	—
High input threshold	V _{IH1}	—	2.0	—	—	V	—
EN terminal input current	V _{IC1}	EN = 3.3 V	—	33	70	μA	—
SYNCHRONIZATION (SYNC)							
Low input threshold	V _{IL2}	—	—	—	0.4	V	—
High input threshold	V _{IH2}	—	2.0	—	—	V	—
Oscillator							
Oscillator frequency	F _{OUT1}	RT = 130 kΩ	440	490	540	kHz	—
Oscillator frequency range	F _{OUT2}		200	—	1000	kHz	—
External sync frequency range	F _{SYNC}	RT = 130 kΩ Fout1 = 490 kHz	545	—	730	kHz	—
Over-current protection							
Over-current threshold voltage	V _{OCP}	(VCC_S-VRS)	72	90	108	mV	*1
Over-voltage protection							
Over-voltage threshold voltage for VFB	V _{OVP1}	For FB	1.14	1.22	1.30	V	—
Over-voltage threshold voltage for VCC	V _{OVP2}	For VCC	30	34	38	V	—
Internal regulator							
Internal regulator output voltage	V _{REG}	C _{REG} = 1 μF	4.5	5.0	5.3	V	—
GND short protection							
Short detection voltage	V _{SCP}	monitor FB	0.15	0.3	0.45	V	—

Note) *1 : This parameter is tested with DC measurement.

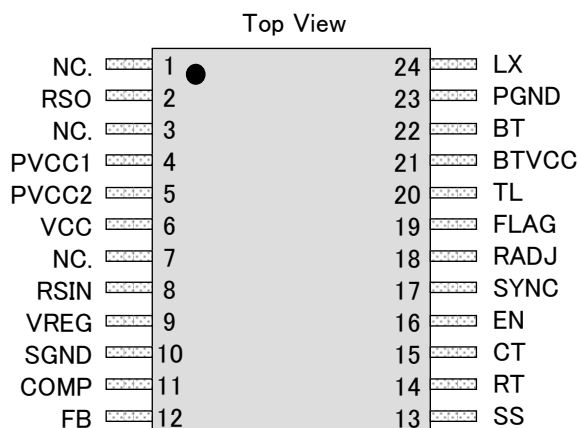
ELECTRICAL CHARACTERISTICS (Continued)

Co = 22 μF, Lo = 10 μH, VOUT Setting = 5.0 V, VCC = 12 V, RT = 130 kΩ, RADJ = 30 kΩ, Rsense = 50 mΩ,
 Ta = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Feedback							
Current feedback output voltage 1	V _{CFB1}	Monitor RADJ FB = 1.1V EN = 3.3 V At RSIN-RSO = 32.5 mV No switching	65	130	195	mV	*1
Current feedback output voltage 2	V _{CFB2}	Monitor RADJ FB = 1.1V EN = 3.3 V At RSIN-RSO = 65 mV No switching	190	260	330	mV	*1
Current feedback factor	V _{CFBF}	Calculation item (V _{CFB2} - V _{CFB1}) / {4 x (65 mV - 32.5 mV)}	0.96	1	1.04	—	—
Under voltage Lock out							
Under Voltage Lock Out threshold voltage	V _{UVLO}	Monitor VCC FB = 1.1V EN = 3.3 V No switching	3.5	3.9	4.3	V	—

Note) *1 : This parameter is tested with DC measurement.

PIN CONFIGURATION

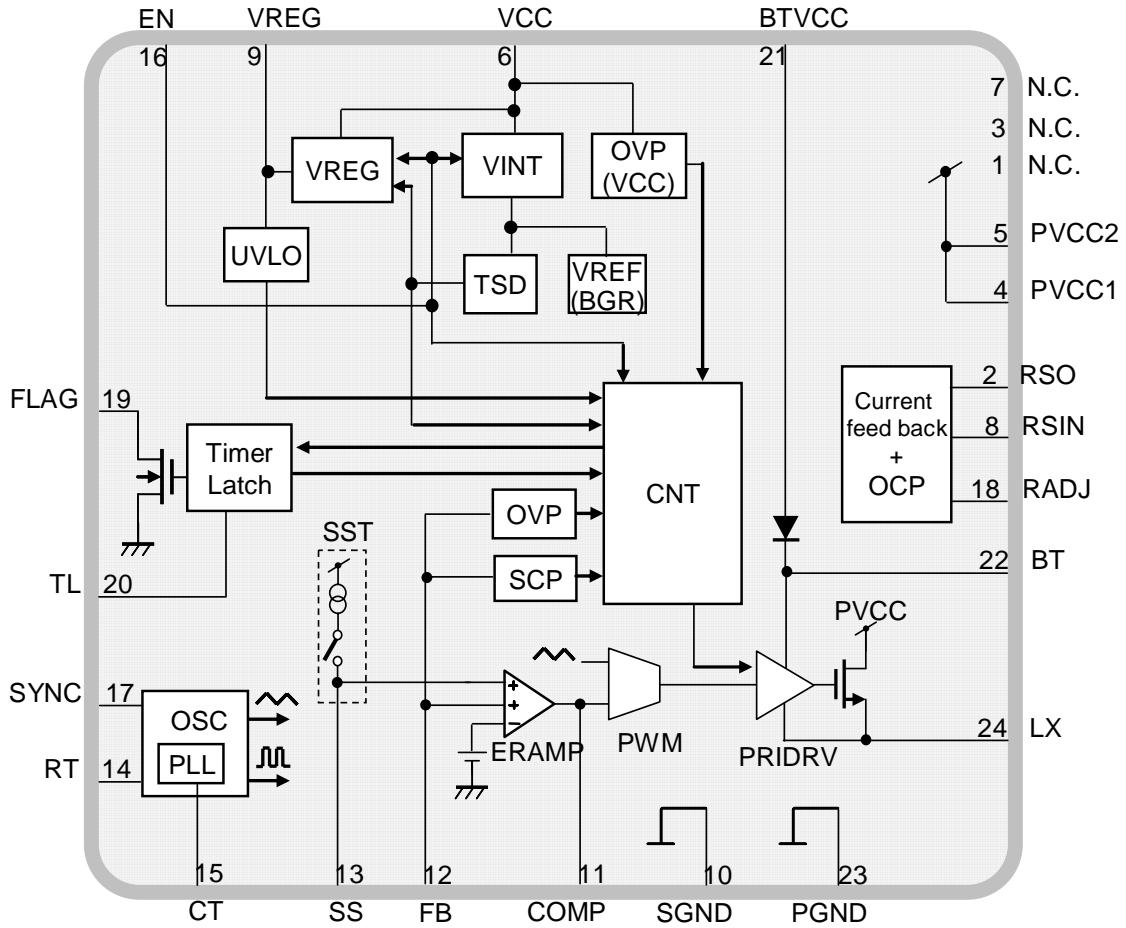


PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	N.C.	—	No connection
2	RSO	Input	Connection to current sensing port
3	N.C.	—	No connection
4	PVCC1	Power Supply	Power supply pin for internal driver
5	PVCC2	Power Supply	Power supply pin for internal driver
6	VCC	Power Supply	Power supply pin
7	N.C.	—	No connection
8	RSIN	Input	Connection to current sensing port
9	VREG	Output	Connect to an external capacitor for internal regulator
10	SGND	Ground	Ground pin
11	COMP	Output	Error amplifier output
12	FB	Input	Error amplifier negative input
13	SS	Output	Soft-start capacitor connection pin
14	RT	Output	Connect to an external resistor for adjustment of oscillation frequency
15	CT	Output	Low Pass filter function pin for PLL
16	EN	Input	Enable pin
17	SYNC	Input	External clock input for adjustment of oscillation frequency
18	RADJ	Output	Connect to an external resistor for adjustment of current feedback
19	FLAG	Output	Error flag output pin
20	TL	Output	Connect to an external capacitor for adjustment of over-current detection time
21	BTVCC	Input	Boot strap input pin
22	BT	Input	Connect to an external capacitor for Boot strap
23	PGND	Ground	Power ground pin
24	LX	Output	Connect to an external inductor and schottky diode

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Notes) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

1. Power ON/OFF sequence

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

AN33014UA consists of one channel and it can be turned ON and OFF by using the EN pin.

EN > 2.0 V : Enabled
EN < 0.4 V : Disabled

1) Power ON Sequence :

- VCC rises to a desired voltage level.
(A 10 ms rise time or more is recommended to control and limit any abnormal current flow via the power transistor when VCC is rising.)
- Apply a voltage level of 2.0 V or higher at EN pin after VCC is steady, and the DCDC will begin to operate.
(It is possible to connect the EN pin to VCC through a resistor, and, in that case, when VCC rises, DCDC will begin to operate.)
- When VREG voltage reaches 4.9 V and above, and after a delay time (charging time of the soft start capacitor) decided by an external capacitor, the DCDC will start to operate.

2) Power OFF Sequence :

- To turn OFF the DCDC output, apply a voltage of 0.4 V or lower to EN pin.
- VOUT will drop after EN pin becomes Low.
(The discharge time is dependent on the applied load current and the feedback resistance connected at the output.)
- The DCDC will turn OFF if the VCC level becomes low even before EN pin becomes low.
The above scenario occurs when the VREG voltage decreases to 4.2 V or less.
(However, the DCDC output voltage will also decrease with VCC when the VCC level drops below a certain minimum level required to maintain the output voltage level.)

3) Points to take note of when re-starting the DCDC :

- Please allow a waiting time of 10 ms or more for the discharge time of the soft start capacitor when starting up the DCDC again after turning it OFF.
The output voltage might overshoot without the soft start function working properly if the DCDC is re-started immediately after it is turned OFF.

4) Points to take note of when shut down :

- Please turn OFF the DCDC by applying a Low voltage of EN pin.

5) Points to take note of pin connection :

- VREG is utilized for internal circuits. do not use it as power supply for other device.
- Please take note on the placement of external parts of RT pin and CT pin as these are sensitive pin that are susceptible to noise effect such as LX pin.

OPERATION (Continued)

2. Start / Stop Control Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

- ON/OFF operation sequence by EN pin control.

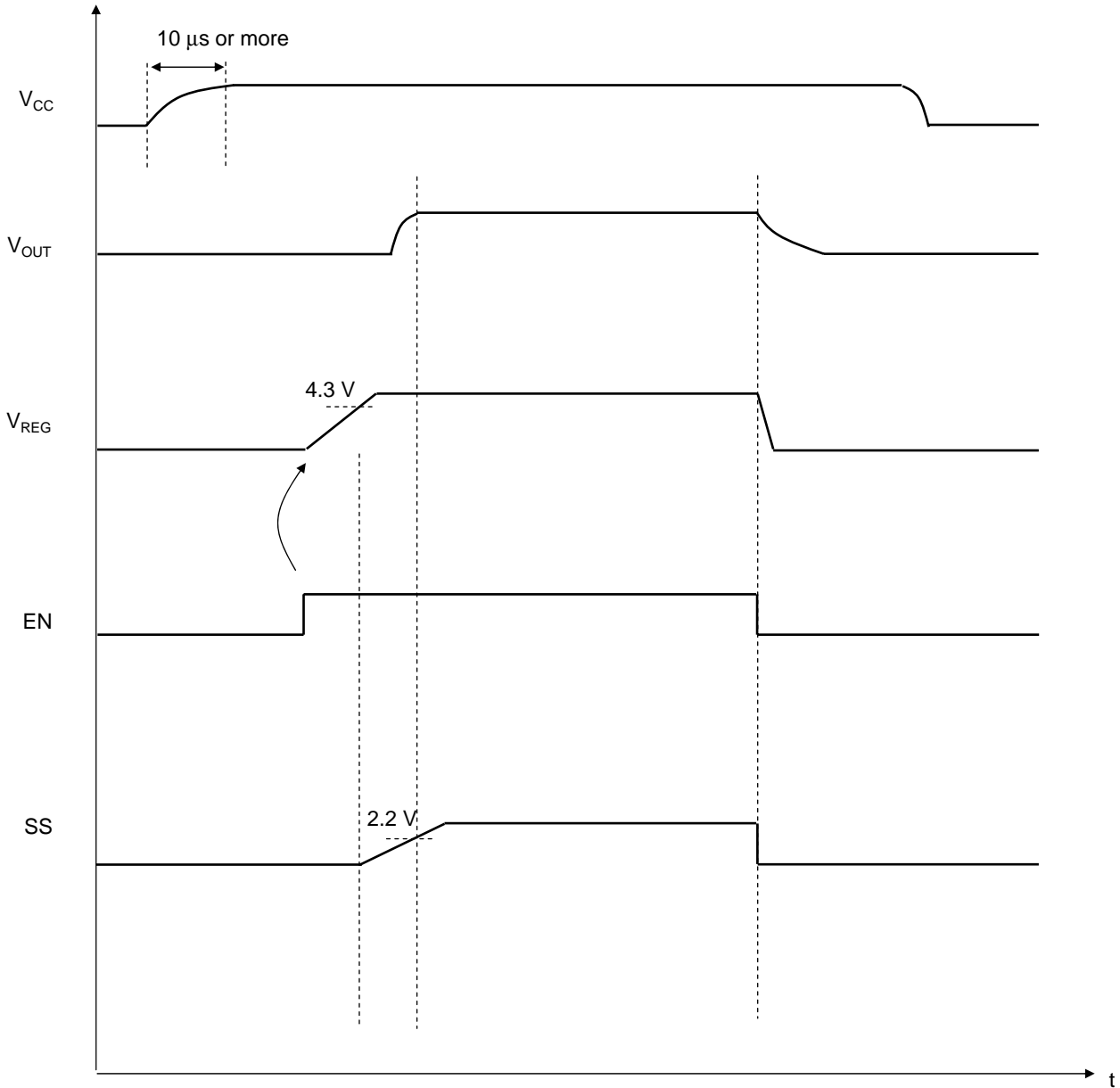


Figure : Power ON/OFF sequence by EN

Note) All values given in the above figure are typical values.

OPERATION (Continued)

2. Start / Stop Control Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

- ON/OFF operation sequence by VCC pin control (EN pin is connected to VCC).

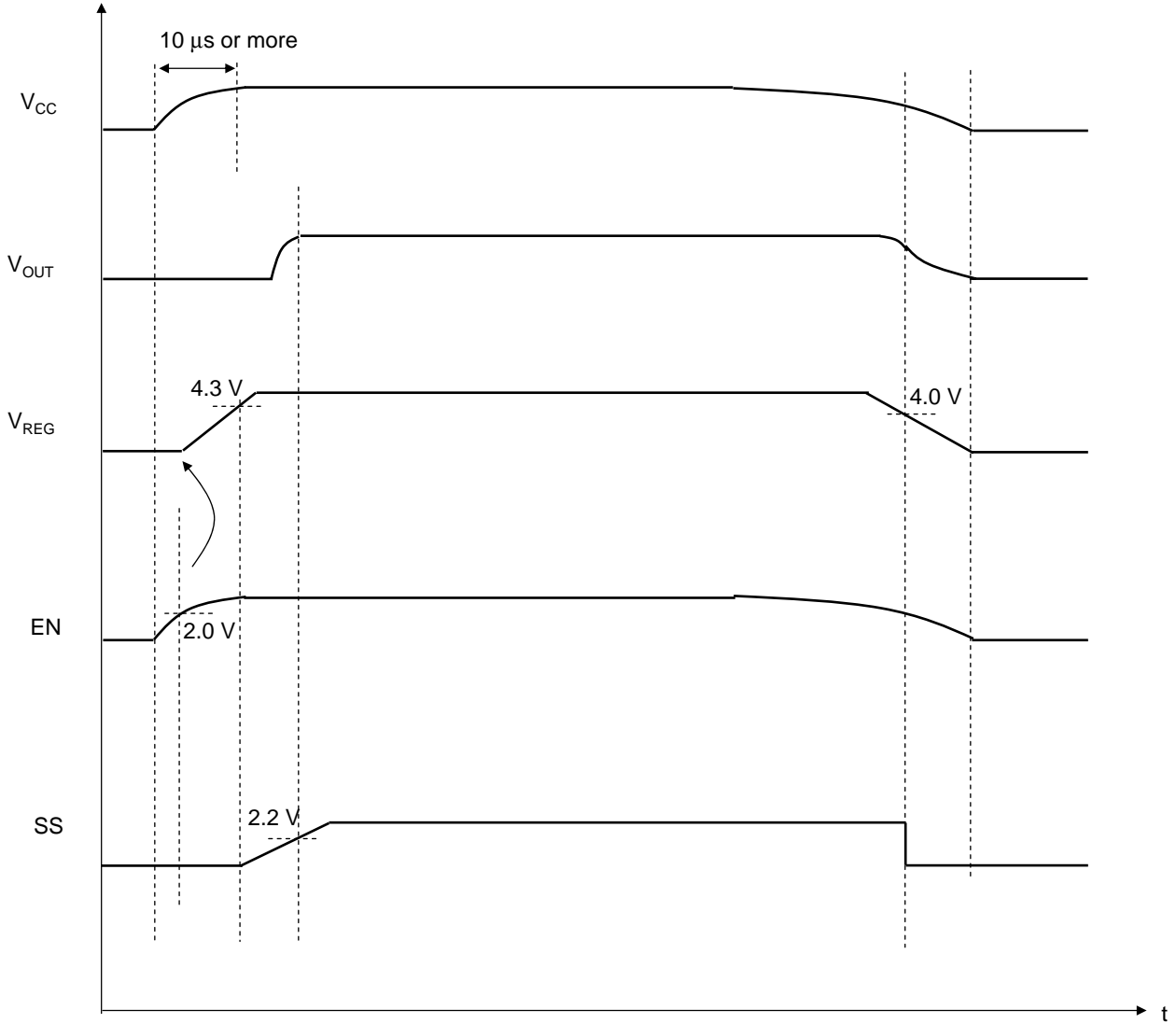


Figure : Power ON/OFF sequence by VCC/EN

Note) All values given in the above figure are typical values.

OPERATION (Continued)**3. Output voltage setting**

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

The output voltage of AN33014UA is set with the external feedback resistance divider arranged between the terminal FB and GND between the DCDC output and the terminal FB. The output voltage is decided depending on the following equation.

$$V_{out} = 1.0 \times \left[1 + \frac{R_a}{R_b} \right]$$

4. Min/Max Duty Operation

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

MinDuty is decided by the minimum ON time. The minimum ON time, $T_{on}(\min)$, is the time that this IC can turn on the high side switch. This is decided by the gate capacitance of the high side switch and the internal timing delay. The following attention is necessary because in applications where the Input/Output voltage difference is great, and the switching frequency is high, there is a possibility to reach the limiting value of the minimum ON time. The minimum ON time, $T_{on}(\min)$, is about 200ns (max).

This IC has the function of MaxDuty, which will not exceed a certain definite value for safety reasons in case of abnormal circumstances. The following attention is necessary because in applications where the Input/Output voltage difference is close, and the switching frequency is high, there is a possibility to reach the limiting value of the minimum OFF time. The minimum OFF time, $T_{off}(\min)$, is about 200ns (max).

$$T_{on}(\min) < \frac{V_{out}}{V_{in}} \times \frac{1}{F}$$

$$T_{off}(\min) < \left(1 - \frac{V_{out}}{V_{in}} \right) \times \frac{1}{F}$$

*) F : Switching frequency

When operating near the Min/Max limited duty, the ripple voltage and the inductor current ripple increases even if the output voltage is stabilized. It is recommended to use on the condition when the turn on switching time and turn off switching time are 200ns or more.

*) Please take note of the output voltage setting when the switching frequency is high.

OPERATION (Continued)

5. Oscillation Frequency

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

The switching frequency of the built-in oscillator circuit can be set from 200 kHz to 1000 kHz, determined by the resistance of the terminal RT, set by external resistance. The setting accuracy of the frequency is approximately ±10%. The equation and the corresponding table are described as follows.

RT [KΩ]	OSC Frequency (KHz)	RT [KΩ]	OSC Frequency (KHz)
56	1015	150	430
62	934	160	406
68	864	180	364
75	796	200	330
82	738	220	302
91	674	240	278
100	620	270	249
110	569	300	225
120	527	330	206
130	490	360	190
150	430		

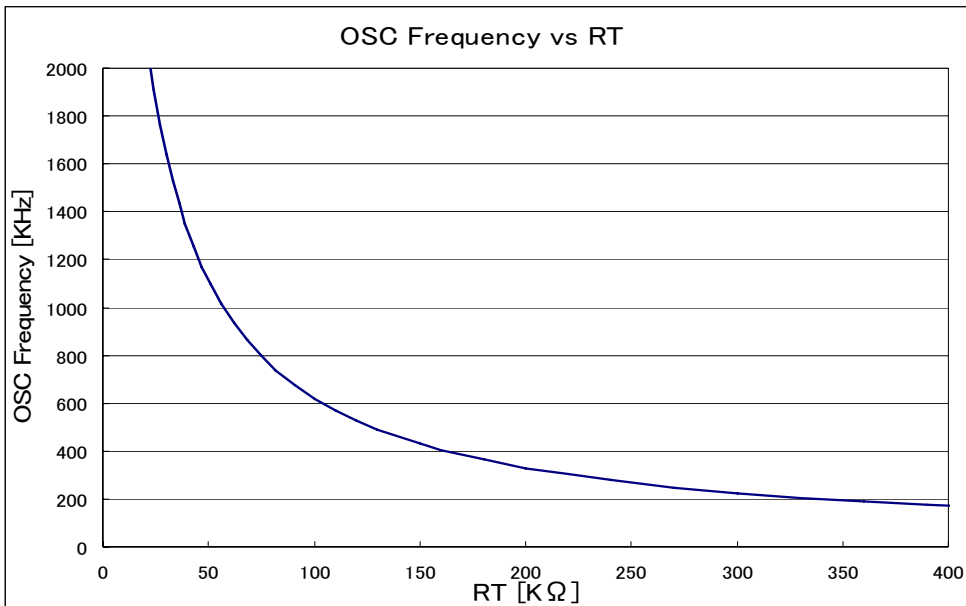


Figure : switching frequency vs external resistance

OPERATION (Continued)

6. Over-Current Protection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

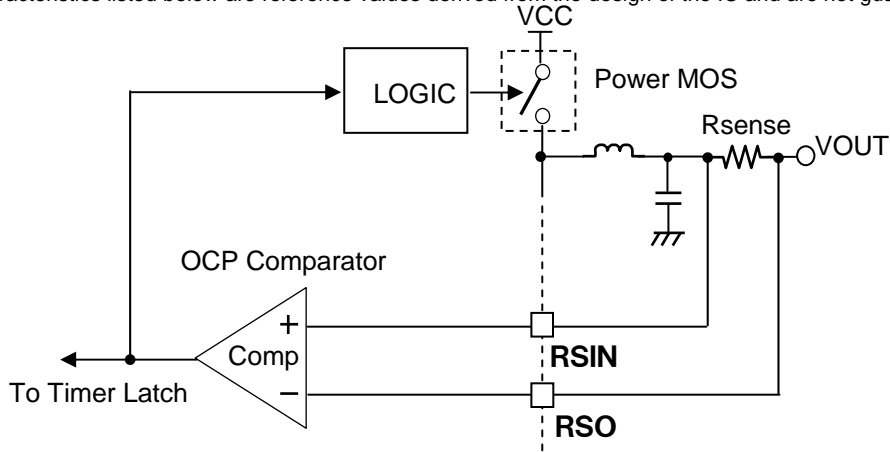


Figure : Over-Current Protection circuit block diagram

Over-current protection function (OCP) restrain output current level when IC detect that DCDC output current is higher than setting level. It turns off the Power MOS in IC when the voltage difference of external resistance Rsense exceeds 90mV(Typ.) so as to stop the supply to DCDC output. Detection current Isense can be calculated as:

$$I_{sense} = 90mV / R_{sense}$$

For safety reason, OCP function is necessary. Please placed sense resistor ($\geq 39m\Omega$) between RSIN and RSO as indicated in above figure.

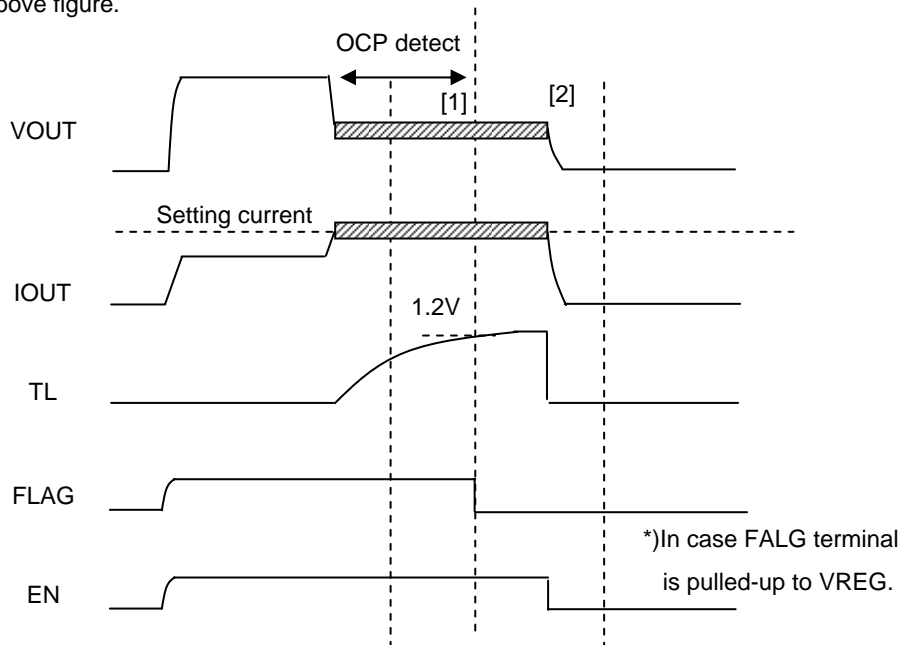


Figure : Method of detection of Over-Current Protection function

[1].DCDC continue to ON and OFF when OCP detect. It restrain average level of DCDC output voltage and DCDC output current.

[2].FLAG output become low when you keep abnormal condition longer than setting time of Timer Latch function.

For safety reason, please disable DCDC by EN control when FLAG output become low.

OPERATION (Continued)

7. Current Feedback function

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

The following expression shows the relation between Current Feedback Adjustment Resistance RRADJ and Sense Resistance RSENSE and Impedance Rcable (ex. External connection cables).

$$R_{RADJ} = Ra \frac{4 \times RSENSE}{Rcable} [\Omega]$$

The following expression shows the relation between Voltage V_USB and RRADJ.

$$V_{USB} = \left\{ 1 + Ra \times \left(\frac{1}{Rb} + \frac{4 \times RSENSE \times IOUT}{R_{RADJ}} \right) \right\} \times 1.0 - Rcable \times IOUT [V]$$

With respect to above equations,

- 1) IOUT is current flowing through RSENSE.
- 2) 1.0 [V] is the internal reference voltage (VREF) of IC.

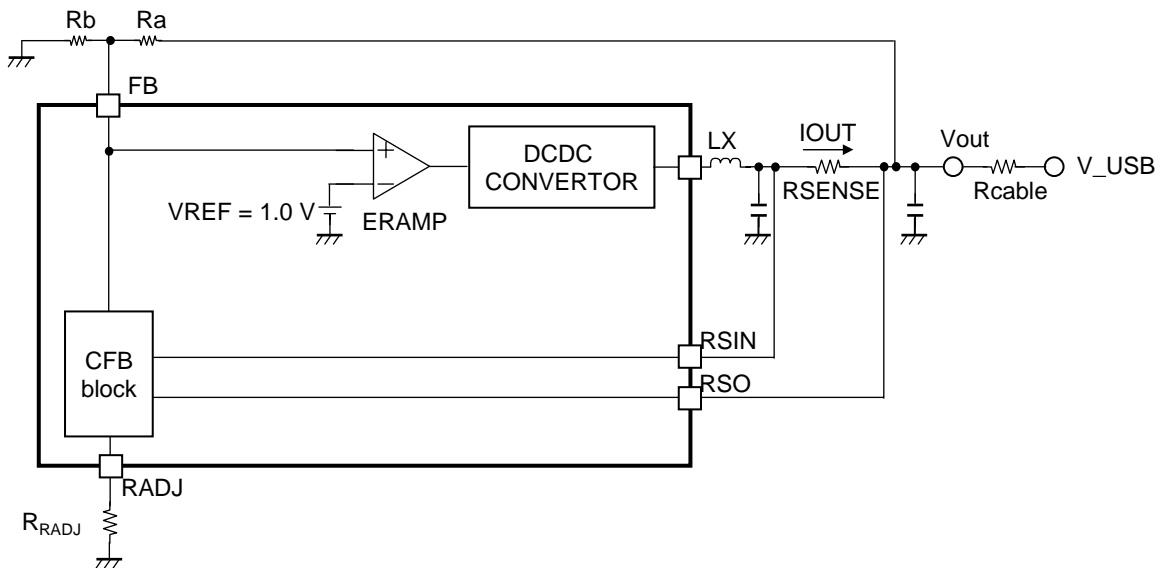


Figure : The diagram of current feed back function

※ This function is suitable at below conditions: output voltage range from 3 V to 7 V, Rcable resistance is equal or less than 1.0 Ω .

The voltage of RSIN pin and RSO pin might be higher than its absolute voltage when Rcable is over than 1.0 Ω . In case there is a change of Rcable's impedance to more than 1.0 Ω by external factor such as a heat, drop in V_USB voltage is to be expected. Referring to formula V_USB* above, when Rcable increased and Radj remain constant, V_USB will drop.

As a safety measure, a sensing resistor must be inserted between RSIN pin & RSO pin to enable the over-current protection function. Sensing resistor value of more than 39 mΩ is recommended.

OPERATION (Continued)

7. Current Feedback function (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

The following expression shows the relation between IO_{UT} and voltage drop ΔV of Impedance R_{cable} (ex. External connection cables).

$$\Delta V = R_{cable} \times IO_{UT}$$

The following expression shows the relation between above formula and Voltage V_{_USB} and R_{RADJ}.

$$\Delta V = 1 + R_a \times \left(\frac{1}{R_b} + \frac{4 \times R_{SENSE} \times IO_{UT}}{R_{RADJ}} \right) \times 1.0V - V_{_USB} [V]$$

At this point,

$$V_{out} = 1 + R_a \times \left(\frac{1}{R_b} + \frac{4 \times R_{SENSE} \times IO_{UT}}{R_{RADJ}} \right) \times 1.0V [V]$$

The following graph shows the expression of ΔV = V_{out} - V_{_USB} against IO_{UT}.
The condition is R_a = 31.2 kΩ, R_b = 7.5 kΩ, R_{SENSE} = 56 mΩ.

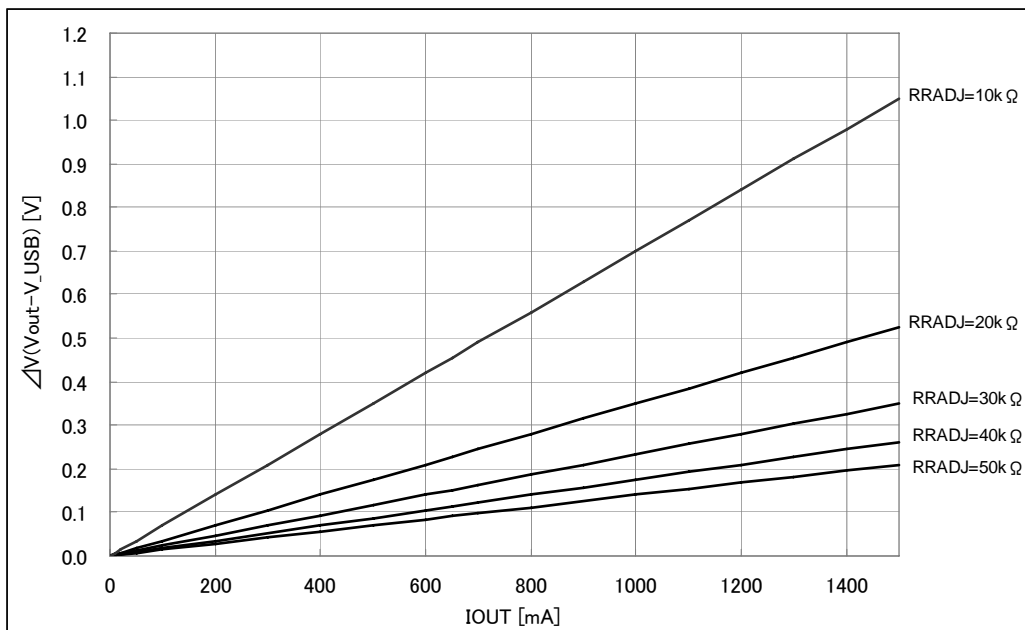


Figure : Δ= V_{out} - V_{_USB} vs IO_{UT}

OPERATION (Continued)**8. Over current protection setting**

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

As a safety measure, a sensing resistor must be inserted between RSIN pin & RSO pin to enable the over-current protection function. Sensing resistor value of more than 39 m Ω is recommended.

If sensing resistor is set at less than 39 m Ω , the capacitor at TL pin should be as small as possible or open to minimize reaction time of Timer Latch block. Please consider the implementation of full evaluation and verification for this setting. Take notice the power dissipation of Sensing resistor.

9. FLAG function after Over current / Short current detection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Stop this product by forcing EN pin to Low when detect OCP or SCP condition by FLAG pin.
In situation when RSIN RSO are less than 1.1V, do note that only SCP detection is active.

When FB is equal or lower than 0.3 V, short current detection is triggered, FLAG pin will be pull to Low state. The response timing is determined by TL pin capacitor value.

Note that the pull down current drivability of FLAG pin is 1.2 mA.

Adjusting of FLAG response time in event of "over current" or "short current" condition is make possible by changing the capacitance of TL pin.

In the event of over current detection, FLAG pin will be pull to Low state. Once FLAG is pull to Low state, it will remained at Low state until IC is reset through EN pin.

APPLICATIONS INFORMATION

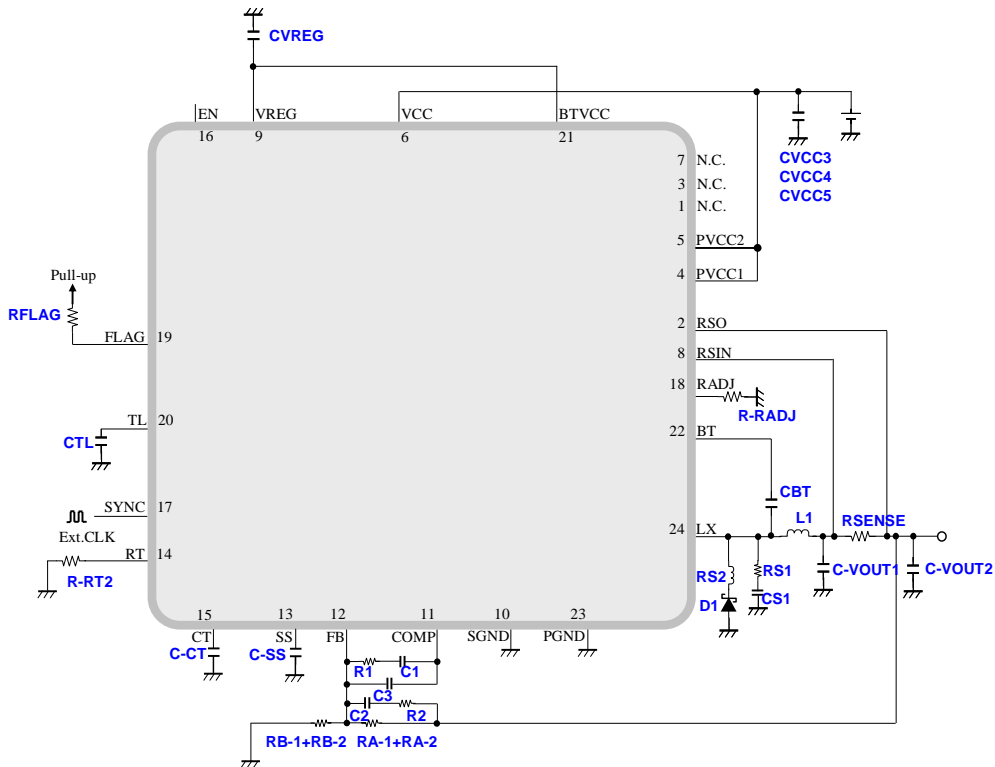


Figure : Application circuit

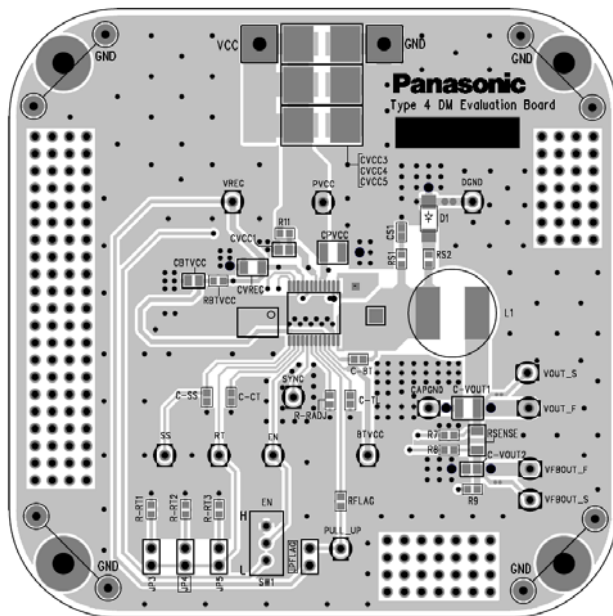


Figure : Top Layer with silk screen
(Top View) with Evaluation board

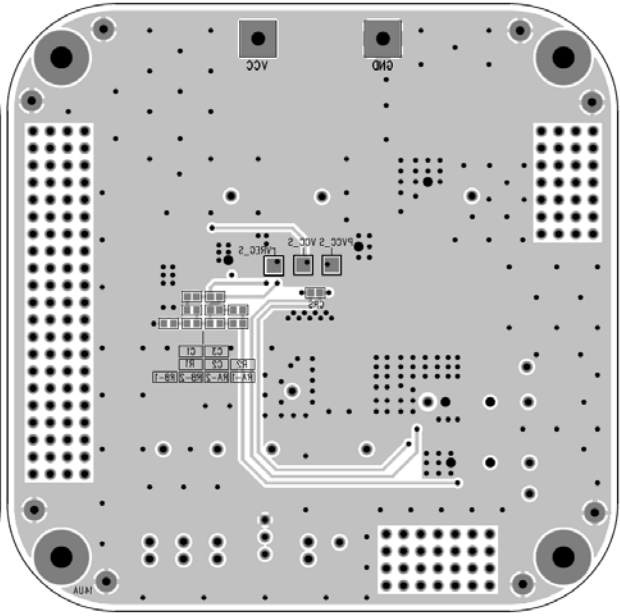


Figure : Bottom Layer with silk screen
(Bottom View) with Evaluation board

Notes) This application circuit and layout is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

APPLICATIONS INFORMATION (Continued)

Reference	Part Name	Value	Maker	Description
C-BT,C-CT, C-SS,C-TL	GCM188R11C104KA01J	0.1 μ F	Murata	Setting Capacitor
C1	GCM1882C1H222JA01J	2.2nF	Murata	Compensation Capacitor
C2	GCM1882C1H471JA01J	470pF	Murata	Compensation Capacitor
C3	GCM1882C1H240JA01J	24pF	Murata	Compensation Capacitor
CVREG	GCM188R71C105KA49J	1 μ F	Murata	VREG Capacitor
CVCC3,CVCC4, CVCC5	CKG57NX7R1H226MT	22 μ F	TDK	Input Capacitor
C-VOUT1	TMK325C7226MM-T	22 μ F	TAIYO,YUDEN	Output Capacitor
C-VOUT2	GCM188R11C104KA01J	0.1 μ F	Murata	Output Capacitor
L1	CDRH8D43-100NC	10 μ H	SUMIDA	Inductor
D1	DB24416	-	Panasonic	Schottky Diode
R1	ERA3AEB752V	R=7.5K	Panasonic	Compensation & Feedback Resistor
R2	ERA3AEB152V	R=1.5K	Panasonic	Compensation & Feedback Resistor
RA-1	ERA3AEB303V	R=30K	Panasonic	Compensation & Feedback Resistor
RB-1	ERA3AEB752V	R=7.5K	Panasonic	Compensation & Feedback Resistor
R-RADJ	ERA3AEB303V	R=30K	Panasonic	Current Feedback Adjustment Resistor
RFLAG	ERA3AEB204V	R=200K	Panasonic	Pull-up Resistor
R-RT2	ERA3AEB134V	R=130K	Panasonic	OSC Setting Resistor (Fsw=490kHz)
RSENSE	ERJ6BWFR050V	R=50m	Panasonic	Output Current Sense Resistor
RA-2,RB-2,R7, R8,R9,RBTVCC	ERJ3GEY0R00V	R=0	Panasonic	-
CS1	GCM1882C1H332JA01J	3300pF	Murata	Snubber Circuit
RS1	ERA3AEB221V	R=220	Panasonic	Snubber Circuit
RS2	MPZ1608S300A	-	TDK	Ferrite Beads

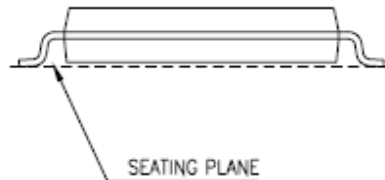
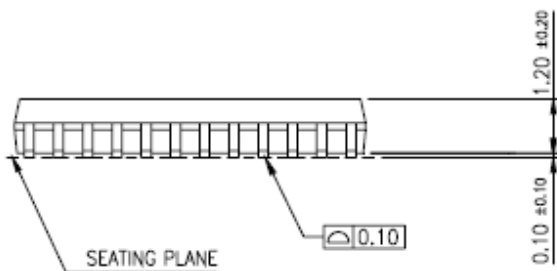
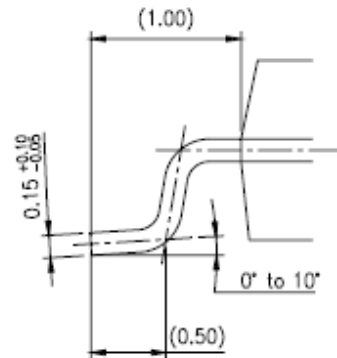
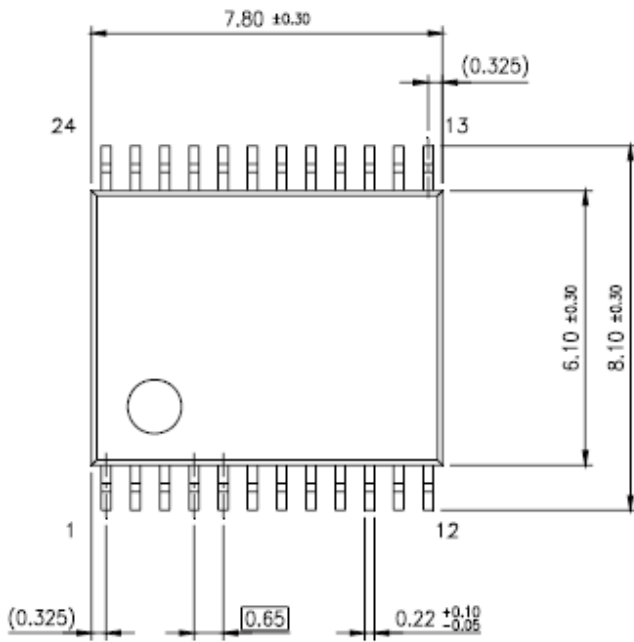
Figure : Recommended component

PACKAGE INFORMATION (Reference Data)

Outline Drawing

Package Code : SSOP024-P-0300F

Unit : mm



Body Material : Br/Sb Free Epoxy resin
Lead Material : Cu Alloy
Lead Finish Method : SnBi Plating

PACKAGE INFORMATION (Reference Data)

Power dissipation (Supplementary explanation)

[Experiment environment]

Power Dissipation (Technical Report) is a result in the experiment environment of SEMI standard conformity. (Ambient air temperature (Ta) is 25 degrees C)

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report) are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation (Thermal Resistance)]

Power Dissipation values (Thermal Resistance) depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value (Technical Report) is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta : Ambient air temperature

※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc : It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj : Semiconductor element surface temperature (Junction temperature.)

Rth(j-c) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a) : The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

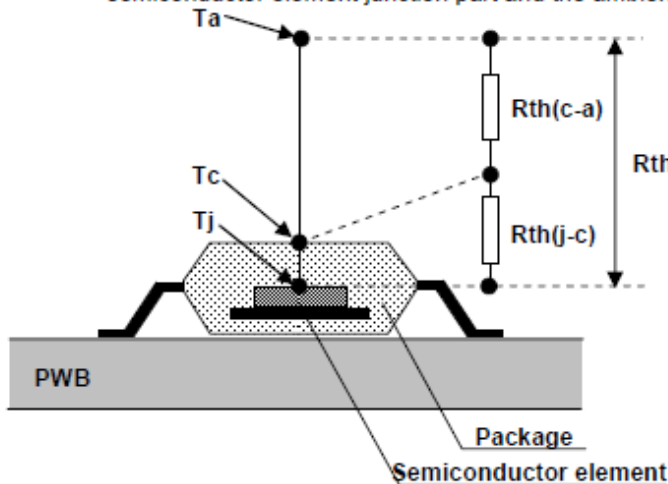


Fig1. Definition image

[Definition formula]

$$Tj = \{Rth(j-c) + Rth(c-a)\} \times P + Ta$$

$$= Rth(j-a) \times P + Ta$$

$$Rth(j-c) = \frac{Tj - Tc}{P} \quad (^\circ C/W)$$

$$Rth(c-a) = \frac{Tc - Ta}{P} \quad (^\circ C/W)$$

$$Rth(j-a) = \frac{Tj - Ta}{P} \quad (^\circ C/W)$$

$$= Rth(j-c) + Rth(c-a)$$

P:power(W)

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3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO
10. Verify the risks which might be caused by the malfunctions of external components.
11. Connect the metallic plates on the back side of the LSI with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates are connected with their respective potentials.

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