

# 15V, 2.5A Synchronous Step-Up DC/DC Converter with Output Disconnect

## FEATURES

- **V<sub>IN</sub> Range:** 1.8V to 5.5V, 500mV After Start-Up
- **Output Voltage Range:** 2.2V to 15V
- **800mA Output Current** for V<sub>IN</sub> = 5V and V<sub>OUT</sub> = 12V
- **Output Disconnects from Input When Shut Down**
- **Synchronous Rectification:** Up to 95% Efficiency
- **Inrush Current Limit**
- Up to 3MHz Adjustable Switching Frequency Synchronizable to External Clock
- Selectable Burst Mode® Operation: 25μA I<sub>Q</sub>
- Output Overvoltage Protection
- Soft-Start
- <1μA I<sub>Q</sub> in Shutdown
- 12-Lead, 3mm × 4mm × 0.75mm Thermally Enhanced DFN and MSOP Packages

## APPLICATIONS

- RF Power
- Piezo Actuators
- Small DC Motors
- 12V Analog Rail From Battery, 5V, or Backup Capacitor

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## DESCRIPTION

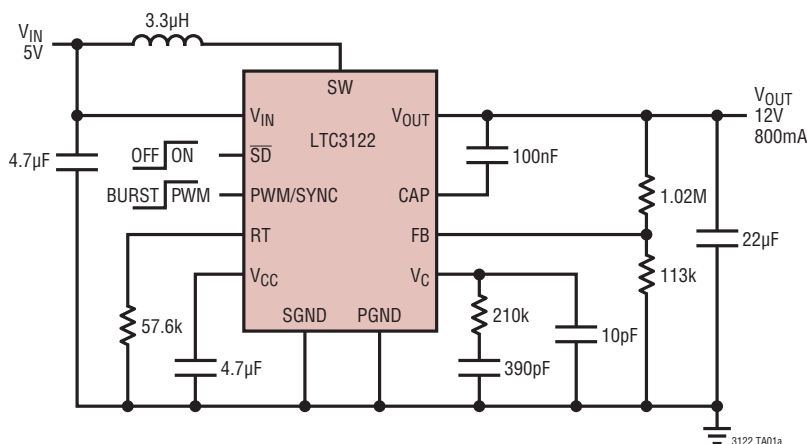
The LTC<sup>®</sup>3122 is a synchronous step-up DC/DC converter with true output disconnect and inrush current limiting. The 2.5A current limit along with the ability to program output voltages up to 15V makes the LTC3122 well suited for a variety of demanding applications. Once started, operation will continue with inputs down to 500mV, extending runtime in many applications.

The LTC3122 features output disconnect in shutdown, dramatically reducing input power drain and enabling V<sub>OUT</sub> to completely discharge. Adjustable PWM switching from 100kHz to 3MHz optimizes applications for highest efficiency or smallest solution footprint. The oscillator can also be synchronized to an external clock for noise sensitive applications. Selectable Burst Mode operation reduces quiescent current to 25μA, ensuring high efficiency across the entire load range. An internal soft-start limits inrush current during start-up.

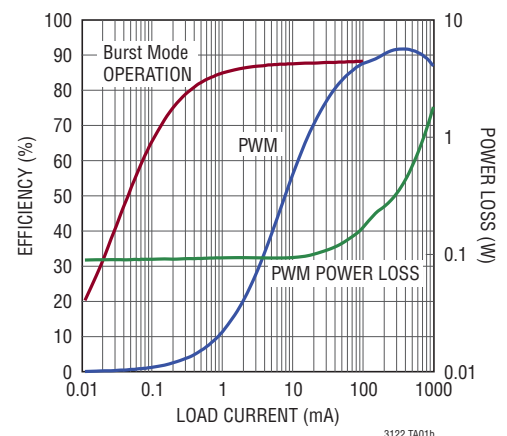
Other features include a <1μA shutdown current and robust protection under short-circuit, thermal overload, and output overvoltage conditions. The LTC3122 is offered in both a low profile 12-lead (3mm × 4mm × 0.75 mm) DFN package and a 12-lead thermally enhanced MSOP package.

## TYPICAL APPLICATION

### 5V to 12V Synchronous Boost Converter with Output Disconnect



### Efficiency Curve



# LTC3122

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

|                                            |                                            |
|--------------------------------------------|--------------------------------------------|
| $V_{IN}$ Voltage .....                     | -0.3V to 6V                                |
| $V_{OUT}$ Voltage .....                    | -0.3V to 18V                               |
| SW Voltage (Note 2) .....                  | -0.3V to 18V                               |
| SW Voltage (Pulsed < 100ns) (Note 2) ..... | -0.3V to 19V                               |
| $V_C$ , RT Voltage .....                   | -0.3V to $V_{CC}$                          |
| CAP Voltage .....                          |                                            |
| $V_{OUT} < 5.7V$ .....                     | -0.3V to ( $V_{OUT} + 0.3V$ )              |
| $5.7V \leq V_{OUT} \leq 11.7V$ .....       | ( $V_{OUT} - 6V$ ) to ( $V_{OUT} + 0.3V$ ) |
| $V_{OUT} > 11.7V$ .....                    | ( $V_{OUT} - 6V$ ) to 12V                  |

|                                                   |                |
|---------------------------------------------------|----------------|
| All Other Pins .....                              | -0.3V to 6V    |
| Operating Junction Temperature Range (Notes 3, 4) |                |
| LTC3122E/LTC3122I .....                           | -40°C to 125°C |
| LTC3122H .....                                    | -40°C to 150°C |
| Storage Temperature Range .....                   | -65°C to 150°C |
| MSE Lead Temperature (Soldering, 10sec) .....     | 300°C          |

## PIN CONFIGURATION

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>TOP VIEW</p> <p>SW 1, PGND 2, <math>V_{IN}</math> 3, PWM/SYNC 4, <math>V_{CC}</math> 5, RT 6, 13 PGND, 12 CAP, 11 <math>V_{OUT}</math>, 10 SGND, 9 <math>\overline{SD}</math>, 8 FB, 7 <math>V_C</math></p> <p>DE PACKAGE<br/>12-LEAD (4mm × 3mm) PLASTIC DFN</p> <p><math>T_{JMAX} = 125^\circ\text{C}</math>, <math>\theta_{JA} = 43^\circ\text{C/W}</math> (NOTE 5), <math>\theta_{JC} = 5^\circ\text{C/W}</math><br/>EXPOSED PAD (PIN 13) IS PGND,<br/>MUST BE SOLDERED TO PCB FOR RATED THERMAL PERFORMANCE</p> | <p>TOP VIEW</p> <p>SW 1, PGND 2, <math>V_{IN}</math> 3, PWM/SYNC 4, <math>V_{CC}</math> 5, RT 6, 13 PGND, 12 CAP, 11 <math>V_{OUT}</math>, 10 SGND, 9 <math>\overline{SD}</math>, 8 FB, 7 <math>V_C</math></p> <p>MSE PACKAGE<br/>12-LEAD PLASTIC MSOP</p> <p><math>T_{JMAX} = 150^\circ\text{C}</math>, <math>\theta_{JA} = 40^\circ\text{C/W}</math> (NOTE 5), <math>\theta_{JC} = 10^\circ\text{C/W}</math><br/>EXPOSED PAD (PIN 13) IS PGND,<br/>MUST BE SOLDERED TO PCB FOR RATED THERMAL PERFORMANCE</p> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL     | PART MARKING* | PACKAGE DESCRIPTION             | TEMPERATURE RANGE |
|------------------|-------------------|---------------|---------------------------------|-------------------|
| LTC3122EDE#PBF   | LTC3122EDE#TRPBF  | 3122          | 12-Lead (4mm × 3mm) Plastic DFN | -40°C to 125°C    |
| LTC3122IDE#PBF   | LTC3122IDE#TRPBF  | 3122          | 12-Lead (4mm × 3mm) Plastic DFN | -40°C to 125°C    |
| LTC3122EMSE#PBF  | LTC3122EMSE#TRPBF | 3122          | 12-Lead Plastic MSOP            | -40°C to 125°C    |
| LTC3122IMSE#PBF  | LTC3122IMSE#TRPBF | 3122          | 12-Lead Plastic MSOP            | -40°C to 125°C    |
| LTC3122HMSE#PBF  | LTC3122HMSE#TRPBF | 3122          | 12-Lead Plastic MSOP            | -40°C to 150°C    |

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 3).  $V_{IN} = 3.6\text{V}$ ,  $V_{OUT} = 12\text{V}$ ,  $RT = 57.6\text{k}$  unless otherwise noted.

| PARAMETER                               | CONDITIONS                                                                                      |   | MIN.               | TYP      | MAX                | UNITS                          |
|-----------------------------------------|-------------------------------------------------------------------------------------------------|---|--------------------|----------|--------------------|--------------------------------|
| Minimum Start-Up Voltage                | $V_{OUT} = 0\text{V}$                                                                           | ● |                    | 1.7      | 1.8                | V                              |
| Input Voltage Range                     | After $V_{OUT} \geq 2.2\text{V}$                                                                | ● | 0.5                |          | 5.5                | V                              |
| Output Voltage Adjust Range             |                                                                                                 | ● | 2.2                |          | 15                 | V                              |
| Feedback Voltage                        |                                                                                                 | ● | 1.178              | 1.202    | 1.225              | V                              |
| Feedback Input Current                  | $V_{FB} = 1.4\text{V}$                                                                          |   |                    | 1        | 50                 | nA                             |
| Quiescent Current, Shutdown             | $V_{SD} = 0\text{V}$ , $V_{OUT} = 0\text{V}$ , Not Including Switch Leakage                     |   |                    | 0.01     | 1                  | $\mu\text{A}$                  |
| Quiescent Current, Active               | $V_C = 0\text{V}$ , Measured On $V_{IN}$ , Non-Switching                                        |   |                    | 500      | 700                | $\mu\text{A}$                  |
| Quiescent Current, Burst                | Measured on $V_{IN}$ , $V_{FB} > 1.4\text{V}$<br>Measured on $V_{OUT}$ , $V_{FB} > 1.4\text{V}$ |   |                    | 25<br>10 | 40<br>20           | $\mu\text{A}$<br>$\mu\text{A}$ |
| N-channel MOSFET Switch Leakage Current | $V_{SW} = 15\text{V}$ , $V_{OUT} = 15\text{V}$ , $V_C = 0\text{V}$                              | ● |                    | 0.1      | 30                 | $\mu\text{A}$                  |
| P-channel MOSFET Switch Leakage Current | $V_{SW} = 0\text{V}$ , $V_{OUT} = 15\text{V}$ , $V_{SD} = 0\text{V}$                            | ● |                    | 0.1      | 70                 | $\mu\text{A}$                  |
| N-channel MOSFET Switch On-Resistance   |                                                                                                 |   |                    | 0.121    |                    | $\Omega$                       |
| P-channel MOSFET Switch On-Resistance   |                                                                                                 |   |                    | 0.188    |                    | $\Omega$                       |
| N-channel MOSFET Current Limit          |                                                                                                 | ● | 2.5                | 3.5      | 4.5                | A                              |
| Maximum Duty Cycle                      | $V_{FB} = 1.0\text{V}$                                                                          | ● | 90                 | 94       |                    | %                              |
| Minimum Duty Cycle                      | $V_{FB} = 1.4\text{V}$                                                                          | ● |                    |          | 0                  | %                              |
| Switching Frequency                     |                                                                                                 | ● | 0.85               | 1        | 1.15               | MHz                            |
| SYNC Frequency Range                    |                                                                                                 | ● | 0.1                |          | 3                  | MHz                            |
| PWM/SYNC Input High                     |                                                                                                 | ● | $0.9 \cdot V_{CC}$ |          |                    | V                              |
| PWM/SYNC Input Low                      |                                                                                                 | ● |                    |          | $0.1 \cdot V_{CC}$ | V                              |
| PWM/SYNC Input Current                  | $V_{PWM/SYNC} = 5.5\text{V}$                                                                    |   |                    | 0.01     | 1                  | $\mu\text{A}$                  |
| CAP Clamp Voltage                       | $V_{OUT} > 6.1\text{V}$ , Referenced to $V_{OUT}$                                               |   | -5.2               | -5.6     | -6.0               | V                              |
| $V_{CC}$ Regulation Voltage             | $V_{IN} < 2.8\text{V}$ , $V_{OUT} > 5\text{V}$                                                  |   | 4                  | 4.25     | 4.5                | V                              |
| Error Amplifier Transconductance        |                                                                                                 | ● | 70                 | 95       | 120                | $\mu\text{S}$                  |
| Error Amplifier Output Current          |                                                                                                 |   |                    | $\pm 25$ |                    | $\mu\text{A}$                  |
| Soft-Start Time                         |                                                                                                 |   |                    | 10       |                    | ms                             |
| $\overline{\text{SD}}$ Input High       |                                                                                                 | ● | 1.6                |          |                    | V                              |
| $\overline{\text{SD}}$ Input Low        |                                                                                                 | ● |                    |          | 0.25               | V                              |
| $\overline{\text{SD}}$ Input Current    | $V_{SD} = 5.5\text{V}$                                                                          |   |                    | 1        | 2                  | $\mu\text{A}$                  |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Voltage transients on the SW pin beyond the DC limit specified in the Absolute Maximum Ratings are non-disruptive to normal operations when using good layout practices, as shown on the demo board or described in the data sheet or application notes.

**Note 3:** The LTC3122 is tested under pulsed load conditions such that  $T_A \approx T_J$ . The LTC3122E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $85^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3122I is guaranteed to meet specifications over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction

temperature range. The LTC3122H is guaranteed to meet specifications over the full  $-40^\circ\text{C}$  to  $150^\circ\text{C}$  operating junction range. The junction temperature ( $T_J$  in  $^\circ\text{C}$ ) is calculated from the ambient temperature ( $T_A$  in  $^\circ\text{C}$ ) and power dissipation ( $P_D$  in Watts) according to the formula:  $T_J = T_A + (P_D \cdot \theta_{JA})$  where  $\theta_{JA}$  is the thermal impedance of the package.

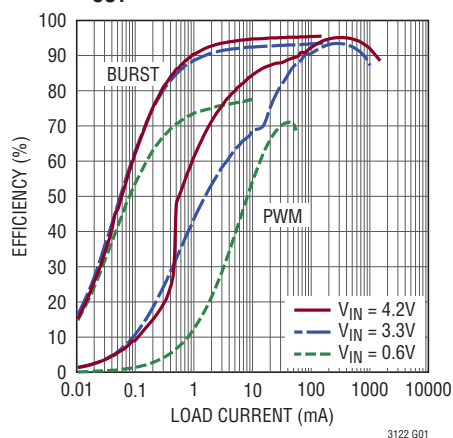
**Note 4:** The LTC3122 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $150^\circ\text{C}$  when overtemperature shutdown is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

**Note 5:** Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal impedance much higher than the rated package specifications.

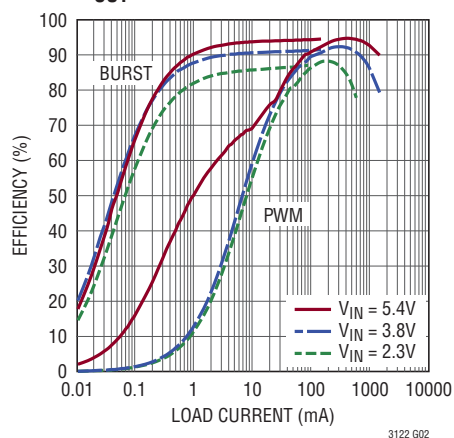
## TYPICAL PERFORMANCE CHARACTERISTICS

Configured as front page application unless otherwise specified.

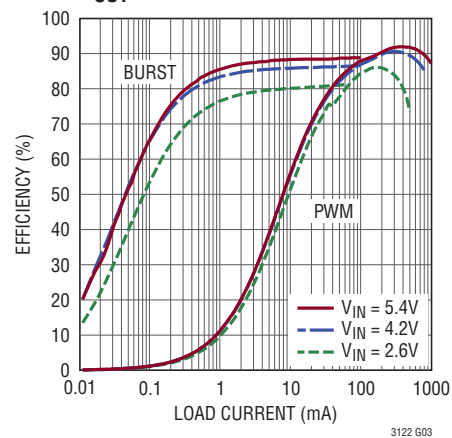
Efficiency vs Load Current,  
 $V_{OUT} = 5V$



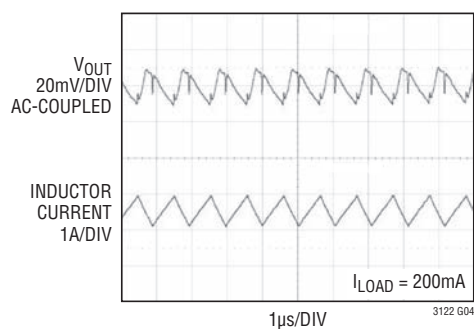
Efficiency vs Load Current,  
 $V_{OUT} = 7.5V$



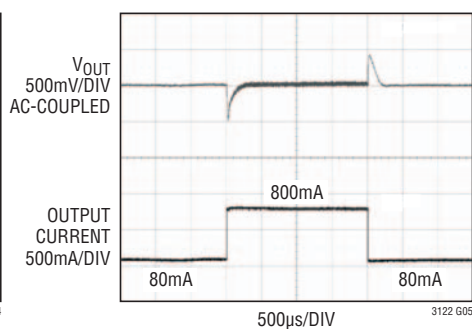
Efficiency vs Load Current,  
 $V_{OUT} = 12V$



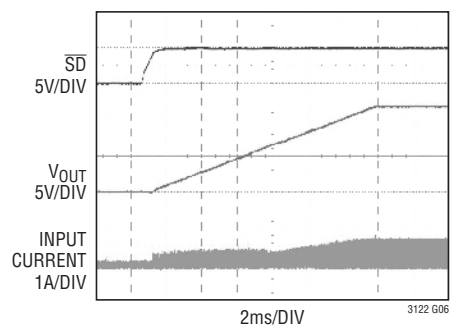
PWM Mode Operation



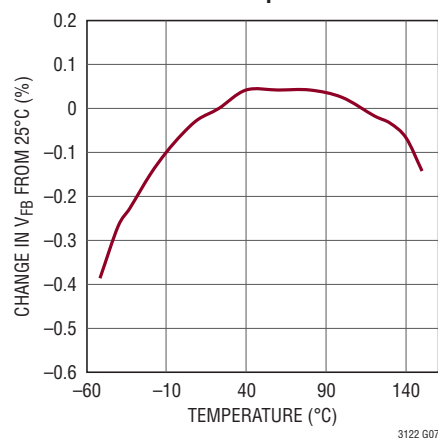
Load Transient Response



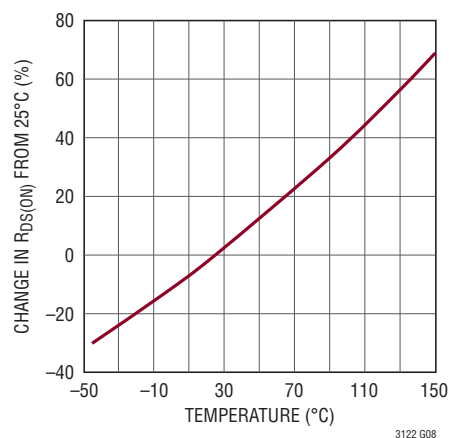
Inrush Current Control



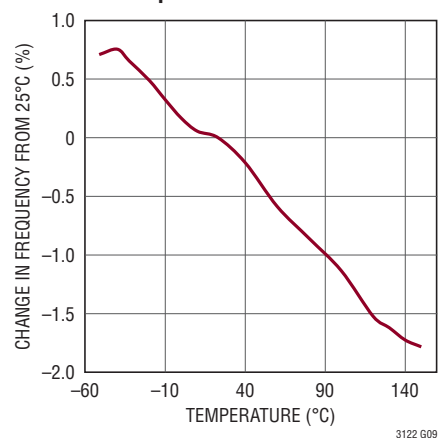
Feedback vs Temperature



$R_{DS(ON)}$  vs Temperature,  
Both NMOS and PMOS

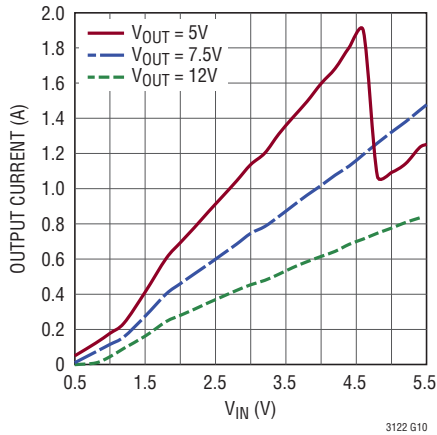


Oscillator Frequency  
vs Temperature

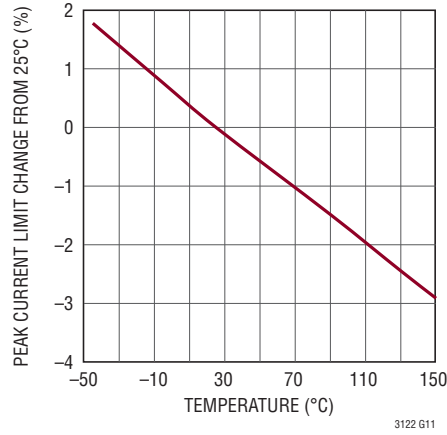


# TYPICAL PERFORMANCE CHARACTERISTICS

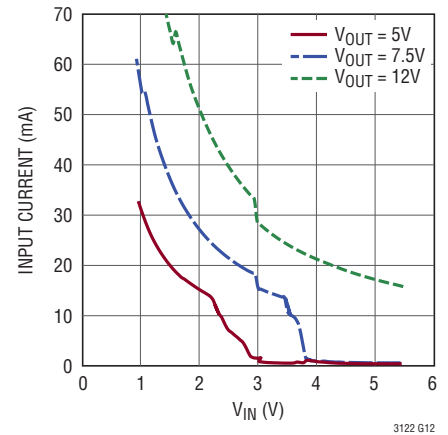
**PWM Mode Maximum Output Current vs  $V_{IN}$**



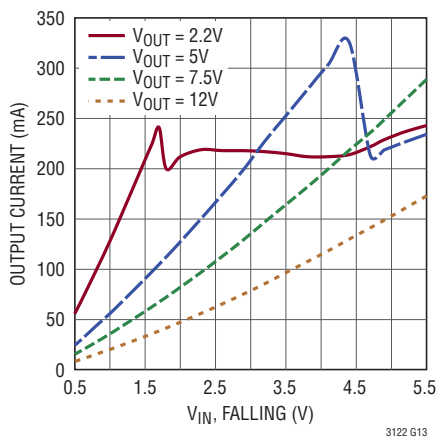
**Peak Current Limit Change vs Temperature**



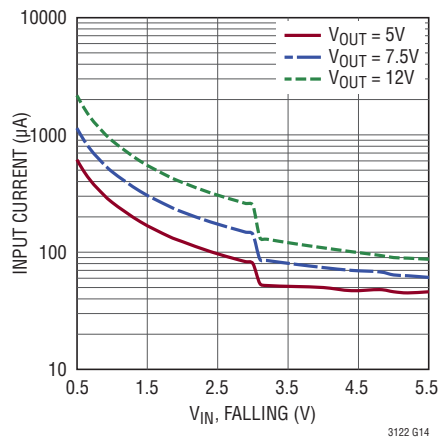
**PWM Operation No Load Input Current vs  $V_{IN}$**



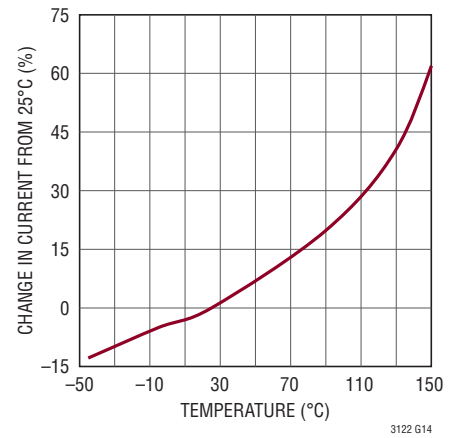
**Burst Mode Maximum Output Current vs  $V_{IN}$**



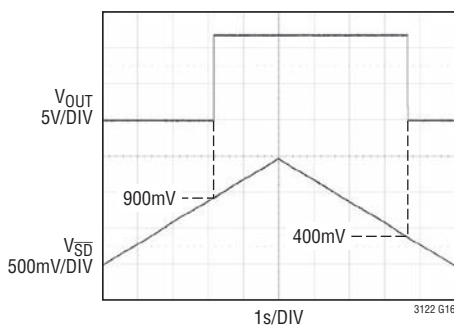
**Burst Mode No Load Input Current vs  $V_{IN}$**



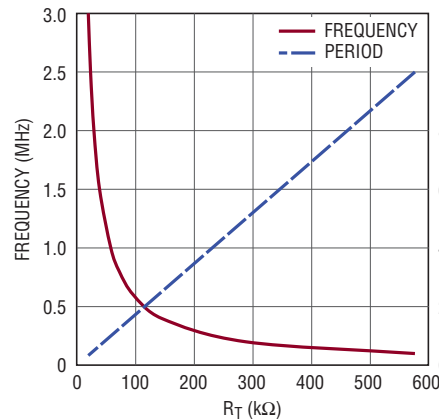
**Burst Mode Quiescent Current Change vs Temperature**



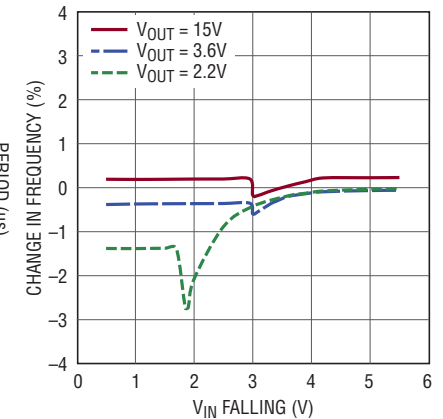
**$\overline{SD}$  Pin Threshold**



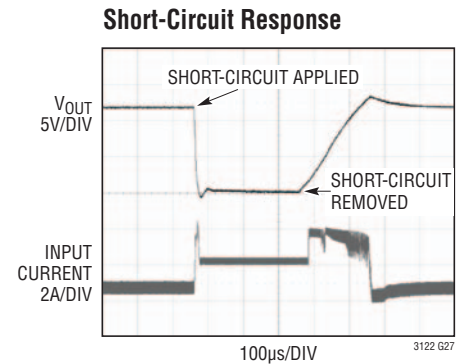
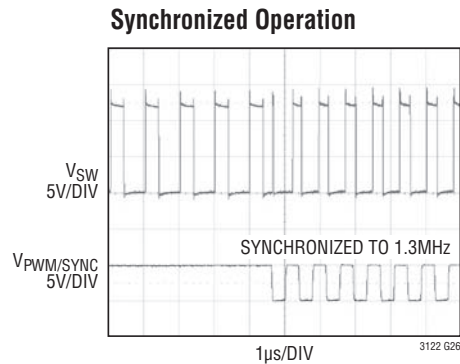
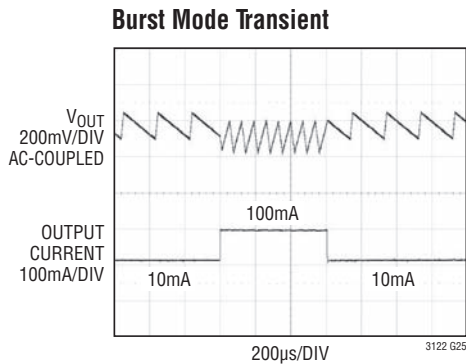
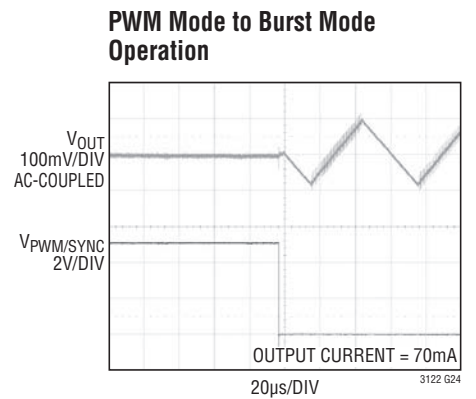
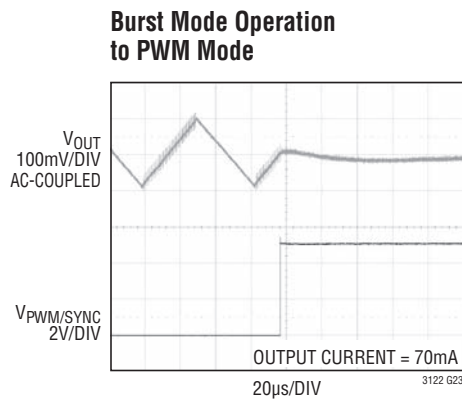
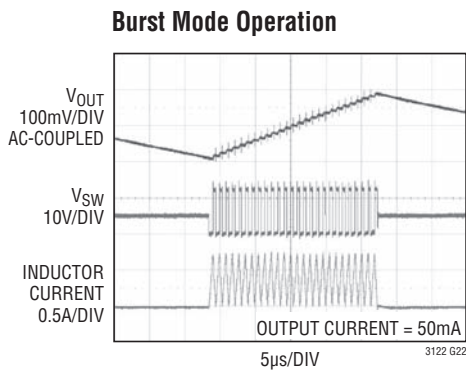
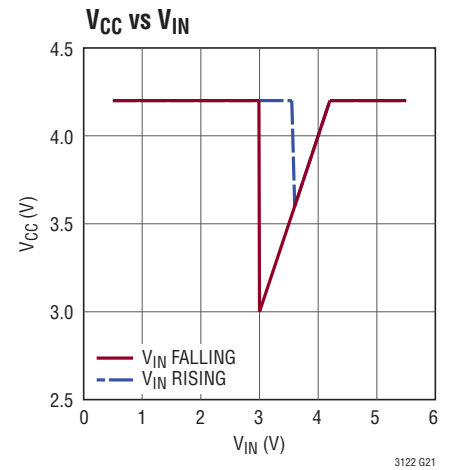
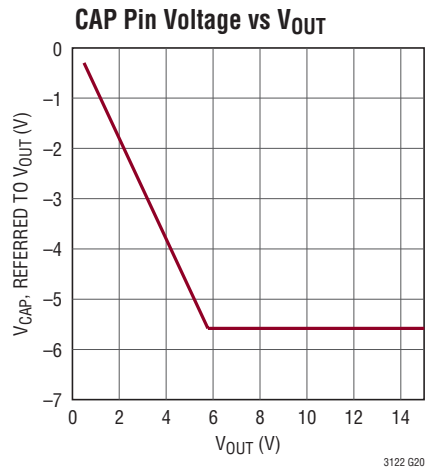
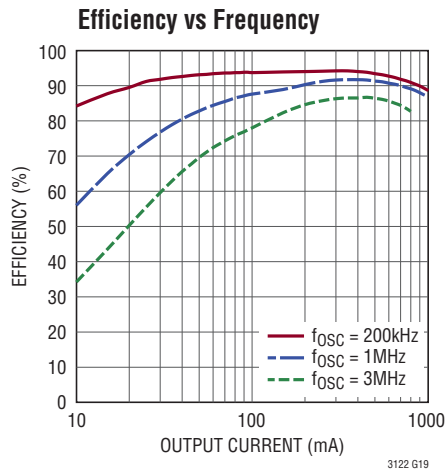
**Frequency vs  $R_T$**



**Frequency Accuracy**



## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**SW (Pin 1):** Switch Pin. Connect an inductor from this pin to  $V_{IN}$ . Keep PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. When  $V_{OUT} \geq V_{IN} + 2V$ , an internal anti-ringing resistor is connected between SW and  $V_{IN}$  after the inductor current has dropped to near zero, to minimize EMI. The anti-ringing resistor is also activated in shutdown and during the sleep periods of Burst Mode operation.

**PGND (Pins 2, 13):** Power Ground. When laying out your PCB, provide a short, direct path between PGND and the output capacitor and tie directly to the ground plane. The exposed pad is ground and **must be** soldered to the PCB ground plane for rated thermal performance.

**$V_{IN}$  (Pin 3):** Input Supply Pin. The device is powered from  $V_{IN}$  unless  $V_{OUT}$  exceeds  $V_{IN}$  and  $V_{IN}$  is less than 3V. Place a low ESR ceramic bypass capacitor of at least 4.7 $\mu$ F from  $V_{IN}$  to PGND. X5R and X7R dielectrics are preferred for their superior voltage and temperature characteristics.

**PWM/SYNC (Pin 4):** Burst Mode Operation Select and Oscillator Synchronization. **Do not leave this pin floating.**

- PWM/SYNC = High. Disable Burst Mode Operation and maintain low noise, constant frequency operation.
- PWM/SYNC = Low. The converter operates in Burst Mode operation, independent of load current.
- PWM/SYNC = External CLK. The internal oscillator is synchronized to the external CLK signal. Burst Mode operation is disabled. A clock pulse width between 100ns and 2 $\mu$ s is required to synchronize the oscillator. An external resistor **must be** connected between RT and GND to program the oscillator slightly below the desired synchronization frequency.

In non-synchronized applications, repeated clocking of the PWM/SYNC pin to affect an operating mode change is supported with these restrictions:

- Boost Mode ( $V_{OUT} > V_{IN}$ ):  $I_{OUT} < 500\mu A$ :  $f_{PWM/SYNC} \leq 100Hz$ ,  $I_{OUT} \geq 500\mu A$ :  $f_{PWM/SYNC} \leq 5kHz$
- Buck Mode ( $V_{OUT} < V_{IN}$ ):  $I_{OUT} < 5mA$ :  $f_{PWM/SYNC} \leq 5Hz$ ,  $I_{OUT} \geq 5mA$ :  $f_{PWM/SYNC} \leq 5kHz$

**$V_{CC}$  (Pin 5):**  $V_{CC}$  Regulator Output. Connect a low-ESR filter capacitor of at least 4.7 $\mu$ F from this pin to GND to provide a regulated rail approximately equal to the lower of  $V_{IN}$  and 4.25V. When  $V_{OUT}$  is higher than  $V_{IN}$ , and  $V_{IN}$  falls below 3V,  $V_{CC}$  will regulate to the lower of approximately  $V_{OUT}$  and 4.25V. A UVLO event occurs if  $V_{CC}$  drops below 1.6V. Switching is inhibited, and a soft-start is initiated when  $V_{CC}$  returns above 1.7V.

**RT (Pin 6):** Frequency Adjust Pin. Connect an external resistor ( $R_T$ ) from this pin to SGND to program the oscillator frequency according to the formula:

$$R_T = 57.6/f_{OSC}$$

where  $f_{OSC}$  is in MHz and  $R_T$  is in k $\Omega$ .

**VC (Pin 7):** Error Amplifier Output. A frequency compensation network is connected to this pin to compensate the control loop. See Compensating the Feedback Loop section for guidelines.

**FB (Pin 8):** Feedback Input to the Error Amplifier. Connect the resistor divider tap to this pin. Connect the top of the divider to  $V_{OUT}$  and the bottom of the divider to SGND. The output voltage can be adjusted from 2.2V to 15V according to this formula:

$$V_{OUT} = 1.202V \cdot (1 + R1/R2)$$

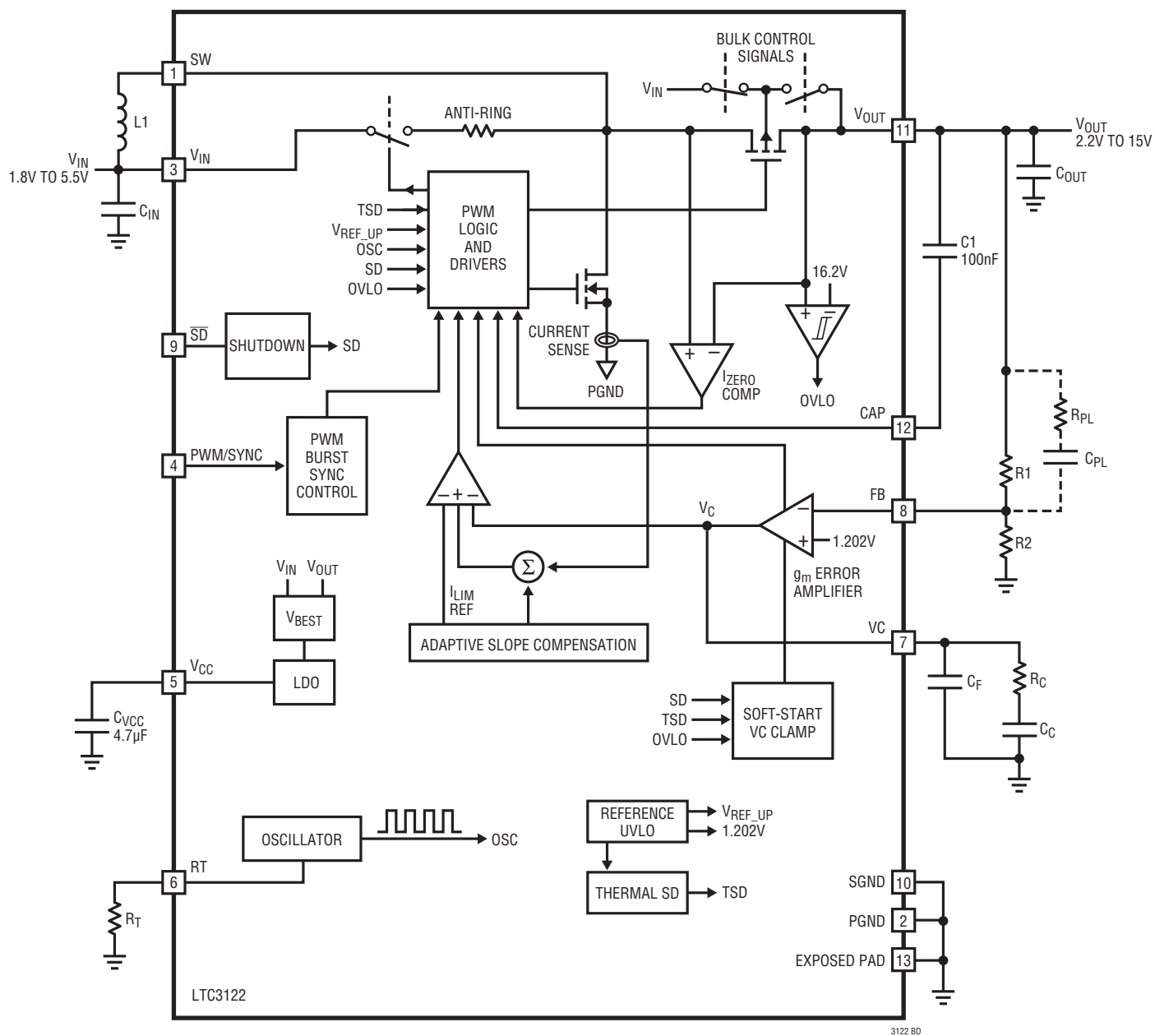
**$\overline{SD}$  (Pin 9):** Logic Controlled Shutdown Input. Bringing this pin above 1.6V enables normal, free-running operation, forcing this pin below 0.25V shuts the LTC3122 down, with quiescent current below 1 $\mu$ A. **Do not leave this pin floating.**

**SGND (Pin 10):** Signal Ground. When laying out a PC board, provide a short, direct path between SGND and the (–) side of the output capacitor.

**$V_{OUT}$  (Pin 11):** Output Voltage Sense and the Source of the Internal Synchronous Rectifier MOSFET. Driver bias is derived from  $V_{OUT}$ . Connect the output filter capacitor from  $V_{OUT}$  to PGND, as close to the IC as possible. A minimum value of 10 $\mu$ F ceramic is recommended.  $V_{OUT}$  is disconnected from  $V_{IN}$  when  $\overline{SD}$  is low.

**CAP (Pin 12):** Serves as the Low Reference for the Synchronous Rectifier Gate Drive. Connect a low ESR filter capacitor (typically 100nF) from this pin to  $V_{OUT}$  to provide an elevated ground rail, approximately 5.6V below  $V_{OUT}$ , used to drive the synchronous rectifier.

## BLOCK DIAGRAM



THE VALUES OF RC, CC, AND CF ARE BASED UPON OPERATING CONDITIONS.  
PLEASE REFER TO COMPENSATING THE FEEDBACK LOOP SECTION FOR  
GUIDELINES TO DETERMINE OPTIMAL VALUES OF THESE COMPONENTS.

3122 BD

## OPERATION

The LTC3122 is an adjustable frequency, 100kHz to 3MHz synchronous boost converter housed in either a 12-lead 4mm × 3mm DFN or a thermally enhanced MSOP package. The LTC3122 offers the unique ability to start-up and regulate the output from inputs as low as 1.8V and continue to operate from inputs as low as 0.5V. Output voltages can be programmed between 2.2V and 15V. The device also features fixed frequency, current mode PWM control for exceptional line and load regulation. The current mode architecture with adaptive slope compensation provides excellent transient load response and requires minimal output filtering. An internal 10ms closed loop soft-start simplifies the design process while minimizing the number of external components.

With its low  $R_{DS(ON)}$  and low gate charge internal N-channel MOSFET switch and P-channel MOSFET synchronous rectifier, the LTC3122 achieves high efficiency over a wide range of load current. High efficiency is achieved at light loads when Burst Mode operation is commanded. Operation can be best understood by referring to the Block Diagram.

### LOW VOLTAGE OPERATION

The LTC3122 is designed to allow start-up from input voltages as low as 1.8V. When  $V_{OUT}$  exceeds 2.2V, the LTC3122 continues to regulate its output, even when  $V_{IN}$  falls to as low as 0.5V. The limiting factors for the application become the availability of the input source to supply sufficient power to the output at the low voltages, and the maximum duty cycle. Note that at low input voltages, small voltage drops due to series resistance become critical and greatly limit the power delivery capability of the converter. This feature extends operating times by maximizing the amount of energy that can be extracted from the input source.

### LOW NOISE FIXED FREQUENCY OPERATION

#### Soft-Start

The LTC3122 contains internal circuitry to provide closed-loop soft-start operation. The soft-start utilizes a linearly increasing ramp of the error amplifier reference voltage from zero to its nominal value of 1.202V in approximately 10ms, with the internal control loop driving  $V_{OUT}$  from

zero to its final programmed value. This limits the inrush current drawn from the input source. As a result, the duration of the soft-start is largely unaffected by the size of the output capacitor or the output regulation voltage. The closed loop nature of the soft-start allows the converter to respond to load transients that might occur during the soft-start interval. The soft-start period is reset by a shutdown command on  $\overline{SD}$ , a UVLO event on  $V_{CC}$  ( $V_{CC} < 1.6V$ ), an overvoltage event on  $V_{OUT}$  ( $V_{OUT} \geq 16.2V$ ), or an overtemperature event (thermal shutdown is invoked when the die temperature exceeds 170°C). Upon removal of these fault conditions, the LTC3122 will soft-start the output voltage.

#### Error Amplifier

The non-inverting input of the transconductance error amplifier is internally connected to the 1.202V reference and the inverting input is connected to FB. An external resistive voltage divider from  $V_{OUT}$  to ground programs the output voltage from 2.2V to 15V via FB as shown in Figure 1.

$$V_{OUT} = 1.202V \left( 1 + \frac{R1}{R2} \right)$$

Selecting an  $R2$  value of 121k $\Omega$  to have approximately 10 $\mu$ A of bias current in the  $V_{OUT}$  resistor divider yields the formula:

$$R1 = 100.67 \cdot (V_{OUT} - 1.202V)$$

where  $R1$  is in k $\Omega$ .

Power converter control loop compensation is set by a simple RC network between  $V_C$  and ground.

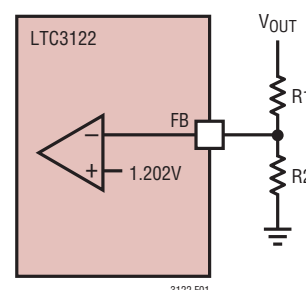


Figure 1. Programming the Output Voltage

## OPERATION

### Internal Current Limit

The current limit comparator shuts off the N-channel MOSFET switch once its threshold is reached. Peak switch current is limited to 3.5A, independent of input or output voltage, except when  $V_{OUT}$  is below 1.5V, resulting in the current limit being approximately half of the nominal peak.

Lossless current sensing converts the peak current signal of the N-channel MOSFET switch into a voltage that is summed with the internal slope compensation. The summed signal is compared to the error amplifier output to provide a peak current control command for the PWM.

### Zero Current Comparator

The zero current comparator monitors the inductor current being delivered to the output and shuts off the synchronous rectifier when this current reduces to approximately 50mA. This prevents the inductor current from reversing in polarity, improving efficiency at light loads.

### Oscillator

The internal oscillator is programmed to the desired switching frequency with an external resistor from the RT pin to GND according to the following formula:

$$f_{OSC}(\text{MHz}) = \left( \frac{57.6}{R_T(\text{k}\Omega)} \right)$$

The oscillator also can be synchronized to an external frequency by applying a pulse train to the PWM/SYNC pin. An external resistor must be connected between RT and GND to program the oscillator to a frequency approximately 25% below that of the externally applied pulse train used for synchronization.  $R_T$  is selected in this case according to this formula:

$$R_T(\text{k}\Omega) = \left( \frac{73.2}{f_{SYNC}(\text{MHz})} \right)$$

### Output Disconnect

The LTC3122's output disconnect feature eliminates body diode conduction of the internal P-channel MOSFET rectifier. This allows for  $V_{OUT}$  to discharge to 0V during

shutdown, and draw no current from the input source. It also allows for inrush current limiting at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output disconnect, there must not be an external Schottky diode connected between SW and  $V_{OUT}$ . The output disconnect feature also allows  $V_{OUT}$  to be pulled high, without reverse current being backed into the power source connected to  $V_{IN}$ .

### Shutdown

The boost converter is disabled by pulling  $\overline{SD}$  below 0.25V and enabled by pulling  $\overline{SD}$  above 1.6V. Note that  $\overline{SD}$  can be driven above  $V_{IN}$  or  $V_{OUT}$ , as long as it is limited to less than the absolute maximum rating.

### Thermal Shutdown

If the die temperature exceeds 170°C typical, the LTC3122 will go into thermal shutdown (TSD). All switches will be turned off until the die temperature drops by approximately 7°C, when the device re-initiates a soft-start and switching can resume.

### Boost Anti-Ringing Control

When  $V_{OUT} \geq V_{IN} + 2V$ , the anti-ringing control connects a resistor across the inductor to damp high frequency ringing on the SW pin during discontinuous current mode operation when the inductor current has dropped to near zero. Although the ringing of the resonant circuit formed by L and  $C_{SW}$  (capacitance on SW pin) is low energy, it can cause EMI radiation.

### $V_{CC}$ Regulator

An internal low dropout regulator generates the 4.25V (nominal)  $V_{CC}$  rail from  $V_{IN}$  or  $V_{OUT}$ , depending upon operating conditions.  $V_{CC}$  is supplied from  $V_{IN}$  when  $V_{IN}$  is greater than 3.5V, otherwise the greater of  $V_{IN}$  and  $V_{OUT}$  is used. The  $V_{CC}$  rail powers the internal control circuitry and power MOSFET gate drivers of the LTC3122. The  $V_{CC}$  regulator is disabled in shutdown to reduce quiescent current and is enabled by forcing the  $\overline{SD}$  pin above its threshold. A 4.7μF or larger capacitor must be connected between  $V_{CC}$  and SGND.

## APPLICATIONS INFORMATION

### Overvoltage Lockout

An overvoltage condition occurs when  $V_{OUT}$  exceeds approximately 16.2V. Switching is disabled and the internal soft-start ramp is reset. Once  $V_{OUT}$  drops below approximately 15.6V, a soft-start cycle is initiated and switching is enabled. If the boost converter output is lightly loaded so that the time constant product of the output capacitance,  $C_{OUT}$ , and the output load resistance,  $R_{OUT}$  is near or greater than the soft-start time of approximately 10ms, the soft-start ramp may end before or soon after switching resumes, defeating the inrush current limiting of the closed loop soft-start following an overvoltage event.

### Short-Circuit Protection

The LTC3122 output disconnect feature allows output short-circuit protection. To reduce power dissipation under overload and short-circuit conditions, the peak switch current limit is reduced to 1.6A. Once  $V_{OUT} > 1.5V$ , the current limit is set to its nominal value of 3.5A.

### $V_{IN} > V_{OUT}$ Operation

The LTC3122 step-up converter will maintain voltage regulation even when the input voltage is above the desired output voltage. Note that operating in this mode will exhibit lower efficiency and a reduced output current capability. Refer to the Typical Performance Characteristics section for details.

### Burst Mode OPERATION

When the PWM/SYNC pin is held low, the boost converter operates in Burst Mode operation to improve efficiency at light loads and reduce standby current at no load. The input thresholds for this pin are determined relative to  $V_{CC}$  with a low being less than 10% of  $V_{CC}$  and a high being greater than 90% of  $V_{CC}$ . The LTC3122 will operate in fixed frequency PWM mode even if Burst Mode operation is commanded during soft-start.

In Burst Mode operation, the LTC3122 switches asynchronously. The inductor current is first charged to 600mA by turning on the N-channel MOSFET switch. Once this current threshold is reached, the N-channel is turned off and the P-channel synchronous switch is turned on, delivering current to the output. When the inductor current discharges to approximately zero, the cycle repeats. In Burst Mode operation, energy is delivered to the output until the nominal regulation value is reached, at which point the LTC3122 transitions to sleep mode. In sleep, the output switches are turned off and the LTC3122 consumes only 25 $\mu$ A of quiescent current. When the output voltage droops approximately 1%, switching resumes. This maximizes efficiency at very light loads by minimizing switching and quiescent losses. Output voltage ripple in Burst Mode operation is typically 1% to 2% peak-to-peak. Additional output capacitance (10 $\mu$ F or greater), or the addition of a small feed-forward capacitor (10pF to 50pF) connected between  $V_{OUT}$  and FB can help further reduce the output ripple.

The maximum output current ( $I_{OUT}$ ) capability in Burst Mode operation varies with  $V_{IN}$  and  $V_{OUT}$ , as shown in Figure 2.

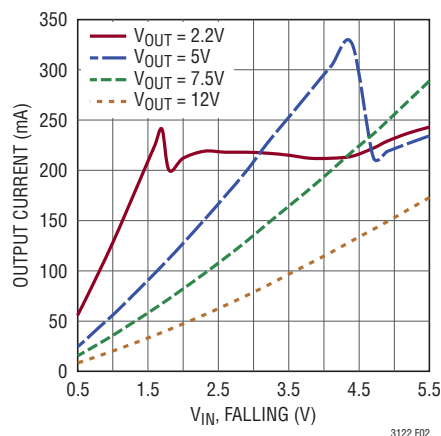
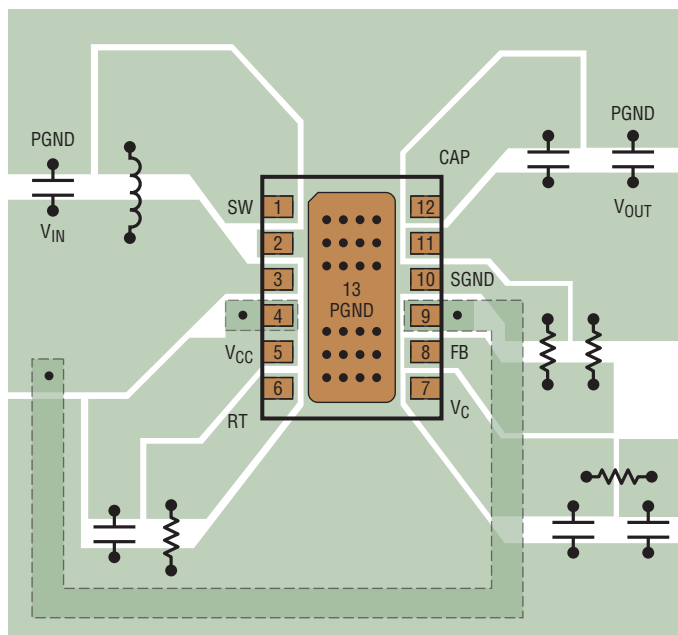


Figure 2. Burst Mode Maximum Output Current vs  $V_{IN}$

## APPLICATIONS INFORMATION

### PCB LAYOUT GUIDELINES

The high switching frequency of the LTC3122 demands careful attention to board layout. A careless layout will result in reduced performance. Maximizing the copper area for ground will help to minimize die temperature rise. A multilayer board with a separate ground plane is ideal, but not absolutely necessary. See Figure 3 for an example of a two-layer board layout.



**Figure 3. Traces Carrying High Current Are Direct (PGND, SW, VIN and VOUT). Trace Area at FB and VC Are Kept Low. Trace Length to Input Supply Should Be Kept Short. VIN and VOUT Ceramic Capacitors Should Be Placed as Close to the LTC3122 Pins as Possible**

### SCHOTTKY DIODE

Although it is not required, adding a Schottky diode from SW to VOUT can improve the converter efficiency by about 4%. Note that this defeats the output disconnect and short-circuit protection features of the LTC3122.

### COMPONENT SELECTION

#### Inductor Selection

The LTC3122 can utilize small surface mount inductors due to its high switching frequency (up to 3MHz). Larger values of inductance will allow slightly greater output cur-

rent capability by reducing the inductor ripple current. The minimum inductance value, L, is inversely proportional to operating frequency and is given by the following equation:

$$L > \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{f \cdot \text{Ripple} \cdot V_{OUT}} \mu\text{H and } L > \frac{3}{f}$$

where:

Ripple = Allowable inductor current ripple (amps peak-to-peak)

f = Switching Frequency in MHz

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low ESR (series resistance of the windings) to reduce the  $I^2R$  power losses, and must be able to support the peak inductor current without saturating. Molded chokes and some chip inductors usually do not have enough core area to support the peak inductor currents of 3A to 4A seen on the LTC3122. To minimize radiated noise, use a shielded inductor.

See Table 1 for suggested components and suppliers.

**Table 1. Recommended Inductors**

| PART NUMBER         | VALUE (μH) | DCR (mΩ) | MAX DC CURRENT (A) | SIZE (mm) W × L × H |
|---------------------|------------|----------|--------------------|---------------------|
| Coilcraft LPS4018   | 1          | 42       | 3.8                | 4 × 4 × 1.8         |
| Coilcraft MSS7341   | 3.3        | 20       | 3.72               | 7.3 × 7.3 × 4.1     |
| Coilcraft MSS1260T  | 33         | 54.9     | 4.34               | 12.3 × 12.3 × 6.2   |
| Coiltronics DRQ73   | 0.992      | 24       | 3.99               | 7.6 × 7.6 × 3.55    |
| Coiltronics SD7030  | 3.3        | 24       | 3                  | 7 × 7 × 3           |
| Coiltronics DR125   | 33         | 59       | 3.84               | 12.5 × 12.5 × 6     |
| Murata LQH6PP       | 1          | 9        | 4.3                | 6 × 6 × 4.3         |
| Murata LQH6PP       | 3.3        | 16       | 3.8                | 6 × 6 × 4.3         |
| Sumida CDRH50D28RNP | 1.2        | 13       | 4.8                | 5 × 5 × 2.8         |
| Sumida CDRH8D28NP   | 3.3        | 18       | 4                  | 8 × 8 × 3           |
| Sumida CDRH129HF    | 33         | 53       | 4.25               | 12 × 12 × 10        |
| Taiyo-Yuden NR6045  | 3          | 31       | 3.2                | 6 × 6 × 4.5         |
| TDK LTF5022T        | 1.2        | 25       | 4.2                | 5 × 5.2 × 2.2       |
| TDK SPM6530T        | 3.3        | 20       | 4.1                | 7 × 7 × 3.2         |
| TDK VLF12060T       | 33         | 53       | 3.4                | 11.7 × 12 × 6       |
| Würth WE-PD         | 3.3        | 32.5     | 3.1                | 7.3 × 7.3 × 2       |

## APPLICATIONS INFORMATION

### Output and Input Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used. Although ceramic capacitors are recommended, low ESR tantalum capacitors may be used as well.

When selecting output capacitors, the magnitude of the peak inductor current, together with the ripple voltage specification, determine the choice of the capacitor. Both the ESR (equivalent series resistance) of the capacitor and the charge stored in the capacitor each cycle contribute to the output voltage ripple.

The ripple due to the charge is approximately:

$$V_{\text{RIPPLE(CHARGE)}} \approx \frac{I_P \cdot V_{\text{IN}}}{C_{\text{OUT}} \cdot V_{\text{OUT}} \cdot f}$$

where  $I_P$  is the peak inductor current.

The ESR of  $C_{\text{OUT}}$  is usually the most dominant factor for ripple in most power converters. The ripple due to the capacitor ESR is:

$$V_{\text{RIPPLE(ESR)}} = I_{\text{LOAD}} \cdot R_{\text{ESR}} \cdot \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

where  $R_{\text{ESR}}$  = capacitor equivalent series resistance.

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. A low ESR bypass capacitor with a value of at least  $4.7\mu\text{F}$  should be located as close to the  $V_{\text{IN}}$  pin as possible.

Low ESR and high capacitance are critical to maintain low output voltage ripple. Capacitors can be used in parallel for even larger capacitance values and lower effective ESR. Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors experience significant loss in capacitance from their rated value with increased DC bias voltage. It is not uncommon for a small surface mount capacitor to lose more than 50%

of its rated capacitance when operated near its rated voltage. As a result it is sometimes necessary to use a larger capacitor value or a capacitor with a larger value and case size, such as 1812 rather than 1206, in order to actually realize the intended capacitance at the full operating voltage. Be sure to consult the vendor's curve of capacitance vs DC bias voltage. Table 2 shows a sampling of capacitors suited for LTC3122 applications.

**Table 2. Representative Output Capacitors**

| MANUFACTURER, PART NUMBER    | VALUE ( $\mu\text{F}$ ) | VOLTAGE (V) | SIZE L x W x H (mm) TYPE, ESR ( $\text{m}\Omega$ )              |
|------------------------------|-------------------------|-------------|-----------------------------------------------------------------|
| AVX, 12103D226MAT2A          | 22                      | 25          | $3.2 \times 2.5 \times 2.79$ , X5R Ceramic                      |
| Kemet, C2220X226K3RACTU      | 22                      | 25          | $5.7 \times 5.0 \times 2.4$ , X7R Ceramic                       |
| Kemet, A700D226M016ATE030    | 22                      | 16          | $7.3 \times 4.3 \times 2.8$ , Alum. Polymer, $30\text{m}\Omega$ |
| Murata, GRM32ER71E226KE15L   | 22                      | 25          | $3.2 \times 2.5 \times 2.5$ , X7R Ceramic                       |
| Nichicon, PLV1E121MDL1       | 82                      | 25          | $8 \times 8 \times 12$ , Alum. Polymer, $25\text{m}\Omega$      |
| Panasonic, ECJ-4YB1E226M     | 22                      | 25          | $3.2 \times 2.5 \times 2.5$ , X5R Ceramic                       |
| Sanyo, 25TQC22MV             | 22                      | 25          | $7.3 \times 4.3 \times 3.1$ , POSCAP, $50\text{m}\Omega$        |
| Sanyo, 16TQC100M             | 100                     | 16          | $7.3 \times 4.3 \times 1.9$ , POSCAP, $45\text{m}\Omega$        |
| Sanyo, 25SVPF47M             | 47                      | 25          | $6.6 \times 6.6 \times 5.9$ , OS-CON, $30\text{m}\Omega$        |
| Taiyo Yuden, TMK325BJ226MM-T | 22                      | 25          | $3.2 \times 2.5 \times 2.5$ , X5R Ceramic                       |
| TDK, CKG57NX5R1E476M         | 47                      | 25          | $6.5 \times 5.5 \times 5.5$ , X5R Ceramic                       |
| Cap-XX GS230F                | 1.2Farads               | 4.5         | $39 \times 17 \times 3.8$ $28\text{m}\Omega$                    |
| Cooper A1030-2R5155          | 1.5Farads               | 2.5         | $\varnothing = 10$ , L = 30 $60\text{m}\Omega$                  |
| Maxwell BCAP0050-P270        | 50Farads                | 2.5         | $\varnothing = 18$ , L = 40 $20\text{m}\Omega$                  |

For applications requiring a very low profile and very large capacitance, the GS, GS2 and GW series from Cap-XX and PowerStor Aerogel Capacitors from Cooper all offer very high capacitance and low ESR in various low profile packages.

A method for improving the converter's transient response uses a small feed-forward series network of a capacitor and

## APPLICATIONS INFORMATION

a resistor across the top resistor of the feedback divider (from  $V_{OUT}$  to FB). This adds a phase-lead zero and pole to the transfer function of the converter as calculated in the Compensating the Feedback Loop section.

### OPERATING FREQUENCY SELECTION

There are several considerations in selecting the operating frequency of the converter. Typically the first consideration is to stay clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz and in that case a 1.5MHz switching converter frequency may be employed. A second consideration is the physical size of the converter. As the operating frequency is increased, the inductor and filter capacitors typically can be reduced in value, leading to smaller sized external components. The smaller solution size is typically traded for efficiency, since the switching losses due to gate charge increase with frequency.

Another consideration is whether the application can allow pulse-skipping. When the boost converter pulse-skips, the minimum on-time of the converter is unable to support the duty cycle. This results in a low frequency component to the output ripple. In many applications where physical size is the main criterion, running the converter in this mode is acceptable. In applications where it is preferred not to enter this mode, the maximum operating frequency is given by:

$$f_{MAX\_NOSKIP} \leq \frac{V_{OUT} - V_{IN}}{V_{OUT} \cdot t_{ON(MIN)}} \text{ Hz}$$

where  $t_{ON(MIN)}$  = minimum on-time = 100ns.

### Thermal Considerations

For the LTC3122 to deliver its full power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the large thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as

possible. If the junction temperature rises above  $\sim 170^{\circ}\text{C}$ , the part will go into thermal shutdown, and all switching will stop until the temperature drops approximately  $7^{\circ}\text{C}$ .

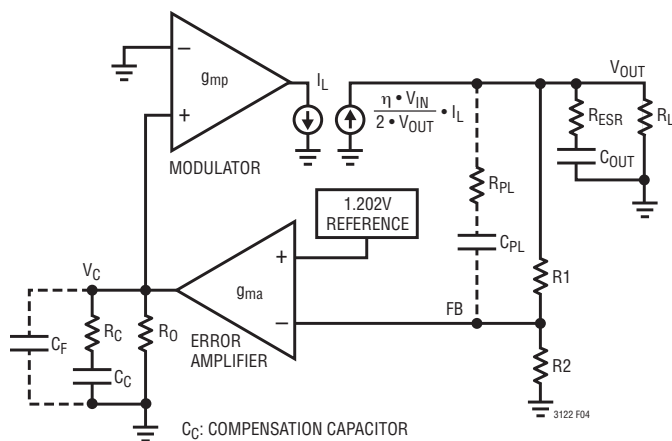
### Compensating the Feedback Loop

The LTC3122 uses current mode control, with internal adaptive slope compensation. Current mode control eliminates the second order filter due to the inductor and output capacitor exhibited in voltage mode control, and simplifies the power loop to a single pole filter response. Because of this fast current control loop, the power stage of the IC combined with the external inductor can be modeled by a transconductance amplifier  $g_{mp}$  and a current controlled current source. Figure 4 shows the key equivalent small signal elements of a boost converter.

The DC small-signal loop gain of the system shown in Figure 4 is given by the following equation:

$$G_{BOOST} = G_{EA} \cdot G_{MP} \cdot G_{POWER} \cdot \frac{R_2}{R_1 + R_2}$$

where  $G_{EA}$  is the DC gain of the error amplifier,  $G_{MP}$  is the modulator gain, and  $G_{POWER}$  is the inductor current to  $V_{OUT}$  gain.



$C_C$ : COMPENSATION CAPACITOR  
 $C_{OUT}$ : OUTPUT CAPACITOR  
 $C_{PL}$ : PHASE LEAD CAPACITOR  
 $C_F$ : HIGH FREQUENCY FILTER CAPACITOR  
 $g_{ma}$ : TRANSCONDUCTANCE AMPLIFIER INSIDE IC  
 $g_{mp}$ : POWER STAGE TRANSCONDUCTANCE AMPLIFIER  
 $R_C$ : COMPENSATION RESISTOR  
 $R_L$ : OUTPUT RESISTANCE DEFINED AS  $V_{OUT}/I_{LOADMAX}$   
 $R_O$ : OUTPUT RESISTANCE OF  $g_{ma}$   
 $R_{PL}$ : PHASE LEAD RESISTOR  
 $R_1, R_2$ : FEEDBACK RESISTOR DIVIDER NETWORK  
 $R_{ESR}$ : OUTPUT CAPACITOR ESR  
 $\eta$ : CONVERTER EFFICIENCY ( $\sim 90\%$  AT HIGHER CURRENTS)

Figure 4. Boost Converter Equivalent Model

## APPLICATIONS INFORMATION

$$G_{EA} = g_{ma} \cdot R_O \approx 950V/V$$

(Not Adjustable;  $g_{ma} = 95\mu S$ ,  $R_O \approx 10M\Omega$ )

$$G_{MP} = g_{mp} = \frac{\Delta I_L}{\Delta V_C} \approx 3.4S \text{ (Not Adjustable)}$$

$$G_{POWER} = \frac{\Delta V_{OUT}}{\Delta I_L} = \frac{\eta \cdot V_{IN}}{2 \cdot I_{OUT}}$$

Combining the two equations above yields:

$$G_{DC} = G_{MP} \cdot G_{POWER} \approx \frac{1.7 \cdot \eta \cdot V_{IN}}{I_{OUT}} V/V$$

Converter efficiency  $\eta$  will vary with  $I_{OUT}$  and switching frequency  $f_{OSC}$  as shown in the typical performance characteristics curves.

$$\text{Output Pole: } P1 = \frac{2}{2 \cdot \pi \cdot R_L \cdot C_{OUT}} \text{ Hz}$$

$$\text{Error Amplifier Pole: } P2 = \frac{1}{2 \cdot \pi \cdot R_O \cdot (C_C + C_F)} \text{ Hz}$$

$$\text{Error Amplifier Zero: } Z1 = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C} \text{ Hz}$$

$$\text{ESR Zero: } Z2 = \frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{OUT}} \text{ Hz}$$

$$\text{RHP Zero: } Z3 = \frac{V_{IN}^2 \cdot R_L}{2 \cdot \pi \cdot V_{OUT}^2 \cdot L} \text{ Hz}$$

$$\text{High Frequency Pole: } P3 > \frac{f_{OSC}}{3}$$

$$\text{Phase Lead Zero: } Z4 = \frac{1}{2 \cdot \pi \cdot (R1 + R_{PL}) \cdot C_{PL}} \text{ Hz}$$

$$\text{Phase Lead Pole: } P4 = \frac{1}{2 \cdot \pi \cdot \left( \frac{R1 \cdot R2}{R1 + R2} + R_{PL} \right) \cdot C_{PL}} \text{ Hz}$$

Error Amplifier Filter Pole:

$$P5 = \frac{1}{2 \cdot \pi \cdot R_C \cdot \left( \frac{C_C \cdot C_F}{C_C + C_F} \right)} \text{ Hz}$$

The current mode zero (Z3) is a right half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection. As a general rule, the frequency at which the open-loop gain of the converter is reduced to unity, known as the crossover frequency  $f_C$ , should be set to less than one third of the right half plane zero (Z3), and under one eighth of the switching frequency  $f_{OSC}$ . Once  $f_C$  is selected, the values for the compensation components can be calculated using a bode plot of the power stage or two generally valid assumptions: P1 dominates the gain of the power stage for frequencies lower than  $f_C$  and  $f_C$  is much higher than P2. First calculate the power stage gain at  $f_C$ ,  $G_{fC}$  in V/V. Assuming the output pole P1 dominates  $G_{fC}$  for this range, it is expressed by:

$$G_{fC} \approx \frac{G_{DC}}{\sqrt{1 + \left( \frac{f_C}{P1} \right)^2}} V/V$$

Decide how much phase margin ( $\Phi_m$ ) is desired. Greater phase margin can offer more stability while lower phase margin can yield faster transient response. Typically,  $\Phi_m \approx 60^\circ$  is optimal for minimizing transient response time while allowing sufficient margin to account for component variability.  $\Phi_1$  is the phase boost of Z1, P2, and P5 while  $\Phi_2$  is the phase boost of Z4 and P4. Select  $\Phi_1$  and  $\Phi_2$  such that

$$\Phi_1 \leq 74^\circ; \Phi_2 \leq \left( 2 \cdot \tan^{-1} \sqrt{\frac{V_{OUT}}{1.2V}} \right) - 90^\circ \text{ and}$$

$$\Phi_1 + \Phi_2 = \Phi_m + \tan^{-1} \left( \frac{f_C}{Z3} \right)$$

where  $V_{OUT}$  is in V and  $f_C$  and Z3 are in kHz.

Setting Z1, P5, Z4, and P4 such that

$$Z1 = \frac{f_C}{\sqrt{a_1}}, P5 = f_C \sqrt{a_1}, Z4 = \frac{f_C}{\sqrt{a_2}}, P4 = f_C \sqrt{a_2}$$

allows  $a_1$  and  $a_2$  to be determined using  $\Phi_1$  and  $\Phi_2$

$$a_1 = \tan^2 \left( \frac{\Phi_1 + 90^\circ}{2} \right), a_2 = \tan^2 \left( \frac{\Phi_2 + 90^\circ}{2} \right)$$

## APPLICATIONS INFORMATION

The compensation will force the converter gain  $G_{\text{BOOST}}$  to unity at  $f_C$  by using the following expression for  $C_C$ :

$$C_C = \frac{10^3 \cdot g_{\text{ma}} \cdot R_2 \cdot G_{fC} (a_1 - 1) \sqrt{a_2}}{2\pi \cdot f_C \cdot (R_1 + R_2) \sqrt{a_1}} \text{ pF}$$

( $g_{\text{ma}}$  in  $\mu\text{S}$ ,  $f_C$  in kHz,  $G_{fC}$  in V/V)

Once  $C_C$  is calculated,  $R_C$  and  $C_F$  are determined by:

$$R_C = \frac{10^6 \cdot \sqrt{a_1}}{2\pi \cdot f_C \cdot C_C} \text{ k}\Omega \text{ (} f_C \text{ in kHz, } C_C \text{ in pF)}$$

$$C_F = \frac{C_C}{a_1 - 1}$$

The values of the phase lead components are given by the expressions:

$$R_{\text{PL}} = \frac{R_1 - a_2 \cdot \left( \frac{R_1 \cdot R_2}{R_1 + R_2} \right)}{a_2 - 1} \text{ k}\Omega \text{ and}$$

$$C_{\text{PL}} = \frac{10^6 (a_2 - 1) (R_1 + R_2)}{2\pi \cdot f_C \cdot R_1^2 \sqrt{a_2}} \text{ pF}$$

where  $R_1$ ,  $R_2$ , and  $R_{\text{PL}}$  are in  $\text{k}\Omega$  and  $f_C$  is in kHz.

Note that selecting  $\Phi_2 = 0^\circ$  forces  $a_2 = 1$ , and so the converter will have Type II compensation and therefore no feedforward:  $R_{\text{PL}}$  is open (infinite impedance) and  $C_{\text{PL}} = 0 \text{ pF}$ . If  $a_2 = 0.833 \cdot V_{\text{OUT}}$  (its maximum), feedforward is maximized;  $R_{\text{PL}} = 0$  and  $C_{\text{PL}}$  is maximized for this compensation method.

Once the compensation values have been calculated, obtaining a converter bode plot is strongly recommended to verify calculations and adjust values as required.

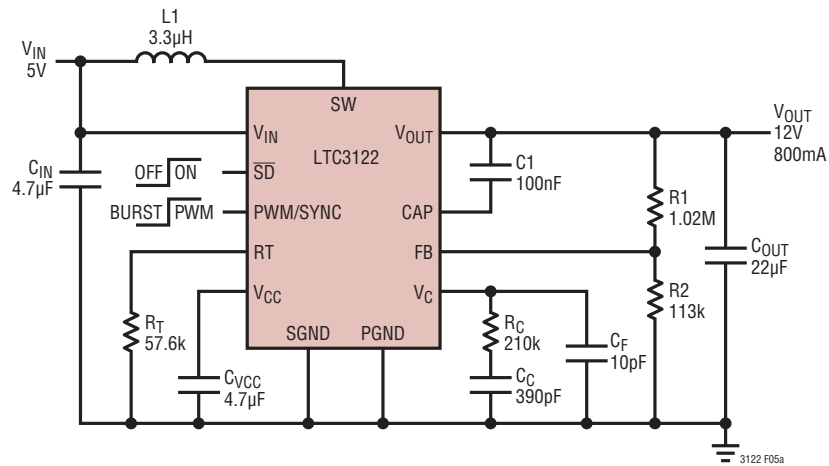
Using the circuit in Figure 5 as an example, Table 3 shows the parameters used to generate the bode plot shown in Figure 6.

**Table 3. Bode Plot Parameters for Type II Compensation**

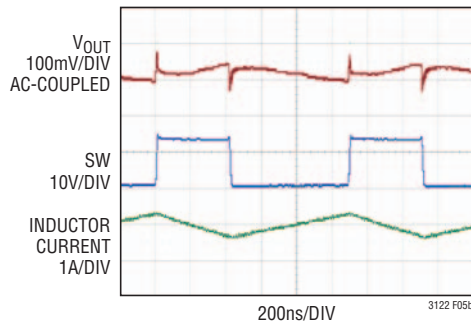
| PARAMETER        | VALUE | UNITS            | COMMENT      |
|------------------|-------|------------------|--------------|
| $V_{\text{IN}}$  | 5     | V                | App Specific |
| $V_{\text{OUT}}$ | 12    | V                | App Specific |
| $R_L$            | 15    | $\Omega$         | App Specific |
| $C_{\text{OUT}}$ | 22    | $\mu\text{F}$    | App Specific |
| $R_{\text{ESR}}$ | 5     | $\text{m}\Omega$ | App Specific |
| $L$              | 3.3   | $\mu\text{H}$    | App Specific |
| $f_{\text{OSC}}$ | 1     | MHz              | Adjustable   |
| $R_1$            | 1020  | $\text{k}\Omega$ | Adjustable   |
| $R_2$            | 113   | $\text{k}\Omega$ | Adjustable   |
| $g_{\text{ma}}$  | 95    | $\mu\text{S}$    | Fixed        |
| $R_O$            | 10    | $\text{M}\Omega$ | Fixed        |
| $g_{\text{mp}}$  | 3.4   | S                | Fixed        |
| $\eta$           | 80    | %                | App Specific |
| $R_C$            | 210   | $\text{k}\Omega$ | Adjustable   |
| $C_C$            | 390   | pF               | Adjustable   |
| $C_F$            | 10    | pF               | Adjustable   |
| $R_{\text{PL}}$  | 0     | $\text{k}\Omega$ | Optional     |
| $C_{\text{PL}}$  | 0     | pF               | Optional     |

From Figure 6, the phase is  $60^\circ$  when the gain reaches 0dB, so the phase margin of the converter is  $60^\circ$ . The crossover frequency is 15kHz, which is more than three times lower than the 108.4kHz frequency of the RHP zero to achieve adequate phase margin.

## APPLICATIONS INFORMATION



Switching Waveforms with 800mA Load



Transient Response with 400mA to 800mA Load Step

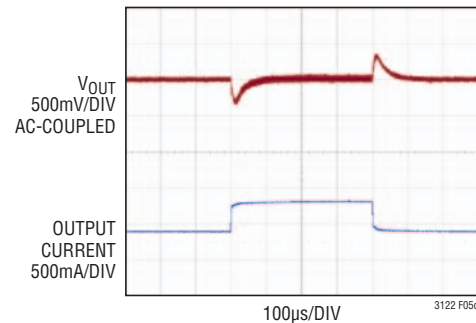


Figure 5. 1MHz, 5V to 12V, 800mA Boost Converter

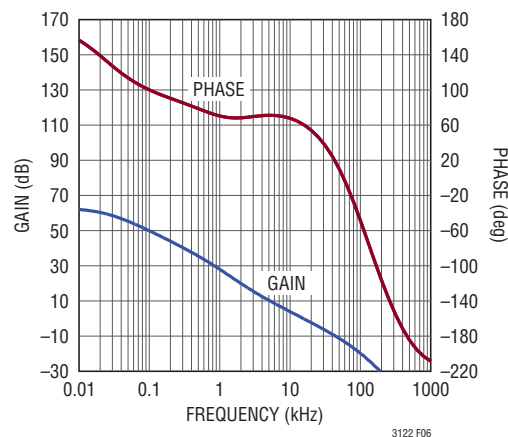


Figure 6. Bode Plot for Example Converter

## APPLICATIONS INFORMATION

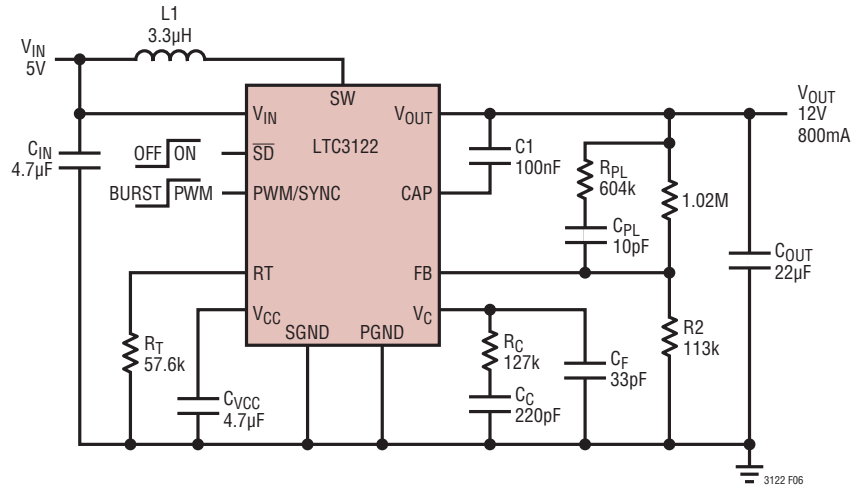


Figure 7. Boost Converter with Phase Lead

The circuit in Figure 7 shows the same application as that in Figure 5 with Type III compensation. This is accomplished by adding  $C_{PL}$  and  $R_{PL}$  and adjusting  $C_C$ ,  $C_F$ , and  $R_C$  accordingly. Table 4 shows the parameters used to generate the bode plot shown in Figure 8.

From Figure 8, the phase margin is still optimized at  $60^\circ$  and the crossover frequency remains 15kHz. Adding  $C_{PL}$  and  $R_{PL}$  provides some feedforward signal in Burst Mode operation, leading to lower output voltage ripple.

Table 4. Bode Plot Parameters for Type III Compensation

| PARAMETER | VALUE | UNITS      | COMMENT      |
|-----------|-------|------------|--------------|
| $V_{IN}$  | 5     | V          | App Specific |
| $V_{OUT}$ | 12    | V          | App Specific |
| $R_L$     | 15    | $\Omega$   | App Specific |
| $C_{OUT}$ | 22    | $\mu F$    | App Specific |
| $R_{ESR}$ | 5     | m $\Omega$ | App Specific |
| $L$       | 3.3   | $\mu H$    | App Specific |
| $f_{OSC}$ | 1     | MHz        | Adjustable   |
| $R_1$     | 113   | k $\Omega$ | Adjustable   |
| $R_2$     | 1020  | k $\Omega$ | Adjustable   |
| $g_{ma}$  | 95    | $\mu S$    | Fixed        |
| $R_O$     | 10    | M $\Omega$ | Fixed        |
| $g_{mp}$  | 3.4   | S          | Fixed        |
| $\eta$    | 80    | %          | App Specific |
| $R_C$     | 127   | k $\Omega$ | Adjustable   |
| $C_C$     | 220   | pF         | Adjustable   |
| $C_F$     | 33    | pF         | Adjustable   |
| $R_{PL}$  | 604   | k $\Omega$ | Adjustable   |
| $C_{PL}$  | 10    | pF         | Adjustable   |

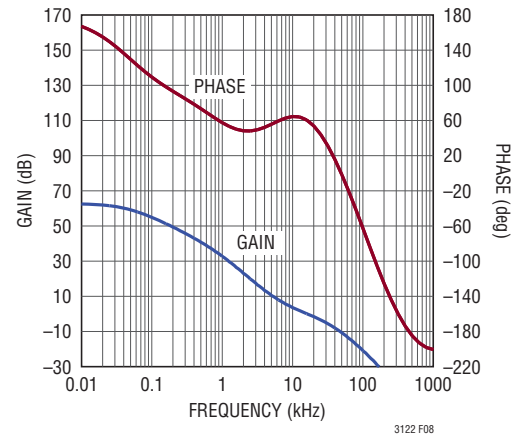
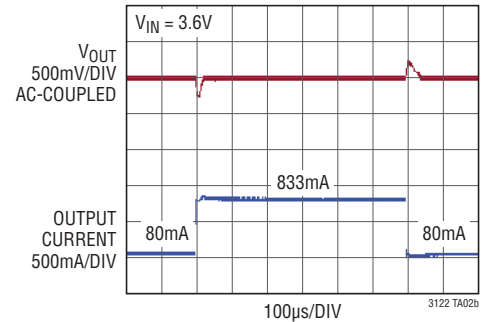
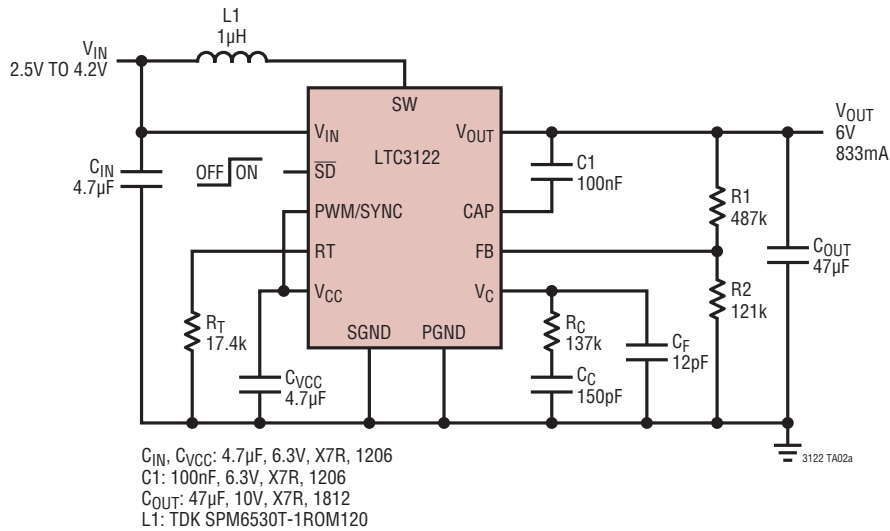


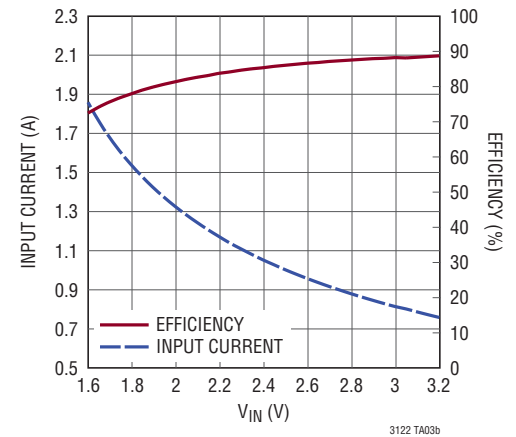
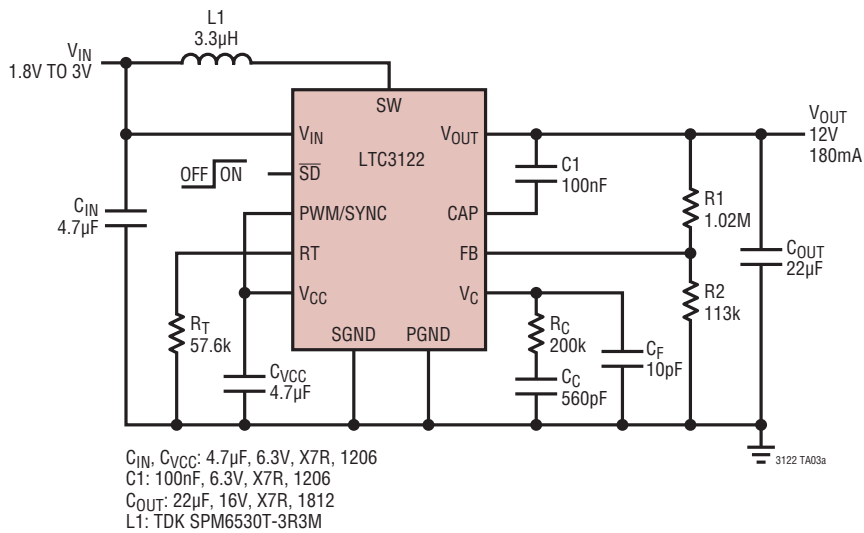
Figure 8. Bode Plot Showing Phase Lead

## TYPICAL APPLICATIONS

## Single Li-Cell to 6V, 5W, 3MHz Synchronous Boost Converter for RF Transmitter

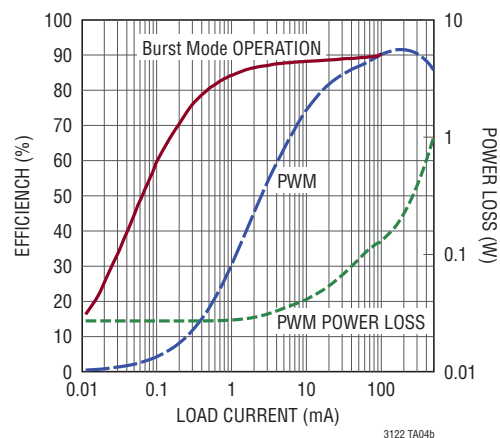
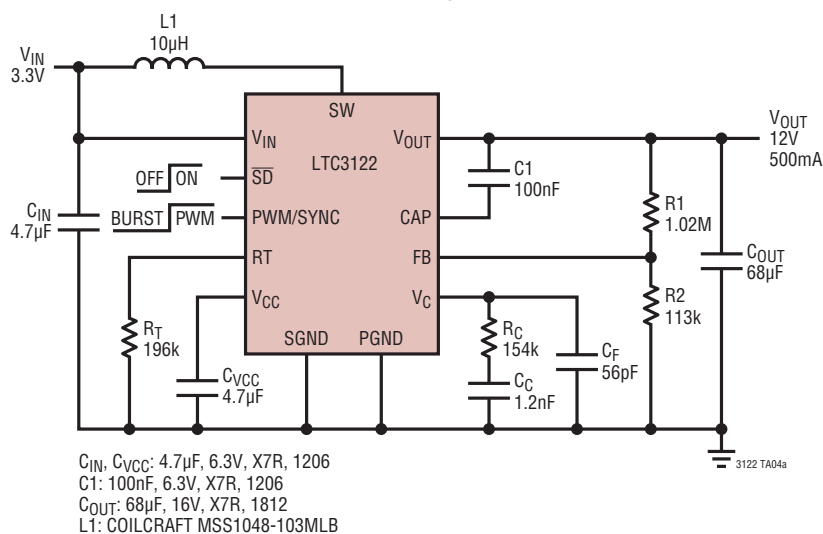


## 2 AA Cell to 12V Synchronous Boost Converter, 180mA

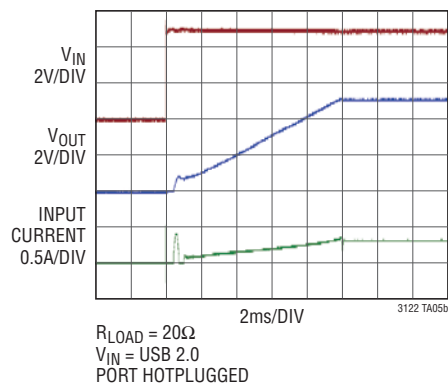
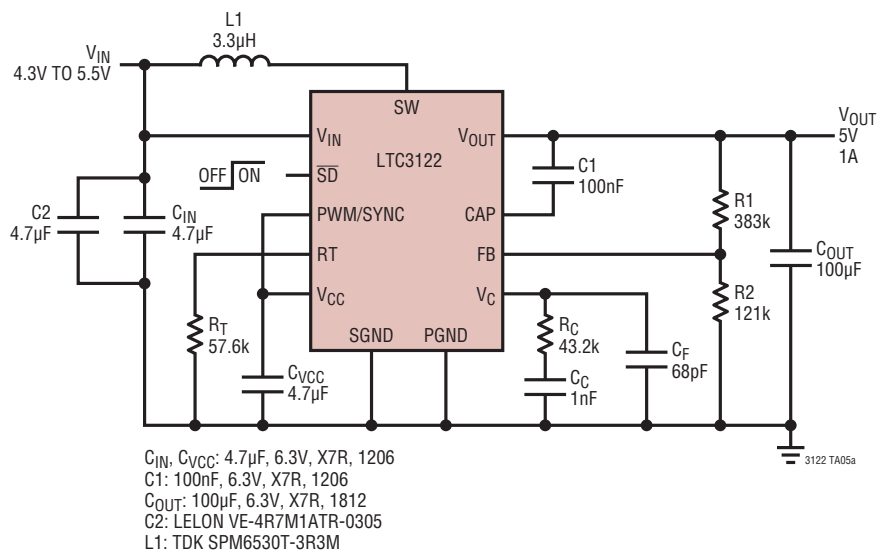


## TYPICAL APPLICATIONS

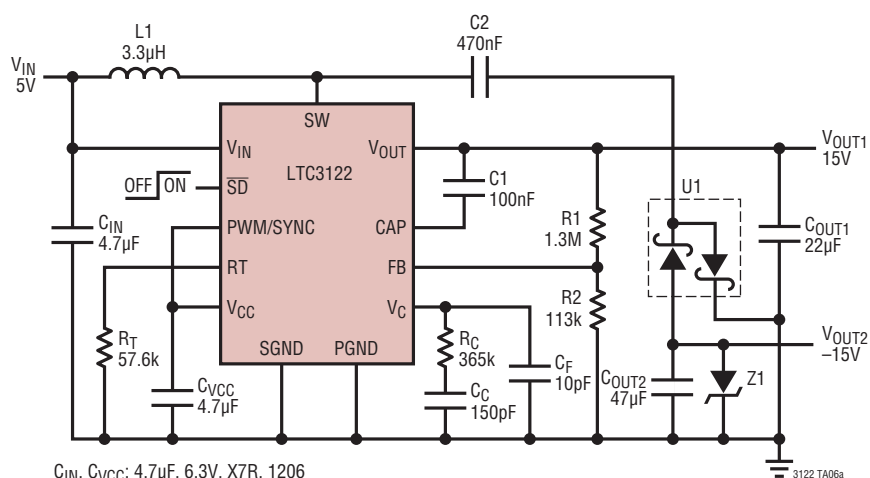
### 3.3V to 12V, 300kHz Synchronous Boost Converter with Output Disconnect, 500mA



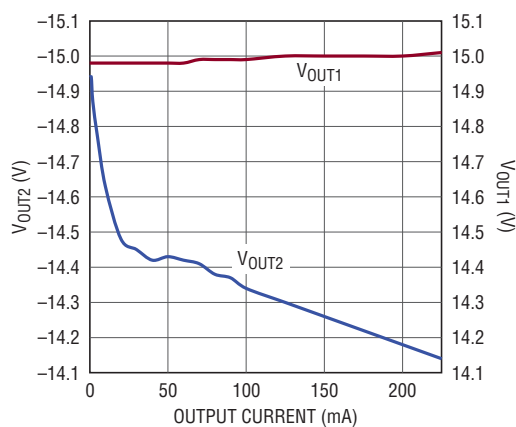
### USB/Battery Powered Synchronous Boost Converter, 4.3V to 5V, 1A



## TYPICAL APPLICATIONS

5V to Dual Output Synchronous Boost Converter,  $\pm 15V$ 

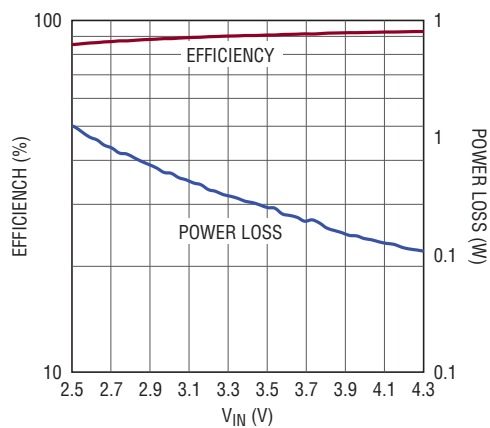
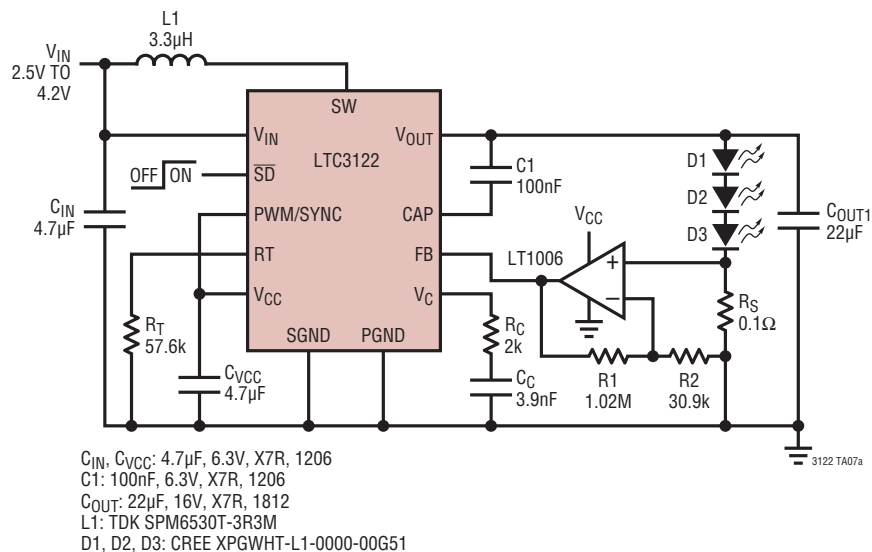
$C_{IN}$ ,  $C_{VCC}$ : 4.7µF, 6.3V, X7R, 1206  
 $C_{OUT2}$ : 47µF, 16V, X7R, 1206  
 $C1$ : 100nF, 6.3V, X7R, 1206  
 $C_{OUT1}$ : 22µF, 16V, X7R, 1812  
 $C2$ : 470nF, 25V, X7R, 1206  
 $L1$ : TDK SPM6530T-3R3M  
 $U1$ : CENTRAL SEMICONDUCTOR CBAT54S  
 $Z1$ : DIODES, INC. DDZ16ASF-7



3122 TA06b

## TYPICAL APPLICATIONS

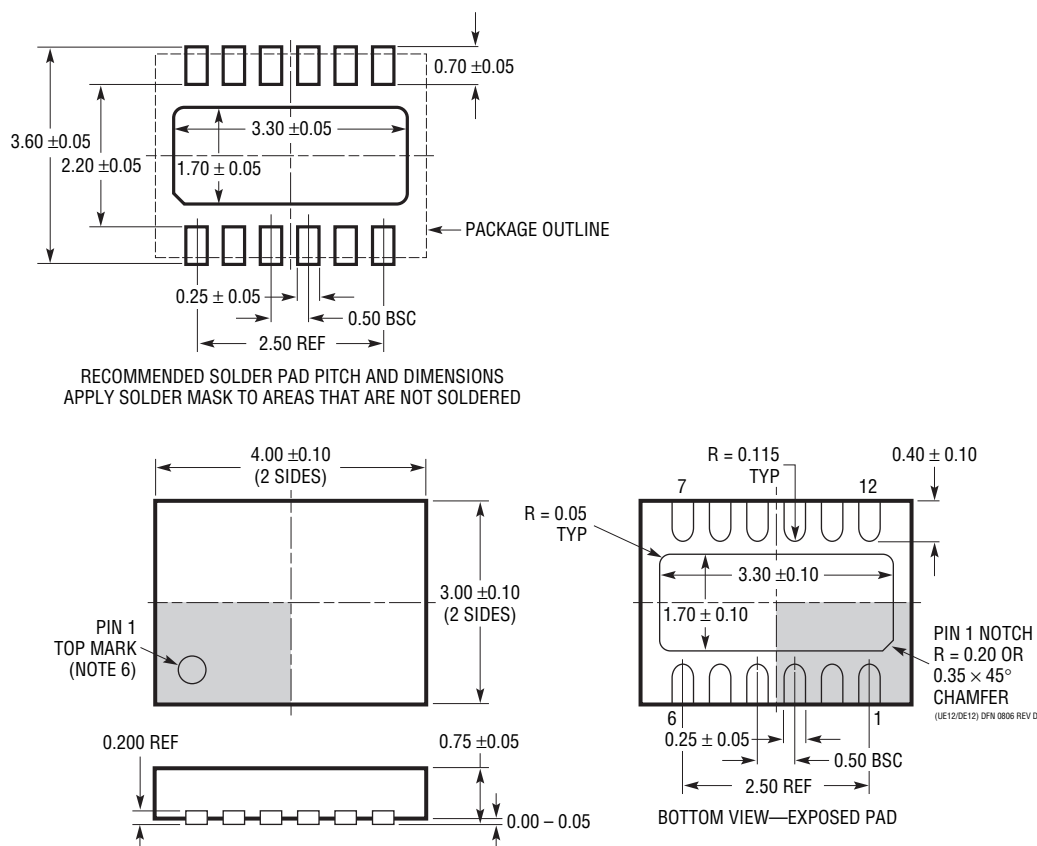
## Single Li-Cell 3-LED Driver, 2.5V/4.2V to 350mA



## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

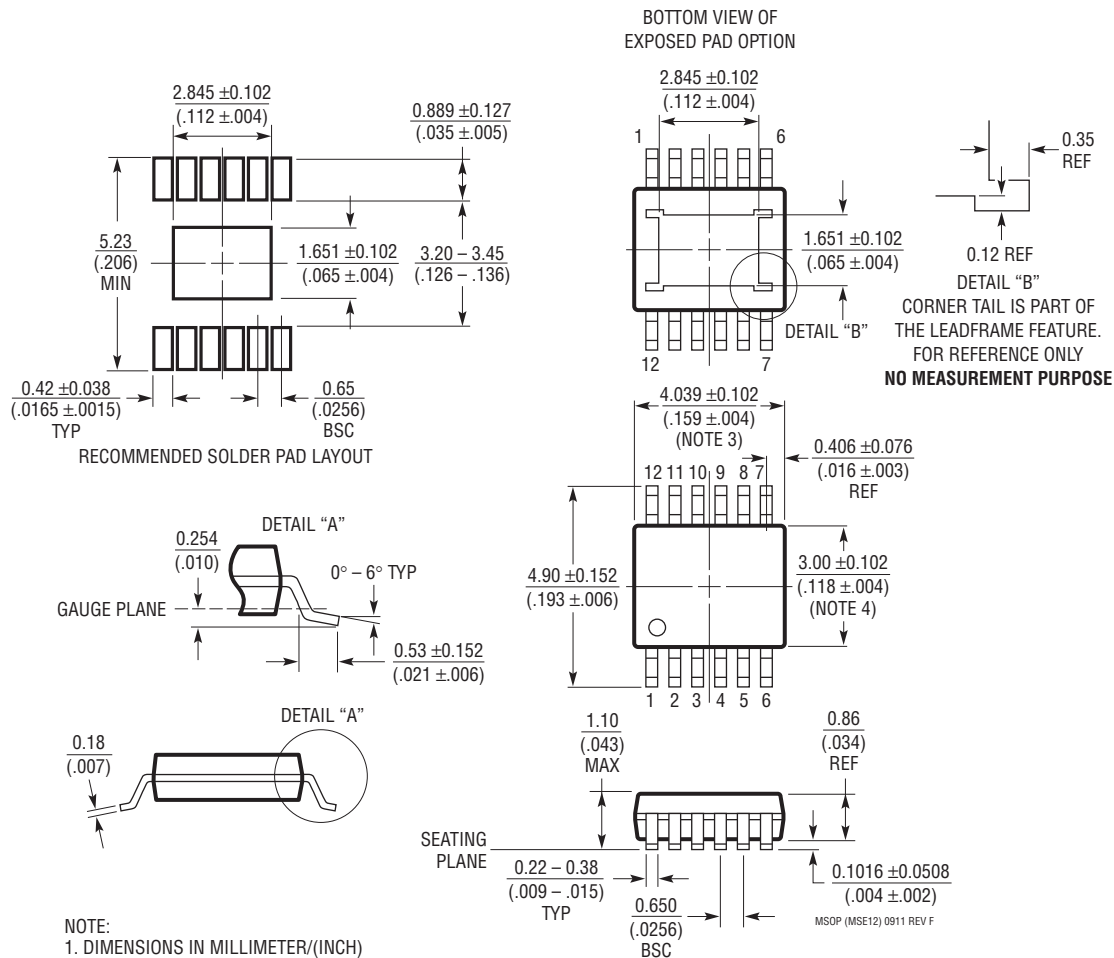
**DE/UE Package**  
**12-Lead Plastic DFN (4mm × 3mm)**  
 (Reference LTC DWG # 05-08-1695 Rev D)



## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

### MSE Package 12-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1666 Rev F)



## REVISION HISTORY

| REV | DATE  | DESCRIPTION                                                                              | PAGE NUMBER |
|-----|-------|------------------------------------------------------------------------------------------|-------------|
| A   | 05/13 | Clarified temperature ranges.                                                            | 2           |
|     |       | Added LTC3122HMSE#PBF to the Order Information.                                          | 2           |
|     |       | Added H-grade to Note 3, clarified N/P channel switch leakage current.                   | 3           |
|     |       | Clarified Load Transient Response graph.                                                 | 4           |
|     |       | Clarified Burst Mode Operation No Load graph.                                            | 5           |
|     |       | Clarified multiple graphs.                                                               | 6           |
|     |       | Clarified SW (Pin 1) description.                                                        | 7           |
|     |       | Clarified the Block Diagram.                                                             | 8           |
|     |       | Clarified Boost Anti-Ringing Control description.                                        | 10          |
|     |       | Clarified Transient Response graph.                                                      | 17          |
|     |       | Clarified components values of Typical Applications, clarified Load Step Response graph. | 19          |
|     |       | Clarified components values of Typical Applications, clarified graphs.                   | 20          |
|     |       | Clarified components values of Typical Applications, clarified graphs.                   | 21          |
|     |       | Clarified components values of Typical Applications, clarified graphs.                   | 24          |

