Z-One™ Digital IBA
No-Bus™ POL Converters
Z-1000 Series

Application Note

TABLE OF CONTENTS

Introduction

This document describes applications of Z-1000 series of No-Bus™ POL converters. It is applicable to the following products: ZY1207, ZY1015, ZY1115, and ZY1120.

1. Reference Documents

ZY1207 Data Sheet
ZY1015 Data Sheet
ZY1115 Data Sheet
ZY1120 Data Sheet
Eutectic Solder Process Application Note
Lead-Free Process Application Note
I/O Filters for Z-One POLs Application Note

2. POL Converter Description

Z-1000 series POL converters are synchronous step-down point-of load regulators. The block-diagram of a Z-1000 series POL converter is shown in Figure 1.

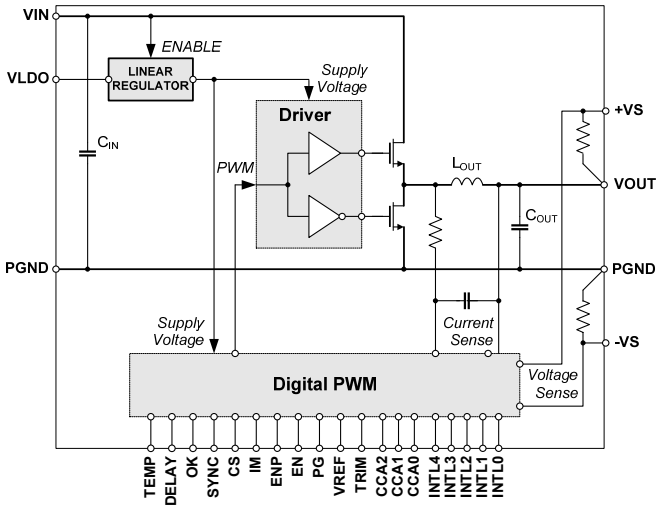

Figure 1. Block-Diagram Of POL Converter

The POL converter includes both input and output capacitance sufficient for normal operation. Additional filter capacitance may be required for further noise reduction and stable operation when a POL converter is powered from high impedance sources.

Control of the POL converter is performed by the digital PWM IC. The digital PWM manages the driver which switches the output FETs. Both the PWM and the driver are powered by the linear regulator that can be connected to the input voltage or an auxiliary power supply. The enable input of the linear regulator is connected to the input voltage to provide guaranteed input UVLO protection.

The POL converter features differential voltage sense. The output current is sensed as the voltage drop across the ESR of the output inductor.

3. Pin and Feature Description

3.1 VLDO, Low Voltage Dropout

Input of the internal linear regulator. Regardless of the input voltage, the V_{VLDO} pin always needs to be greater than 4.75V for normal operation of the POL converter.

3.2 IM, Interleave Mode

Input with an internal pull-up resistor. When the pin is left floating, the phase lag of the POL converter is set by INTL0…INTL4 pins. If the pin is pulled low, the phase lag is set to 0°. Pulling all INTL pins and the IM pin low configures a POL converter as a master. The master determines the clock on the SYNC line.

3.3 TEMP, Temperature Measurement

Voltage output of the internal temperature sensor measuring the junction temperature of the controller IC. The voltage range from 0.2 to 2.0V corresponds to the temperature range from -40°C to 140°C.

3.4 ENP, Enable Polarity

Input with an internal pull-up resistor. When the ENP pin is pulled low, the polarity of the EN input is inverted.

3.5 DELAY, Power-up Delay

Input of the POR circuit with an internal pull-up resistor. By connecting a capacitor between the pin and PGND, a power-up delay can be programmed.

3.6 CCA[0:2], Compensation Coefficient Address

Inputs with internal pull-ups to select one of 7 sets of digital filter coefficients.

3.7 VREF, Voltage Reference

Output of the 2V internal voltage reference that is used to program the output voltage of the POL converter.

3.8 EN, Enable

Input with an internal pull-up resistor. The POL

converter is turned off, when the pin is pulled low (see ENP to inverse polarity).

3.9 OK, Fault Status

Open drain input/output with an internal pull-up resistor. The POL converter pulls the OK pin low, if a fault occurs. Pulling low the OK input by an external circuitry turns off the POL converter.

3.10 SYNC, Frequency Synchronization Line

Bidirectional input/output with an internal pull-up resistor. If the POL converter is configured as a master, the SYNC line propagates a clock to other POL converters. If the POL converter is configured as a slave, the internal clock recovery circuit synchronizes the POL converter to the clock of the SYNC line.

3.11 PG, Power Good

Open drain input/output with an internal pull-up resistor. The pin is pulled low by the POL converter, if the output voltage is outside of the window defined by the Power Good High and Low thresholds.

3.12 TRIM, Output Voltage Trim

Input of the TRIM comparator for the output voltage programming.

3.13 CS, Current Share/Sense Bus

Open drain digital input/output with an internal pull-up resistor. The duty cycle of the digital signal is proportional to the output current of the POL converter.

3.14 INTL[4:0], Interleave Bits

Inputs with internal pull-up resistors. The encoded number determines the phase lag of the POL converter, if its IM pin is left floating.

3.15 –VS and +VS

The differential voltage input of the POL converter feedback loop.

3.16 VIN

Input voltage.

3.17 VOUT

Output voltage.

3.18 PGND

Power ground. Common for VIN and VOUT.

4. Application Information

4.1 Output Voltage Trim

4.1.1 Trim Resistor

The output voltage can be programmed by a single resistor connected between the VREF and TRIM pins. The resistance of the trim resistor can be determined from the equation below:

$$R_{TRIM} = \frac{20 \times (5.5 - V_{OUT})}{V_{OUT}},\ \text{k}\Omega$$

where V_{OUT} is the desired output voltage in Volts.

Tolerance of the R_{TRIM} needs to be 0.1% to obtain the output voltage setpoint accuracy specified in POL converters data sheets.

If the R_{TRIM} is open or the TRIM pin is shorted to PGND, V_{OUT} will be set to 0.5V. If the R_{TRIM} is shorted, V_{OUT} will be 5.5V.

4.1.2 Trim Voltage

The output voltage of the POL converter can also be programmed with an external voltage source applied directly to the TRIM pin. The feature makes the POL converter compatible with a variety of power management margining controllers. In this case, the output voltage is determined by the following equation:

$$V_{OUT} = 2.75 \times V_{TRIM},\ \text{V}$$

V_{TRIM} shall never exceed 2.0V and the source driving V_{TRIM} shall have an output impedance not greater than 20Ω. For a V_{TRIM} from 0 to 0.18V V_{OUT} will be set to 0.5V. The output voltage setpoint accuracy specified in the data sheets is not guaranteed, when V_{OUT} is set by V_{TRIM} unless V_{TRIM} is generated by dividing down V_{REF}.

Note, that V_{TRIM} can only be used to determine the static output voltage setpoint and cannot be used for the slew rate control. Rising and falling slew rates for all voltage transitions are internally set at 0.1V/ms and -0.5V/ms respectively and always override externally programmed slew rates as shown in Figure 2 and Figure 3.

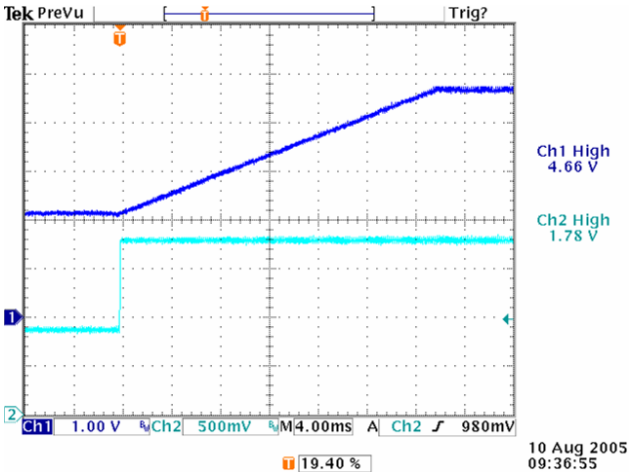

Figure 2. Trim Up Transition. Ch1 – Vout, Ch2 – Vtrim

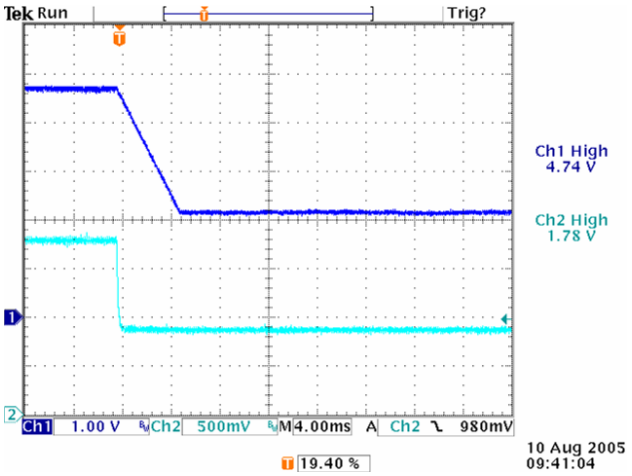

Figure 3. Trim Down Transition. Ch1 – Vout, Ch2 – Vtrim

4.1.3 Margining

Margining can be implemented either by changing the trim voltage as described in the previous paragraph or by changing the resistance between the REF and TRIM pins.

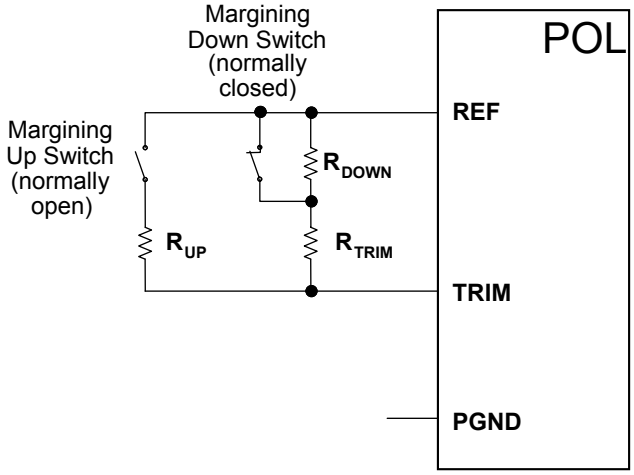

Figure 4. Margining Configuration

In the schematic shown in Figure 4, the nominal output voltage is set with the trim resistor R_{TRIM} calculated from the equation in the paragraph 4.1.1. Resistors R_{UP} and R_{DOWN} are added to margin the output voltage up and down respectively and determined from the equations below.

$$R_{UP} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{5 \times R_{TRIM} - \Delta V\%}{\Delta V\%} \right), \text{ k}\Omega$$

$$R_{DOWN} = (20 + R_{TRIM}) \times \left(\frac{\Delta V\%}{100 - \Delta V\%} \right), \text{ k}\Omega$$

where R_{TRIM} is the value of the trim resistor in kΩ and ΔV% is the absolute value of desired margining expressed in percents of the nominal output voltage.

During normal operation the resistors are removed from the circuit by the switches. The "Margining Down" switch is normally closed shorting the resistor R_{DOWN} while the "Margining Up" switch is normally open disconnecting the resistor R_{UP}.

The switches can be implemented with small-signal FETs or inexpensive analog switches available from a variety of semiconductor manufacturers. For example, a 5Ω dual switch in SO-8 package is available from both Texas Instruments (p/n SN74CBT3306) and Fairchild Semiconductor (p/n FST3306).

An alternative configuration of the margining circuit is shown in Figure 5. In this configuration both

switches are normally open that may be advantageous in some implementations.

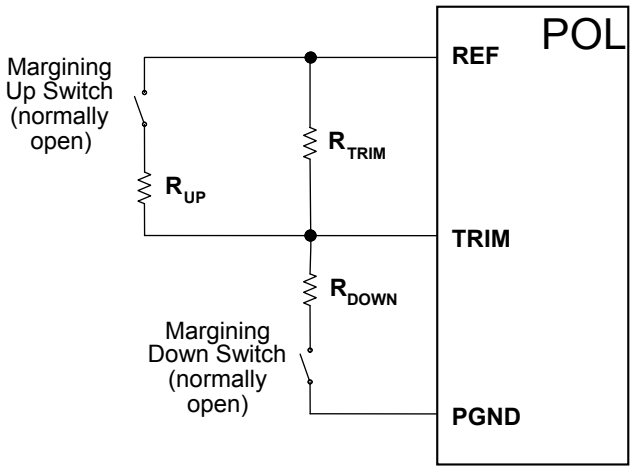

Figure 5. Alternative Margining Configuration

R_{UP} and R_{DOWN} for this configuration are determined from the following equations:

$$R_{UP} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{5 \times R_{TRIM} - \Delta V\%}{\Delta V\%} \right), \text{ k}\Omega$$

$$R_{DOWN} = \frac{20 \times R_{TRIM}}{20 + R_{TRIM}} \times \left(\frac{100 - \Delta V\%}{\Delta V\%} \right), \text{ k}\Omega$$

Caution: Noise injected into the TRIM node may affect accuracy of the output voltage and stability of the POL converter. Always minimize the PCB trace length from the TRIM pin to external components to avoid noise pickup.

4.2 Enable and Enable Polarity

The EN pin is referenced to PGND. If the ENP pin is left floating, then pulling low the EN pin will disable the POL converter. If the ENP pin is connected to PGND, then pulling low the EN pin will enable the POL converter. A summary of EN and ENP combinations is shown in Table 1.

Table 1. EN and ENP Combinations

ENP	EN	POL Converter State
OPEN	OPEN	ON
OPEN	PGND	OFF
PGND	OPEN	OFF
PGND	PGND	ON

An open collector switch is recommended to control the voltage between the EN pin and the PGND pin. The EN pin is pulled up to 3.3V internally, so no external voltage source is required. To prevent damage to the POL converter, the users should avoid connecting a resistor between the EN pin and the VIN pin or applying an external voltage higher than 3.3V to the EN and ENP pins

4.3 Sequencing and Tracking

The POL converter features guaranteed rising and falling output voltage slew rates, turn-on and turn-off delays, and programmable power-up delay

4.3.1 Rising and Falling Slew Rates

The output voltage tracking is accomplished by internally setting up the rising slew rate of the output voltage to 0.1V/ms and falling slew rate to -0.5V/ms. To achieve the slew rates, the output voltage is being changed in 12.5mV steps where duration of each step determines the slew rate. For example, ramping up to a 1.0V output will require 80 steps with the duration of 125µs for each step.

The duration of each voltage step is calculated by dividing the master clock frequency generated by the master POL. Since all POL converters in a system are synchronized to the master clock, the matching between voltage slew rates of different outputs is very accurate as shown in Figure 6 and Figure 7.

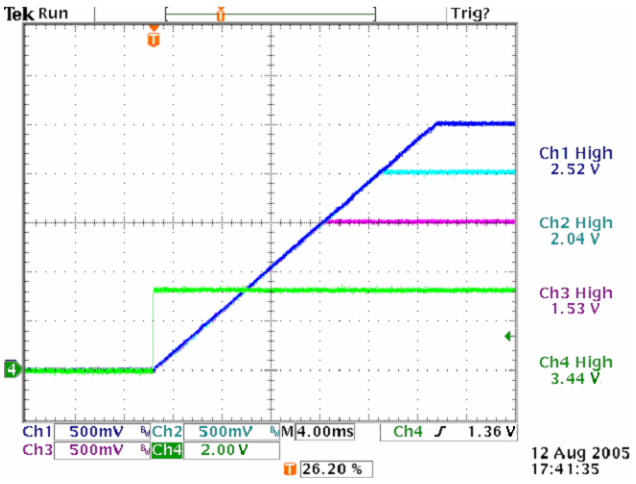

Figure 6. Turn-On Process In Multi-Ouput System. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – EN pin

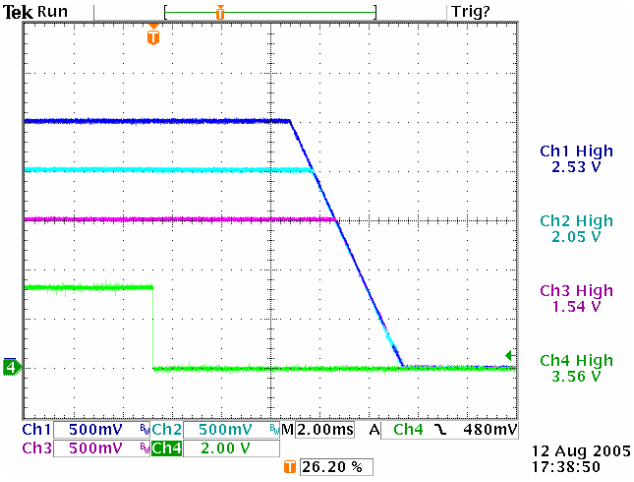

Figure 7. Turn-Off Process In Multi-Output System. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – EN pin

Turn-on tracking is guaranteed both when POL converters are turned ON via the Enable signal (Figure 6) and by application of the input voltage (Figure 8) if OK pins of POL converters are interconnected.

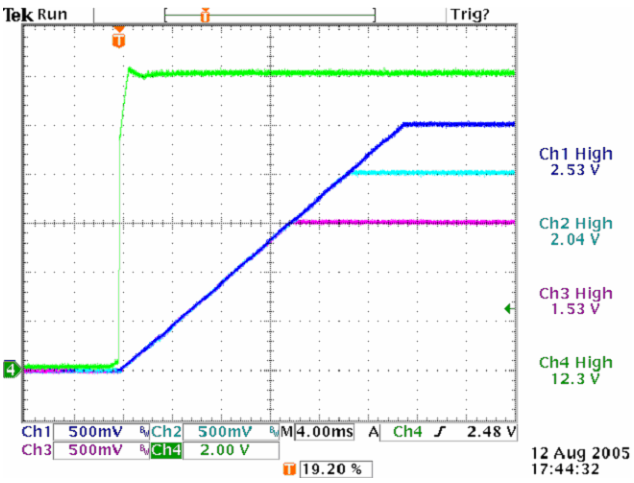

Figure 8. Turn-On Process In Multi-Ouput System. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – Vin

During the turn-on process, a POL converter not only delivers the current required by the load (I_{LOAD}), but also charges the load capacitance. The charging current can be determined from the equation below:

$$I_{CHG} = 10^{-4} \times C_{LOAD}\ , \text{A}$$

Where, C_{LOAD} is the load capacitance in µF, and I_{CHG} is the charging current in Amps.

When selecting the capacitive load, the user needs to ensure that:

$$I_{LOAD} + I_{CHG} < I_{OCP}\ ,$$

where I_{OCP} is the overcurrent protection threshold of the POL converter. If the condition is not met, then the overcurrent protection will be triggered during the turn-on process. To avoid this, the external capacitive load should be reduced until the condition above is met.

Turn-off tracking and delays are guaranteed when POL converters are turned of via the Enable signal (Figure 7). When the input voltage is removed, the outputs will decay as a function of the load as soon as the input voltage drops below the UVLO threshold as shown in Figure 9.

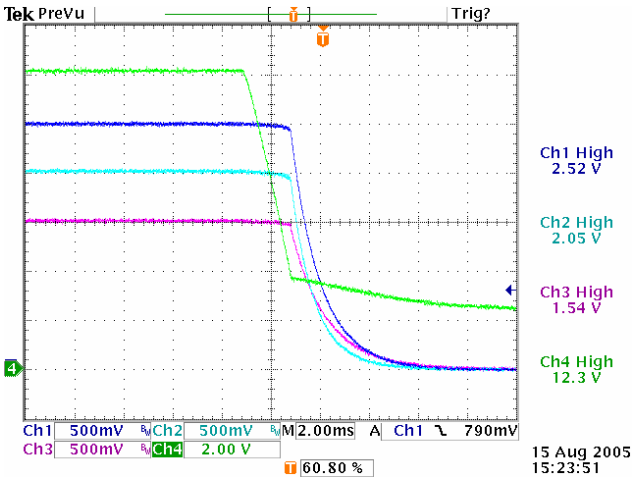

Figure 9. Turn-Off Process In Multi-Ouput System. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – Vin

4.3.2 Turn-On Delay

Turn-on delay is defined as an interval between the instant the EN pin changes to its ON state and the output voltage starts ramping up.

The turn-on delay is guaranteed by design. The duration of the turn-on delay is 0ms as shown in Figure 6.

4.3.3 Turn-Off Delay

Turn-off delay is defined as an interval between the instant the EN pin changes to its OFF state and the output voltage reaches zero.

The turn-off delay is guaranteed by design. The value of the turn-off delay is 11ms and it includes the ramp-down time as shown in Figure 10.

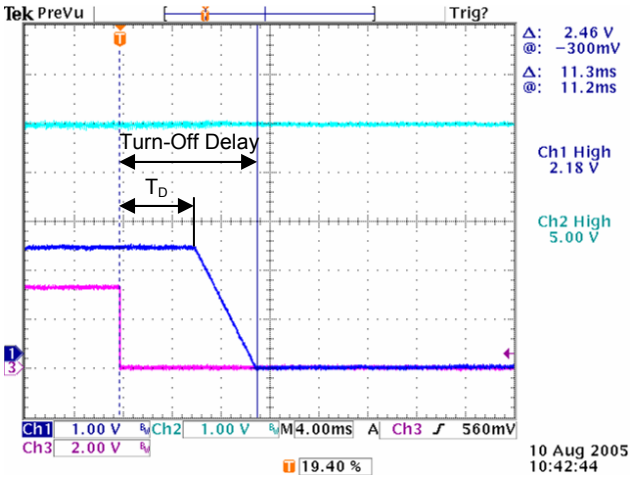

Figure 10. Turn-Off via Enable. Ch1 – Vout, Ch2 – Vin, Ch3 – EN pin

As it can be seen from the figure, the internally calculated delay T_D is determined by the equation below.

$$T_D = 11 - 2 \times V_{OUT}\text{, ms}$$

The ability of the POL converters to automatically adjust T_D as a function of the output voltage allows achieving tracking during turn-off of multiple POL converters as shown in Figure 7.

4.3.4 Power-Up Delay

In case when a POL converter is permanently enabled (for example both ENP and EN are left floating) the user can program the power-up delay. The power-up delay is defined as an interval between the instant when the input voltage reaches the UVLO threshold and the output voltage starts ramping up.

The default value of the power-up delay is 0ms as shown in Figure 11 and Figure 8.

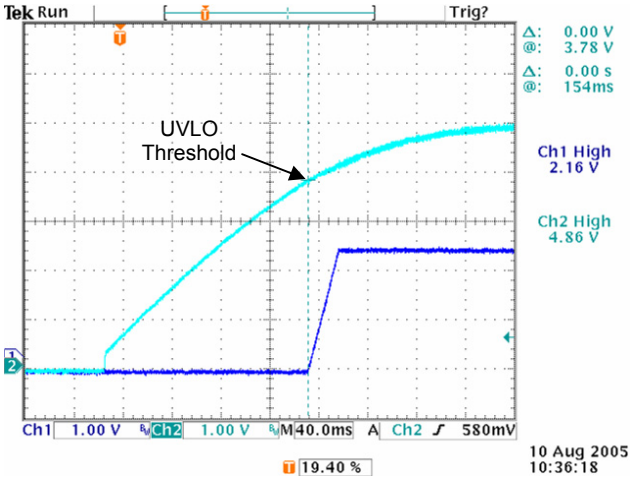

Figure 11. Power-Up, C_{DELAY}=0. Ch1 – Vout, Ch2 – Vin

The power-up delay is programmed by the addition of a capacitor between the DELAY and PGND pins. The relationship between the value of the delay capacitor and the power-up delay is described by the equation below:

$$T_{DELAY\_25C} = (240 + 0.65 \times T) \times C_{DELAY}\text{, ms}$$

where C_{DELAY} is the value of the delay capacitor in µF and T is the temperature of the POL converter at power-up in degree Celsius. Therefore, for example, a 0.47µF capacitor at room temperature will set the power-up delay to approximately 120ms as shown in Figure 12.

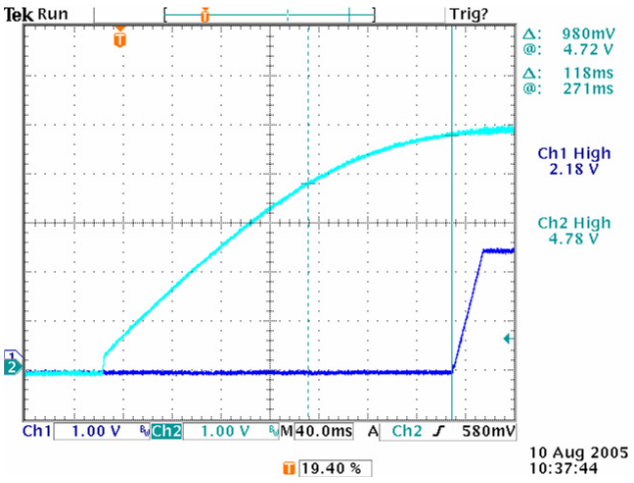

Figure 12. Power-Up, C_{DELAY}=0.47µF. Ch1 – Vout, Ch2 – Vin

As it can be seen from the equation above, the power-up delay decreases at lower temperatures

and increases at higher temperatures assuming the value of C_{DELAY} is independent of the temperature. In reality capacitors show some sort of temperature dependency that needs to be taken into account when the power-up delay is calculated. An example of temperature dependency of the power–up delay is shown in Figure 13.

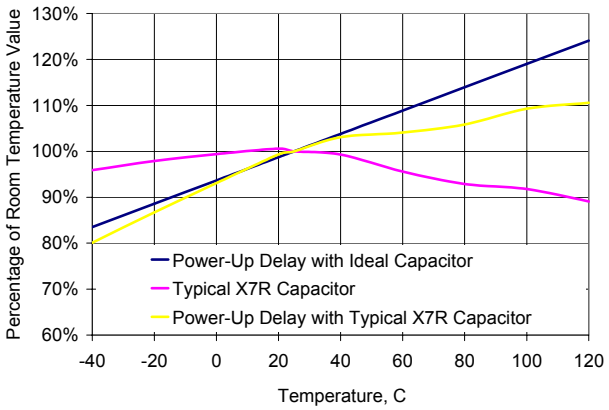

Figure 13. Temperature Dependency Of Power-Up Delay

The value of a typical X7R ceramic capacitor decreases at both temperature extremes. Since the power-up delay has a positive temperature coefficient, using an X7R capacitor actually reduces the power-up delay deviation over temperature. The worst case is the cold start at -40°C where the power-up delay is 20% shorter than its room temperature value. However, the power-up delay exhibits only ±10% deviation over commercial temperature range.

If the same power up delay is required for multiple POL converters (for example POL converters connected in parallel), it is not necessary to connect a delay capacitor to each POL converter. Moreover, such approach may result in a mismatch of power-up delays due to capacitor and POL converter tolerances. The preferred way to ensure that multiple POL converters have the same power-up delay is shown in Figure 14.

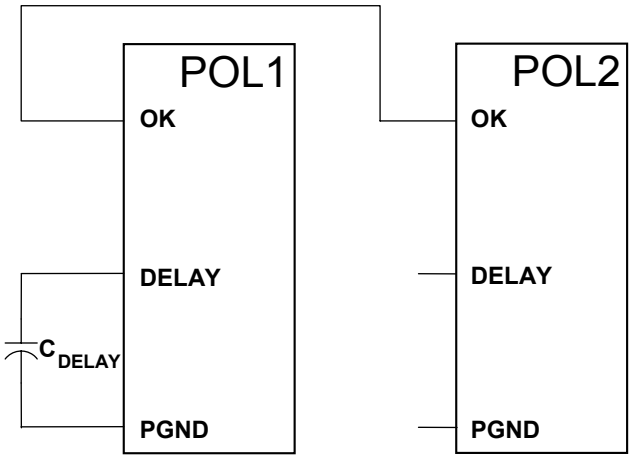

Figure 14. Power-Up Delay Programming For Multiple Converters

In this configuration, only one delay capacitor is used to program the power-up delay for any number of POL converters. All POL converters requiring the same power-up delay are connected via OK pins.

A POL converter is off as long as its OK line is pulled low (either internally or externally). During the power-up, all OK pins are internally pulled low until the input voltage reaches the UVLO threshold. The POL converter with a C_{DELAY} connected to its DELAY pin will continue holding the OK line low after the input voltage reaches the UVLO threshold until the C_{DELAY} is fully charged. At this point, the POL converter will release its OK line enabling all POL converters connected to the OK line.

Note, that the power-up delay does not affect the power-down process. POL converters turn off when the input voltage drops below the UVLO threshold as shown in Figure 15.

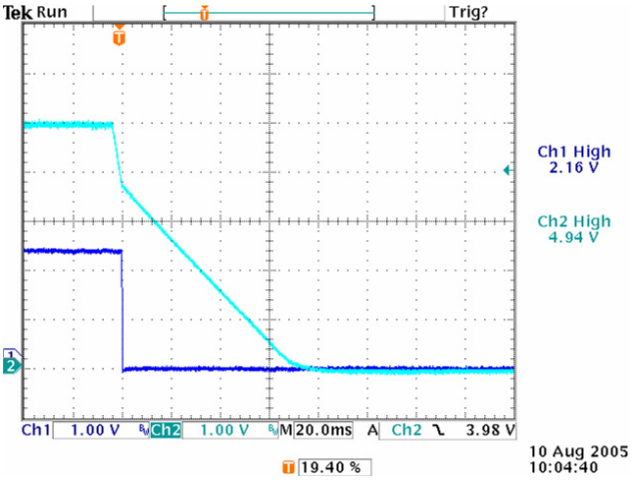

Figure 15. Power-Down Process. Ch1 – Vout, Ch2 – Vin

4.3.5 Cascading

Cascading is a sequential turn-on process when one output is enabled only after a previous output reaches its regulation band.

The POL converters allow cascading by simply interconnecting PGOOD and EN pins without addition of external components as shown in Figure 16.

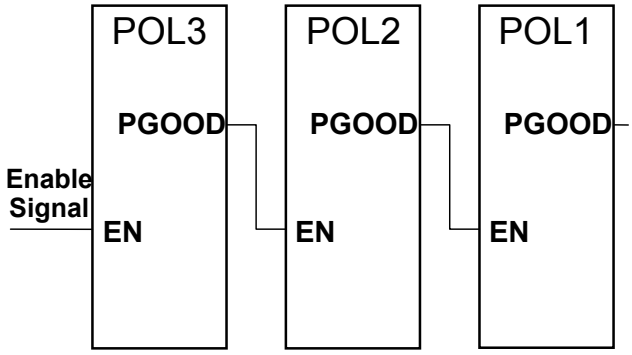

Figure 16. Cascading Configuration

In this configuration, POL3 is controlled via the Enable signal. It will turn on as soon as the EN pin changes to its ON state. POL2 will be enabled when the output of POL3 is in a steady state condition and within the Power Good window (90%-110% of V_{OUT3}). POL1 will be enabled when the output of POL2 is in a steady state condition and within the Power Good thresholds (90%/110% of V_{OUT2}) as shown in Figure 17.

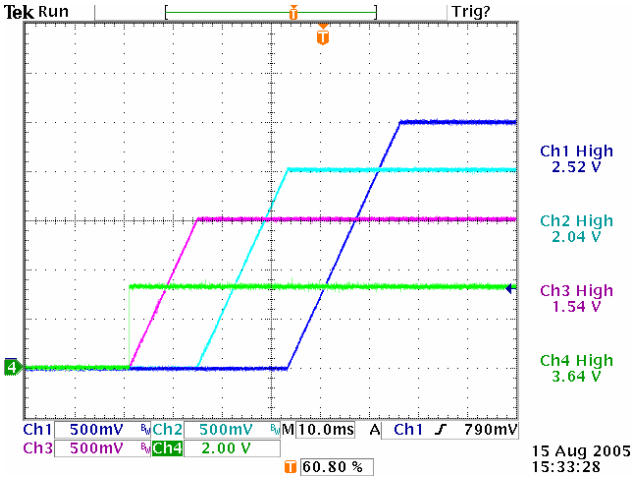

Figure 17. Cascading Turn-On. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – EN pin

Cascading can also be accomplished in a configuration where the Enable signal is not utilized and POL converters turn on as soon as the input voltage is applied as shown in Figure 18

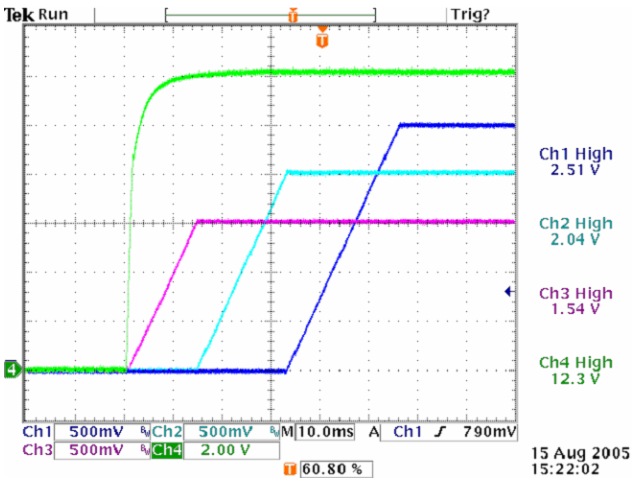

Figure 18. Cascading Turn-On. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – Vin

The turn-off process occurs in the same sequence – POL3 turns off when the EN pin changes state. Once V_{OUT3} starts ramping down, the Power Good is pulled low turning off POL2, and so on as shown in Figure 19.

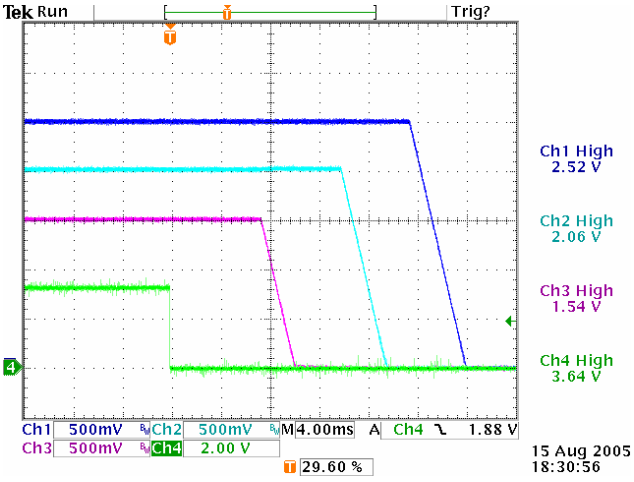

Figure 19. Cascading Turn-Off. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – EN pin

Note that the PGOOD pin of a POL converter is pulled low when the output voltage of the POL converter is ramping up or down. It occurs during turn-on and turn-off as well as during the output voltage adjustment such as margining. The PGOOD pin is pulled low for the duration of the ramping process as shown in Figure 20.

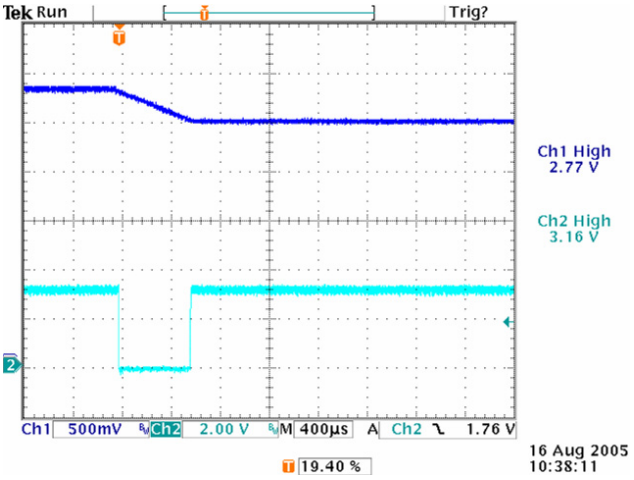

Figure 20. Power Good Is Pulled Low During Voltage Transitions. Ch1 – Vout, Ch2 – PGood pin

If the Power Good signal is used to enable another POL converter as shown in Figure 16, the user must ensure the following condition is met to prevent that the subsequent POL converter turns off:

$$\Delta V_M < 1.1 - 0.2 \times V_{OUT},$$

where, ΔV_M is the absolute value of margining in Volts and V_{OUT} is the output voltage of the POL converter that is being controlled (e.g. POL2 in Figure 16) by the Power Good signal of the POL converter that is being margined (POL3 in Figure 16). If the condition is not met, the output voltage of POL2 will start ramping down during margining of POL3.

In most cases, the condition is easily met. For example, assume the output voltage of POL3 is 1.5V and it is margined by 10%. If the nominal output voltage of POL2 is 2.0V then ΔV_{M3} equals 0.2V which is significantly less than $1.1\text{-}0.2\times V_{OUT2}=0.7V$. The condition is met and margining of POL3 will have no effect on the output of POL2.

4.3.6 Turn-On Into Prebiased Output

A cascaded or sequenced turn-on frequently leads to a prebias – a condition when a POL converter has to turn on into the output that already has some voltage (prebias). This voltage may be caused by clamping diodes connected between different outputs or leakage through parasitics within multivoltage ICs.

The POL converters can turn-on directly into a prebiased output without degradation of performance or changes to the rising slew rate as shown in Figure 21.

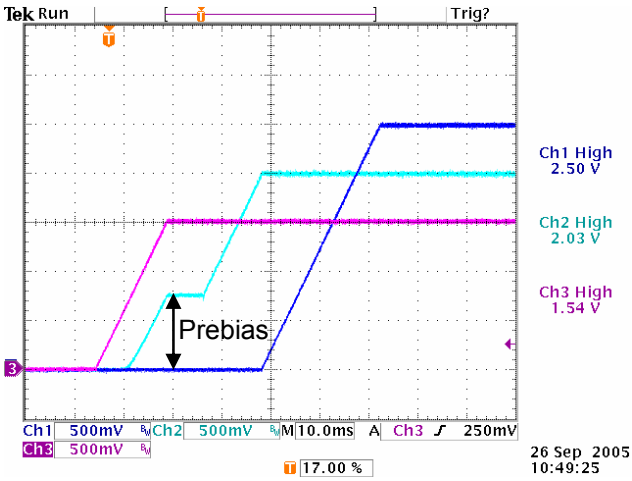

Figure 21. Turn-On Into Prebiased Output

The POL converters do not discharge the prebiased output during the turn-on and can turn-on into the prebias as high as their nominal voltage setpoint.

4.4 Power Good

The Power Good feature is active only when the output voltage is on a steady state level. The PGOOD pin is pulled low during transitions of the output voltage from one level to other as shown in Figure 20 and Figure 23.

When active, the PGOOD is pulled low, if the output voltage is outside of the Power Good window formed by the Power Good Low and Power Good High thresholds. The thresholds are specified in percentages of the output voltage and track the output voltage setpoint.

PGOOD is an open drain output that is pulled up internally to 3.3V. PGOOD pins of different POL converters can be directly interconnected to generate a system Power Good signal. This automatic AND feature ensures that the system Power Good signal is high only when all output voltages are within their respective Power Good windows.

An implementation of the system Power Good with an LED indicator is shown in Figure 22.

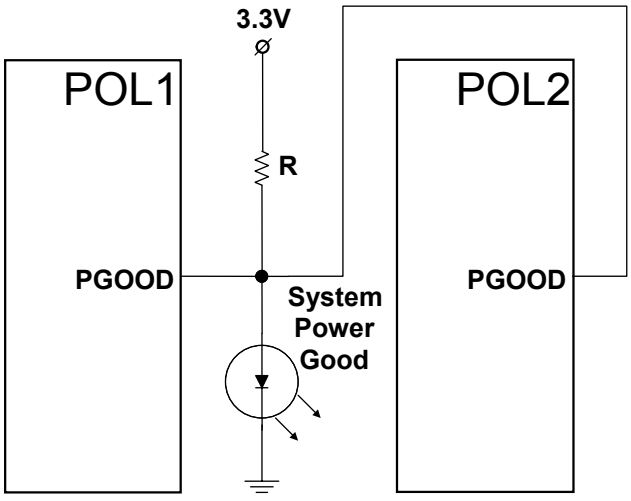

Figure 22. Implementation Of System Power Good Indicator

4.5 Protections

The POL converters have a comprehensive set of protections. The set includes the output over- and undervoltage protections, the overcurrent protection, and the overtemperature protection. All protections turn off the affected POL converter, however certain protections trigger a fast turn-off opening both FETs simultaneously, while others trigger a regular turn-off ramping the output voltage down according to the turn-off delay and falling slew rate specifications. A summary of all protections is shown in Table 2 and Figure 23.

Table 2. Summary Of Protections

Protection	Type	Turn-Off	Low Side FET
OCP	Hiccup	Fast	Off
UVP	Hiccup	Regular	Controlled
OTP	Hiccup	Regular	Controlled
OVP	Latching	Fast	On

Thresholds of the overvoltage and undervoltage protections as well as Power Good limits are set as percentage of the output voltage and track the output voltage setpoint, even if it is changed by the output voltage adjustment or by margining.

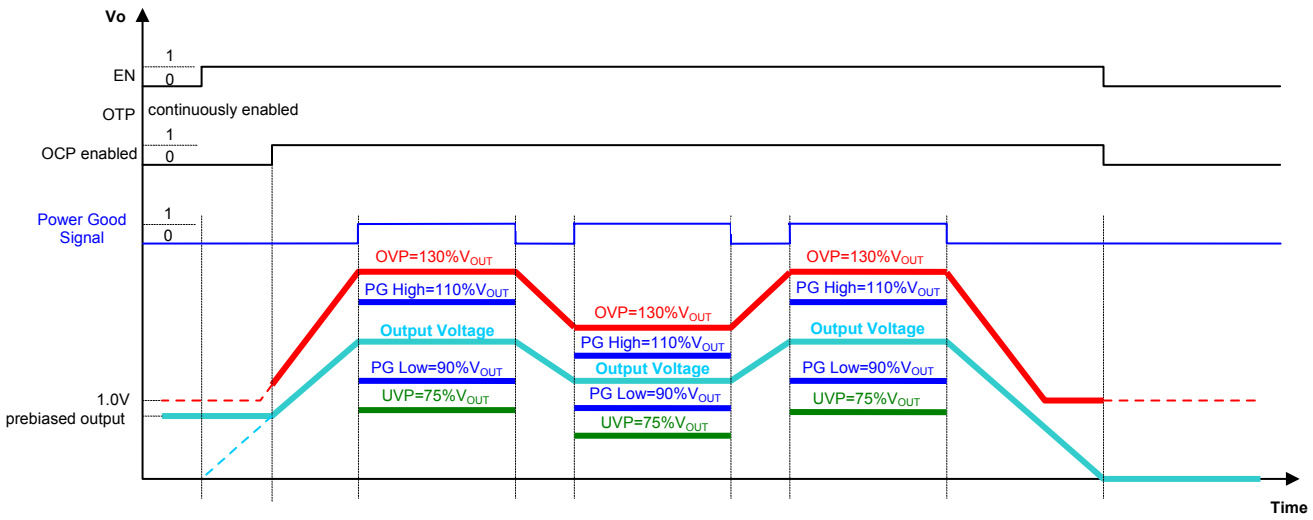

Figure 23. Protections Enable Conditions

4.5.1 Overcurrent Protection (OCP)

OCP is active whenever the output voltage exceeds the prebias voltage (if any). When the output current reaches the OCP threshold, the output voltage will start decreasing. As soon as the output voltage decreases below the undervoltage protection threshold, both high side and low side switches of the POL converter are turned off instantly (fast turn-off).

When the OCP is triggered, the POL converter will attempt to restart every 130ms until the current reduces below the OCP threshold as shown in Figure 24.

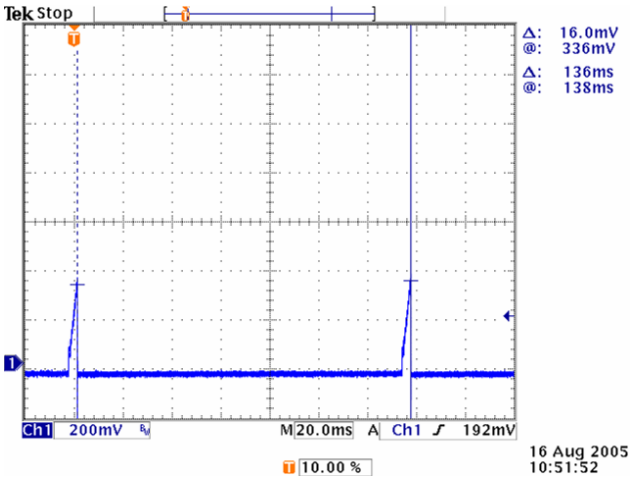

Figure 24. Overcurrent Protection

Temperature compensation is added to keep the OCP threshold approximately constant at temperatures above room temperature.

4.5.2 Undervoltage Protection (UVP)

The UVP is only active during steady state operation of the POL converter to prevent nuisance tripping. If the output voltage decreases below the UVP threshold and there is no OCP fault, the output voltage is ramped down according to sequencing and tracking specifications (regular turn-off).

When the UVP is triggered, the POL converter will attempt to restart every 130ms until the output voltage increases above the UVP threshold. When restarting, the output voltage meets delay and slew rate specifications as shown in Figure 25.

130ms is the interval from the instant when the output voltage has reached zero Volts until the output voltage starts ramping up again.

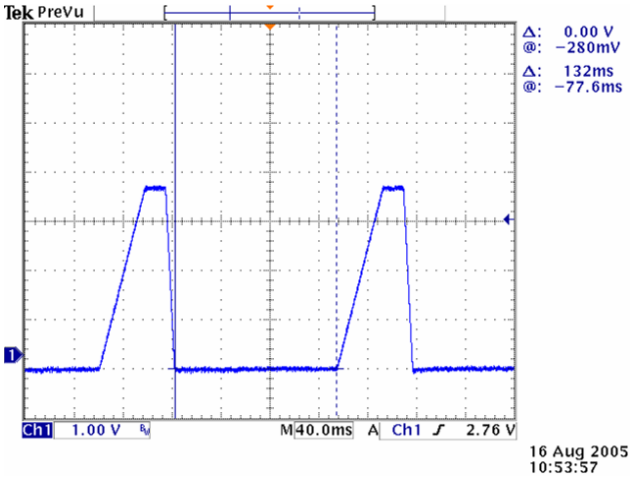

Figure 25. Undervoltage Protection

4.5.3 Overtemperature Protection (OTP)

OTP is active whenever the POL converter is powered up. If the junction temperature of the controller exceeds 120°C, the POL converter turns off. The output voltage is ramped down according to sequencing and tracking specifications (regular turn-off).

When the OTP is triggered, the POL converter will attempt to restart once the junction temperature of the controller has decreased below 110°C, but not earlier than 130ms after its output reached zero volts. When restarting, the output voltage will meet the delay and slew rate specifications as shown in Figure 25.

4.5.4 Overvoltage Protection (OVP)

The OVP is active whenever the output voltage of a POL converter exceeds the pre-bias voltage (if any). If the output voltage exceeds the OVP threshold, the high side switch is turned off instantly, and simultaneously the low side switch is turned on to ensure reliable protection of sensitive loads. The switch provides a low impedance path to quickly dissipate energy stored in the output filter and achieve effective voltage limitation.

When the OVP is triggered, the POL converter will turn off and stay off. The POL can be turned on after 130ms, if the output voltage reduces below the OVP threshold and the EN pin is recycled, or the input voltage is recycled.

4.6 Fault Propagation

The feature adds flexibility to fault management by giving users control over propagation of fault signals within and outside of the system. The propagation means that a fault in one POL converter can turn off other POL converters, even if those are not directly affected by the fault.

The fault propagation is useful for a variety of systems, but is almost always mandatory for the loads that are sensitive to the voltage differential between the outputs such as multivoltage ASICs (core and I/O voltages) or memory with active bus terminators (supply and termination voltages).

The propagation is accomplished by interconnecting OK pins of individual POL converters as shown in Figure 26. If a POL converter has a fault (OCP, UVP, OVP, or OTP), it will pull its OK pin low. The low OK signal initiates regular turn-off of other POL converters connected to the OK line.

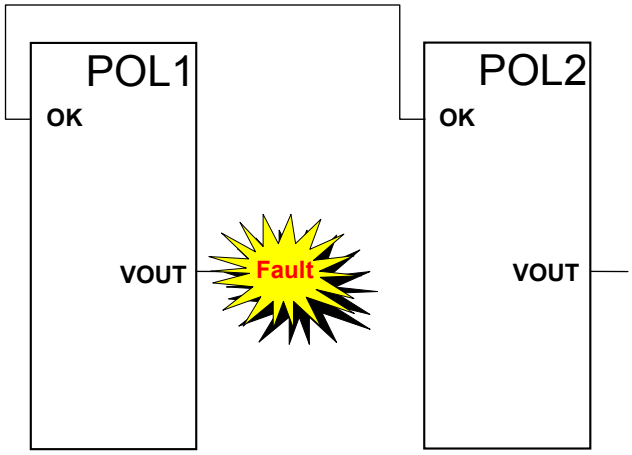

Figure 26. Fault Propagation Configuration

An example of the fault propagation is shown in Figure 27 and Figure 28. In this three-output system, the POL converter powering one of the outputs (Ch 2 in Figure 27) encounters a UVP fault. The POL converter turns off and pulls its OK pin low. If the OK pin is not connected to the OK pins of other POL converters in the system, those POL converters continue operating normally while the faulty converter is trying to restart every 130ms as shown in Figure 27.

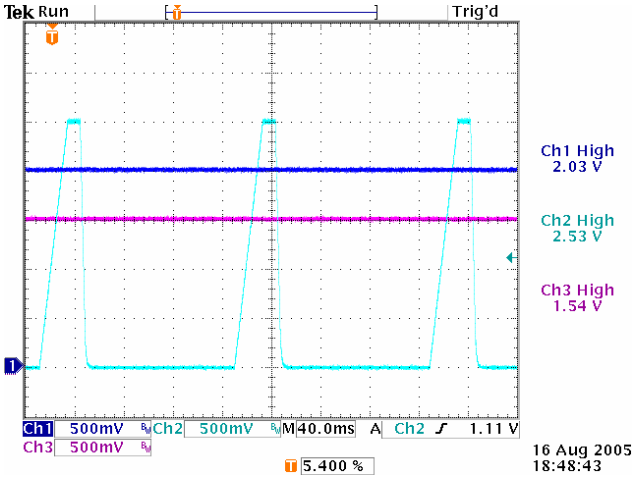

Figure 27. UVP fault on Vout2. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3.

If the OK pins of all POL converters in the system are interconnected, then the fault in one of the POL converters causes simultaneous turn-off of all POL converters in the system. The faulty POL converter controls behavior of other POL converters as shown in Figure 28.

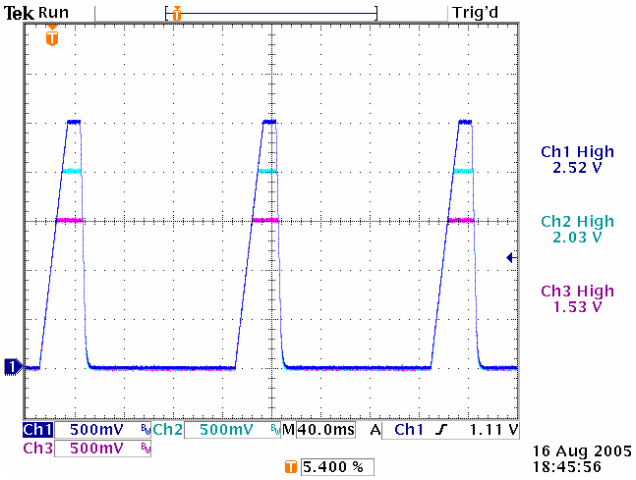

Figure 28. UVP fault on Vout2. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3. OK Pins Of All POL Converters Are Connected Together

4.7 PWM Parameters

The POL converters utilize a digital PWM controller. The controller enables users to manage key PWM performance parameters, such as switching frequency, interleave, and feedback loop compensation.

4.7.1 Switching Frequency Synchronization

It is strongly recommended that POL converters are synchronized to the same switching frequency by interconnecting the SYNC pins as shown in Figure 29. The synchronization frequency can be either generated by a POL converter configured as a master or by an external clock generator. To configure a POL converter as a master, ground its IM pin and INTL0…INTL4 pins. Any POL converter can be configured as a master, but there can be only one master per group of POL converters connected via the SYNC pins. The frequency of the synchronization signal determines switching frequency as well as all timing relationships (delays, slew rates, etc.).

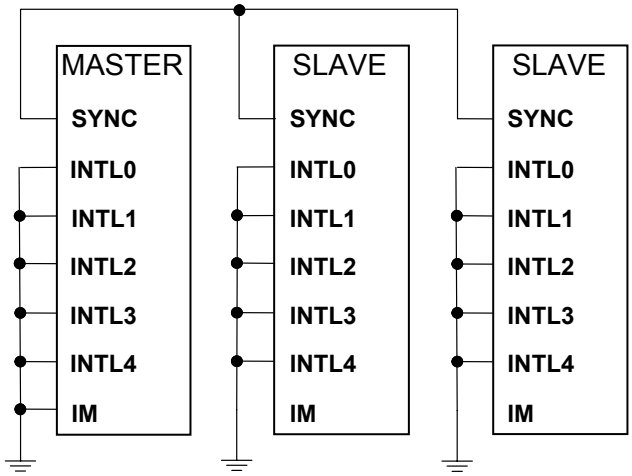

Figure 29. Frequency Synchronization And Interleave

Scope picture of the signal on the SYNC line generated by a master POL converter is shown in Figure 30. The frequency of the signal is 500kHz ± 5% and the SYNC line is internally pulled up to 3.3V. For normal operation, the 10% to 90% rise time measured directly at SYNC pins of all POL converters shall not exceed 300ns. The number of POL converters connected to the same SYNC line is limited only by the rise time and pull-down capability of the SYNC pin. To improve signal integrity, it is allowable to add external pull-ups to a 3.3V source provided the sink current does not exceed specified in the respective POL converter data sheets.

If POL converters are synchronized to an external clock, IM pins of all POL converters should be left open so they operate in the slave mode. An external clock must meet requirements detailed in POL converter data sheets.

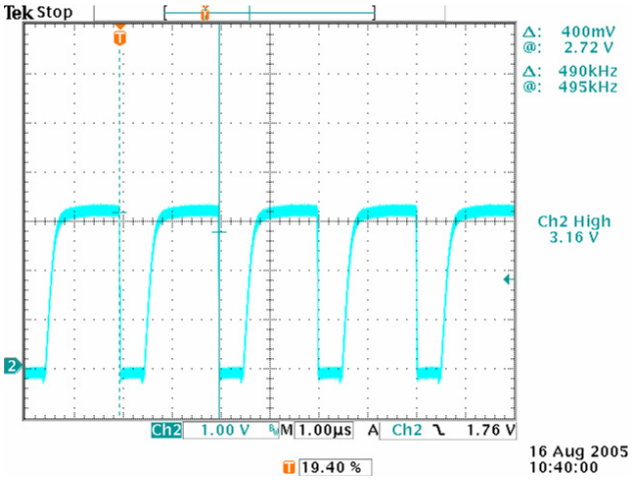

Figure 30. SYNC Line Waveform

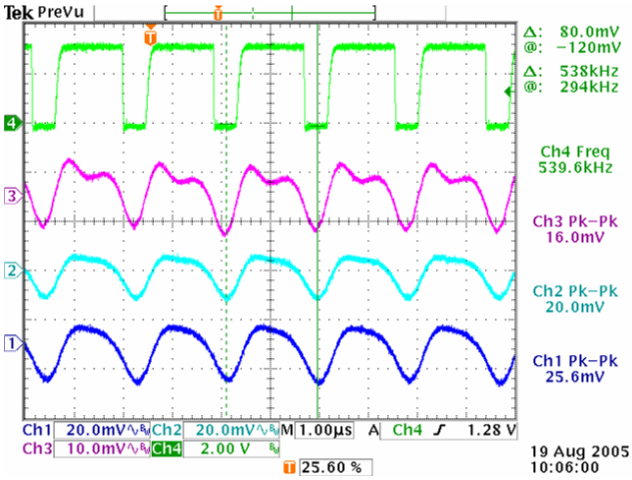

Figure 31. Output Voltage Noise, No Interleave. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – SYNC pin

If a POL converter is used as a single or independent power supply, it should be configured as a master with the IM and all INTL pins connected to the ground. If the IM pin of an independent single POL converter is left floating, the POL converter will remain off until a clock signal is applied to the SYNC pin.

4.7.2 Interleave

The interleave feature allows spreading the switching energy over the entire switching cycle and reducing magnitude of the switching noise. Interleave is defined as a phase lag between the synchronizing slope of the master clock on the SYNC pin and the PWM signal of a POL converter.

The interleave is programmed by INTL0…INTL4 pins. The pins are grounded or left floating forming a binary number that multiplied by 11.25° represents the phase lag of the POL converter. For example, INTL0…INTL3 grounded and INTL4 floating represent binary 10000 or decimal 16. Therefore such INTL pin arrangement will program an interleave of 16x11.25°=180°.

Note:. POL converters based on the 36-pin horizontal mechanical platform (ZY1207 and similar) have only INTL2…INTL4 pins brought out. INTL0 and INTL1 are grounded internally to the POL converter thus limiting the interleave step size to 45°.

All POL converters shown in Figure 29 have an interleave of 0°. They draw current from the input at the same time as shown in Figure 31.

The noise reflected back to the input source in this configuration is a sum of noise generated by each individual POL converter. It results in high magnitude of the fundamental switching frequency noise reflected back to the input source as shown in Figure 32.

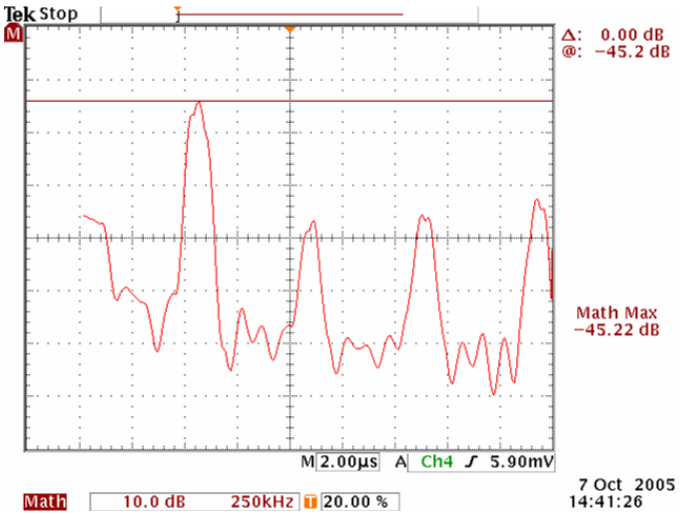

Figure 32. Input Noise Spectrum, No Interleave

The peak can be suppressed with an input filter optimized for 500kHz switching frequency, such as Power-One FC series: http://www.power-one.com/resources/products/appnote/filters_fc_ds.pdf.

Alternatively, the input voltage noise can be reduced by programming interleave as shown in Figure 33.

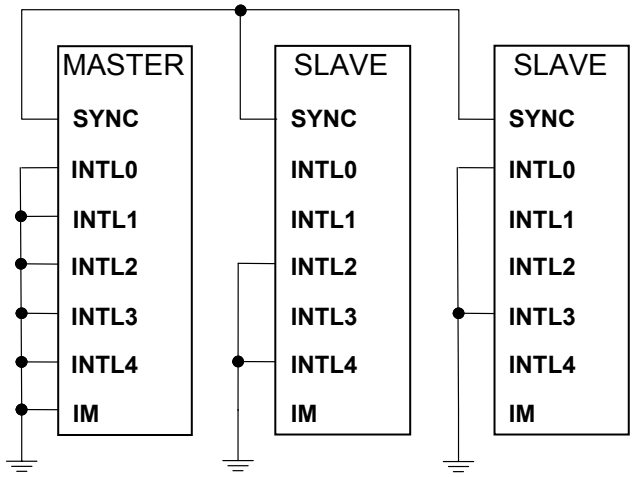

Figure 33. Interleave. Master Has Phase Lag Of 0°, Slaves – 123.75° and 247.5°.

Instead of all three POL converters switching at the same time as in the previous example, the POL converters will switch at 0°, 123.75°, and 247.5° as shown in Figure 34.

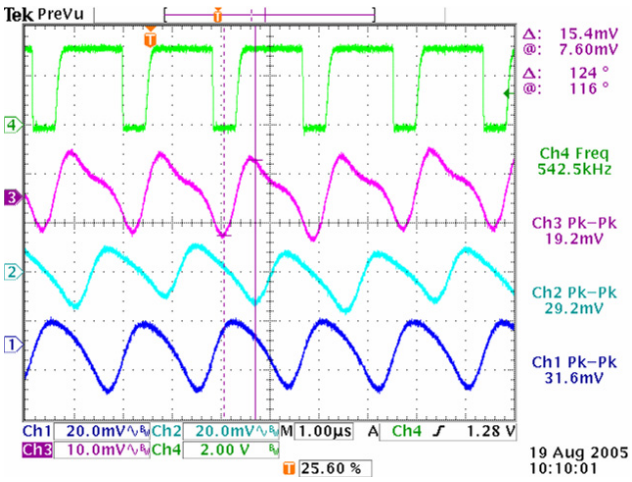

Figure 34. Output Voltage Noise, Interleave. Ch1 – Vout1, Ch2 – Vout2, Ch3 – Vout3, Ch4 – SYNC pin

In this case, the switching energy is spread across the cycle resulting in app. 3dB reduction of the switching frequency peak as shown in Figure 35.

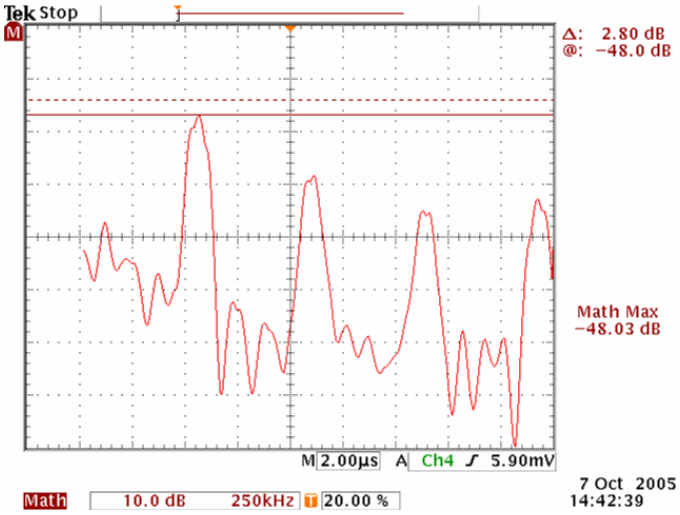

Figure 35. Input Noise Spectrum, Interleave

The interleave feature is similar to that of multiphase converters, however, unlike in the case of multiphase converters, interleave does not have to be equal to 360/N, where N is the number of POL converters in the system. Interleave is independent of the number of POL converters and fully programmable.

If the connection of INTL0…4 pins is changed while the POL converter is operating, the change will not take effect until the input power to the POL converter is recycled or until its DELAY pin is pulled low and released.

4.7.3 Feedback Loop Compensation

The transfer function of a Z-1000 Series No-Bus™ POL converter is shown in Figure 36. It is a third order function with two zeros and three poles.

Positions of poles and zeroes and therefore performance of the POL converter are determined by coefficients of the digital filter. The filter is characterized by four numerator and three denominator coefficients. The coefficients are automatically loaded upon power up of the POL converter.

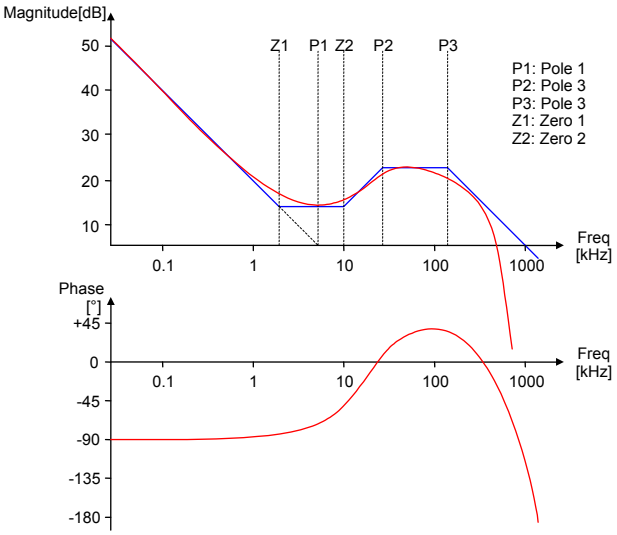

Figure 36. Transfer Function of PWM

The POL converters have seven user selectable sets of digital filter coefficients. It is possible to optimize performance of the POL converters for various application conditions by selecting one of the sets shown in.

The sets can be selected by CCA0…2 pins. The pins are grounded or left floating forming a binary number calling out a specific set of the coefficients. For example, if all three pins are left floating, a binary 111 is formed and the set number 7 is called out.

If the connection of CCA0…2 pins is changed while the POL converter is operating, the change will not take effect until the input power to the POL converter is recycled or until its DELAY pin is pulled low and released.

Table 3. Sets Of Digital Filter Coefficients

Parameter			Value							Units
Set Number (CCA0…2)			7	6	5	3 / 4	2	1	0	
Recommended Input Voltage Range			8 - 12	8 - 12	8 - 12	3.3 - 5.0	3.3 - 5.0	3.3 - 5.0	6 - 11	V
Recommended Output Capacitance Range	Type		Ceramic and Tantalum	Tantalum	Ceramic	Ceramic and Tantalum	Tantalum	Ceramic	Ceramic and Tantalum	
	Ceramic	C	50-400	N/A	100-400	50-200	N/A	100-400	50-200	µF
		ESR	5	N/A	5	5	N/A	5	5	mΩ
	Tantalum	C	220-2,000	440-10,000	N/A	220-880	100-1,000	N/A	220-880	µF
		ESR	20-40	10-40	N/A	40	10-25	N/A	40	mΩ

4.8 Current Share

The POL converters are equipped with the digital current share function. To activate the current share, simply interconnect the CS pins of the POLs connected in parallel. The digital signal transmitted over the CS line will assure equal current sharing between all POL converters.

Note that all POL converters connected in parallel must have the same value of the trim resistor. If the value of the trim resistor is changed dynamically (e.g. for margining), the user needs to ensure the change is synchronized between all current sharing converters. Otherwise a voltage transient could be observed on the output. If the transient is too high, it can trigger UVP or OVP of a POL converter.

The SYNC and the OK pins of all POL converters connected in parallel should be interconnected to synchronize their switching frequencies and provide the fault propagation.

The POL converters connected in parallel can operate with different interleave settings. For the most optimal output noise reduction, the interleave should be set to 360°/N, where N is the number of POL converter connected in parallel.

4.9 Performance Parameters Monitoring

The POL converters can monitor and report their own performance parameters such as output current

and temperature.

4.9.1 Output Current Monitoring

The output current is measured using the ESR of the output inductor. The current readings are adjusted based on temperature of the POL converter to compensate for the change of the inductor's ESR with temperature.

The output current information is converted internally into a digital format and reported via the CS pin. The CS pin is an open drain I/O that is internally pulled up to 3.3V. The digital signal on the CS pin is a 500 kHz square wave. The negative duty cycle of the CS signal is proportional to the output current of the POL converter as shown in Figure 37 and Figure 38. The exact current to duty cycle ratio is specified in the respective POL converters data sheets.

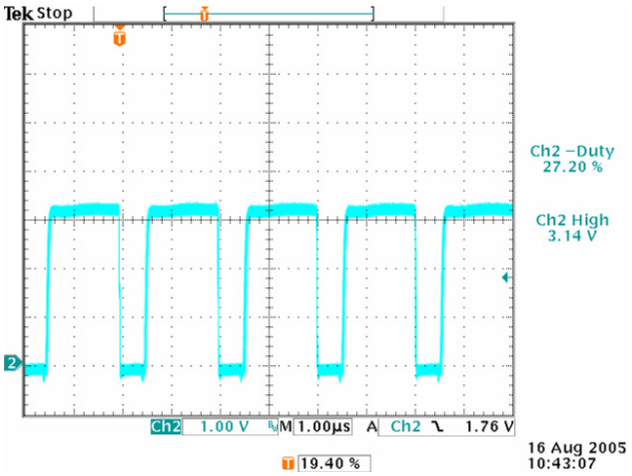

Figure 37. ZY1207 Current Sense Signal. Iout=3.5A

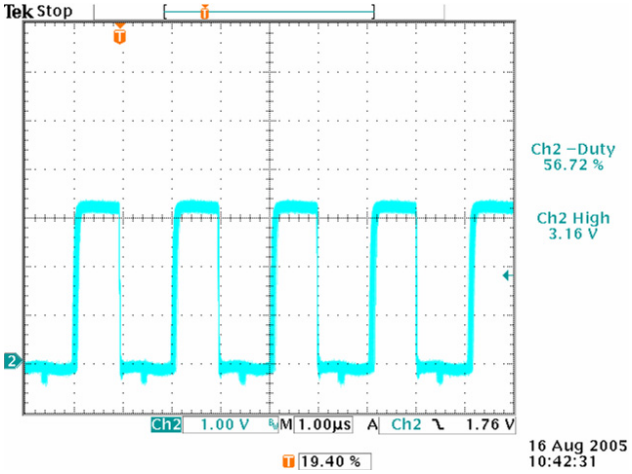

Figure 38. ZY1207 Current Sense Signal. Iout=7A

If POL converters are connected in parallel, the signal on the CS line represents the highest current being delivered by any of current sharing POL converters. Given the accuracy of the current share, the signal can be used to estimate the current delivered by each individual POL converter as well as the total output current.

Note: Capacitive loading of the CS pin needs to be minimized to ensure the 10-90% rising edge of the signal is less than 100ns. If the condition is not met, the output voltage may rise by app 0.3V.

4.9.2 Output Temperature Monitoring

The temperature of a POL converter is measured by the thermal sensor built into the controller IC. Temperature information is converted internally into an analog voltage and reported via the TEMP pin. The voltage on the TEMP pin changes from 0.2V to 2.0V when the temperature changes from -40°C to 140°C. The relationship is linear so the temperature of a POL converter can be determined from the voltage on the TEMP pin by the equation below:

$$T_{POL} = (V_{TEMP} - 0.2) \times 100 - 40\ ,\ °C$$

where T_{POL} is the temperature of the POL converter in degree Celsius and V_{TEMP} is the voltage measured on the TEMP pin.

The internal source impedance of the TEMP pin is 6.4kΩ.

5. Transition from Z-7000 to Z-1000

The Z-1000 Series No-Bus™ POL converters are footprint compatible with the Z-7000 Series POL converters utilized with ZM7xxx Series Digital Power Managers. It gives power system engineers an opportunity to use Z-7000 POL converters with a Digital Power Manager during system development and characterization and transition to the more cost effective Z-1000 POL converts in mass production. The transition does not require any PCB layout change and is accomplished by adding or removing jumpers as described below.

5.1 Transition Details For 25-Pin POLs

The schematic in Figure 39 shows external components and jumpers required for operation of Z-1000 POL converters based on the 25-pin vertical or horizontal mechanical platforms (e.g. ZY1115, ZY1015, ZY1120).

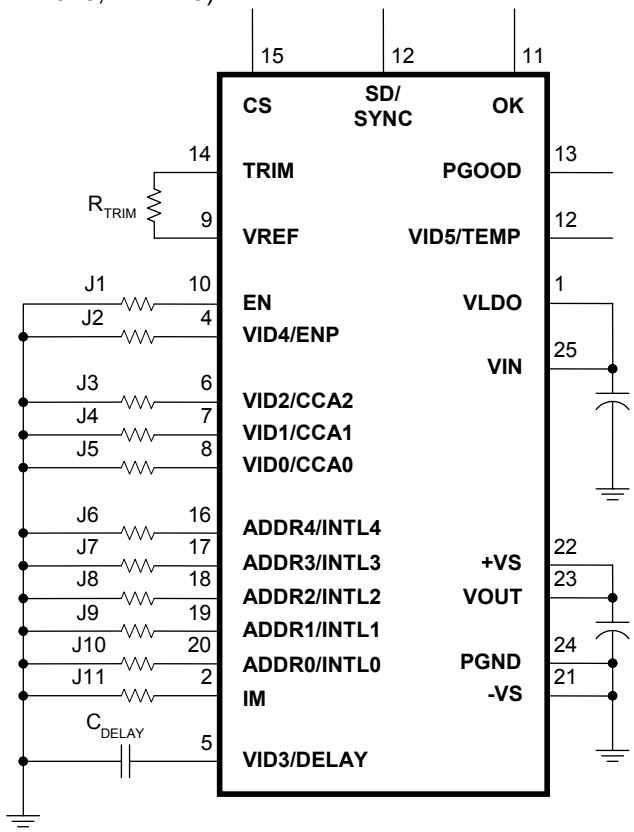

Figure 39. Schematic For Transition Between Z-7000 and Z-1000. 25-Pin POL Is Shown

Notes: 1. If a pin name is different between Z-1000 and Z-7000 POLs, both names are listed in the schematic, separated by a forward slash (e.g. SD/SYNC). The pin name before the slash pertains to Z-7000 POLs
2. Connections of pins CS, SD/SYNC, OK, VLDO, VIN, +VS, VOUT, PGND, and -VS do not change during the transition from Z-7000 to Z-1000 POLs.

No external components and even fewer jumpers are required for operation of Z-7000 POL converters as detailed in Table 4.

Table 4. Transition Table For Schematic In Figure 39

Ref.	Z-1000	Z-7000
R_{TRIM}	Required to set V_{OUT}	Not Used
C_{DELAY}	As required to program power-up delay	Not Used
J1	As required for Enable control	Yes
J2	As required to program Enable polarity	Not Used
J3	As required to configure feedback loop	Not Used
J4	As required to configure feedback loop	Not Used
J5	As required to configure feedback loop	Not Used
J6	As required to program interleave	As required to set POL address Bit 4
J7	As required to program interleave	As required to set POL address Bit 3
J8	As required to program interleave	As required to set POL address Bit 2
J9	As required to program interleave	As required to set POL address Bit 1
J10	As required to program interleave	As required to set POL address Bit 0
J11	As required to configure Master POL	Not Used

5.2 Transition Details For 36-Pin POLs

The schematic in Figure 40 shows external components and jumpers required for operation of Z-1000 POL converters based on the 36-pin horizontal mechanical platform (e.g. ZY1207).

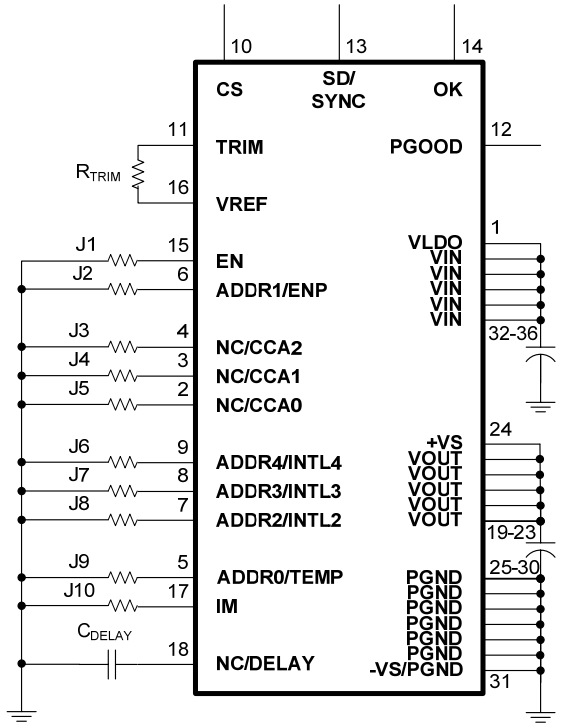

Figure 40. Schematic For Transition Between Z-7000 and Z-1000. 36-Pin POL Is Shown

Notes: 1. If a pin name is different between Z-1000 and Z-7000 POLs, both names are listed in the schematic, separated by a forward slash (e.g. SD/SYNC). The pin name before the slash pertains to Z-7000 POLs
2. Connections of pins CS, SD/SYNC, OK, VLDO, VIN, +VS, VOUT, PGND, and –VS/PGND do not change during the transition from Z-7000 to Z-1000 POLs

No external components and even fewer jumpers are required for operation of Z-7000 POL converters as detailed in Table 5.

Table 5. Transition Table For Schematic In Figure 40

Ref.	Z-1000	Z-7000
R_{TRIM}	Required to set V_{OUT}	Not Used
C_{DELAY}	As required to program power-up delay	Not Used
J1	As required for Enable control	Yes
J2	As required to program Enable polarity	As required to set POL address Bit 1
J3	As required to configure feedback loop	Not Used
J4	As required to configure feedback loop	Not Used
J5	As required to configure feedback loop	Not Used
J6	As required to program interleave	As required to set POL address Bit 4
J7	As required to program interleave	As required to set POL address Bit 3
J8	As required to program interleave	As required to set POL address Bit 2
J9	Not Used	As required to set POL address Bit 0
J10	As required to configure Master POL	Not Used

6. Z-1000 Design Tool

The Z-1000 design tool is an Excel-based tool that needs only basic inputs to create a complete power system design.

6.1.1 Installation

The design tool is downloaded from the Power-One website as self-extracting executable file. Running the installer will place the Excel file to C:\Program Files\Power-One\Z-1000 Utility (overwriting previous versions), and add a shortcut to it on the desktop and in the start menu. It may be uninstalled via the Windows control panel.

6.1.2 Features

- Design Wizard chooses and configures Z-1000 series POL converters based on user defined voltages and currents
- Auto-Compensation finds best CCA for specifc capacitor configuration
- Auto-Interleaving to minimize input and output ripple
- Trim resistor calculation
- Power-up delay capacitor calculation
- Step response simulation
- Pin diagram output showing all connections

6.1.3 Design Example

The following example shows the steps in using the tool. A design will be created for the specifications shown below.

- V_{IN}=4.5 to 5.5V
- V_{OUT1}=3.3V, 10A, power-up delay = 10ms, C_{OUT}=2x220µF/50mΩ and a 10µF/2mΩ
- V_{OUT2}=2.5V, 30A, power-up delay = 20ms, C_{OUT}=4x330µF/40mΩ and 2x10µF/2mΩ

The Z-1000 Design Tool is opened by double clicking on the icon on the desktop or via the start menu. Upon opening the tool, if asked to enable macros, follow the on-screen instructions to do so. Upon pressing **Start** on the Intro screen, a user can enter the V_{IN} range and number of outputs as shown in Figure 41.

Note: Press Enter or click outside the cell in order to be able to press the **Next** button.

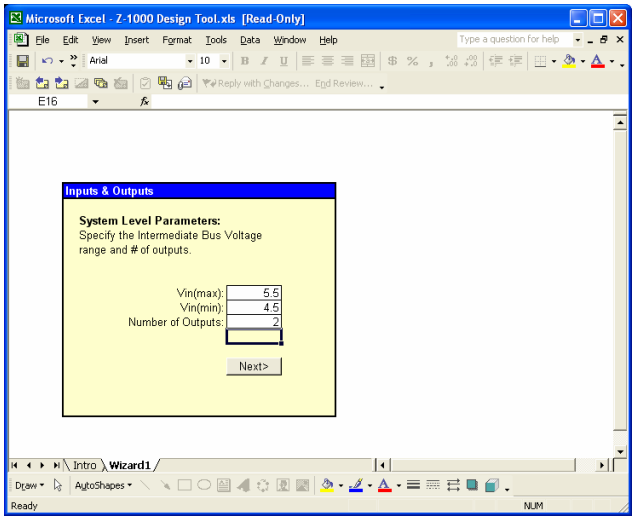

Figure 41. Inputs and Outputs Worksheet

Next, the desired output voltages and currents are entered. The valid range of V_{OUT} is shown above the data table as shown in Figure 42.

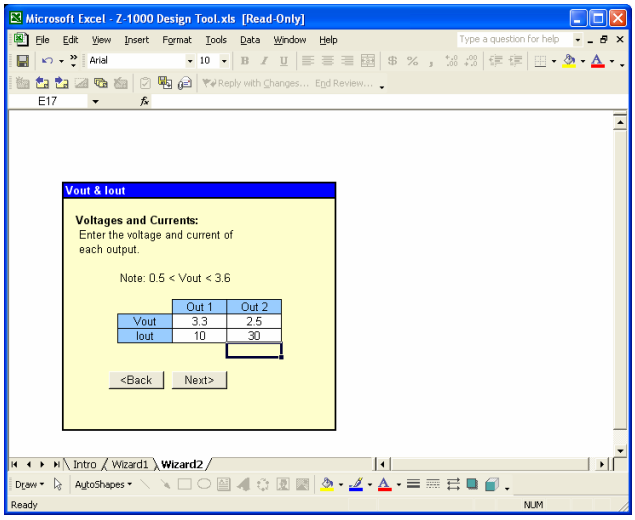

Figure 42. Voltages and Currents Worksheet

Upon pressing **Next**, the design tool picks the recommended parts as shown in Figure 43. The recommended parts and quantities may be overridden if desired. The **POL Type** drop-down list contains all available part types. Several pertinent notes are shown at the bottom of the Excel window.

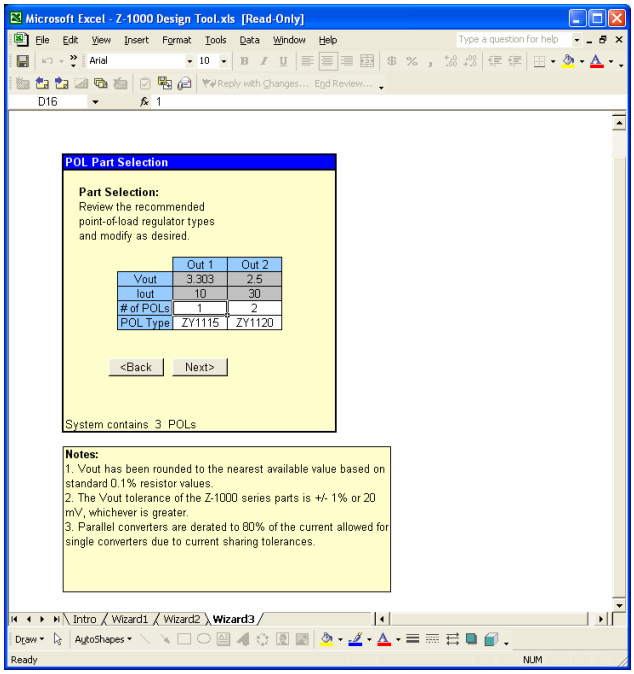

Figure 43. Part Selection Worksheet

In the sheet shown in Figure 44, the power-up delay time and output capacitor values may be specified. The users have the option to keep the default values, or enter their own values. In this case, the values specified in the example statement are entered.

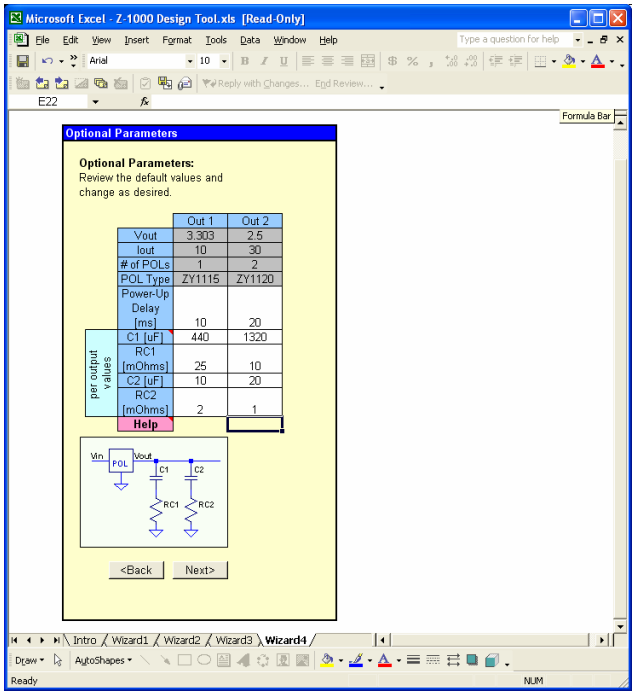

Figure 44. Optional Parameters Worksheet

Upon pressing **Next**, the completed configuration summary table is shown (see Figure 45). The design tool has chosen the required Rtrim and Cdelay. For Rtrim, the nearest standard 0.1% value is used, while for Cdelay, the nearest standard 5% value is used.

The tool also configures the OK and CS connections. All POL converters with identical power-up delays are synchronized by tying their OK lines together and using a single delay capacitor. The CS lines of all paralleled POL converters are tied together.

The Interleave, and CCA (Compensation Coefficient Address) configurations have been chosen for optimum performance (see 6.1.4 and 6.1.5).

Note: The red triangles in the corner of some cells indicate that help notes will pop up if the mouse is hovered over the cell.

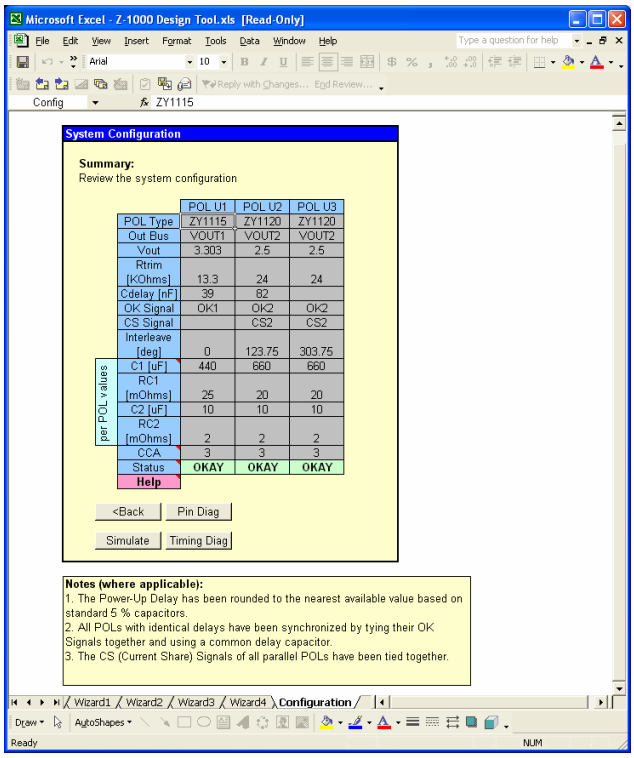

Figure 45. System Configuration Worksheet

By pressing the **Simulate** button, the user can see the step response, peak error, phase margin, and bandwidth for each POL converter as shown in Figure 46. Here, the CCA and Vin may also be changed to see the effects.

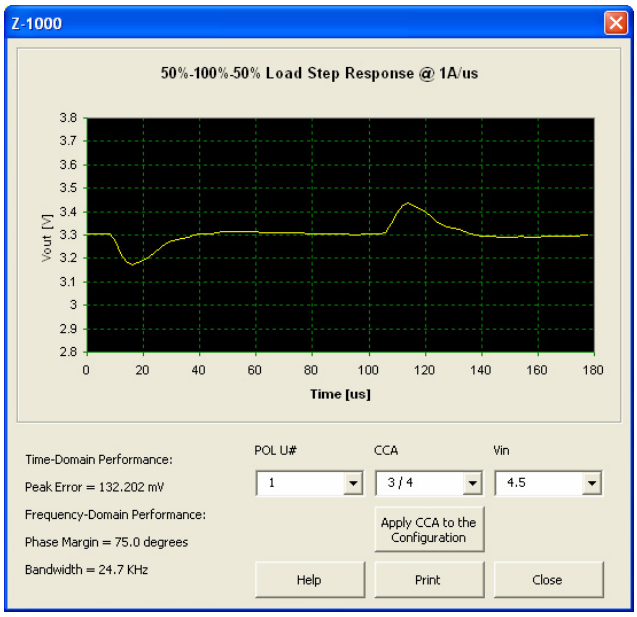

Figure 46. Simulation Window

Note: Since CCAs 3 and 4 are the identical, they are shown as 3 / 4 in the drop-down box.

Pressing the **Timing Diagram** button on the System Configuration sheet brings up the graph shown Figure 47. The **Back** button is available to go back to the System Configuration sheet.

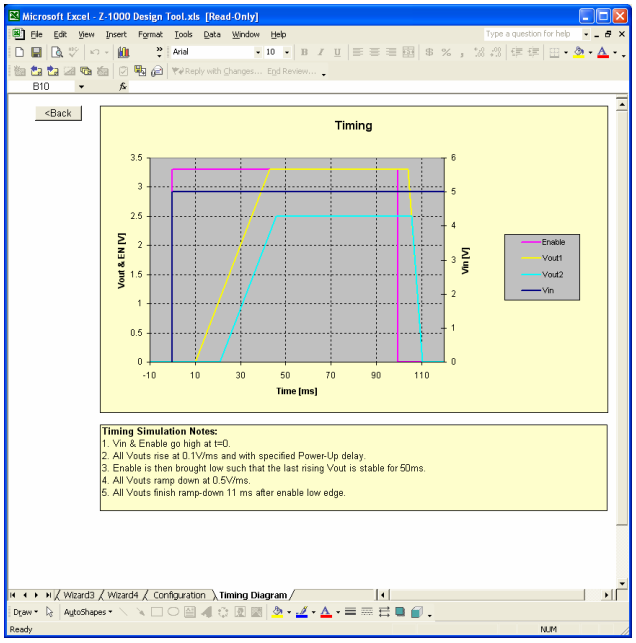

Figure 47. Timing Diagram

Pressing the **Pin Diagram** button on the System Configuration sheet brings up the window shown in Figure 48. The VLDO, IM, CCA, INTL, OK, and CS pin connections are all shown as customized to the specific design. The Pin Diagram is formatted as a printable (multi-page if needed) document with a title block that may be customized for documentation purposes. T he values of Cin, Cout, Rtrim, and Cdelay are shown below each POL converter symbol.

The **Back** button is available to go back to the System Configuration sheet.

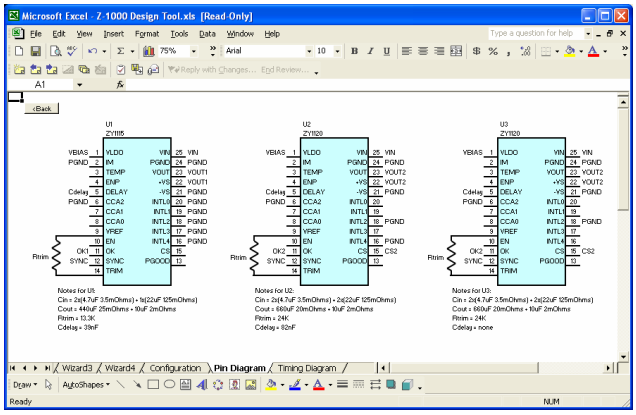

Figure 48. Pinout Diagram

The resulting design file can be saved for future reference. Since the base file is Read-Only, Excel will ask to save it under a different name. This way, the base file does not get altered.

6.1.4 Auto-Interleaving Scheme

Interleaving – applying a phase shift between the switching actions of multiple converters operating at the same frequency – is an effective means of reducing both input and output switching ripple and noise. Interleaving is applied so that the switching ripple tends to cancel. For paralleled POLs converters, it is always optimal to have even spacing so their output ripple is minimized e.g.

Phase shift between paralleled POLs = 360/(number of POLs in parallel) [degrees]

To minimize input ripple, the POL converters connected to each output bus should have a phase shift as a group so they do not switch current to the input bus at the same time. The tool calculates the phase shift (interleave angle) based on the number of outputs and inputs. The interleave angles are then rounded to the nearest available setting.

6.1.5 Auto-Compensation Scheme

The design tool features an Auto-Compensation algorithm that operates as follows:

- Each CCA value is tested at the min, nom, and max Vin conditions
  - Seven CCA values and three input voltage values give 21 cases for each POL converter
- For each case, system performance is evaluated by an overall score that looks at AC and transient performance
- The CCA is chosen based on min/max optimization of the score over Vin
- For each CCA, the worst score over the three Vin conditions is recorded
- Then, the best CCA is chosen out of these worst-case values